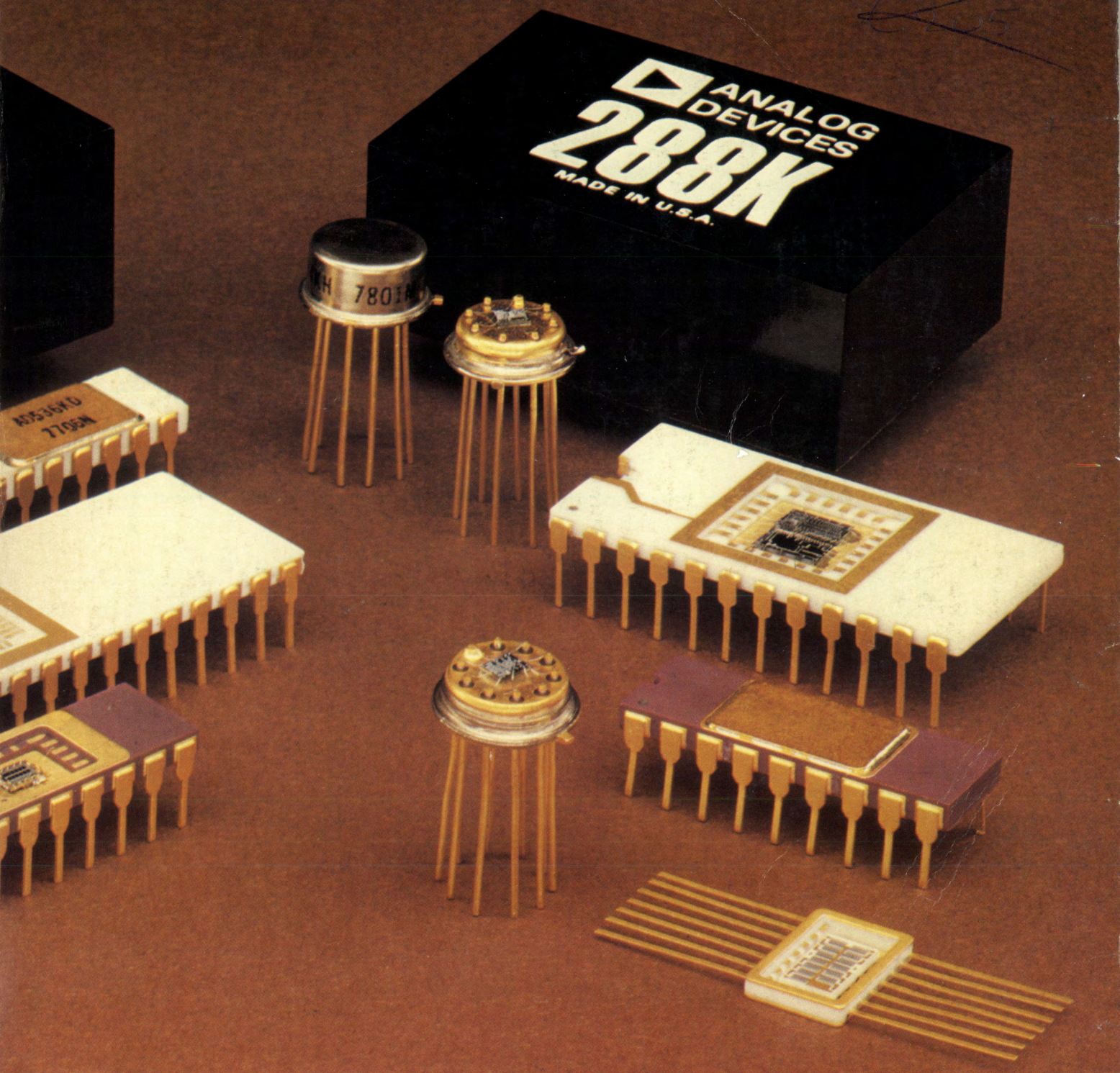
DATA ACQUISITION PRODUCTS CATALOG



ANALOG DEVICES

Index

DATA ACQUISITION PRODUCTS CATALOG

Introduction

Since its inception more than twelve years ago, Analog Devices has continually expanded its line of interface, signal conditioning, display devices and subsystems for the data acquisition, measurement and control market with easy-to-use advanced designs at low cost.

Utilizing state-of-the-art processing in technologies such as bipolar, CMOS and I^2L, Analog Devices offers over 400 products including integrated circuit operational amplifiers and data converters, CMOS switches and multiplexers, dual transistors, digital panel meters, data acquisition devices, microcomputer analog input/output subsystems and measurement and control systems. Analog Devices offers data acquisition components in monolithic integrated circuit, hybrid and modular form; leadership and innovations in these fields allows Analog Devices to offer the broadest range of data acquisition devices available at the best speed, accuracy and cost available.

Analog Devices is continually improving on the technologies needed to serve users of precision data acquisition components. Monolithic and hybrid integrated circuits and modules (cards and potted circuits) offer their own advantages.

Modules typically offer the highest performance in terms of speed, accuracy and functional completeness; ease of application is high with modules and the user spends less time in development and documentation.

Of the IC products, hybrids provide the highest performance and are the most complete, functionally. Bipolar devices yield stable references, high performance current switches and resistance networks which are laser-trimmed; bipolar I^2L processing allows high quality linear and digital circuitry to be fabricated on the same silicon chip. CMOS products use voltage switches in a current-steering mode for full four-quadrant multiplying operation; the inherent high-density logic capability and low power dissipation of CMOS are combined with fast current settling characteristics.

Bipolar and CMOS devices permit the most design flexibility, are small, and feature very high performance-per-cost figures.

These products are manufactured at six facilities around the world, with an additional integrated circuit plant scheduled to open June, 1978 in Wilmington, Massachusetts to expand I^2L and BiFET processing capability.

The continuing application of present state-of-the-art and the invention of future state-of-the-art processes strengthens Analog Devices' leadership position in semiconductor data acquisition components.

The continuing march towards easy-to-use products is supplemented by more than ten years of applications experience and numerous technical publications and design notes which detail operation of devices from op-amps to microprocessor-based systems.

Backing up these design and manufacturing capabilities is a network of sales offices and representatives throughout the United States and most of the world, staffed by experienced sales and applications engineers and offering in most locations, local stocking of Analog Devices' products.

Many products comply with Military Specifications MIL-STD-883B and MIL-STD-105D or Industry Specifications, Weapon Specifications or Ordnance Documents, as specified by Military or Customer requirements. Analog Devices Semiconductor has complete capabilities for the 100% screening of devices per method 5004 of MIL-STD-883B.

G.S.A. APPROVAL
Many products in this catalog are covered under G.S.A. contacts. Request a copy of Analog Devices' "Authorized Federal Supply Schedule Price List" for details.

Contents

Operational Amplifiers

Orientation
Operational Amplifiers

The amplifiers listed in this catalog are intended to provide cost-effective solutions to the bulk of op-amp requirements in precision measurement and control, as well as to more-general requirements in electronic circuits. The technical data included here*cover the properties of some 20 op-amp families, comprising about 75 distinct types. Some are general purpose, others provide near-optimum performance for specific classes of applications.

They differ in a variety of ways, for example, circuit technology, circuit architecture, input properties, output properties, operating temperature range, degree of isolation, and in terms of the many performance specifications. Some are high-performance modules, most are monolithic IC's, some are two- or three-chip hybrid IC's.

BACKGROUND

The operational amplifier is today the most-widely used analog subassembly. It is safe to say that its *basic* properties and applications are sufficiently understood by most circuit designers and builders. However, the basis for choice, the subtleties of using op amps in circuits for best results (especially in precision measurement and control), and the varieties of possible applications are less clearly understood by op amp users, in varying degrees.

In these few pages, we shall address the question of making a proper choice of op amp type for an application, in relation to the extensive array of device properties presented in the data sheets that follow. A Selection Guide, to help narrow the area of choice quickly, is to be found on page 14.

For those users requiring basic tutorial material, and detailed information on getting the most out of op amps, we have provided on page 13 a bibliography that should make available up to 99% of information needed now and then, with "fanout" to the vast body of literature that – with some redundancy – will provide the remainder. It should come as no surprise to successful users of Analog Devices op amps that a number of the references are to the applications sections of data sheets included in this catalog.

SELECTION PRINCIPLES

There are three fundamental aspects to the rational selection of an operational amplifier for a given application: establishing the circuit architecture, defining the performance levels, and choosing the amplifier(s).

*In addition to the products listed here, which are recommended for new designs, a number of older products are still available; they are listed on page 599. Data sheets are available upon request.

1. To obtain a circuit building block to implement a defined functional job, the principal choices are either to purchase a committed functional device or to design a circuit employing op amps to perform the function. For example, to obtain a difference between two voltages, one may either purchase an instrumentation or isolation amplifier, or design a suitable subtraction circuit using op amps. If a committed functional building block, with appropriate specs and price, is not available, the circuit designer must start by developing schematic diagrams of circuits that will perform the function simply using "ideal" operational amplifiers. Many commonly used circuits can be found in textbooks, "cookbooks", and linear circuit books, as well as in application notes and data sheets.

2. Recognizing that the choice of an op amp depends on both the overall circuit requirements and the characteristics of available op amps, the designer should interpret the desired overall performance in terms of the parameters of op amps, and establish acceptable ranges of parameters, and their variation with time, temperature, supply voltage, etc. Examples of the key parameters are the input offset voltage, input bias and offset currents, and the high-frequency performance and transient behavior of the op-amp block (and its effect on the closed-loop circuit) for large and small signals. It will be helpful to develop an application checklist, which includes such considerations as the character of the input signals and their impedance, the output load, the desired accuracy – static and dynamic – and the environmental conditions.

3. The designer must then relate acceptable performance of the op-amp building block to the specifications and prices of available devices from preferred suppliers, bearing in mind a firm understanding of the way in which manufacturers define their specifications, and how definitions can differ in a way that may be misleading. A set of definitions used by Analog Devices follows the next section.

HOW THE OPERATIONAL AMPLIFIERS ARE CLASSIFIED

To assist the designer in distinguishing among the many types available from Analog Devices, we have provided a Selection Guide, in which amplifiers are grouped in terms of common properties which have been optimized in order to satisfy the needs of specific classes of applications. Once the choice has been narrowed to the manageable number of types in any group, distinctions can be drawn in terms of other requirements or considerations. In general, IC's can be distinguished from modules by the "AD" prefix.

Temperature Range and Nomenclature. The principal division in the Specification Guide is by temperature range. Analog Devices operational-amplifier nomenclature uses suffixes to

permit ready identification of the temperature range for which device operation to meet critical specifications has been designed or selected. The most popular range comprises the "commercial" temperatures from 0°C to 70°C; it is designated by suffixes such as J, K, L, M, in order of increasingly tighter specs (e.g., AD741L). Also popular is the "military" range, −55°C to +125°C, designated by S, T, U, (e.g., AD510S); not all families have types with specified performance in this range. There are a few types designed for operation in the "industrial" range, −25°C to +85°C, designated by A, B (e.g., model 51B). Wide-range types will generally meet the same or better specs in a narrower temperature range. A few types are second-sources for products originally introduced by other manufacturers. In those instances, the generic nomenclature is used (or enlarged upon, if superior selections are offered — e.g., AD301AL).

Within the "commercial" range, there are eight divisions by class of application, based on optimization of one or more key specifications. Six of these divisions are also found to have comparable devices specified for the "military" range. Versions of many devices in this class are available to meet requirements of MIL-STD 883B; the availability of such devices will be noted on the data sheets.

1. *General-Purpose IC's.* Amplifiers in this group include our lowest-cost devices.* They are best-suited for general purpose designs with moderate drift requirements, down to 15μV/°C max (AD201A), bias currents of 2nA max (AD208), and gain-bandwidths to 8MHz (AD301A). Typical applications include summing, inverting, impedance buffering (followers), and active filtering. They are also useful for developing nonlinear transfer functions, with appropriate external circuitry.

Bipolar monolithic technology is used for all types; the AD308 achieves its low bias current via superbeta transistors. The AD741 is internally compensated; it does not require external capacitance for frequency compensation. On the other hand, the AD301A's ability to be externally compensated, by either lag or feedforward circuitry, permits circuits with a wide range of dynamic performance characteristics to be handled. Extended-temperature-range equivalents are the AD101A, AD201A, AD741, AD108 and AD208.

2. *Low Bias-Current, High Input-Impedance, FET-Input IC's and Modules.* These types use the inherently high impedance and low leakage current of junction field-effect transistors (FET's) to deal with configurations that either provide the measurement of low currents or require the use of high-resistance circuitry.

Typical applications range from general-purpose high-impedance circuitry to integrators, current-to-voltage converters, and log-function generation, to measurements with high-impedance transducers, such as photomultipliers, flame detectors, pH cells, and radiation detectors.

The performance range is from the 75fA (75×10^{-15} A) maximum bias current of the AD515L electrometer to the 50pA max of the general purpose, lowest-cost AD540J.

The high-speed internally compensated AD528K combines FET-input performance (15pA max bias current) with fast slewing (50V/μs min, increasable by external capacitance) and 10MHz unity-gain bandwidth. Low bias current does not necessarily imply large voltage offsets; the AD515K combines a 150fA (0.15pA) max bias current with 1.0mV max offset and 15μV/°C max voltage drift; comparable figures for model 52K are 3pA, 0.5mV, and 1μV/°C.

Extended-temperature-range equivalents are AD503S, AD506S, AD528S, and AD540S.

Except for Model 52J/K, the types in this group either are completely monolithic or employ matched FET's and a special bipolar amplifier chip designed to accommodate the input FET's electrically. In nearly all the IC's, thin-film resistors are deposited on the chip at critical circuit locations to ensure stability; low offsets and drift are achieved by laser-trimming of circuit balance. All FET-input op amps from Analog Devices are manufactured to meet their published bias-current specifications *after full warmup* (some manufacturers specify *initial* current, which is lower than warmed-up bias current). Our published max bias-current specification applies to either input (some manufacturers call "bias current" the *average* of the two input currents). Bias current of junction FET's approximately doubles for every 10°C increase of temperature.

3. *Electrometers.* This class comprises the lowest bias-current devices, the AD515 IC's and models 310 and 311 modules. The AD515L, with its 75fA input bias current, 1mV max offset, and 25μV/°C offset tempco, has differential inputs, and can be used in voltage measurements at high impedance, as a follower, or in current measurements, as an inverter, or even differentially.

The 310K is primarily an inverting amplifier, with 10fA (10^{-14} A) max bias current at the negative input (±1nA at the positive input), 10mV offset voltage (adjustable to zero), and 10μV°C tempco; the 311K is primarily non-inverting, with the same specifications, and the 10fA max bias current is specified for the *positive* input. This type can be used differentially but asymmetrically; an example is the 311 as a follower-with-gain, using low-value resistors in the feedback network).

These amplifiers differ from the AD515 in design technique, as well as in manufacturing technology. The 310 and 311 are a unique pair of amplifiers that achieve their outstanding input specifications with *parametric-amplifier* inputs. A high-frequency carrier, applied to a varactor bridge, is modulated by the differential input voltage of the amplifier, transformer-coupled, amplified, and demodulated. Although it intrinsically has noise-free amplification, a parametric circuit also has substantial input capacitance — 30pF differential for model 310, vs. 2.4pF total for AD515 — always a consideration in low-current measurement, because of the long charging time at low currents. On the other hand, the 310/311 can withstand fault voltages up to ±300V between the inputs. Noise is also a consideration in low-level amplifiers. Typical current noise for the AD515 is 3fA (peak-to-peak) in the 0.1 to 10Hz band; current noise for the 310/311 is 1fA (peak-to-peak) in the 0.01 to 1Hz band. Corresponding voltage noise if 4μV p-p (AD515, 0.1 to 10Hz) and 10μV p-p (310/311, 0.01 to 1Hz).

These amplifiers do not have standard extended-temperature-range equivalents.

4. *High-Accuracy Low-Drift Differential-Input IC's and Modules.* "Chopperless" low-drift designs with differential inputs, optimized for voltage offset and drift, dc open-loop gain, and CMR, should be considered for high-accuracy instrumentation, low-level transducer bridge circuits, precision voltage comparators, and for impedance buffer designs.

Performance of internally compensated premium amplifiers in this group ranges from the AD517L's 25μV max offset voltage and 0.5μV/°C drift, combined with 1nA max bias current (1.5nA max over the temperature range), and CMR of 110dB min, to the low-cost AD741L's maximum offset of 0.5mV and

*Some extended temperature-range versions have also been included in this group, when they can uniquely provide improved performance specifications in the "commercial" range at competitive cost.

max offset tempco of 5μV/°C, with 100nA max bias current over the temperature range, and CMR of 90dB min. The best overall performer in this group in high impedance applications is the FET-input model 52K, which combines low offset and drift (0.5mV and 1μV/°C) with 3pA bias current.

Among *uncompensated* op amps, the premium range is from the AD504M, with 0.5mV maximum offset voltage, 0.5μV/°C max drift, 100nA max bias current over the temperature range, and 110dB CMR, to the low-cost AD301AL, with max offset of 0.5mV, max drift of 5μV/°C, max bias current of 45nA over the temperature range, and minimum CMR of 90dB. For applications in which low noise is essential, the AD504M has 100%-tested guaranteed maximum voltage noise of 0.6μV p-p, for the frequency range 0.1 to 10Hz, and maximum spot noise of 13, 10, and 9nV/$\sqrt{Hz}$ and 1.3, 0.6, and 0.3pA/$\sqrt{Hz}$, at 10Hz, 100Hz, and 1000Hz, respectively.

External dynamic compensation permits considerably greater bandwidths, at higher gains, than are available with the compensated AD517 and AD510 families. For example, with a 3.9pF compensating capacitor, the AD504's typical small-signal bandwidth is 100kHz at a gain of 200, vs. 1.5kHz for the internally compensated AD510; under the same conditions, the full-power bandwidth of the AD504 is 30kHz, vs. 1.5kHz for the AD510. With feedforward compensation, the AD301AL has a full-power bandwidth in excess of 150kHz, for inverting applications.

Except for model 52, all of the amplifiers in this class are monolithic*. The AD741J/K/L and the AD301AL are selected from production lots of the generic AD741 and AD101A types. The AD504, AD510, and AD517 are thermally balanced for low drift and high gain (independent of output loading), with inputs that are bootstrapped for high CMR and protected against overloads to prevent bias-current degradation due to reverse breakdown. Thin-film resistors, deposited on the chip, are another key to the stability of these amplifiers. The AD510 and the AD517 employ super-beta input transistors to achieve low bias current, and they are laser-trimmed at the wafer-probe stage (LWT) to achieve their excellent offset-voltage specifications at low cost. Since the bias currents are always of one polarity, they can be nulled at a given temperature with simple circuitry; and the change over the temperature range will be considerably less than for low-cost FET-input amplifiers having comparable specifications.

Extended-temperature-range equivalents are AD504S, AD510S, AD714S, and AD517S.

5. *High-Accuracy Modules Using Chopper Techniques* The amplifiers in this class are widely accepted as the best choice when it is essential to maintain low voltage offsets and bias currents with time and temperature or whenever external offset adjustments are not practical in the application. Using carrier modulation techniques, these designs achieve drifts to 0.1μV/°C and long-term stability to ½μV/mo. Typical applications include error-summing amplifiers for servo loops, precision regulators, and input amplifiers for laboratory-grade metering instruments and test equipment.

Two forms of amplifier are available. The *noninverting chopper-amplifier* (260 and 261 families) is a high-gain feedback amplifier, containing a MOSFET chopper, optimized for follower-with-gain applications. The chopper converts the difference between the dc or low-frequency input voltage, at high impedance, and the feedback voltage to a high-frequency square-wave, amplifies it with no drift, and demodulates and filters the result to produce an output waveform that is an amplified version of the input. The closed-loop gain is determined by the attenuation ratio of the feedback resistor-pair.

The initial offset is ±25μV max (trimmable to zero), with average drift-vs.-temperature of 0.1μV/°C max (model 261K). Bias current is respectable, at 300pA max, with a tempco of 10pA/°C max, to minimize errors with high-impedance sources.

Maximum noise voltage is 0.4μV peak-to-peak, from 0.01 to 1.0Hz, and 1.0μV, from 0.01 to 10Hz. Small-signal bandwidth, established by an external compensating capacitor that is chosen as a function of gain, is 100Hz.

Inverting chopper-stabilized amplifiers (234 and 235 families) employ narrow-band chopper amplifiers to measure the summing-point voltage of the main amplifier (which should be a null), chop, amplify, filter, and feed to the positive input of the main amplifier an amplified correction signal. Thus, the offset voltage and drift of the main amplifier (including the effects of input bias current) are reduced by the gain of the chopper amplifier, without a corresponding reduction of bandwidth.

Chopper and chopper-stabilized amplifiers should be considered when long-term stability must be maintained with time and temperature, and wherever maintenance-free operation of instruments and remote circuits is essential. Typical applications include amplification of microvolt-level signals, precision integration, and analog computing.

The 234 and 235 families differ principally in bandwidth. The 235 family is somewhat quieter, with lower offset and higher dc gain than the 234's; the 234 family have considerably greater bandwidth: 2.5MHz small-signal unity-gain and 500kHz min full power, vs. 1MHz and 5kHz(min). Maximum offset of model 235L is ±15μV (externally adjustable to zero), with drift less than 0.1μV/°C. Bias current is ±50pA max, with a max tempco of 0.5pA/°C. Maximum noise, 0.01 to 1Hz, is 2μV p-p.

These amplifiers do not have standard extended-temperature-range equivalents.

6. *Wide Bandwidth, Fast-Settling IC's and Modules.* High-speed op amps are characterized by high slewing rates, fast settling time, and wide bandwidth. Fast setling time is especially important in applications with rapidly changing or switched analog data, in buffers, d/a converters, and multiplexer circuitry; wide small-signal bandwidth is important in preamplification and in handling low-level wideband ac signals; high slewing rate is associated with fast settling time and is also important in handling ac signals having large magnitudes with minimal distortion, since the large-signal bandwidth is closely related to the slewing rate.

The products in this category with outstanding specifications are models 50J/K and 48J/K. Settling of model 50 to within 0.05% is guaranteed within 200ns in the inverting connection and 300ns non-inverting, with closed-loop gain of 2. Max slewing rate is 500V/μs inverting, 400V/μs noninverting, and small-signal unity-gain bandwidth is 70MHz; full-power bandwidth is 8MHz, min. In addition, these devices will deliver ±100mA of output current at ±10V, an important factor in video and line-driver circuitry, and in driving capacitive loads. For example, the current required to sustain 500V/μs in a 100pF load is I = C dV/dt = 50mA. Model 48J/K is optimized for settling time: 500ns maximum to 0.01%, inverting or non-inverting, with output of ±20mA at ±10V.

There are four families of IC's in this category, with slewing

*In the AD510, the compensating capacitor is bonded to the header, alongside the monolithic amplifier chip.

rates ranging from 25V/μs min to 100V/μs min. The AD509S is the fastest slewing (100V/μs min) and settling (500ns min to 0.1% and 2.5μs min to 0.01%). The AD507K is the best all-around performer, with small-signal bandwidth of 35MHz, slewing rate of 25V/μs min, and typical settling to 0.1% within 900ns, in addition to open-loop dc gain of 10^5 min, drift of 15μV/°C max, and bias current of 15nA max. The AD518J is the lowest in cost, yet it slews at 50V/μs min, and typically settles to within 0.1% in 800ns, with single-capacitor compensation. And the AD528K has FET inputs, with low initial offset (1mV max) and bias current (15pA max), and dynamics similar to those of the AD518.

Extended-temperature-range equivalents are models 51A/B, AD507S, AD509S, AD518S, and AD528S.

7. *Differential FET-Input High-Out Modules.* This beefy group comprises models 50 and 171. The model 50 (J & K) will furnish up to ±100mA at ±10V out. In addition, it is an excellent wideband amplifier, with 70MHz small-signal gain-bandwidth, 500V/μs minimum slewing rate, and settling time of 200ns maximum to 0.05%, as an inverter, and almost as good performance in non-inverting applications. In addition to the applications suggested for it in the wide-bandwidth category, it is useful for such applications as a current booster/buffer for op amps dealing with low-level signals — either outside the loop or inside the loop. It is protected against short circuits to ground or to either supply.

Extended-temperature-range equivalents are models 51A/B.

The model 171 has a large output voltage swing, ±140V at ±10mA, when used with ±150V supplies. However, it need not operate symmetrically; any combination of power-supply voltages between the limits of 15 to +300V for the positive side and -15 to -300V for the negative side is acceptable (including single-supply operation), provided that the total voltage across the amplifier is within the range of 30 to 300V. The output will swing to within 10V of the V_S^+ and V_S^- supply rails. The output and both inputs are protected against short circuits to common or to either supply. Model 171K has an open-loop gain of 10^6 min, offset of 1mV, drift of 15μV/°C max, bias current of 20pA max, CMR of 100dB min, unity-gain small-signal bandwidth of 3MHz, and slewing rate of 10V/μs. Typical applications include high compliance-voltage current source, high-voltage follower-with-gain, high-voltage integrator, differential amplifier for high-common-mode-voltage bridge applications, and high-voltage reference supply.

Model 171 does not have standard extended-temperature-range equivalents.

8. *Isolated Operational Amplifier Module.* Model 277 combines a high-performance uncommitted operational-amplifier input stage with a precision, isolated output stage, an isolated dual ±15V power supply, and transformer-coupled isolation circuitry, to form a versatile isolation amplifier. It is rated to withstand input/output common-mode voltage of 3500V rms max (60Hz, 1 minute), and peak continuous ac or dc of ±2500V max, and has input-output CMR of 160dB min at dc and 120dB min at 60Hz, with leakage current of 1μA @ CMV of 115V rms, 60Hz ($Z_L = 10^{12}\Omega \| 16pF$).

The input-stage performance makes many op-amp applications feasible: ±1μV/°C max offset tempco (trimmed, model 277K), bias current of ±20nA max, open-loop gain of 106dB min. In addition, isolated power output of ±15mA max at ±15V, referred to input common, is available for auxiliary front-end circuitry. The output stage has gain of 1V/V, nonlinearity of 0.05% max, 1.5kHz full-power bandwidth, and 50μV/°C offset tempco.

Typical applications for the 277 include general isolated op-amp circuitry, programmable-gain isolated amplifier, isolated power source and amplifier for bridge measurements, instrumentation amplifier, instrumentation-grade process-signal isolator, and current-shunt measurements.

The extended-temperature-range equivalent of models 277J/K is model 277A.

DEFINITIONS OF SPECIFICATIONS

Absolute Maximum Differential Voltage
Under most operating conditions, feedback maintains the error voltage between inputs to nearly zero volts. However, in some applications, such as voltage comparators, the voltage between the inputs can become large. This specification defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.

Common-Mode Rejection
An ideal operational amplifier responds only to the difference voltage between inputs ($e^+ - e^-$) and produces no output for a *common-mode voltage*, that is, when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, or variations in offset voltage as a function of common-mode level, common-mode input voltages are not eliminated at the output. If the output error voltage, due to a known magnitude of common-mode voltage, is referred to the input (dividing by the closed-loop gain), it reflects the equivalent *common-mode error voltage* (CME) between the inputs. Common-mode rejection ratio (CMRR) is defined as the ratio of common-mode voltage to the resulting common-mode error voltage. Common-mode rejection is often expressed logarithmically: CMR (in dB) = 20 $\log_{10}$ (CMRR).

The precise specification of CMR is complicated by the fact that the common-mode voltage error can be a highly nonlinear function of common-mode voltage and also varies with temperature. As a consequence, CMR data published by Analog Devices are average figures, assuming an end-point measurement over the common-mode range specified. The incremental CMR about small values of common-mode voltage may be greater than the average CMR specified (unfortunately, the incremental CMR may be less in the neighborhood of large CMV). Published CMR specifications for op amps pertain to very low-frequency voltages, unless specified otherwise; CMR decreased with increasing frequency.

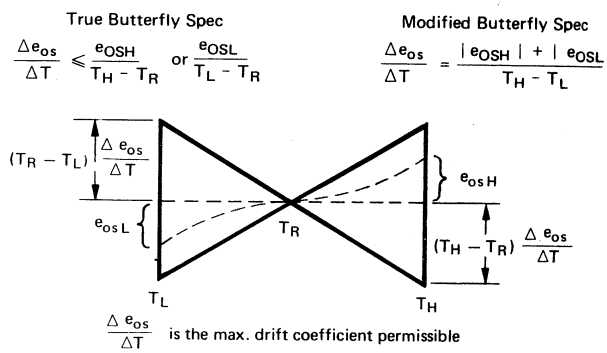
Common-Mode Voltage, Maximum
For differential-input amplifiers, the voltage at both inputs can swing about ground (power-supply common) level. *Common-mode voltage* is defined as any voltage (above or below ground) that could be observed at both inputs. The maximum common-mode voltage is defined as that voltage which will produce less than a specified value of common-mode error. This establishes the maximum input voltage for the voltage-follower connection.

Drift vs. Supply
Offset voltage, bias current, and difference current vary as supply voltage is varied. Usually, dc errors due to this effect are negligible compared to drift with temperature. No inference may be drawn from this low-frequency specification concerning the effects of rapid variation of voltage at the supply terminals.

Drift vs. Temperature
Offset voltage, bias current, and difference current all change, or "drift", from their initial values with temperature. This is

by far the most important source of error in most precision applications. The temperature coefficients (tempcos) of those parameters are all defined as the average slope over a specified temperature range. Drift can be a nonlinear function of temperature (though it is often quite linear over limited temperature ranges); the slopes generally are greater at the extremes of temperature than around normal ambient (+25°C), which generally means that for small temperature excursions in the vicinity of +25°C, the specification is conservative.

Analog Devices precision operational amplifiers are specified by three- (or more-) point measurements, at 25°C and at the high and low extremes of the range (T_H, T_L), with the amplifier adjusted to zero at room temperature. The sum of the magnitudes of the drifts in the two ranges must be less than the specified drift rate ($\mu V/^\circ C$ or $nA/^\circ C$) multiplied by the total temperature range (modified "butterfly"), or, in some cases, the magnitude of the drifts in both ranges must be less than the specified drift rate multiplied by the respective temperature ranges ("true butterfly").



The lowest-cost second-source IC amplifiers are specified only in terms of the maximum value of the parameter (e.g., offset voltage) over temperature in the specified range.

Drift vs. Time

Offset voltage, bias current, and difference current change with time as components age. It is important to realize that drift with time is random, and rarely — if ever — accumulates linearly for healthy devices. For example, voltage drift for a chopper-stabilized amplifier might be quoted at 1μV/day, whereas cumulative drift over 30 days might not exceed 5μV, or 15μV in a year (e.g., model 235). A convenient rule of thumb for extrapolation is to divide the drift for a stated interval by the square root of its ratio to any other interval of interest.

Full-Power Response

The large-signal and small-signal response characteristics of operational amplifiers differ substantially. An amplifier's output will not respond to large signal changes as fast as the small-signal bandwidth characteristics would predict, primarily because of slew-rate limiting in the output stages. Full-power response is specified in two ways: full linear response and full peak response. Full linear response is specified in terms of the maximum frequency, at unity closed-loop gain, for which a sinusoidal input signal will produce full output at rated load without exceeding a pre-determined distortion level. There is no industry-wide accepted value for the distortion level which determines the full-linear-response limitation, but we use 3% as a maximum acceptable limit for modules.

In many applications, the distortion caused by exceeding the full linear response can be comfortably ignored, but a more-serious effect (often overlooked) is an effect equivalent to a dc offset voltage that can be generated when full linear response is exceeded, due to rectification of the asymmetrical feedback waveform or overloading of the input stage by large distortion signals at the summing junction.

Another frequency response that is often of interest is the maximum frequency at which full output swing may be obtained, irrespective of distortion. This is termed "full peak response" and can often be found in a plot of output voltage swing vs. frequency.

Initial Bias Current

Bias current is defined as the current required at either input from an infinite source impedance to drive the output to zero (assuming zero common-mode voltage). For differential amplifiers, bias current is present at both the negative and the positive input. All Analog Devices specifications pertain to the *larger* of the two, *not the average.* For single-ended amplifiers (i.e., chopper types), bias current refers to the current at the input terminal.

Initial bias current, I_b, is the bias current at either input, specified at +25°C ambient with the input junctions *at normal operating temperature* (some manufacturers specify initial bias current at power turn-on. Such specifications may be misleading. For example, in FET-input amplifiers, bias current is doubled for each 10°C increase; since junction temperatures may warm up to 20°C or more above ambient, the "initial bias current" spec may be met only during a brief interval after the power is turned on and I_b may be quadrupled under ordinary operating conditions.)

Initial Difference Current

Difference current is defined as the difference between the bias currents at the two inputs. The input circuitry of differential amplifiers is generally symmetrical, so that bias currents at both inputs tend to be equal and tend to track with changes in temperature and supply voltage. Therefore, difference current is often about 0.1 times the bias current at either input, assuming that initial bias current has not been compensated at the input terminals. For amplifiers in which bias currents track, it is often possible to reduce voltage errors due to bias current and its variations by the use of equal resistance loads at both inputs.

Input Impedance

Differential input impedance is defined as the impedance between the two input terminals at +25°C, assuming that the error voltage is nulled or very near zero volts. To a first approximation, dynamic impedance can be represented by a capacitor in parallel with a resistor.

Common-mode impedance, expressed as a resistance in parallel with a capacitance, is defined as the impedance between each input and power-supply common, specified at +25°C. For most circuits, common-mode impedance on the negative input has little significance, except for the capacitance which it adds at the summing junction (one exception is electrometer circuitry). However, common-mode impedance on the plus input sets the upper limit on closed-loop input impedance for the non-inverting configuration. Common-mode impedance is a nonlinear function of both temperature and common-mode voltage. For FET-input amplifiers, common-mode resistance is reduced by a factor of two for each 10° of temperature rise. As a function of common-mode voltage, the resistive component is defined as the average resistance for a common-mode change from zero to the maximum common-mode voltage. Incremental resistance may be less than the specified average value, especially at full-scale for some FET-input amplifiers.

Input Offset Voltage

Offset voltage is defined as the voltage required at the input

from zero source impedance to drive the output to zero; its magnitude is measured by closing the loop (using low values of resistance) to establish a large fixed gain, measuring the amplified error at the output, and dividing the measured value by the gain.

The initial offset voltage is specified at +25°C and rated supply voltage. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer.

Input Noise

Input voltage- and current-noise characteristics can be specified and analyzed in much the same way as offset-voltage and bias-current characteristics. In fact, long-term drift can be considered as noise which occurs at very low frequencies. The primary difference is that, when evaluating noise performance, bandwidth must be considered. Also rms noise from different sources is summed by root-sum-of-squares, rather than linear, addition. Depending on the amplifier design, noise may have differing characteristics as a function of frequency, being dominated by "1/f noise", resistor noise, or junction noise, at various frequencies.

For this reason, several noise specifications are given. Low-frequency noise in the band 0.01 to 1Hz (or 0.1 to 10Hz) is specified as peak-to-peak, with a 3.3σ uncertainty, signifying that 99.9% of the observed peak-to-peak excursions will fall within the specified limits. Wideband noise is specified as rms. For some types, spectral-density plots or "spot noise", at specific frequencies, in $\mu V/\sqrt{Hz}$ or $pA/\sqrt{Hz}$, are provided.

Open-Loop Gain

Open-loop gain is defined as the ratio of a change of output voltage to the voltage applied between the amplifier inputs to produce the change. Gain is specified at dc. In many applications, the frequency dependence of gain is important; for this reason, the typical open-loop gain as a function of frequency is published for each amplifier type. See also *unity gain small-signal response.*

Overload Recovery

Overload recovery is defined as the time required for the output voltage to recover to the rated output voltage from a saturated condition caused by a 50% overdrive. Published specifications apply for low impedances and contain the assumption that overload recovery is not degraded by stray capacitance in the feedback network.

Rated Output

Rated output *voltage* is the minimum peak output voltage which can be obtained at rated current or a specified value of resistive load before clipping or out-of-spec nonlinearity occurs. Rated output *current* is the minimum guaranteed value of current supplied at the rated output voltage (or other specified voltage). Load impedances less than the specified (or implied) value can be used, but the maximum output voltage will decrease, distortion may increase, and the open-loop gain will be reduced. (All models are short-circuit protected to ground, and many are safe against shorts to the supplies.)

Settling Time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value. Settling time, therefore, includes the time required: for the signal to propagate through the amplifier, for the amplifier to slew from the initial value, recover from slew-rate-limited overload (if it occurs), and settle to a given error in the linear range. It may also include a "long tail" due to the time required to reach thermal equilibrium, or the settling time of compensation circuits. Settling time is usually specified for the condition of unity gain, relatively low impedance levels, and no (or a specified value of) capacitive loading, and any specified compensation. A full-scale unipolar step input is used, and both polarities are tested.

Although settling time can generally be grossly inferred from the other amplifier specifications (an amplifier that has extra-wide small-signal bandwidth, extra-fast slewing, and excellent full-power response may reasonably – but not always – be expected to have fast settling), the settling time cannot usually be rationally predicted from the other dynamic specifications.

Slewing Rate

The slewing rate of an amplifier, usually in volts per microsecond (V/μs), defines the maximum rate of change of output voltage for a large input step change.

Unity-Gain Small-Signal Response

Unity-gain small-signal response is the frequency at which the open-loop gain falls to 1V/V, or 0dB under a specified compensation condition. "Small signal" indicates that, in general, it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew-rate limiting or signal rectification. For amplifiers with symmetrical response for signals applied to either input, the dynamic behavior will be consistent for both inverting and non-inverting configurations. However, if feedforward compensation is used, fast response will be available only on the negative input, restricting fast applications of the device to the inverting mode.

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"Simple Rules for Choosing Resistance Values in Adder-Subtractor Circuits" by D. Sheingold, ANALOG DIALOGUE 10-1, 1976

"Specifying and Measuring a Low-Noise FET-Input IC Op Amp"
by Bill Maxwell, ANALOG DIALOGUE 8-2, 1974

USEFUL TUTORIAL MATERIAL IN DATA SHEETS

Electrometer Circuitry, see AD515 and Models 310/311

High-Speed Amplifiers, see AD518 and Models 50/51

Low-Drift Differential Op Amp Performance, see AD504

Low-Level Applications of Chopper-Stabilized Amplifiers:
Inverting, see Models 234, 235
Non-Inverting, see Model 261

Selection Guide
Operational Amplifiers

0 to 70°C TEMPERATURE RANGE

SPECIFICATIONS (typical at rated supply voltage and load, and T_A = 25°C, unless noted otherwise.)

General Purpose IC's	Offset Voltage mV max	$\Delta E_{os}/\Delta T$ $\mu V/^\circ C$ max	Bias Current nA max	Slew Rate V/μs	Page
AD301A	7.5	30	250	0.5 to 10*	17
AD741C Internal Comp.	6.0	No Spec.	500	0.5	65
AD201A -25°C to +85°C	2.0	15	75	0.5 to 10*	17
AD741 Internal Comp.	5.0	No Spec.	500	0.5	65

FET-Input Low Bias — Current IC's and Modules	Bias Current pA max	Offset Voltage mV max	$\Delta E_{os}/\Delta T$ $\mu V/^\circ C$ max	Slew Rate V/μs	
AD515J/K/L IC	0.3/0.15/0.075	3/1/1	50/15/25	0.3	41
52J/K Module	3	0.5	3/1	0.25 min	75
AD506J/K/L IC	15/10/5	3.5/1.5/1	75/25/10	3.0	21
AD503J/K IC	15/10	50/20	75/25	3.0	21
AD528J/K IC	30/15	3/1	50/25	50	57
AD540J/K IC	50/25	50/20	75/25	6.0	61

Electrometer IC's and Modules	Bias Current fA max	Offset Voltage mV max	$\Delta E_{os}/\Delta T$ $\mu V/^\circ C$ max	Slew Rate V/ms min	
310J/K Inverting Module	10	10	30/10	0.4	97
311J/K Noninverting Module	10	10	30/10	0.4	97
AD515J/K/L IC Differential	300/150/75	3/1/1	50/15/25	30.0	41

High Accuracy Low-Drift IC's and Modules	Offset mV max	$\Delta E_{os}/\Delta T$ $\mu V/^\circ C$ max	Bias Current nA max	Slew Rate V/μs	
AD517J/K/L IC	0.1/0.05/0.025	3/1/0.5	5/2/1	0.1	47
AD510J/K/L IC	0.1/0.05/0.025	3/1/0.5	25/13/10	0.1	37
AD504J/K/L/M IC	2.5/1.5/0.5/0.5	5/3/1/0.5	200/100/80/80	0.12 to 2.5*	25
52J/K Module	0.5	3/1	0.003	0.25 min	75
AD301AL IC	0.5	5.0	30	0.5 to 10*	17
AD515K IC	1.0	15	0.00015	0.3	41
AD741J/K/L IC	3/2/0.5	20/15/5	200/75/50	0.5	65

High Accuracy Low-Drift Chopper Amplifier Modules	Offset μV max	$\Delta E_{os}/\Delta T$ $\mu V/^\circ C$ max	Bias Current pA max	Slew Rate V/μs	
235J/K/L Inverting	25/25/15	0.5/0.25/0.1	100/50/50	0.3	85
234J/K/L Inverting	50/20/20	1.0/0.3/0.1	100	30	81
261J/K Low-Noise, Non-Inverting	25	0.3/0.1	300	100V/s	91
260J/K Low-Cost, Non-Inverting	25	0.3/0.1	300	100V/s	89

Fast, Wideband IC's and Modules	Settling Time to 0.1% μs	Slew Rate V/μs, min	$\Delta E_{os}/\Delta T$ $\mu V/^\circ C$ max	I_{BIAS} nA max	
50J/K Module	0.1 (INV, max)	500 (INV)	50/15	2	71
51A/B Module (-25°C to +85°C)	0.15 (INV, max)	400 (INV)	50/20	2	71
48J/K Fast Settling Module	0.5 (0.01%, max)	110 (INV)	50/15	0.05/0.025	69
AD509J/K/S IC	0.2/0.5 max/0.5 max	80/80/100	20/30/30	250/200/200	33
AD518J/K IC	0.8	50	10 typ/15 max	500/250	53
AD528J/K FET-Input IC	0.8	50	50/25	0.03/0.015	57
AD507J/K IC	0.9	20/25	30/15	25/15	29

High-Output Modules	max E_{out}	max I_{out}	$\Delta E_{os}/\Delta T$ $\mu V/^\circ C$	I_{BIAS} pA max	
171J/K	±140V	±10mA	50/15	50/20	77
50J/K	±10V	±100mA	50/15	2000	71
51A/B -25°C to +85°C	±10V	±100mA	50/20	2000	71

Isolated Op Amp Modules		
277J/K	Inverting, non-inverting, differential op-amp applications, Input offset drift 3/1$\mu V/^\circ C$ (nulled), bias current 20nA max, CMR 160dB min at dc, 120dB min at 60Hz, max CMV 3500V rms (60Hz, 1 min), ±2500V peak or dc, continuous, isolated power output, ±15mA @ ±15V.	133

*Inverting — Actual value depends on compensation.

−55°C to +125°C EXTENDED TEMPERATURE RANGE

SPECIFICATIONS (typical at rated supply voltage and load, and T_A = 25°C, unless noted otherwise.)

General Purpose IC's	Offset Voltage mV max	$\Delta E_{os}/\Delta T$ $\mu V/^\circ C$ max	Bias Current nA max	Slew Rate V/μs	Page
AD201A (−25°C to +85°C)	2.0	15	75	0.5 to 10*	17
AD741	5.0	No Spec.	500	0.5	65
AD101A	2.0	15	75	0.5 to 10*	17

FET- Input Low-Bias Current IC's	Bias Current pA max	Offset Voltage mV, max	$\Delta E_{os}/\Delta T$ $\mu V/^\circ C$ max	Slew Rate V/μs	
AD506S	10	1.5	50	3.0	21
AD503S	10	20	50	3.0	21
AD528S	15	1.0	25	50	57
AD540S	25	20	50	6.0	61

High Accuracy, Low-Drift IC's	Offset mV	$\Delta E_{os}/\Delta T$ $\mu V/^\circ C$	Bias Current nA max	Slew Rate V/μs	
AD517S	0.05	1.0	2.0	0.1	47
AD510S	0.05	1.0	13.0	0.1	37
AD504S	0.5	1.0 nulled	80.0	0.12	25
AD741S	2.0	15 untrimmed	75.0	0.5	65

Fast Wideband IC's	Settling Time μs to 0.1%	Slew Rate V/μs, min	$\Delta E_{os}/\Delta T$ $\mu V/^\circ C$ max	Bias Current nA max	
AD509S	0.5	100	30	200	33
AD518S	0.8	50	20	250	53
AD528S	0.8	50	25	0.015	57
AD507S	0.9	20	20	15	29

Fast Wideband High-Output Modules		Settling Time to 0.05%, μs	Slew Rate V/μs, min	$\Delta E_{os}/\Delta T$ $\mu V/^\circ C$ max	I_{BIAS} nA max	
51A/B	−25°C to +85°C Spec −55°C to +100°C Oper.	250 (INV)	400 (INV)	50/20	2	71

ISOLATED OP AMP MODULE

277A	−25°C to +85°C	Inverting, non-inverting, differential op-amp applications, input offset drift 3/1μV/°C (nulled), bias current 20nA max, CMR 160dB min @ dc 120dB min @ 60Hz, max CMV 3500V rms (60Hz, 1 min), ±2500V peak or dc, continuous, isolated power output, ±15mA @ ±15V	133

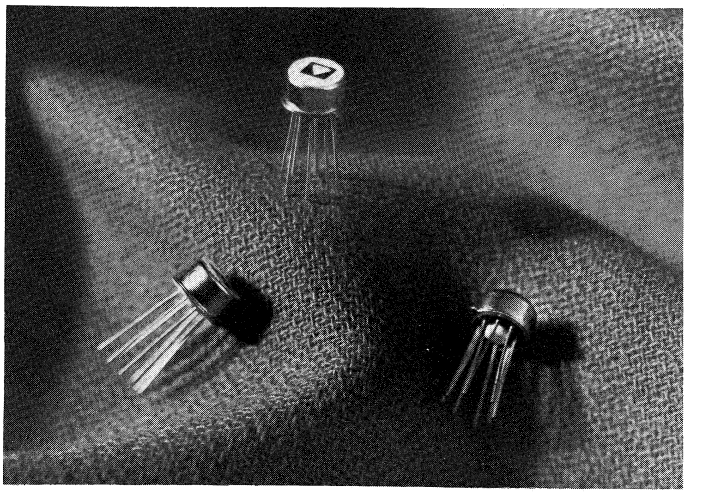
*Inverting – Actual value depends on compensation.

General Purpose Low Cost IC Operational Amplifier

AD101A, AD201A, AD301A, AD301AL

FEATURES

- **Low Bias and Offset Current**
- **Single Capacitor External Compensation for Operating Flexibility**
- **Nullable Offset Voltage**
- **No Latch-Up**
- **Fully Short Circuit Protected**
- **Wide Operating Voltage Range**

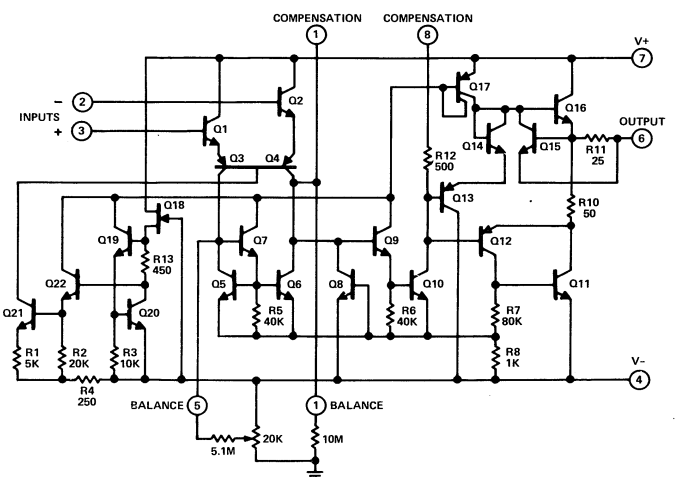


GENERAL DESCRIPTION

The Analog Devices AD101A, AD201A, AD301A and AD301AL are high performance monolithic operational amplifiers. All the circuits feature full short circuit protection, external offset voltage nulling, wide operating voltage range, and the total absence or "latch-up". Because frequency compensation is performed externally with a single capacitor (30pF maximum), the AD101A, AD201A, AD301A and AD301AL provide greater flexibility than internally compensated amplifiers since the degree of compensation can be fitted to the specific system application.

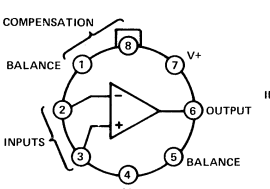
The AD101A and AD201A have identical specifications in the TO-99 package; the former guaranteed over the −55°C to +125°C temperature range, and the latter over −25°C to +85°C. The AD201A is also available in the mini-DIP package for high performance operation over the 0 to +70°C temperature range. The AD301A is specified for operation over the 0 to +70°C temperature range in both the TO-99 and mini-DIP packages. The AD301AL is the highest accuracy version of this series. Improved processing and additional electrical testing allow the user to achieve precision performance at low cost. The device provides substantially increased accuracy by reducing errors due to offset voltage (0.5mV max), offset voltage drift (5.0μV/°C max), bias current (30nA max), offset current (5nA max), voltage gain (80,000 min), PSRR (90dB min), and CMRR (90dB min). The AD301AL is also specified from 0 to +70°C and is available in the TO-99 can or 8-pin mini-DIP.

SCHEMATIC DIAGRAM

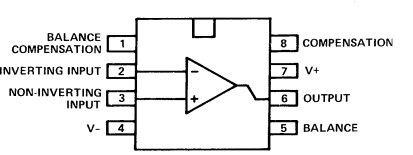


CONNECTION DIAGRAMS (TOP VIEW)

TO-99



Mini-DIP

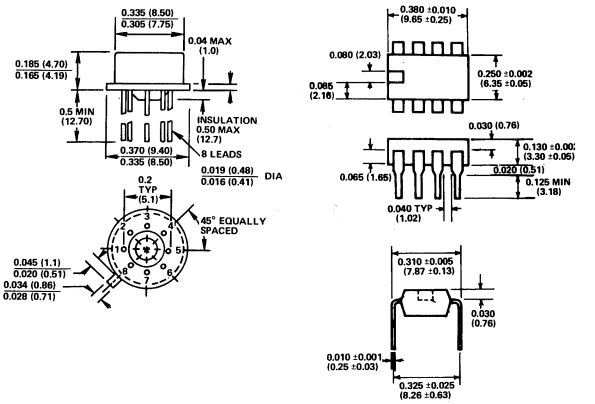


SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

ABSOLUTE MAXIMUM RATINGS	AD101A, AD201A, AD301A, AD301AL unless otherwise specified
Supply Voltage	
AD101A, AD201A	±22V
AD301A, AD301AL	±18V
Power Dissipation[1]	
TO-99 (Metal Can)	500mW
Dual In-Line (Mini-DIP)	500mW
Differential Input Voltage	±30V
Input Voltage[2]	±15V
Output Short Circuit Duration[3]	Indefinite
Operating Temperature Range	
AD101A	−55°C to +125°C
AD201A (TO-99)	−25°C to +85°C
AD201A (Mini-DIP)	0 to +70°C
AD301A, AD301AL	0 to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60sec)	300°C

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)[4]

Parameter	Conditions	AD101A/AD201A Min	AD101A/AD201A Typ	AD101A/AD201A Max	AD301A Min	AD301A Typ	AD301A Max	AD301AL Min	AD301AL Typ	AD301AL Max	Units
Input Offset Voltage	$R_S \leq 50k\Omega$		0.7	2.0		2.0	7.5		0.3	0.5	mV
Input Offset Current			1.5	10		3	50		3	5	nA
Input Bias Current			30	75		70	250		15	30	nA
Input Resistance		1.5	4		0.5	2		1.5	4		MΩ
Supply Current	V_S = ±20V		1.8	3.0							mA
	V_S = ±15V					1.8	3.0		1.8	3	mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 2k\Omega$	50	160		25	160		80	300		V/mV
The Following Specifications Apply Over the Operating Temperature Ranges[4]											
Input Offset Voltage	$R_S \leq 50k\Omega$			3.0			10		0.5	1	mV
Input Offset Current				20			70		5	10	nA
Average Temp. Coefficient of Input Offset Voltage	$T_A(\text{min}) \leq T_A \leq T_A(\text{max})$		3.0	15		6.0	30		2	5	μV/°C
Average Temp. Coefficient of Input Offset Current	+25°C≤T_A≤T_A(max)		0.01	0.1		0.01	0.3		0.01	0.1	nA/°C
	T_A(min)≤T_A≤+25°C		0.02	0.2		0.02	0.6		0.01	0.1	nA/°C
Input Bias Current				100			300		30	45	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 2k\Omega$	25			15			40	100		V/mV
Input Voltage Range	V_S = ±20V	±15									V
	V_S = ±15V				±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	80	96		70	90		90	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	80	96		70	96		90	100		dB
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±12	±14		±12	±14		±12	±14		V
	V_S = ±15V, R_L = 2kΩ	±10	±13		±10	±13		±10	±13		V
Supply Current	$T_A = T_A(\text{max})$, V_S = ±20V		1.2	2.5					1.8	3	mA

[1] The maximum desirable junction temperature of the AD101A is +150°C; that of the AD201A, AD301A and AD301AL is +100°C. For operating at elevated temperatures, devices must be derated based upon a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case. The thermal resistance of the Dual In-Line package is +160°C/W, junction to ambient.

[2] For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

[3] For the AD301A and AD301AL continuous short circuit is allowed for case temperatures to +70°C and ambient temperatures to +55°C.

[4] Unless otherwise specified, these specifications apply for supply voltages and ambient temperatures of ±5V to ±20V and −55°C to +125°C for the AD101A, ±5V to ±20V and −25°C to +85°C for the AD201AH (0 to +70°C for the AD201AN), and ±5V to ±15V and 0 to +70°C for the AD301A and AD301AL.

Specifications subject to change without notice.

ORDERING GUIDE

MODEL	TEMP RANGE	ORDER NUMBER
AD301AL	0 to +70°C	AD301AL*
AD201A	−25°C to +85°C	AD201A*
AD301A	0 to +70°C	AD301A*
AD101A	−55°C to +125°C	AD101AH
AD101A	−55°C to +125°C	AD101AF

* Add package type letter: H = TO-99, N = Mini-DIP

FREQUENCY COMPENSATION CIRCUITS

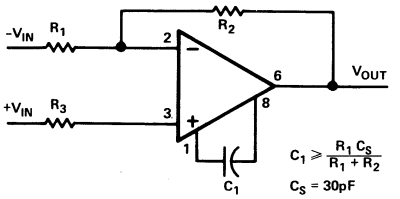


Figure 1. Single Pole Compensation

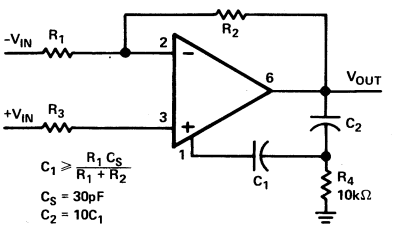


Figure 2. Two Pole Compensation

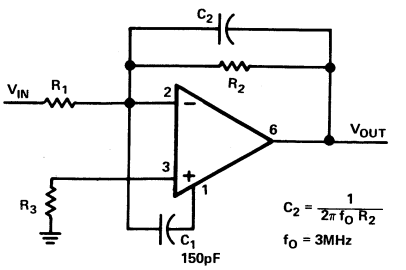
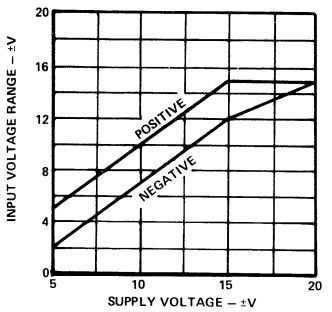
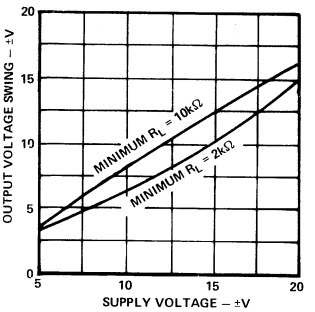


Figure 3. Feedforward Compensation

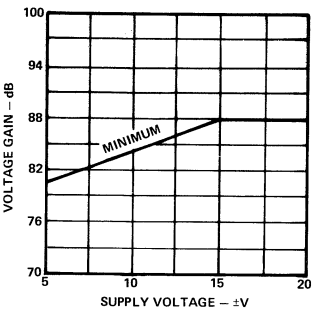
GUARANTEED PERFORMANCE CURVES (Curves apply over the Operating Temperature Ranges)



Input Voltage Range

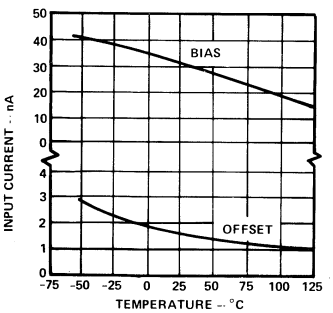


Output Swing

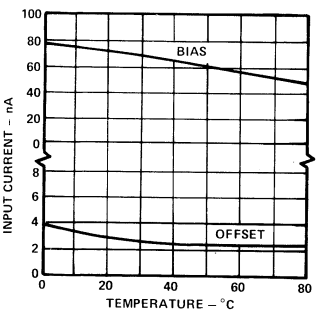


Voltage Gain

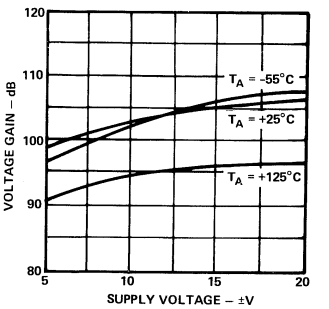
TYPICAL PERFORMANCE CURVES[4]



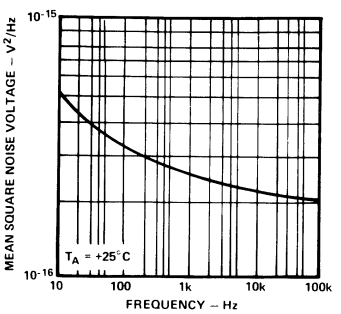
Input Current AD101A, AD201A



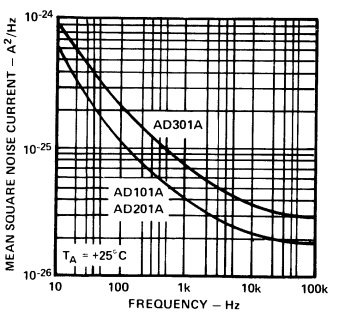
Input Current – AD301A



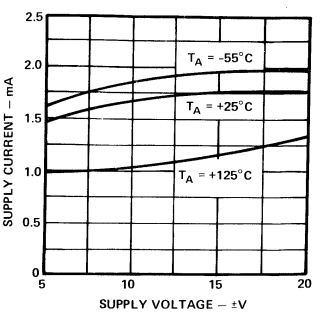
Voltage Gain



Input Noise Voltage

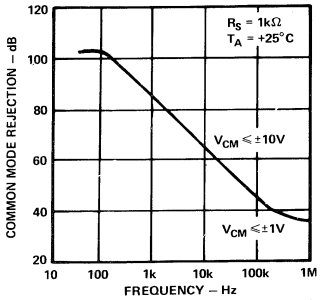


Input Noise Current

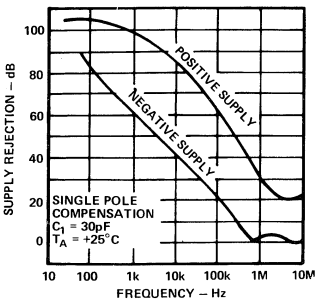


Supply Current

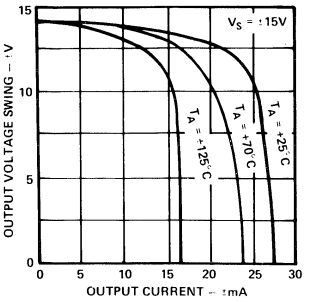
TYPICAL PERFORMANCE CURVES



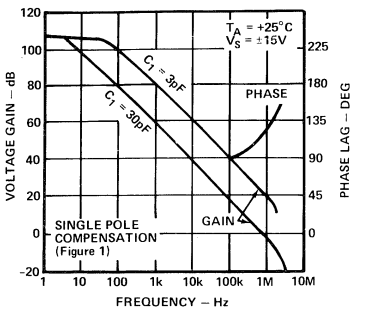
Common Mode Rejection



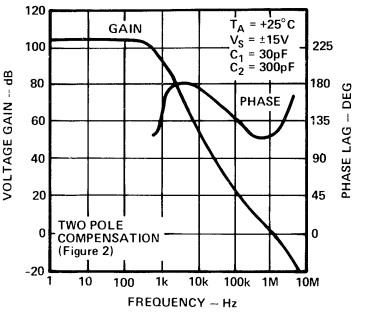
Power Supply Rejection



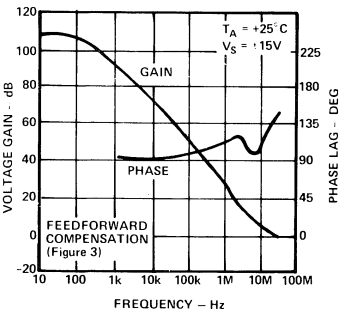
Current Limiting



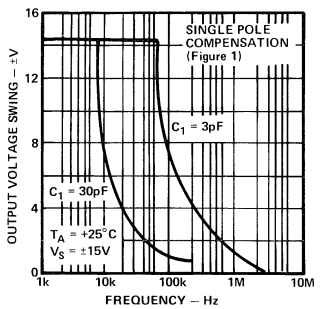
Open Loop Frequency Response



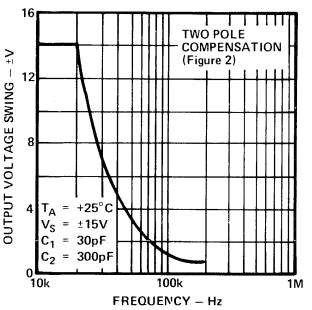
Open Loop Frequency Response



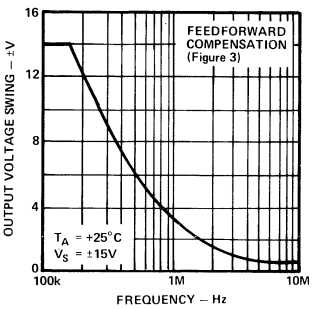
Open Loop Frequency Response



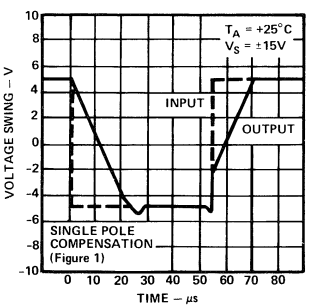
Large Signal Frequency Response



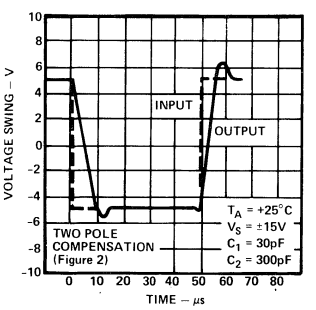
Large Signal Frequency Response



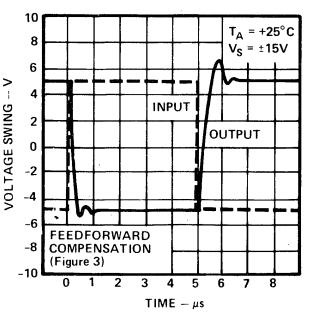
Large Signal Frequency Response



Voltage Follower Pulse Response



Voltage Follower Pulse Response



Inverter Pulse Response

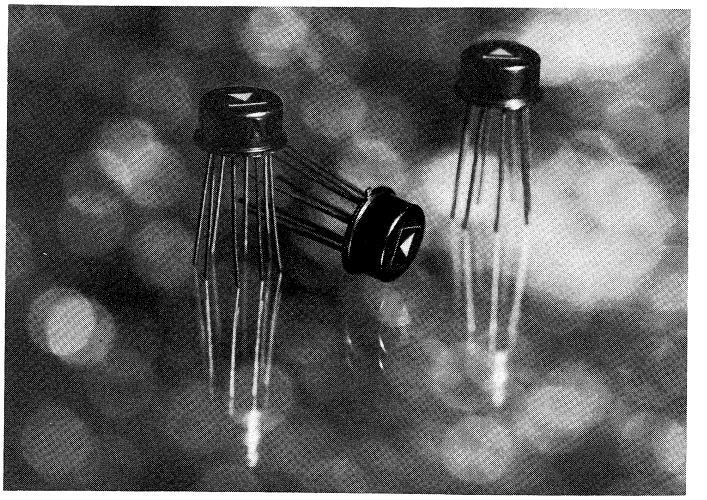
ANALOG DEVICES

High Accuracy Low Offset IC FET-Input Op Amps

AD503, AD506

FEATURES

Low I_b: 15pA max (AD503J, AD506J)
5pA max (AD506L)
Low V_{OS}: 1mV max (AD506L)
Low Drift: 25μV/°C max (AD503K, AD506K)
10μV/°C max (AD506L)



PRODUCT DESCRIPTION

The AD503J/AD506J, AD503K/AD506K, AD506L and AD503S/AD506S are IC FET input op amps which provide the user with input currents of a few pA, high overall performance, low cost, and accurately specified, predictable operation. The devices achieve maximum bias currents as low as 5pA, minimum gain of 75,000, CMRR of 80dB, and a minimum slew rate of 3V/μs. They are free from latch-up and are short circuit protected. No external compensation is required as the internal 6dB/octave rolloff provides stability in closed loop applications.

The AD503 is suggested for all general purpose FET input amplifier requirements where low cost is of prime importance. The AD506, with specifications otherwise similar to the AD503, offers significant improvement in offset voltage and nulled offset voltage drift by supplementing the AD503 configuration with internal laser trimming of thin film resistors to provide typical offset voltages below 1mV.

Both the AD503 and AD506 provide performance comparable to modular FET op amps. Because of their monolithic construction, however, their cost is significantly below that of modules, and becomes even lower in large quantities.

The AD503 and AD506 are especially designed for applications involving the measurement of low level currents or small voltages from high impedance sources, in which bias current can be a primary source of error. Input bias current contributes to error in two ways: (1) in current measuring configurations, the bias current limits the resolution of a current signal; (2) the bias current produces a voltage offset which is proportional to the value of input resistance (in the case of an inverting configuration) or source impedance (when the noninverting "buffer" connection is used). The AD503 and AD506 IC FET input amplifiers, therefore, are of use where small currents are to be measured or where relatively low voltage drift is necessary despite large values of source resistance.

All the circuits are supplied in the TO-99 package; the AD503J, K and AD506J, K and L are specified for 0 to +70°C temperature range operation; the AD503S and AD506S for operation from -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD503 and AD506 op amps meet their published input bias current and offset voltage specs after full warmup. Conventional high speed IC testing does not allow for self-heating of the chip due to internal power dissipation under operating conditions.
2. The bias currents of the AD503 and AD506 are specified as a maximum for *either* input. Conventional IC FET op amps generally specify bias currents as the average of the two input currents.
3. Offset voltage nulling of the AD503 and AD506 is accomplished without affecting the operating current of the FET's and results in relatively small changes in temperature drift characteristics. The additional drift induced by nulling is only ±0.8μV/°C per millivolt of nulled offset for the AD506 and ±2.0μV/°C per millivolt of nulled offset for the AD503, compared to several times this for other IC FET op amps.
4. The gain of the AD503 and AD506 is measured with the offset voltage nulled. Nulling a FET input op amp can cause the gain to decrease below its specified limit. The gain of the AD503 and AD506 is fully guaranteed with the offset voltage both nulled and unnulled.
5. Bootstrapping of the input FET's achieves a superior CMRR of 80dB, while reducing bias currents and maintaining them constant through the CMV range.
6. To maximize the reliability inherent in IC construction, every AD503/AD506 is stored for 48 hours at 200°C, temperature cycled from -65°C to +125°C, and receives a high impact shock test. All guaranteed dc parameters are 100% computer tested, including offset voltage drift. AC performance and noise parameters are continually reviewed.

SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise noted)

PARAMETER	AD503J	AD503K	AD503S
OPEN LOOP GAIN[1]			
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	20,000 min (50,000 typ)	50,000 min (120,000 typ)	**
T_A = min to max	15,000 min	40,000 min	25,000 min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±13V typ)	*	*
@ R_L = 10kΩ, T_A = min to max	±12V min (±14V typ)	*	*
Load Capacitance[2]	750pF	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	100kHz	*	*
Slew Rate, Unity Gain	3.0V/μs min (6.0V/μs typ)	*	*
Settling Time, Unity Gain (to 0.1%)	10μs	*	*
INPUT OFFSET VOLTAGE[3]	50mV max (20mV typ)	20mV max (8mV typ)	**
vs. Temperature, T_A = min to max	75μV/°C max (30μV/°C typ)	25μV/°C max (10μV/°C typ)	50μV/°C max (20μV/°C typ)
vs. Supply, T_A = min to max	400μV/V max (200μV/V typ)	200μV/V max (100μV/V typ)	**
INPUT BIAS CURRENT			
Either Input[4]	15pA max (5pA typ)	10pA max (2.5pA typ)	**
INPUT IMPEDANCE			
Differential	$10^{11}\ \Omega \| 2pF$	*	*
Common Mode	$10^{12}\ \Omega \| 2pF$	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	15μV (p-p)	*	*
5Hz to 50kHz	5.0μV (rms)	*	*
f = 1kHz (spot noise)	30.0nV/√Hz	*	*
INPUT VOLTAGE RANGE			
Differential[5]	±3.0V	*	*
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{IN} = ±10V	70dB min (90dB typ)	80dB min (90dB typ)	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	±(5 to 22)V
Quiescent Current	7mA max (3mA typ)	*	*
TEMPERATURE			
Operating, Rated Performance	0 to +70°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*

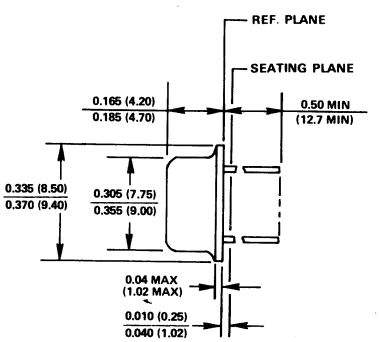
NOTES:
[1] Open Loop Gain is specified with V_{OS} both nulled and unnulled.
[2] A conservative design would not exceed 500pF of load capacitance.
[3] Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[4] Bias current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
[5] See comments in Input Considerations section.

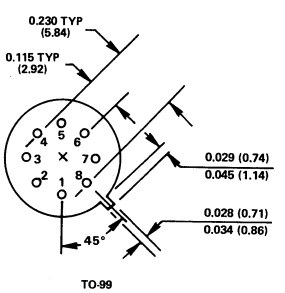
*Specifications same as for AD503J.
**Specifications same as for AD503K.
Specifications subject to change without notice.

AD506J	AD506K	AD506L	AD506S
*	**	75,000 min (100,000 typ)	**
*	**	50,000 min	25,000 min
*	*	*	*
*	*	*	*
1000pF	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
3.5mV max (1.0mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.4mV typ)	1.5mV max (0.5mV typ)
*	**	10μV/°C max (5μV/°C typ)	50μV/°C max (20μV/°C typ)
**	100μV/V max (50μV/V typ)	100μV/V max (50μV/V typ)	100μV/V max (50μV/V typ)
*	**	5pA max (2pA typ)	**
*	*	*	*
*	*	*	*
40μV (p-p)	*	*	*
8μV (rms)	*	6μV (rms)	*
80nV/√Hz	*	25nV/√Hz	*
±4V	*	*	*
*	*	*	*
*	**	**	**
*	*	*	*
*	*	*	±(5 to 22)V
7mA max (5mA typ)	*	*	*
*	*	*	-55°C to +125°C
*	*	*	*

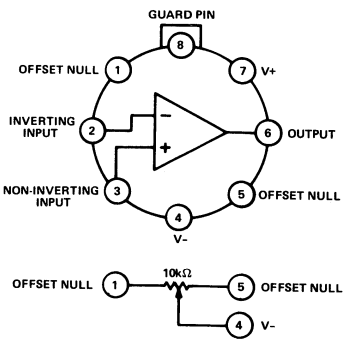
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).





PIN DESIGNATIONS



APPLICATIONS CONSIDERATIONS

Bias Current

Most IC FET op amp manufacturers specify maximum bias currents as the value immediately after turn-on. Since FET bias currents double every 10°C and since most FET op amps have case temperature increases of 15°C to 20°C above ambient, initial "maximum" readings may be only ¼ of the true warmed up value. Furthermore, most IC FET op amp manufacturers specify I_b as the average of both input currents, sometimes resulting in twice the "maximum" bias current appearing at the input being used. The total result is that 8X the expected bias current may appear at either input terminal in a warmed up operating unit.

The AD503 and AD506 specify maximum bias currents at either input after warmup, thus giving the user the values he expected.

Improving Bias Current Beyond Guaranteed Values

Bias currents can be substantially reduced in the AD503 and AD506 by decreasing the junction temperature of the device. One technique to accomplish this is to reduce the operating supply voltage. This procedure will decrease the power dissipation of the device, which will in turn result in a lower junction temperature and lower bias currents. The supply voltage effect on bias current is shown in Figure 1.

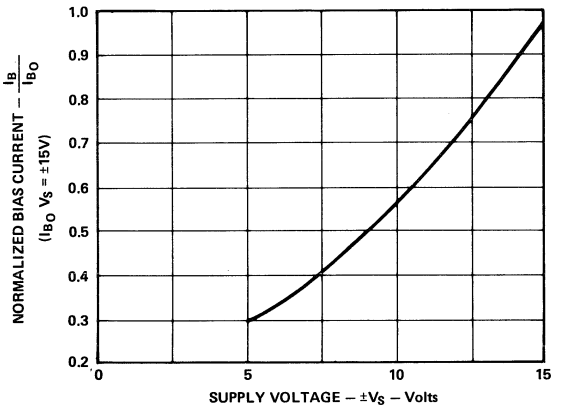


Figure 1. Normalized Bias Current vs. Supply Voltage

Operation of the AD503K and AD506K at ±5V reduces the warmed up bias current by 70% to a typical value of 0.75pA.

A second technique is the use of a suitable heat sink. Wakefield Engineering Series 200 heat sinks were selected to demonstrate this effect. The characteristic bias current vs. case temperature above ambient is shown in Figure 2. Bias current has been normalized with unity representing the 25°C free air reading.

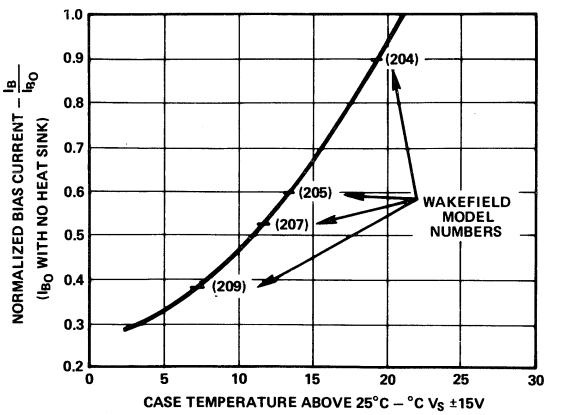


Figure 2. Normalized Bias Current vs. Case Temperature

Note that the use of the model 209 heat sink reduces warmed up bias current by 60% to 1.0pA in the AD503/AD506K.

Both of these techniques may be used together for obtaining lower bias currents. Remember that loading the output can also affect the power dissipation.

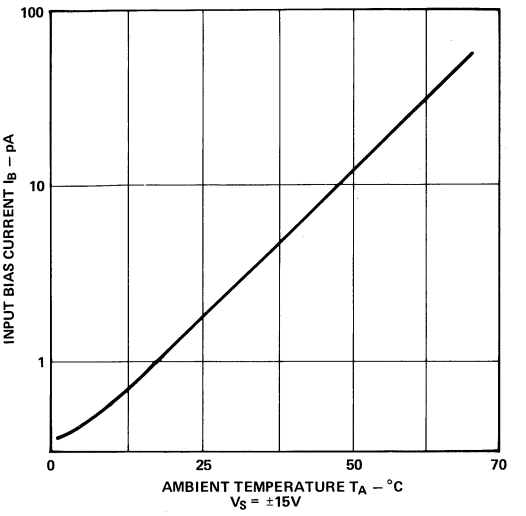


Figure 3. Input Bias Current vs. Temperature

Input Considerations

The common mode input characteristic is shown in Figure 4. Note that positive common mode inputs up to +13.5 volts and negative common mode inputs to $-V_S$ are permissible, without incurring excessive bias currents. To prevent possible damage to the unit, do not exceed $V_{CM} = V_S$.

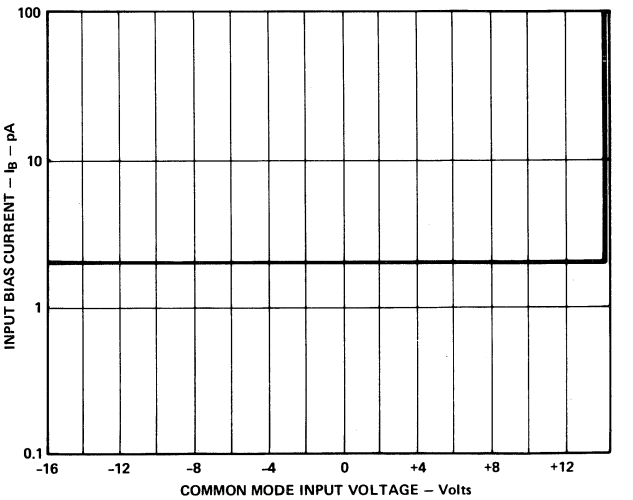


Figure 4. Input Bias Current vs. Common Mode Voltage

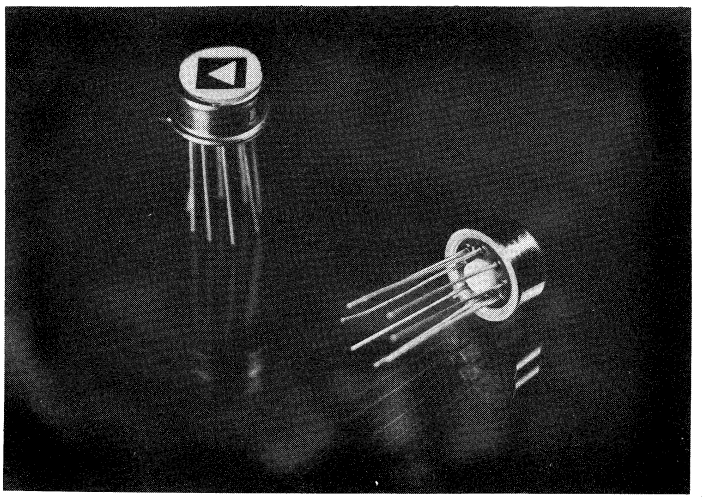
Like most other FET input op amps, the AD503 and AD506 display a degraded bias current specification when operated at moderate differential input voltages. The AD503 maintains its specified bias current up to a differential input voltage of ±3V typically, while the AD506's bias current performance is not significantly degraded for $V_{diff} \leqslant 4V$ typically. Above V_{diff} = ±3V in the AD503 and V_{diff} = ±4V in the AD506, the bias current will increase to approximately 400μA. This is not a failure mode. Above ±10V differential input voltage, the bias current will increase 100μA/V_{diff} (in volts), and other parameters may suffer degradation.

ANALOG DEVICES

High Accuracy IC Operational Amplifier

AD504

FEATURES
Low V_{OS}: 500μV max (AD504M)
High Gain: 10^6 min (AD504L, M, S)
Low Drift: 0.5μV/°C max (AD504M)
Free of Popcorn Noise



PRODUCT DESCRIPTION

The Analog Devices AD504J, K, L, M and S are the first IC operational amplifiers to provide ultra-low drift and extremely high gain comparable to that of modular amplifiers and the frequency response and slew rate of general purpose IC op amps. A new double integrator circuit concept combined with a precise thermally balanced layout achieves gain greater than 10^6, offset voltage drift of less than 1μV/°C, small signal unity gain bandwidth of 300kHz, and slew rate of 0.12V/μs. Because of monolithic construction, the cost of the AD504 is significantly below that of modules, and becomes even lower with larger quantity requirements. The amplifier is externally compensated for unity gain with a single 470pF capacitor; no compensation is required for gains above 500. The inputs are fully protected, which permits differential input voltages of up to $\pm V_S$ without voltage gain or bias current degradation due to reverse breakdown. The output is also protected from short circuits to ground and/or either supply voltage and is capable of driving 1000pF of load capacitance. The AD504J, K, L and M are supplied in the hermetically sealed TO-99 package and are specified for operation over the 0 to +70°C temperature range. The AD504S is specified over the -55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

1. Fully guaranteed and 100% tested 1μV/°C maximum voltage drift combined with voltage offset of 500μV (AD504L).
2. Fully protected input ($\pm V_S$) and output circuitry. The input protection circuit prevents offset voltage and bias current degradation due to reverse breakdown, and is of critical importance in this type of device whose overall performance is strongly dependent on front-end stability.
3. Single capacitor compensation eliminates elaborate stabilizing networks while providing flexibility not possible with an internally compensated op amp. This feature allows bandwidth to be optimized by the user for his particular application.
4. High gain is maintained independent of offset nulling, power supply voltage and load resistance.
5. Bootstrapping of the critical input transistor quad produces CMRR and PSRR compatible with the tight 1μV/°C drift. CMRR and PSRR are both in the vicinity of 120dB.
6. Noise performance is closely monitored at Outgoing QC to insure compatibility with the low error budgets afforded by the performance of all other parameters.
7. Every AD504 is stored for 48 hours at 200°C, temperature cycled 10 times from -65°C to +200°C and subjected to a high G shock test to assure reliability and long term stability.
8. The 100 piece price of the AD504 is 1/3 to 1/2 less than that of modular low drift operational amplifiers and is competitive with the price of less accurate IC op amps.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

PARAMETER	AD504J	AD504K	AD504L
OPEN LOOP GAIN			
V_{OS} = ±10V, $R_L \geq 2k\Omega$	250,000 min (4 x 10^6 typ)	500,000 min (4 x 10^6 typ)	10^6 min (8 x 10^6 typ)
@ T_A = 0 to +70°C	125,000 min (10^6 typ)	250,000 min (10^6 typ)	500,000 min (10^6 typ)
OUTPUT CHARACTERISTICS			
Voltage at $R_L \geq 2k\Omega$, T_A = 0 to +70°C	±10V min (±13V typ)	*	*
Load Capacitance	1000pF	*	*
Output Current	10mA min	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal, C_c = 390pF	300kHz	*	*
Full Power Response, C_c = 390pF	1.5kHz	*	*
Slew Rate, Unity Gain, C_c = 390pF	0.12V/μs	*	*
INPUT OFFSET VOLTAGE			
Initial Offset, $R_S \leq 10k$	2.5mV max (0.5mV typ)	1.5mV max (0.5mV typ)	0.5mV max (0.2mV typ)
vs Temp, T_A = 0 to +70°C, V_{OS} nulled	5.0μV/°C max (0.5μV/°C typ)	3.0μV/°C max (0.5μV/°C typ)	1.0μV/°C max (0.3μV/°C typ)
T_A = 0 to +70°C, V_{OS} unnulled†	10μV/°C max (1.5μV/°C typ)	5.0μV/°C max (1.5μV/°C typ)	2.0μV/°C max (1.0μV/°C typ)
vs Supply	25μV/V max	15μV/V max	10μV/V max
@ T_A = 0 to +70°C	40μV/V	25μV/V max	15μV/V max
vs Time	20μV/mo	15μV/mo	10μV/mo
INPUT OFFSET CURRENT			
@ T_A = 25°C	40nA max	15nA max	10nA max
INPUT BIAS CURRENT			
Initial	200nA max	100nA max	80nA max
T_{min} to T_{max}	300nA max	150nA max	100nA max
vs Temp, T_{min} to T_{max}	300pA/°C	250pA/°C	200pA/°C
INPUT IMPEDANCE			
Differential	0.5MΩ	1.0MΩ	1.3MΩ
Common Mode	100MΩ‖4pF	*	*
INPUT NOISE			
Voltage, 0.01 to 10Hz	1.0μV (p-p)	*	*
100Hz	10nV/√Hz(rms)	*	*
1kHz	8nV/√Hz(rms)	*	*
Current, 0.01 to 10Hz	50pA(p-p)	*	*
100Hz	0.6pA/√Hz(rms)	*	*
1kHz	0.5pA/√Hz(rms)	*	*
INPUT VOLTAGE RANGE			
Differential or Common Mode, Max Safe	$\pm V_S$	*	*
Common Mode Rejection, V_{IN} = ±10V	94dB min (120dB typ)	100dB min (120dB typ)	110dB min (120dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Current, Quiescent	±4.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)
TEMPERATURE RANGE			
Operating, Rated Performance	0 to +70°C	*	*
Storage	-65°C to +150°C	*	*

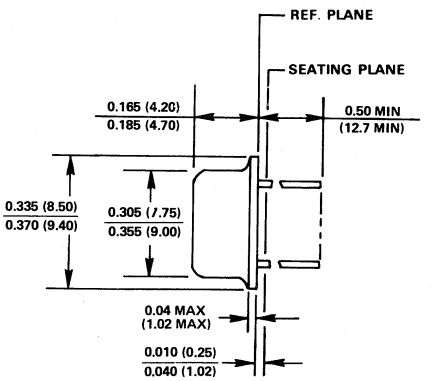
*Specifications same as for AD504J.
†This parameter is not 100% tested. Typically, 90% of the units meet this limit.
Specifications subject to change without notice.

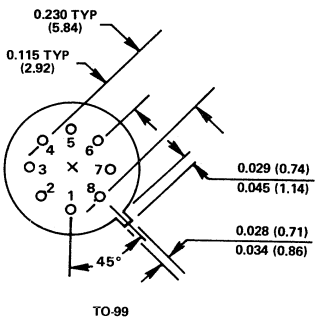
NOTE
Analog Devices 100% tests and guarantees all specified maximum and minimum limits. Certain parameters, because of the relative difficulty and cost of 100% testing, have been specified as "typical" numbers. At ADI, "typical" numbers are subjected to rigid statistical sampling and outgoing quality control procedures, resulting in "typicals" that are indicative of the performance that can be expected by the user.

AD504M	AD504S
10^6 min (8 x 10^6 typ)	10^6 min (8 x 10^6 typ)
500,000 min (10^6 typ)	250,000 min
*	*
*	*
*	*
*	*
*	*
*	*
*	*
0.5mV max (0.2mV typ)	0.5mV max
0.5μV/°C max (0.2μV/°C typ)	1.0μV/°C max (0.3μV/°C typ)
1.0μV/°C max (0.5μV/°C typ)	2.0μV/°C max (1.0μV/°C typ)
10μV/V max	10μV/V max
15μV/V max	20μV/V max
10μV/mo	10μV/mo
10nA max	10nA max
80nA max	80nA max
100nA max	200nA max
200pA/°C	200pA/°C
1.3MΩ	1.3MΩ
*	*
0.6μV (p-p) max	*
10nV/$\sqrt{Hz}$ max	*
9nV/$\sqrt{Hz}$ max	*
1.3pA/$\sqrt{Hz}$ max	*
0.6pA/$\sqrt{Hz}$ max	*
0.3pA/$\sqrt{Hz}$ max	*
*	*
110dB min (120dB typ)	110dB min (120dB typ)
*	*
*	*
±3.0mA max (±1.5mA typ)	±3mA max (±1.5mA typ)
*	-55°C to +125°C
*	-65°C to +150°C

OUTLINE DIMENSIONS

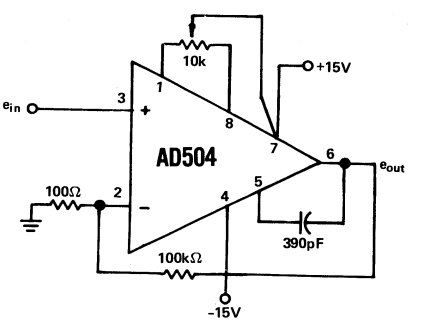
Dimensions shown in inches and (mm).





TO-99

PIN CONNECTIONS



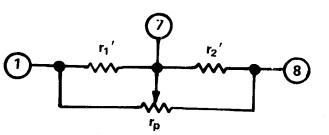


Figure 1. High Resolution, High Stability Nulling Circuit

DYNAMIC PERFORMANCE

The dynamic performance of the AD504, although comparable to most general purpose op amps, is superior to most low drift op amps. Figure 2 shows the small signal frequency response for both open and closed loop gains for a variety of compensating values. Note that the circuit is completely stable for C_c = 390pF with a -3dB bandwidth of 300kHz; with C_c = 0, the -3dB bandwidth is 50kHz, at a gain of 2000.

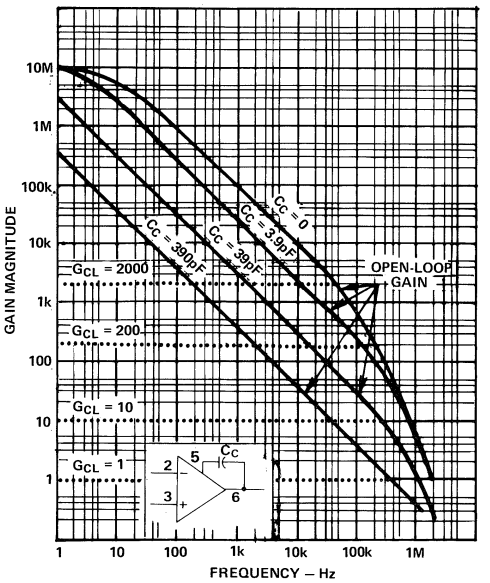


Figure 2. Small Signal Gain vs Frequency

NOISE CHARACTERISTICS

An op amp of the caliber of the AD504 must have correspondingly low noise levels if the user is to be assured he will be able to take advantage of its exceptional dc characteristics. Of primary importance in this type of amplifier is the absence of popcorn noise and minimum I/f or "flicker" noise in the 0.01Hz to 10Hz frequency band. Sample noise testing is done on every lot to guarantee that better than 90% of all devices will meet the noise specifications.

Separate voltage and current noise levels referred to the input are specified to enable the designer to calculate or optimize signal-to-noise ratio based on any desired source resistance. The spot noise figures are useful in determining total wideband noise over any desired bandwidth. (See Figure 3)

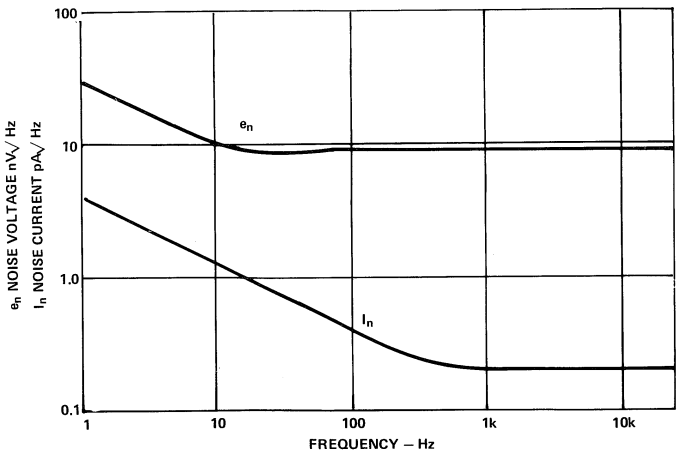


Figure 3. Spot Noise vs Frequency

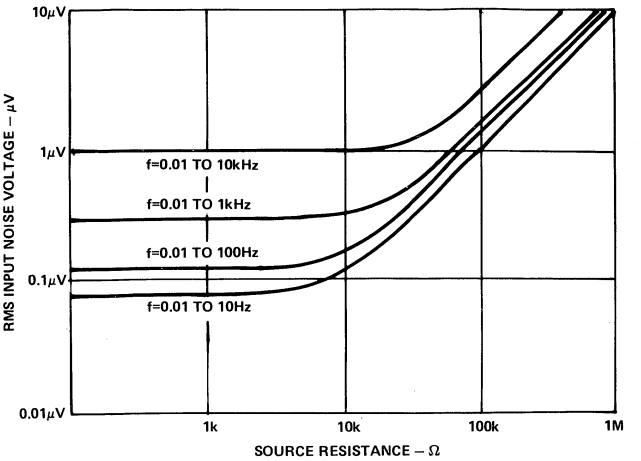


Figure 4. RMS Noise vs Source Resistance

NULLING THE AD504

Since calculations show that superior drift performance can be realized with the AD504, special care should be taken to null it in the most advantageous manner. Using the actual values of resistors in the AD504, it is possible to calculate, under worst case conditions, that the total adjustment range of the AD504 is approximately 8mV. Since the amplifier may often be trimmed to within 1μV, this represents an adjustment of 1 part in 8000. This type of accuracy would require a pot with 0.0125% resolution and stability. Because of the problems of obtaining a pot of this stability, a slightly more sophisticated nulling operation is recommended for applications where offset drift is critical (See Figure 1.)

NULLING PROCEDURE

1. Null the offset to zero using a commercially available pot (suggest r_p = 10kΩ).
2. Measure pot halves r_1 and r_2.
3. Calculate . . . . . .

$$r'_1 = \frac{r_1 \times 50k\Omega}{50k\Omega - r_1}, \quad r'_2 = \frac{r_2 \times 50k\Omega}{50k\Omega - r_2}$$

4. Insert r'_1 and r'_2 (closest 1% fixed metal film resistors).
5. Use an industrial quality 100kΩ pot (r_p) to fine tune the trim.

For applications in which stringent nulling is not required, the user may choose a simplified nulling scheme as shown in Figure 5. For best results the wiper of the potentiometer should be connected directly to pin 7 of the op amp. This is true for both nulling schemes.

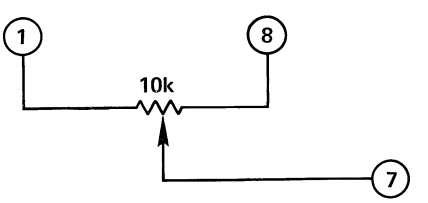
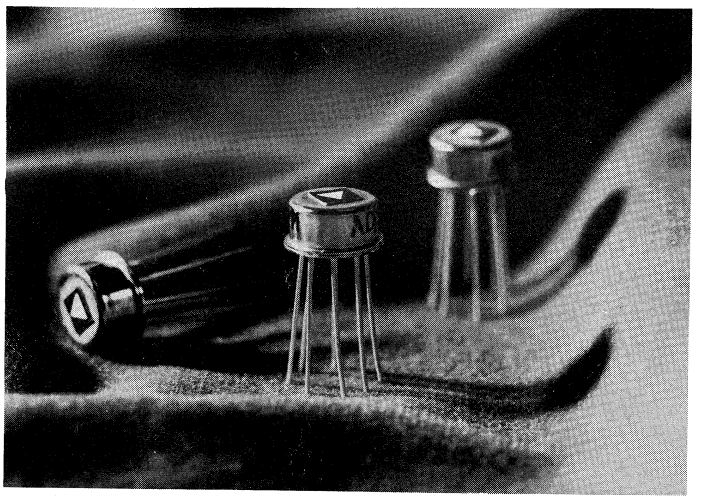


Figure 5. Simplified Nulling Circuit

IC, Wideband, Fast Slewing, General Purpose Operational Amplifier

AD507

FEATURES
Gain Bandwidth: 100MHz
Slew Rate: 20V/μs min
I_B: 15nA max (AD507K)
V_{os}: 3mV max (AD507K)
V_{os} Drift: 15μV/°C max (AD507K)
High Capacitive Drive



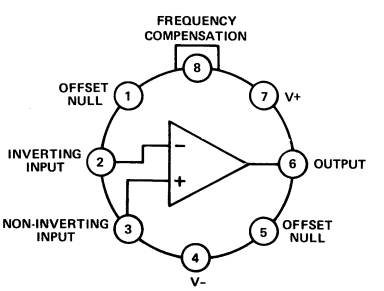
PRODUCT DESCRIPTION

The Analog Devices AD507J, K and S are low cost monolithic operational amplifiers that are designed for general purpose applications where high gain bandwidth and high speed are significant requirements. The devices also provide excellent dc performance with low input offset voltage, low offset voltage drift and low bias current. The AD507 is a low cost, high performance alternative to a wide variety of modular and IC op amps; a brief review of the specifications confirms its outstanding price/performance characteristics.

The AD507 is recommended for use where low cost and all around performance, especially at high frequencies, are needed. It is particularly well suited as a fast, high impedance comparator, integrator or wideband amplifier and in sample/hold circuits. It is unconditionally stable for all closed loop gains above 10 without external compensation; the frequency compensation terminal is used for stability at lower closed loop gains. The circuit is short circuit protected and offset voltage nullable. The AD507J and K are specified over the 0 to +70°C temperature range, the AD507S over the full military temperature range, −55°C to +125°C. All devices are packaged in the hermetic TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Excellent dc and ac performance combined with low cost.
2. The AD507 will drive several hundred pF of output capacitance without oscillation.
3. All guaranteed dc parameters, including offset voltage drift, are 100% tested.
4. To insure compliance with gain bandwidth and slew rate specifications, all devices are tested for ac performance characteristics.
5. To take full advantage of the inherent high reliability of IC's, every AD507S is stored for 48 hours @ +150°C, temperature cycled from −65°C to +150°C and receives a high impact shock test.



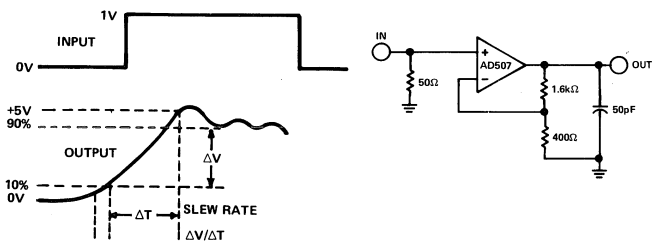
TO-99 PIN CONFIGURATION

SPECIFICATIONS (typical at +25°C and ±15V dc, unless otherwise noted)

PARAMETER	AD507J	AD507K	AD507S
OPEN LOOP GAIN			
R_L = 2kΩ, C_L = 50pF	80,000 min (150,000 typ)	100,000 min (150,000 typ)	100,000 min (150,000 typ)
@ T_{min} to T_{max}	70,000 min	85,000 min	70,000 min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, C_L = 50pF, T_{min} to T_{max}	±10V min (±12V typ)	*	±10V min (±12V typ)
Current @ V_o = ±10V	±10mA min (±20mA typ)	*	±15mA min (±22mA typ)
Short Circuit Current	25mA	*	25mA
FREQUENCY RESPONSE			
Unity Gain, Small Signal			
@ A = 1 (open loop)	35MHz	*	*
@ A = 100 (closed loop)	100MHz	*	*
Full Power Response	320kHz min (600kHz typ)	400kHz min (600kHz typ)	400kHz min (600kHz typ)
Slew Rate	±20V/μs min (±35V/μs typ)	±25V/μs min (±35V/μs typ)	20V/μs min (35V/μs typ)
Settling Time (to 0.1%)	900ns	*	*
INPUT OFFSET VOLTAGE			
Initial	5.0mV max (3.0mV typ)	3.0mV max (1.5mV typ)	4mV max (0.5mV typ)
Avg vs Temp, T_{min} to T_{max}	15μV/°C	15μV/°C max (8μV/°C typ)	20μV/°C max (8μV/°C typ)
vs Supply, T_{min} to T_{max}	200μV/V max	100μV/V max	100μV/V max
INPUT BIAS CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
INPUT OFFSET CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
Avg vs Temp, T_{min} to T_{max}	0.5nA/°C	0.2nA/°C	0.2nA/°C
INPUT IMPEDANCE			
Differential	40MΩ min (300MΩ typ)	*	65MΩ min (50MΩ typ)
Common Mode	1000MΩ	*	*
INPUT VOLTAGE NOISE			
f = 10Hz	100nV/√Hz	*	*
f = 100Hz	30nV/√Hz	*	*
f = 100kHz	12nV/√Hz	*	*
INPUT VOLTAGE RANGE			
Differential, Max Safe	±12.0V	*	*
Common Mode Voltage Range, T_{min} to T_{max}	±11.0V	*	*
Common Mode Rejection @ ±5V, T_{min} to T_{max}	74dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	4.0mA max (3.0mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-55°C to +125°C
Operating	-25°C to +85°C	*	-65°C to +150°C
Storage	-65°C to +150°C	*	*

*Specifications same as AD507J.

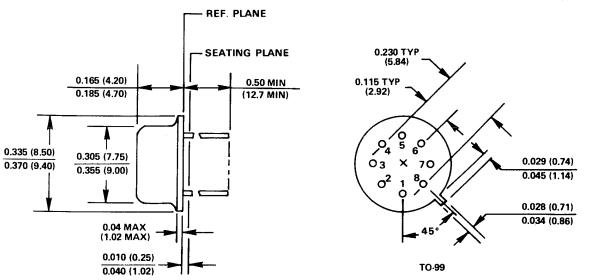
Specifications subject to change without notice.



Slew Rate Definition and Test Circuit

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



APPLICATION CONSIDERATIONS

The AD507 combines excellent dc characteristics and dynamic performance with ease of application. Because it is a wideband, high speed amplifier, care should be exercised in its stabilization. Several practical stabilization techniques are suggested to insure proper operation and minimize user experimentation.

GENERAL PURPOSE WIDEBAND COMPENSATION

The following considerations are intended to provide guidance in critical wideband applications. While not necessary in all cases, the considerations are of prime importance for the user attempting to obtain the highest performance from his circuit design.

High Gain Conditions

The AD507 is fully compensated *internally* for all closed loop gains above 10; however, it is necessary to load the amplifier with 50pF. In many applications this minimum capacitive load will be provided by the load or by a cable at the output of the AD507, making an additional 50pF unnecessary. Figure 1 shows the suggested configuration for general purpose use for closed loop gains above 10.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD507 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagrams show each individual capacitor directly connected to the appropriate terminal (pin 7 [V+] and pin 6 [Output]). In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

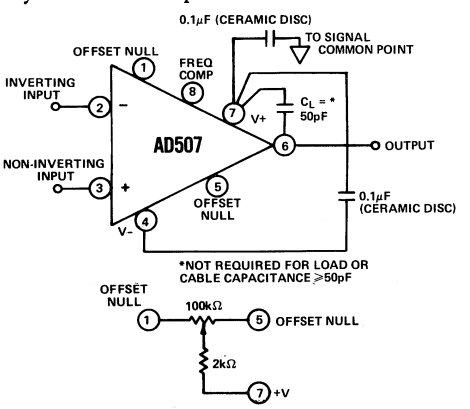


Figure 1. General Purpose Configuration to Closed Loop Gain > 10

Low Gain Conditions

For low closed loop gain applications, the AD507 should be compensated with a 20pF capacitor from pin 8 (frequency compensation) to signal common or pin 7 (V+). This configuration also requires a 30pF feedback capacitor from pin 6 (Output) to pin 8 (see Figure 2). The 50pF minimum load capacitance recommended for uncompensated applications is not required when the AD507 is used in the compensated mode. This compensation results in a unity gain frequency of approximately 10 to 12MHz.

The excellent input characterisitcs of the AD507 make it useful in low frequency applications where both dc and ac performance superior to the 741 type of op amp is desired. Some experimentation may be necessary to optimize the AD507 for the specific requirement. The unity gain bandwidth can be reduced by increasing the value of the compensation capacitor in inverse proportion to the desired bandwidth reduction. It is advisable to increase the feedback capacitor at the same time, maintaining its value about 50% larger than the compensation capacitor. Because the AD507 is fundamentally a wideband amplifier, careful power supply decoupling and compensation component layout are required even in low bandwidth applications.

OFFSET VOLTAGE NULLING

Note that the offset voltage null circuit includes a 2kΩ resistor in series with the wiper arm of the 100kΩ potentiometer. This resistor is not absolutely required, but its use can prevent a condition of false null that can be obtained at the ends of the pot range. The knowledgeable user should have no trouble differentiating between nulling in the pot mid-range and erratic end-range behavior when the wiper is connected directly to V+.

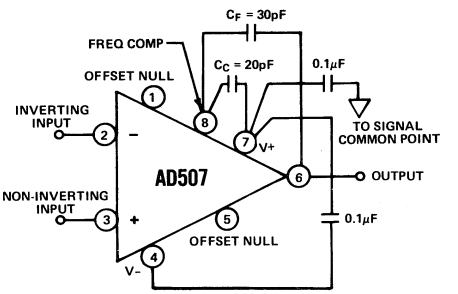


Figure 2. Configuration for Unity Gain Applications

HIGH CAPACITIVE LOADING

Like all wideband amplifiers, the AD507 is sensitive to capacitive loading. Unlike many, however, the AD507 can be used to effectively drive reasonable capacitive loads in virtually all applications, and capacitive loads of several hundred picofarads in a number of specific configurations.

In an inverting gain of ten configuration, the internally compensated amplifier will drive more than 200pF in addition to the recommended 50pF load, or a total of over 250pF. Under such conditions, the slew rate will be only slightly reduced, and the overall settling time somewhat lengthened.

In general, the capacitive drive capability of the AD507 will increase in high gain configurations which reduce closed loop bandwidth.

In any wideband application, it is essential to return the load currents supplied by the amplifier to the power supply without sharing a path with input or feedback signals. This consideration becomes particularly important when driving capacitive loads which may resonate with short lengths of interconnecting wire.

FAST SETTLING TIME

A small capacitor (C_S in Figure 3) will improve the settling time of the AD507, when it is used with large feedback resistors. The AD507 input capacitance (typically 2 or 3pF), together with additional circuit capacitance, will introduce an unwanted pole of open-loop response. The extra phase shift introduced, for example, by 4pF of input capacitance, and

5kΩ input source impedance, will result in an underdamped transient response, and long settling time. A small (1.5 to 3.0pF) feedback capacitor will introduce a zero in the open-loop transfer function, reducing the phase shift and increasing the damping, which will more than compensate for the slight reduction in closed-loop bandwidth.

BIAS COMPENSATION NOT REQUIRED

Circuit applications using conventional op amps generally require that the source resistances be matched at the inputs to cancel the effects of the input currents and take advantage of low offset current. In circuits similar to that shown in Figure 3, the compensation resistance would be equal to the parallel combination of R_I and R_F, and for large values would require a bypass capacitor. The AD507 is specially designed to cancel the input currents so as to reduce them to the offset current level. As a result, optimum performance can be obtained even though no bias compensation is used, and the non-inverting input can be connected directly to the signal common.

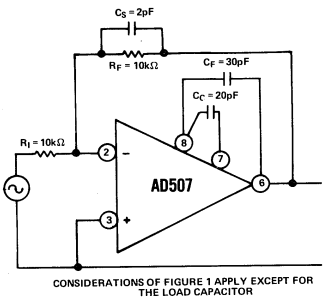
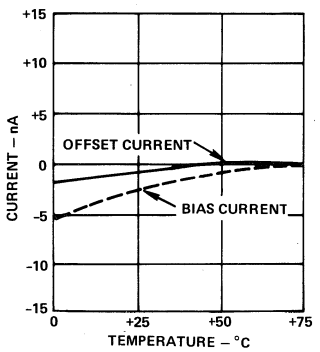
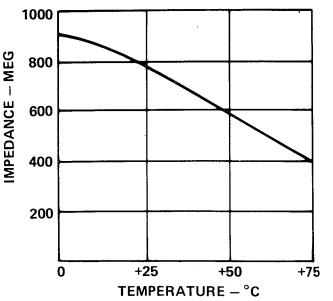


Figure 3. Fast Settling Time Configuration

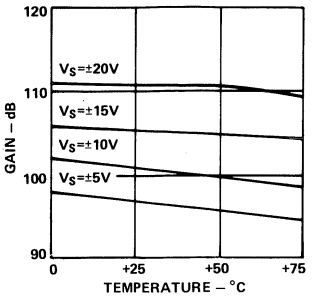
TYPICAL PERFORMANCE CURVES



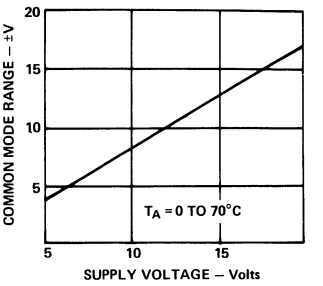
Input Bias Current and Offset Current vs Temperature



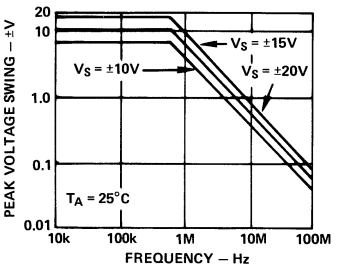
Input Impedance vs Temperature



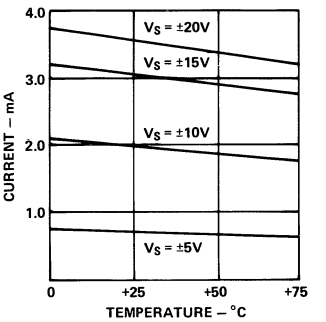
Open Loop Voltage Gain vs Temperature



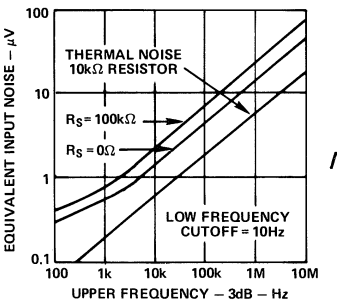
Common Mode Voltage Range vs Supply Voltage



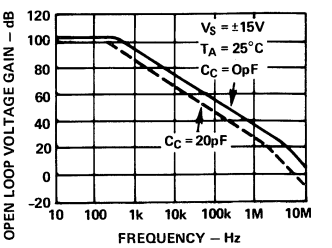
Output Voltage Swing vs Frequency



Power Supply Current vs Temperature



Broadband Input Noise Characteristics



Open Loop Gain vs Frequency

ANALOG DEVICES

High Speed, Fast Settling IC Op Amp

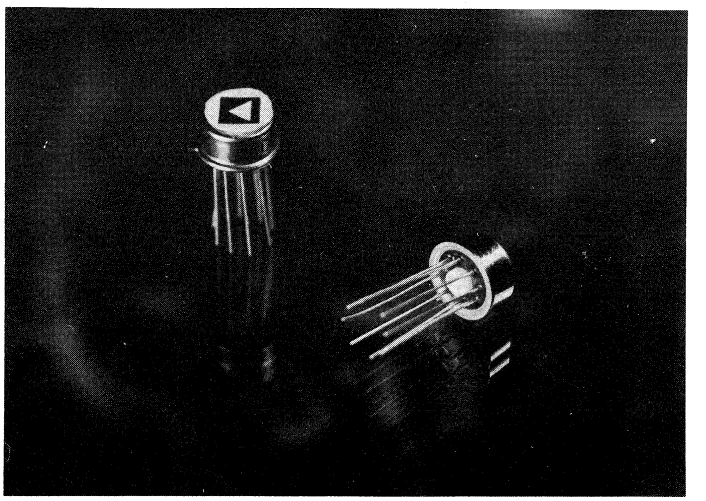
AD509

FEATURES

- Fast Settling Time (100% Tested)
  - 0.1% in 500ns max
  - 0.01% in 2.5μs max
- High Slew Rate: 100V/μs min
- Low I_{OS}: 25nA max
- Guaranteed V_{OS} Drift: 30μV/°C max
- High CMRR: 80dB min
- Drives 500pF
- Low Price

APPLICATIONS

- D/A and A/D Conversion
- Wideband Amplifiers
- Multiplexers
- Pulse Amplifiers



PRODUCT DESCRIPTION

The AD509J, AD509K and AD509S are monolithic operational amplifiers specifically designed for applications requiring fast settling times to high accuracy. The AD509K and AD509S are 100% tested and guaranteed to settle to 0.1% in 500ns max and 0.01% in 2.5μs max, with typical performance that is twice as fast. Other comparable dynamic parameters include a small signal bandwidth of 20MHz, slew rate of 100V/μs min and a full power response of 150kHz min. The devices are internally compensated for all closed loop gains greater than 3, and are compensated with a single capacitor for lower gains.

The input characteristics of the AD509 are consistent with 0.01% accuracy over limited temperature ranges; offset current is 25nA max, offset voltage is 8mV max, nullable to zero, and offset voltage drift is limited to 30μV/°C max. PSRR and CMRR are typically 90dB.

The AD509 is designed for use with high speed D/A or A/D converters where the minimum conversion time is limited by the amplifier settling time. If 0.01% accuracy of conversion is required, a conversion cannot be made in a shorter period than the time required for the amplifier to settle to within 0.01% of its final value.

All devices are supplied in the TO-99 package. The AD509J and AD509K are specified for 0 to +70°C temperature range; the AD509S for operation from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD509K and AD509S are 100% tested and guaranteed to settle to 0.01% of its final value in less than 2.5μs.
2. The AD509 is internally compensated for all closed loop gains above 3, and compensated with a single capacitor for lower gains; thus eliminating the elaborate stabilizing techniques required by other high speed IC op amps.
3. The AD509 will drive capacitive loads of 500pF without any deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time.
4. Common Mode Rejection, Gain and Noise are compatible with a 0.01% accuracy device.

SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

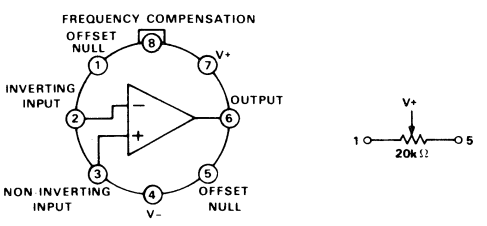
MODEL	AD509J	AD509K	AD509S
OPEN LOOP GAIN			
R_L = 2kΩ	7,500 min (15,000 typ)	10,000 min (15,000 typ)	**
@ T_A = min to max	5,000 min	7,500 min	**
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±12V typ)	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	20MHz	*	*
Full Power Response, V_O = ±10V	120kHz min (1.6MHz typ)	150kHz min (2.0MHz typ)	**
Slew Rate, R_L = 2kΩ, V_O = ±10V, C_L = 50pF	80V/μs min (120V/μs typ)	*	100V/μs min (120V/μs typ)
Settling Time			
to 0.1%	200ns	500ns max (200ns typ)	**
to 0.01%	1.0μs	2.5μs max (1.0μs typ)	**
INPUT OFFSET VOLTAGE			
Initial	10mV max (5mV typ)	8mV max (4mV typ)	**
T_A = min to max	14mV max	11mV max	**
Avg vs. Temperature, T_A = min to max	20μV/°C	30μV/°C max (20μV/°C typ)	**
vs. Supply, T_A = min to max	200μV/V max	100μV/V max	**
INPUT BIAS CURRENT			
Initial	250nA max (125nA typ)	200nA max (100nA typ)	**
T_A = min to max	500nA max	400nA max	**
INPUT OFFSET CURRENT			
Initial	50nA max (20nA typ)	25nA max (10nA typ)	**
T_A = min to max	100nA max	50nA max	**
INPUT IMPEDANCE			
Differential	40MΩ min (100MΩ typ)	50MΩ min (100MΩ typ)	**
INPUT VOLTAGE RANGE			
Differential, max safe	±15V	*	*
Common Mode Voltage Range			
T_A = min to max	±10V	*	*
Common Mode Rejection, V_{cm} = ±5V			
T_A = min to max	74dB min (90dB typ)	80dB min (90dB typ)	**
INPUT VOLTAGE NOISE			
f = 10Hz	100nV/√Hz	*	*
f = 100Hz	30nV/√Hz	*	*
f = 100kHz	19nV/√Hz	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	6mA max (4mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*

*Specification same as AD509J.
**Specification same as AD509K.
Specifications and prices subject to change without notice.

PIN CONFIGURATION & PHYSICAL DIMENSIONS

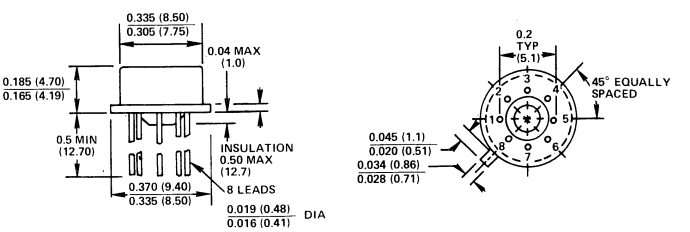
Dimensions shown in inches and (mm).

TO-99



TOP VIEW

TO-99



APPLYING THE AD509

MEASURING SETTLING TIME. Settling time is defined as that period required for an amplifier output to swing from 0 volts to full scale, usually 10 volts, and to settle to within a specified percentage of the final output voltage. For high accuracy systems, the accuracy requirement is normally specified as either 0.1% (10-bit accuracy) or 0.01% (12-bit accuracy) of the 10 volt output level. The settling time period is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vicinity of 10 volts, and a final time period to recover from internal saturation and other effects, and settle within the specified error band. Because settling time depends on both linear and nonlinear factors, there is no simple approach to predicting its final value to different levels of accuracy. In particular, extremely high slew rates do not assure a rapid settling time, since this is only one of many factors affecting settling time. In most high speed amplifiers, after the amplifier has slewed to the vicinity of the final output voltage, it must recover from internal saturation and then allow any overshoot and ringing to damp out. These definitions are illustrated in Figure 1.

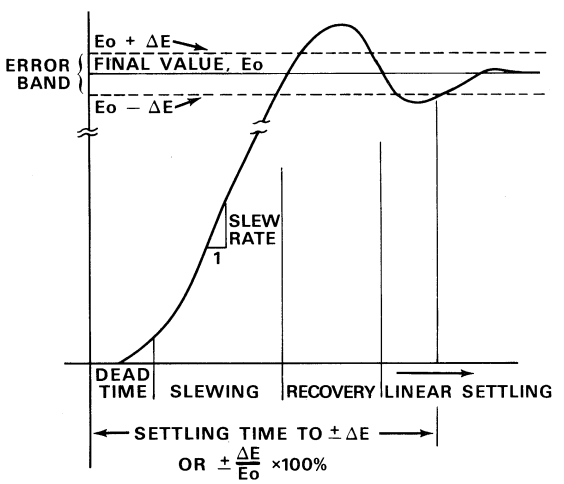


Figure 1. Settling Time

The AD509K and AD509S are 100% tested and guaranteed to settle to 0.1% in 500ns and 0.01% in 2.5μs (see Test Circuit, Figure 2). Note that the devices are tested compensated, at a gain of one, with a 50pF capacitive load. There is no appreciable degradation in settling time when the capacitive load is increased to 500pF, as discussed below. The settling time is computed by summing the output and the input into a differential amplifier, which then drives a scope

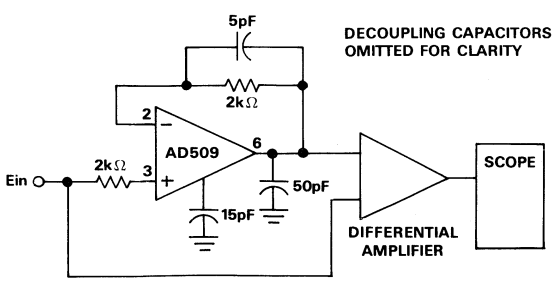


Figure 2. AD509 Settling Time Test Circuit

display. The resultant waveform of ($E_o - E_{in}$) of a typical AD509 is shown in Figure 3. Note that the waveform crosses the 1mV point representing 0.01% accuracy in approximately 1.5μs. The top trace represents the output signal; the bottom trace represents the error signal.

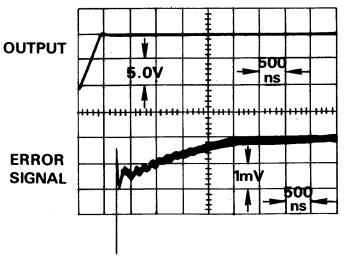


Figure 3. Settling Time of AD509

SETTLING TIME VS. R_f AND R_i. Settling time of an amplifier is a function of the feedback and input resistors, since they interact with the input capacitance of the amplifier. When operating in the non-inverting mode, the source impedance should be kept relatively low; e.g., 5kΩ; in order to insure optimum performance. The small feedback capacitor (5pF) is used in the settling time test circuit in parallel with the feedback resistor to reduce ringing. This capacitor partially cancels the pole formed in the loop gain response as a result of the feedback and input resistors, and the input capacitance.

SETTLING TIME VS. CAPACITIVE LOAD. The AD509 will drive capacitive loads of 500pF without appreciable deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time. Figure 4 shows the settling time of a typical AD509, compensated for unity gain with a 15pF capacitor, with a 500pF capacitive load on the output. Note that settling time to 0.01% is still under 2.0μs.

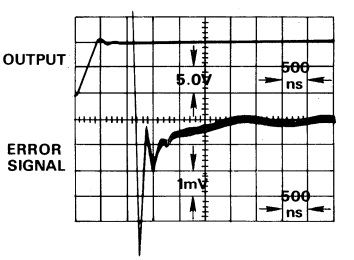


Figure 4. AD509 with 500pF Capacitive Load

SUGGESTIONS FOR MINIMIZING SETTLING TIME. The AD509 has been designed to settle to 0.01% accuracy in 1 to 2.5μs. However, this amplifier is only a building block in a circuit that also has a feedback network, input and output connections, power supply connections, and a number of external components. What has been painstakingly gained in amplifier design can be lost without careful circuit design. Some of the elements of a good high speed design are.....

CONNECTIONS. It is essential that care be taken in the signal and power ground circuits to avoid inducing or generating extraneous voltages in the ground signal paths.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD509 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal (pin 7 [V+]).

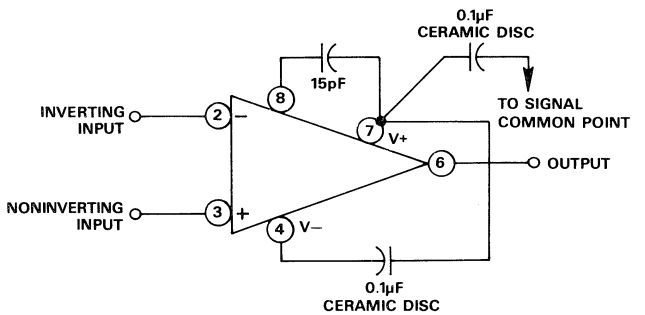


Figure 5. Configuration for Unity Gain Applications

In addition, it is suggested that all connections be short and direct, and as physically close to the case as possible, so that the length of any conducting path shared by external components will be minimized.

COMPONENTS. Resistors are preferably metal film types, because they have less capacitance and stray inductance than wirewound types, and are available with excellent accuracies and temperature coefficients.

Diodes are hot carrier types for the very fastest-settling applications, but 1N914 types are suitable for more routine uses.

Capacitors in critical locations are polystyrene, teflon, or polycarbonate to minimize dielectric absorption.

CIRCUIT. For the fastest settling times, keep leads short, orient components to minimize stray capacitance, keep circuit impedance levels as low as consistent with the output capabilities of the amplifier and the signal source, reduce all external load capacitances to the absolute minimum. Don't overlook sockets or printed circuit board mounting as possible sources of dielectric absorption. Avoid pole-zero mismatches in any feedback networks used with the amplifier. Minimize noise pickup.

DYNAMIC RESPONSE OF AD509

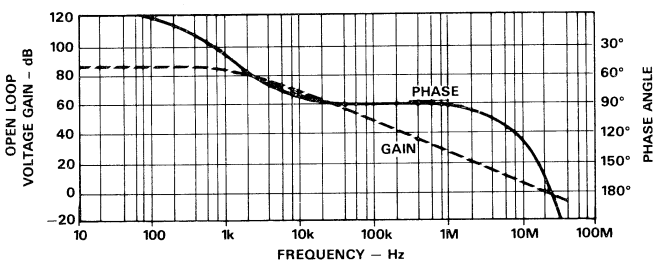


Figure 6. Open Loop Frequency and Phase Response

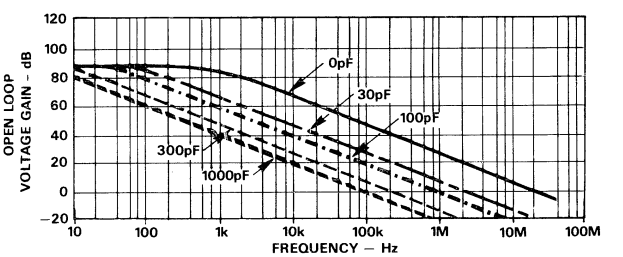


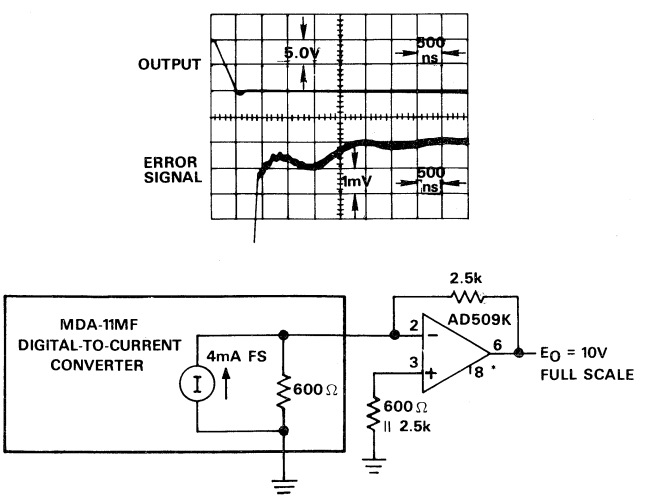
Figure 7. Open Loop Frequency Response for Various C_C's

USING THE AD509 AS AN OUTPUT AMPLIFIER FOR A FAST SETTLING D/A CONVERTER

Many D/A converters are actually digital-to-current converters; that is, the digital input code is represented by an output current. The output current is usually then fed into an output amplifier to convert the current into a voltage. The minimum conversion time of the whole D/A converter function is thus limited by the speed of the DAC itself and the time for the amplifier to settle to its final value. For example, the total settling time of the converter and the amplifier can be represented by a sum of squares approximation. Many high frequency op amps which settle to 0.1% accuracy in 500ns to 1μs require a much longer period to reach higher accuracies, thus becoming the limiting factor to rapid conversion. The AD509K and AD509S are 100% tested and guaranteed to settle to 0.01% of a 10V step in 2.5μs max and 0.1% in 500ns max.

The AD590K is shown connected as an output amplifier with the Analog Devices model MDA-11MF, an 11-bit fast settling Digital-to-Current Converter.

Note in Figure 8 the D/A system settles to 0.01% accuracy in less than 2μs.



* Note that since the closed loop gain of the amplifier is greater than 3, no compensation is needed, thus reducing settling time.

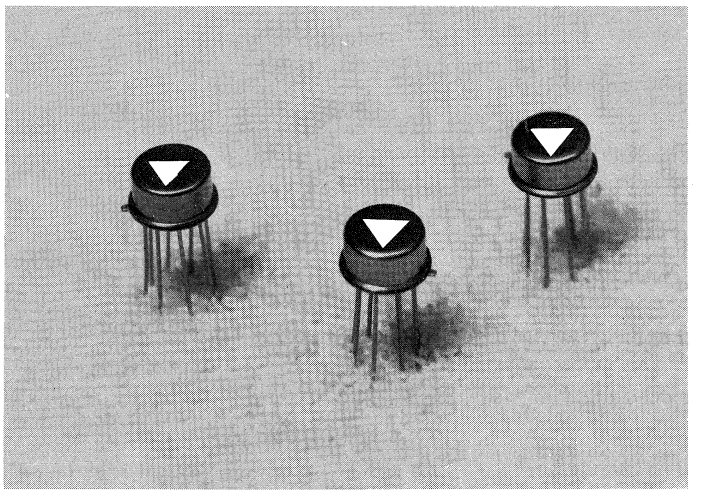
Figure 8. AD509 as an Output Amplifier with a Fast Digital-to-Current Converter

ANALOG DEVICES

Low Cost, Laser Trimmed, Precision IC Op Amp

AD510

FEATURES
Low Cost
Low V_{OS}: 25μV max (AD510L), 100μV max (AD510J)
Low V_{OS} Drift: 0.5μV/°C max (AD510L)
Internally Compensated
High Open Loop Gain: 10^6 min
Low Noise: 1μV p-p 0.01 to 10Hz



PRODUCT DESCRIPTION

The AD510 is the first low cost high accuracy IC op amp available. Analog Devices' precise thermally-balanced layout combined with high-yield IC processing provides truly superlative op amp performance at the lowest possible cost ($5.95, J in 100's). The device is internally compensated, thus eliminating the need for an additional external capacitor.

A truly precision device, the AD510 achieves laser trimmed offset voltages less than 25μV max and offset voltage drifts of 0.5μV/°C max (nulled). Bias currents and offset currents are available at less than 10nA and 2.5nA respectively, while open loop gain is maintained at over 1,000,000, even under loaded conditions. Designed along a thermal axis, the AD510 is unaffected by thermal gradients across the monolithic chip caused by current loading.

The AD510 has fully protected inputs, permitting differential input voltages of up to $\pm V_S$ without voltage gain or bias current degradation due to reverse breakdown. The output is also protected from short circuits and drives 1000pF of load capacitance without oscillation.

The AD510 is specifically designed for applications requiring high precision at the lowest possible cost, such as bridge instruments, stable references, followers and analog computation. Packaged in a hermetically-sealed TO-99 metal can, the AD510 is available in three versions of performance (J, K and L) over the commercial temperature range, 0 to +70°C and one version (S) over the full military temperature range, -55°C to +125°C.

PRODUCT HIGHLIGHTS

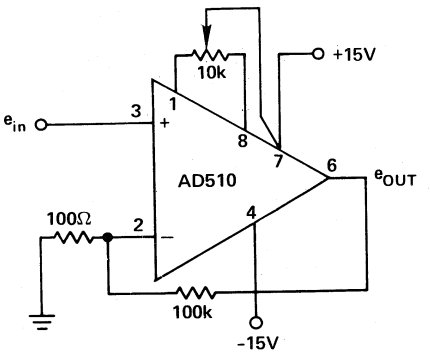
1. Offset voltage drift is guaranteed and 100% tested on all models with a controlled temperature drift bath with the offset voltage nulled. Offset voltage on the AD510L is tested following a 3 minute warm-up.
2. The AD510 offers fully protected input (to $\pm V_S$) and output circuitry. The input protection circuit prevents offset voltage and bias current degradation due to reverse breakdown, a critical factor in high accuracy op amps where overall performance is strongly dependent on front-end stability.
3. Internal compensation eliminates the need for elaborate and costly stabilizing networks, often required by many high accuracy IC op amps.
4. A thermally balanced layout maintains high gain (1,000,000 min, K, L and S) independent of offset nulling, power supply voltage and output loading.
5. Bootstrapping of critical input transistors produces CMRR and PSRR of 110dB min and 100dB min, respectively.
6. Every AD510 is baked for 48 hours at +150°C, temperature cycled 10 times from -65°C to +200°C, and subjected to a high G shock test to assure reliability and long term stability.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	AD510J	AD510K	AD510L	AD510S
OPEN LOOP GAIN				
V_{OS} = ±10V, $R_L > 2k\Omega$	250,000 min	10^6 min	**	**
T_{min} to T_{max}	125,000 min	500,000 min	**	250,000
OUTPUT CHARACTERISTICS				
Voltage @ $R_L \geq 2k\Omega$, T_{min} to T_{max}	±10V min	*	*	*
Load Capacitance	1000pF	*	*	*
Output Current	10mA min	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	300kHz	*	*	*
Full Power Response	1.5kHz	*	*	*
Slew Rate, Unity Gain	0.10V/μs	*	*	*
INPUT OFFSET VOLTAGE				
Initial Offset, $R_S \leq 10k\Omega$	100μV max	50μV max	25μV max	**
vs. Temp., T_{min} to T_{max}	3.0μV/°C max	1.0μV/°C max	0.5μV/°C	**
vs. Supply	25μV/V max	10μV/V max	**	**
T_{min} to T_{max}	40μV/V max	15μV/V max	**	20μV/V max
INPUT OFFSET CURRENT				
Initial	5nA max	4nA max	2.5nA max	**
T_{min} to T_{max}	8nA max	6nA max	4nA max	10nA max
INPUT BIAS CURRENT				
Initial	25nA max	13nA max	10nA max	**
T_{min} to T_{max}	40nA max	20nA max	15nA max	30nA max
vs. Temp, T_{min} to T_{max}	±100pA/°C	±50pA/°C	±40pA/°C	**
INPUT IMPEDANCE				
Differential	4MΩ	6MΩ	**	**
Common Mode	100MΩ‖4pF	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	1μV p-p	*	*	*
f = 10Hz	18nV/$\sqrt{Hz}$	*	*	*
f = 100Hz	13nV/$\sqrt{Hz}$	*	*	*
f = 1kHz	10nV/$\sqrt{Hz}$	*	*	*
Current, f = 10Hz	0.5pA/$\sqrt{Hz}$	*	*	*
f = 100Hz	0.3pA/$\sqrt{Hz}$	*	*	*
f = 1kHz	0.3pA/$\sqrt{Hz}$	*	*	*
INPUT VOLTAGE RANGE				
Differential or Common Mode max safe	$\pm V_S$	*	*	*
Common Mode Rejection, V_{in} = ±10V	94dB min	110dB min	**	**
Common Mode Rejection, T_{min} to T_{max}	94dB	100dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	±(5 to 22)V
Current, Quiescent	4mA max	3mA max	**	**
TEMPERATURE RANGE				
Operating Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*

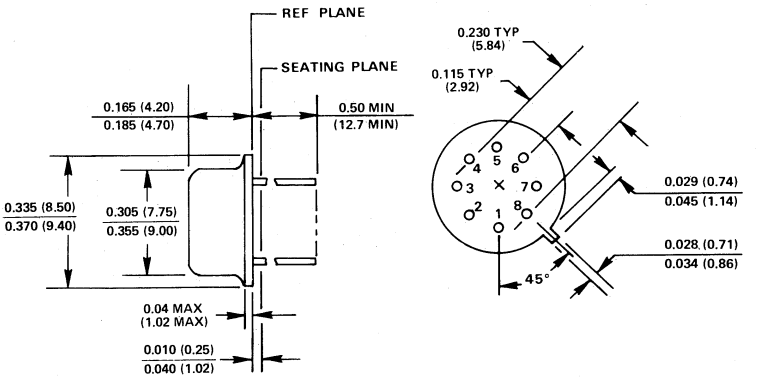
NOTES:
*Specifications same as AD510J
**Specifications same as AD510K
Specifications subject to change without notice.

TYPICAL
NON-INVERTING AMPLIFIER CONFIGURATION



OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

TO–99



NULLING THE AD510

Nulling the AD510 can be achieved using the high resolution circuit of Figure 1.

1. Null the offset to zero using a commercially available pot (approximately 10kΩ).
2. Measure pot halves, R_1 and R_2.
3. Calculate . . . $R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1}$ $R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$
4. Insert R_1' and R_2' (closest 1% fixed metal film resistors).
5. Use an industrial quality 100kΩ pot (r_p) to fine tune the trim.

Nulling to within 1 microvolt can be achieved using this technique. For best results, the wiper of the potentiometer should be connected directly to pin 7 of the op amp.

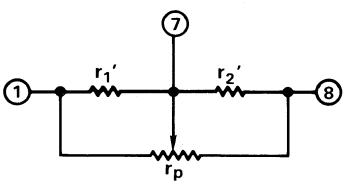


Figure 1. High Resolution, High Stability Nulling Circuit

THE AD510L IN A SIMPLE INSTRUMENTATION AMPLIFIER

The circuit of Figure 2 illustrates a simple instrumentation amplifier suitable for use with strain gauges, thermocouples and other transducers. It provides high input impedance to ground at each of the differential input terminals and excellent common mode rejection.

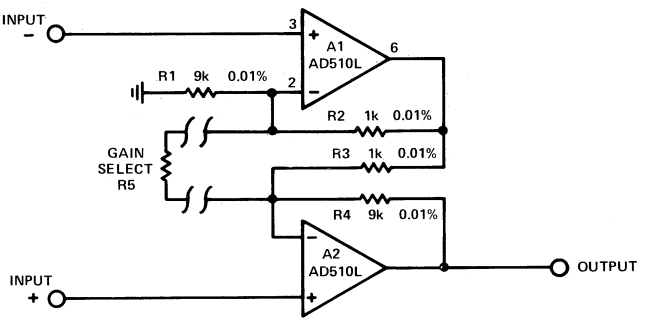


Figure 2. Instrumentation Amplifier

The configuration shown is designed for a gain of 10, however the gain can be varied upwards by adding a gain select resistor R_5. In operation, amplifier A_1 provides a gain of 10/9 for signals at the negative input terminal. This output feeds the inverting amplifier A_2, which has a gain of 9, resulting in an overall gain of 10. For signals at the positive input, the output of A_1 is at ground potential and the amplifier A_2 provides a gain of 10. Thus, the circuit has a gain of 10 for differential signals and 0 for common mode signals; the very high CMRR and open loop gain of the AD510L automatically produces common mode rejection of at least 25,000 at dc at a gain of 10 and over 1,000,000 at a gain of 1000. The common mode rejection, of course, depends upon the resistor ratios and their specified tolerance. Less accurate resistors can be used if the network is trimmed.

For gains of 10 the frequency response is down 3dB at 500kHz, for gains of 1000, 2kHz. Full output of ±10V can be attained up to 1800Hz.

The common mode rejection at 60Hz is limited by the finite gain bandwidth of A_1 causing a phase lag on the negative input signal. At 60Hz the CMRR measures 72dB at a gain of 1000 and 62dB at a gain of 10.

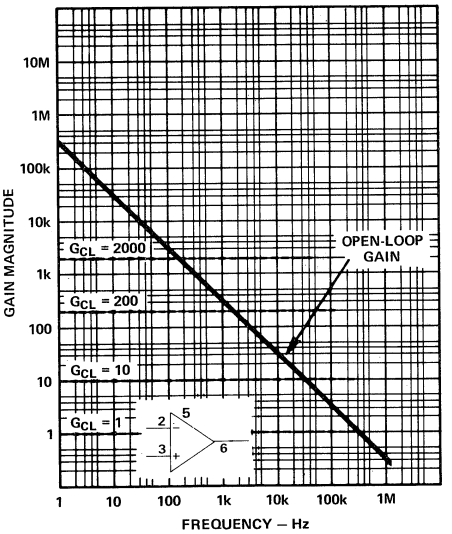


Figure 3. Small Signal Gain vs. Frequency

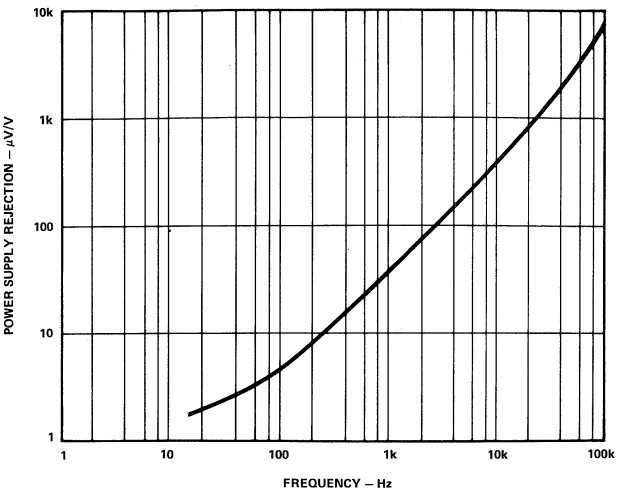


Figure 4. PSRR vs. Frequency

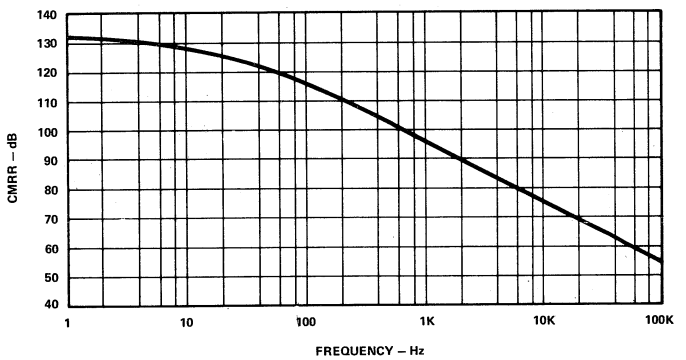


Figure 5. CMRR vs. Frequency

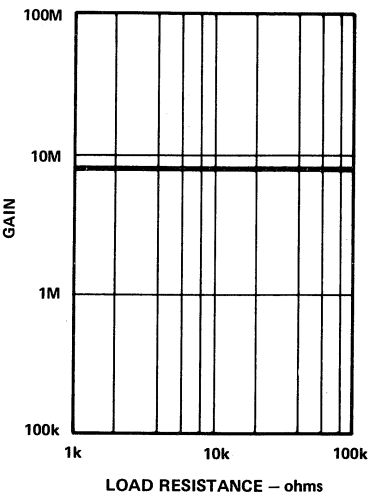


Figure 6. Gain vs. Load Resistance

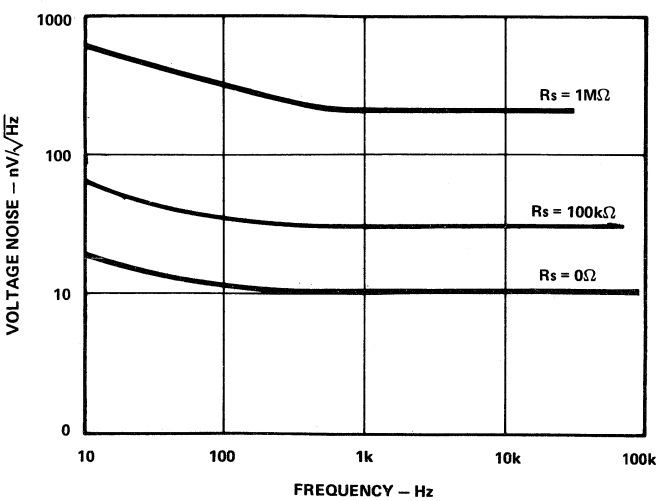


Figure 7. Voltage Noise vs. Frequency

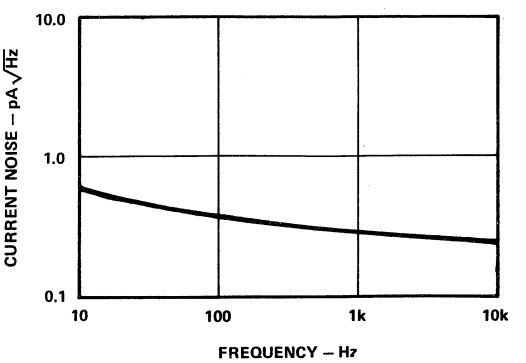


Figure 8. Current Noise vs. Frequency

ANALOG DEVICES

Precision, Low-Power FET-Input Electrometer Op Amp

AD515

FEATURES

Ultra Low Bias Current: 0.075pA max (AD515L)
0.150pA max (AD515K)
0.300pA max (AD515J)

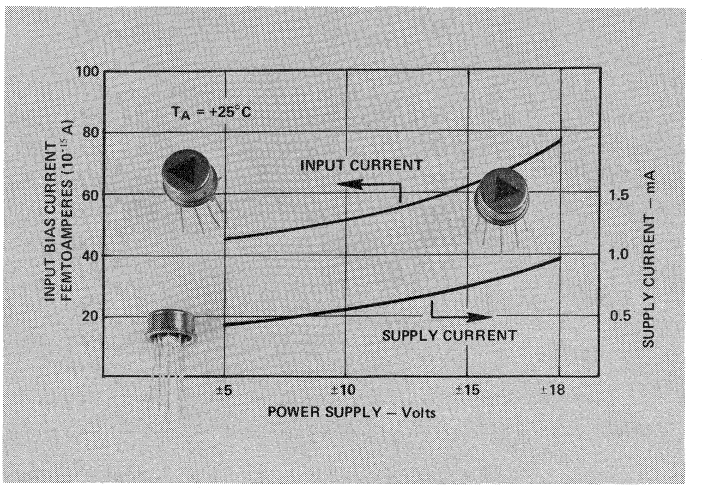
Low Power: 1.5mA max Quiescent Current (0.8mA typ)

Low Offset Voltage: 1.0mV max (AD515 K & L)

Low Drift: 15μV/°C max (AD515K)

Low Noise: 4μV p-p, 0.1 to 10Hz

Low Cost



PRODUCT DESCRIPTION

The AD515 series of FET-input operational amplifiers are second generation electrometer designs offering the lowest input bias currents available in any standard operational amplifier. The AD515 also delivers laser-trimmed offset voltage, low drift, low noise and low power, a combination of features not previously available in ultra-low bias current circuits. All devices are internally compensated, free of latch-up, and short circuit protected.

The AD515 delivers a new level of versatility and precision to a wide variety of electrometer and very high impedance buffer measurement situations, including photo-current detection, vacuum ion-gauge measurement, long term precision integration, and low drift sample/hold applications. The device is also an excellent choice for all forms of biomedical instrumentation such as pH/pIon sensitive electrodes, very low current oxygen sensors, and high impedance biological microprobes. In addition, the low cost and pin compatibility of the AD515 with standard FET op amps will allow designers to upgrade the performance of present systems at little or no additional cost. The 10^{15} ohm common mode input impedance, resulting from a solid bootstrap input stage, insures that the input bias current is essentially independent of common mode voltage.

As with previous electrometer amplifier designs from Analog Devices, the case is brought out to its own connection (pin 8) so that the case can be independently connected to a point at the same potential as the input, thus minimizing stray leakage to the case. This feature will also shield the input circuitry from external noise and supply transients, as well as reducing common mode input capacitance from 0.8pF to 0.2pF.

The AD515 is available in three versions of bias current and offset voltage, the "J", "K", and "L"; all are specified for rated performance from 0 to +70°C and supplied in a hermetically sealed TO-99 package.

PRODUCT HIGHLIGHTS

1. The AD515 provides the lowest bias currents available in an integrated circuit amplifier.
   - The ultra low input bias currents are specified as the maximum measured at either input with the device fully warmed up on ±15 volt supplies at +25°C ambient with no heat sink. This parameter is 100% tested.
   - By using ±5 volt supplies, input bias current can typically be brought below 50fA.
2. The input offset voltage on all grades is laser trimmed to a level typically less than 500μV.
   - The offset voltage drift is the lowest available in an FET electrometer amplifier.
   - If additional nulling is desired, the amount required will have a minimal effect on offset drift (approximately 3μV/°C per millivolt).
3. The low quiescent current drain of 0.8mA typical and 1.5mA maximum, which is among the lowest available in operational amplifier designs of any type, keeps self-heating effects to a minimum and renders the AD515 suitable for a wide range of remote probe situations.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from much over one Megohm up to 10^{11} ohm, the Johnson noise of the source will easily dominate the noise characteristic.
5. Every AD515 is subjected to long term, high temperature stabilization bakes, temperature cycled ten times from –65°C to +150°C, and given a high G shock test prior to final testing to insure reliability and long term stability.

SPECIFICATIONS (typical @ +25°C with V_S = ±15V dc, unless otherwise specified)

MODEL	AD515J	AD515K	AD515L
OPEN LOOP GAIN (Note 1)			
V_{out} = ± 10V, $R_L \geqslant 2k\Omega$	20,000V/V min	40,000V/V min	25,000V/V min
$R_L \geqslant 10k\Omega$	40,000V/V min	100,000V/V min	50,000V/V min
T_A = min to max $R_L \geqslant 2k\Omega$	15,000V/V min	40,000V/V min	25,000V/V min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±12V typ)	*	*
@ R_L = 10kΩ, T_A = min to max	±12V min (±13V typ)	*	*
Load Capacitance (Note 2)	1000pF	*	*
Short Circuit Current	10mA min (25mA typ)	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	350kHz	*	*
Full Power Response	5kHz min (16kHz typ)	*	*
Slew Rate Inverting Unity Gain	0.3V/μs min (1.0V/μs typ)	*	*
Overload Recovery Inverting Unity Gain	100μs max (16μs typ)	*	*
INPUT OFFSET VOLTAGE (Note 3)	3.0mV max (0.4mV typ)	1.0mV max (0.4mV typ)	1.0mV max (0.4mV typ)
vs. Temperature, T_A = min to max	50μV/°C max	15μV/°C max	25μV/°C max
vs. Supply, T_A = min to max	400μV/V max (50μV/V typ)	100μV/V max	200μV/V max
INPUT BIAS CURRENT			
Either Input (Note 4)	300fA max	150fA max	75fA max
INPUT IMPEDANCE			
Differential	$1.6pF \| \| 10^{13}\Omega$	*	*
Common Mode	$0.8pF \| \| 10^{15}\Omega$	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	4.0μV (p-p)	*	*
f = 10Hz	$75nV/\sqrt{Hz}$	*	*
f = 100Hz	$55nV/\sqrt{Hz}$	*	*
f = 1kHz	$50nV/\sqrt{Hz}$	*	*
Current, 0.1 to 10Hz	0.003pA (p-p)	*	*
10Hz to 10kHz	0.01pA rms	*	*
INPUT VOLTAGE RANGE			
Differential	±20V min	*	*
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{IN} = ±10V	66dB min (94dB typ)	80dB min	70dB min
Maximum Safe Input Voltage (Note 5)	$\pm V_S$	*	*
POWER SUPPLY			
Rated Performance	±15V typ	*	*
Operating	±5V min (±18V max)	*	*
Quiescent Current	1.5mA max (0.8mA typ)	*	*
TEMPERATURE			
Operating, Rated Performance	0 to +70°C	*	*
Storage	-65°C to +150°C	*	*

*Specifications same as AD515J.

NOTES:
1. Open Loop Gain is specified with or without nulling of V_{OS}.
2. A conservative design would not exceed 750pF of load capacitance.
3. Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
4. Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.
5. If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can handle overload currents of 0.5mA indefinitely without damage. See next page.

Specifications and prices subject to change without notice.

LAYOUT AND CONNECTION CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading. The AD515, with its combination of low offset voltage (normally eliminating the need for trimming), low quiescent current (minimal source heating, possible battery operation), internal compensation and small physical size lends itself very nicely to installation at the signal source or inside a probe. Also, as a result of the high load capacitance rating, the AD515 can comfortably drive a long signal cable.
2. The use of guarding techniques is essential to realizing the capability of the ultra-low input currents of the AD515. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation, and hence, no leakage. The guard will also act as a shield to reduce noise pick-up and serves an additional function of reducing the effective capacitance to the input line. The case of the AD515 is brought out separately to pin 8 so that the case can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry, and reduces common-mode input capacitance to about 0.2pF. Figure 1 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and non-inverting applications. If pin 8 is not used for guarding, it should be connected to ground or a power supply to reduce noise.

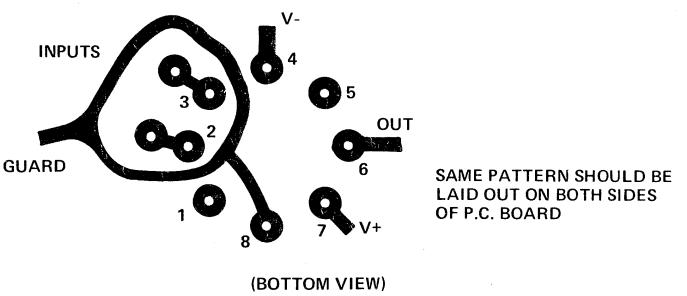


Figure 1. Board Layout for Guarding Inputs with Guarded TO-99 Package

3. Printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD515 can deliver. The best performance will be realized by using a teflon IC socket for the AD515; but at least a teflon stand-off should be used for the high-impedance lead. If this is not feasible, the input guarding scheme shown in Figure 1 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.
4. Another important concern for achieving and maintaining low leakage currents is complete cleanliness of circuit boards and components. Completed assemblies should be washed thoroughly in a low residue solvent such as TMC Freon or high-purity methanol followed by a rinse with deionized water and nitrogen drying. If service is anticipated in a high contaminant or high humidity environment, a high dielectric conformal coating is recommended. All insulation materials except Kel-F or teflon will show rapid degradation of surface leakage at high humidities.

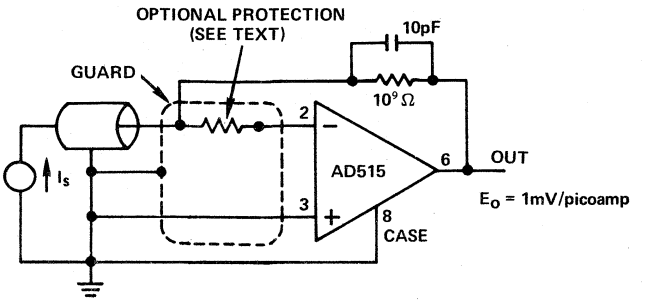


Figure 2. Picoampere Current-to-Voltage Converter Inverting Configuration

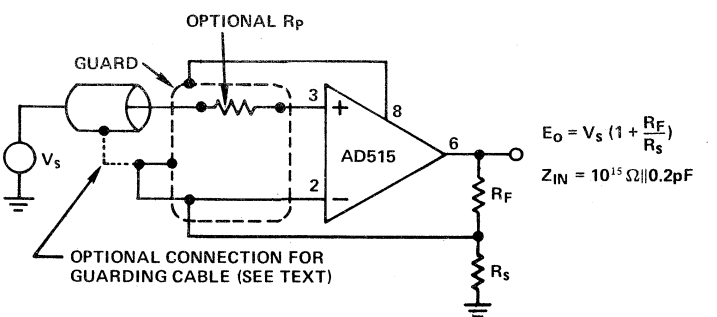


Figure 3. Very High Impedance Non-Inverting Amplifier

INPUT PROTECTION

The AD515 is guaranteed for a maximum safe input potential equal to the power supply potential. The unique bootstrapped input stage design also allows differential input voltages of up to ±20 volts (or within 10 volts of the sum of the supplies) while maintaining the full differential input resistance of $10^{13}\Omega$, as shown in Figure 10. This makes the AD515 suitable for low speed comparator situations employing a direct connection to a high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD515 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 0.5mA (for example, 200kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figures 2 and 3 show proper connections.

COAXIAL CABLE AND CAPACITANCE EFFECTS

If it is not possible to attach the AD515 virtually on top of the signal source, considerable care should be exercised in designing the connecting lines carrying the high impedance signal. Shielded coaxial cable must be used for noise reduction, but use of coaxial cables for high impedance work can add problems from cable leakage, noise, and capacitance. Only the best polyethylene or virgin teflon (not reconstituted) should be used to obtain the highest possible insulation resistance.

Cable systems should be made as rigid and vibration-free as possible since cable movement can cause noise signals of three types, all significant in high impedance systems. Frictional movement of the shield over the insulation material generates a charge which is sensed by the signal line as a noise voltage. Low noise cable with graphite lubricant such as Amphenol 21-537 will reduce the noise, but short rigid lines are better. Cable movements will also make small changes in the internal cable capacitance and capacitance to other objects. Since the total charge on these capacitances cannot be changed instantly, a noise voltage results as predicted from: $\Delta V = Q/\Delta C$. Noise voltage is also generated by the motion of a conductor in a magnetic field.

The conductor-to-shield capacitance of coaxial cable is normally about 30pF/foot. Charging this capacitance can cause considerable stretching of high impedance signal rise-time, thus cancelling the low input capacitance feature of the AD515. There are two ways to circumvent this problem. For inverting signals or low-level current measurements, the signal is carried on the line connected to the inverting input and shielded (guarded) by the ground line as shown in Figure 2. Since the signal is always at virtual ground, no voltage change is required and no capacitances are charged. In many circumstances, this will de-stabilize the circuit; if so, capacitance from output to inverting input will stabilize the circuit.

Non-inverting and buffer situations are more critical since the signal line voltage and therefore charge will change, causing signal delay. This effect can be reduced considerably by connecting the cable shield to guard potential instead of ground, an option shown in Figure 3. Since such a connection results in positive feedback to the input, the circuit may destabilize and oscillate. If so, capacitance from positive input to ground must be added to make the net capacitance at pin 3 positive. This technique can considerably reduce the effective capacitance which must be charged.

Typical Performance Curves

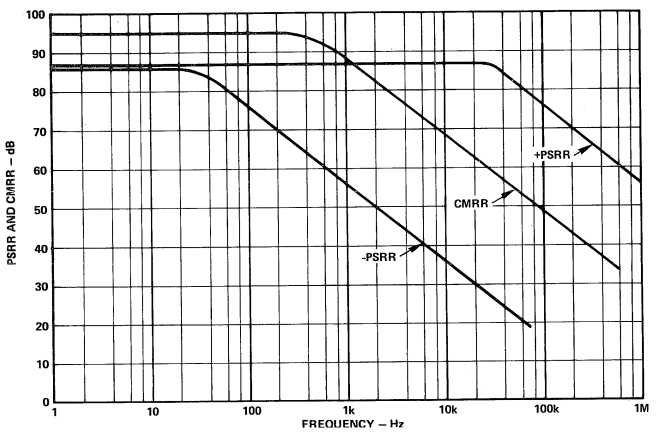


Figure 4. PSRR and CMRR Versus Frequency

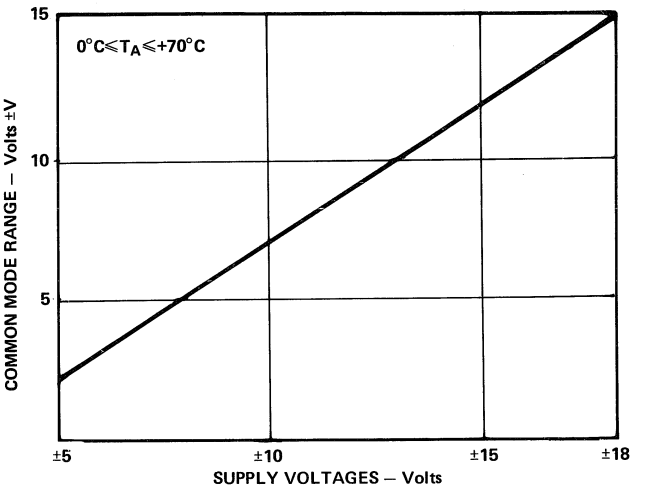


Figure 6. Input Common Mode Range Versus Supply Voltage

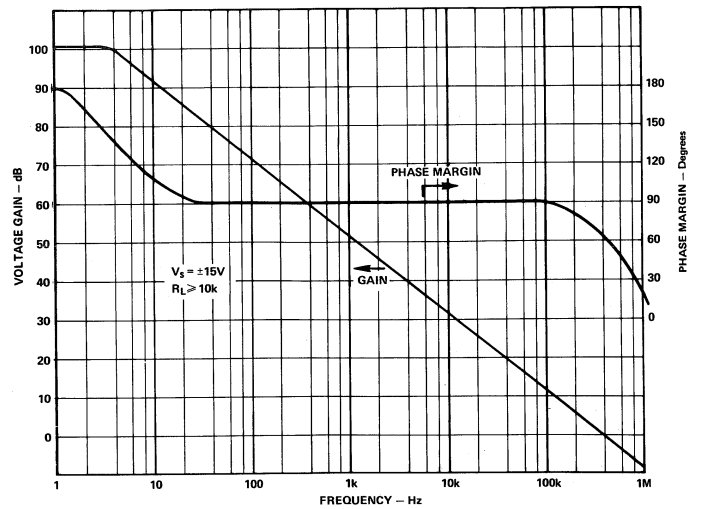


Figure 5. Open Loop Frequency Response

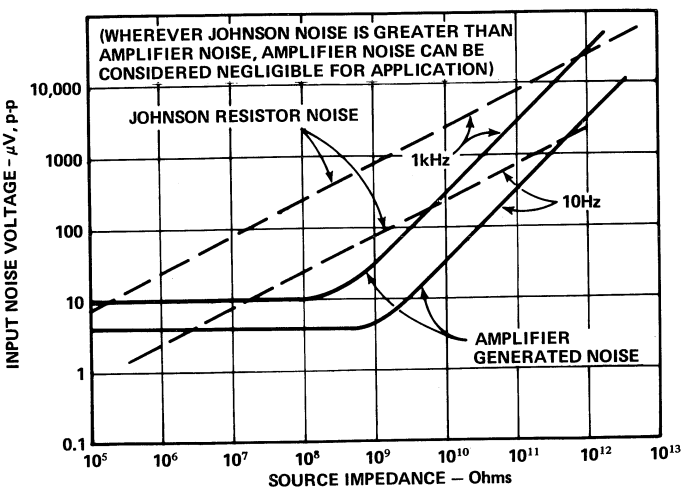


Figure 7. Peak-to-Peak Input Noise Voltage Versus Source Impedance and Bandwidth

ELECTROMETER APPLICATION NOTES

The AD515 offers the lowest input bias currents available in an integrated circuit package. This design will open up many new application opportunities for measurements from very high impedance and very low current sources. Performing accurate measurements of this sort requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD515 and perhaps extending its performance limits.

1. As with all junction FET input devices, the temperature of the FET's themselves is all-important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature.
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if it is possible to reduce the required power supplies, this should be done since internal power consumption contributes the largest component of self-heating. To minimize this effect, the quiescent current of the AD515 has been reduced to a level much lower than that of any other electrometer-grade device, but additional performance improvement can be gained by lowering the supply voltages, to ±5 volts if possible. The effects of this are shown in Figure 8, which shows typical input bias current and quiescent current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10 volts at the output will cause at least an additional 25 milliwatts dissipation in the output stage (and some in other stages) over the typical 24 milliwatts, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated. Therefore, although many DC performance parameters are specified driving a 2kΩ load, to reduce this additional dissipation, we recommend restricting the load impedance to be at least 10kΩ.

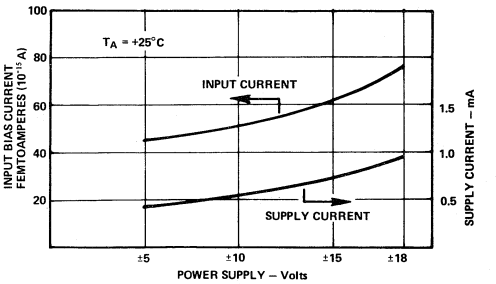


Figure 8. Input Bias Current and Supply Current Versus Supply Voltage

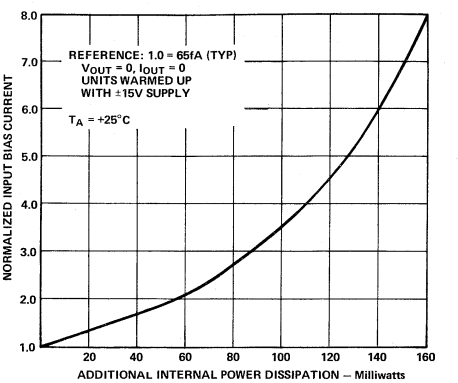


Figure 9. Input Bias Current Versus Additional Power Dissipation

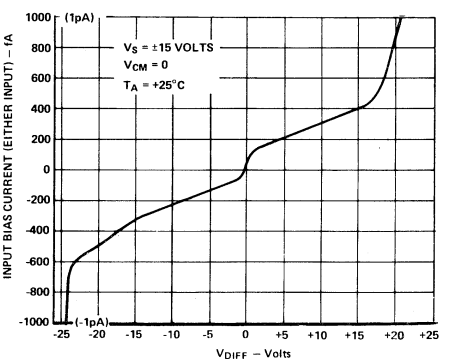
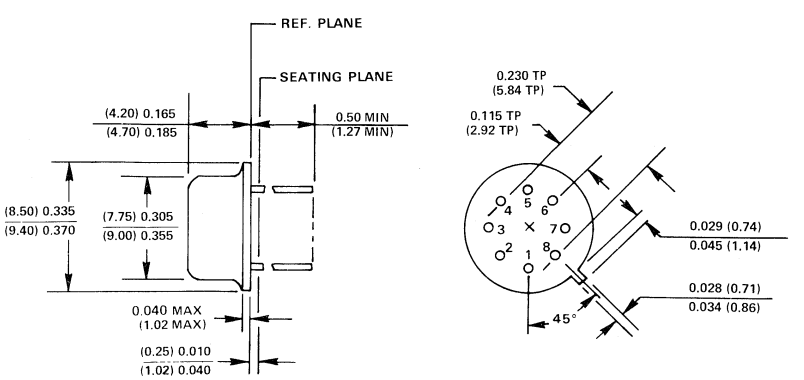


Figure 10. Input Bias Current Versus Differential Input Voltage

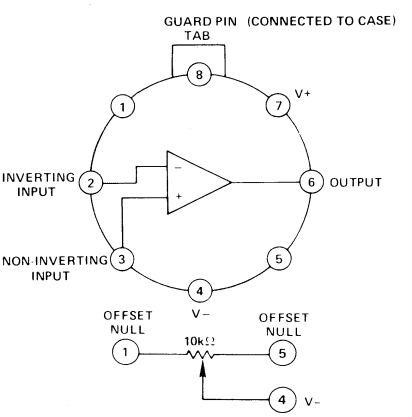
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-99

PIN CONFIGURATION



TOP VIEW

AD515 CIRCUIT APPLICATION NOTES

The AD515 is quite simple to apply to a wide variety of applications because of the pre-trimmed offset voltage and internal compensation, which minimize required external components and eliminate the need for adjustments to the device itself. The major considerations in applying this device are the external problems of layout and heat control which have already been discussed. In circuit situations employing the use of very high value resistors, such as low level current to voltage converters, electrometer operational amplifiers can be destabilized by a pole created by the small capacitance at the negative input. If this occurs, a capacitor of 2 to 5pF in parallel with the resistor will stabilize the loop. A much larger capacitor may be used if desired to limit bandwidth and thereby reduce wideband noise.

Selection of passive components employed in high impedance situations is critical. High-megohm resistors should be of the carbon film or deposited ceramic oxide to obtain the best in low noise and high stability performance. The best packaging for high-megohm resistors is a glass body sprayed with silicone varnish to minimize humidity effects. These resistors must be handled very carefully to prevent surface contamination. Capacitors for any high impedance or long term integration situation should be of a polystyrene formulation for optimum performance. Most other types have too low an insulation resistance, or high dielectric absorption.

Unlike situations involving standard operational amplifiers with much higher bias currents, balancing the impedances seen at the input terminals of the AD515 is usually unnecessary and probably undesirable. At the large source impedances where these effects matter, obtaining quality, matched resistors will be difficult. More important, instead of a cancelling effect, as with bias current, the noise voltage of the additional resistor will add by root-sum-of-squares to that of the other resistor thus increasing the total noise by about 40%. Noise currents driving the resistors also add, but in the AD515 are significant only above $10^{11}\Omega$.

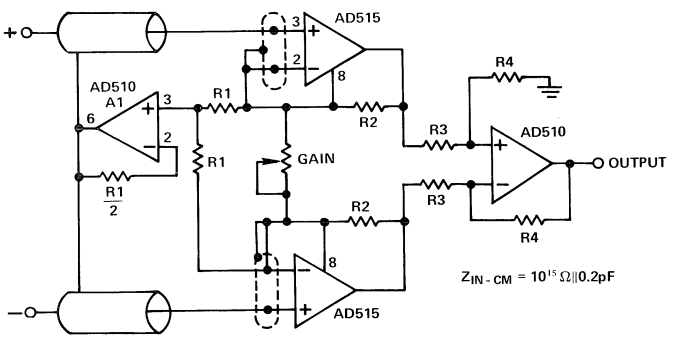


Figure 11. Very High Impedance Instrumentation Amplifier

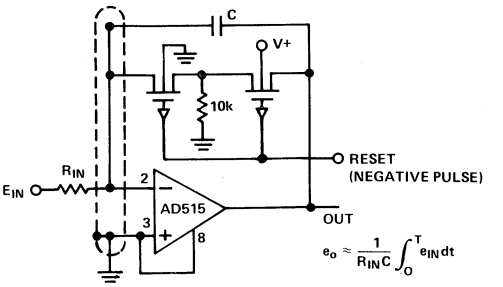


Figure 12. Low Drift Integrator with Low-Leakage Guarded Reset

LOW-LEVEL CURRENT TO VOLTAGE CONVERTERS

Figure 2 shows a standard low-level current-to-voltage converter. To obtain higher sensitivity, it is obvious to simply use a higher value feedback resistor. However, high value resistors above $10^9\Omega$ tend to be expensive, large, noisy and unstable. To avoid this, it may be desirable to use a circuit configuration with output gain, as in Figure 13. The drawback is that input errors of offset voltage drift and noise are multiplied by the same gain, but the precision performance of the AD515 makes the tradeoff easier.

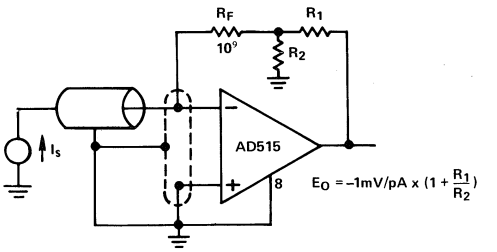


Figure 13. Picoampere to Voltage Converter with Gain

One of the problems with low-level leakage current testing or low-level current transducers (such as Clark oxygen sensors) is finding a way to apply voltage bias to the device while still grounding the device and the bias source. Figure 14 shows a technique in which the desired bias is applied at the non-inverting terminal thus forcing that voltage at the inverting terminal. The current is sensed by R_F, and the AD521 instrumentation amplifier converts the floating differential signal to a single-ended output.

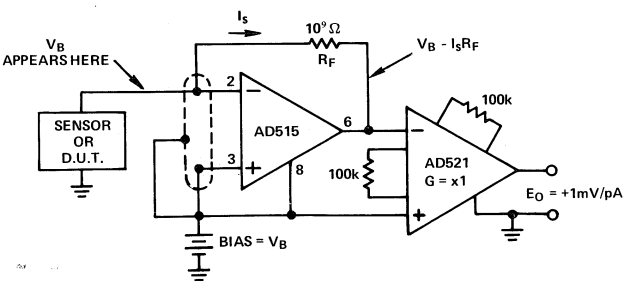


Figure 14. Current-to-Voltage Converter with Grounded Bias and Sensor

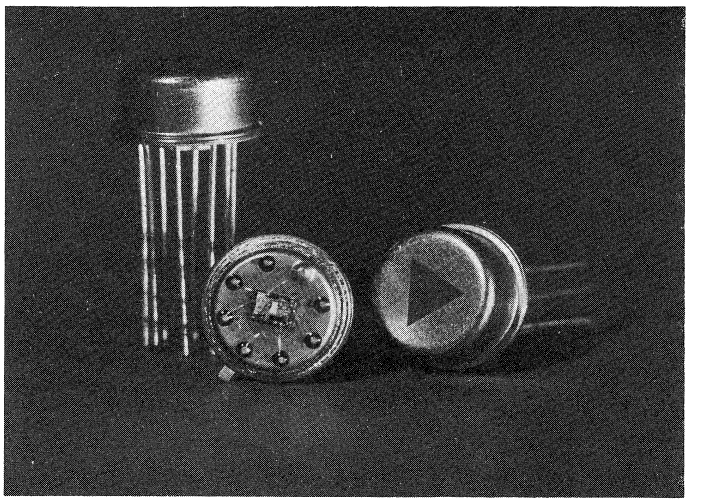
ANALOG DEVICES

Low Cost, Laser Trimmed, Precision IC Op Amp

AD517

FEATURES

Low Input Bias Current: 1nA max (AD517L)
Low Input Offset Current: 0.25nA max (AD517L)
Low V_{OS}: 25μV max (AD517L), 150μV max (AD517J)
Low V_{OS} Drift: 0.5μV/°C (AD517L)
Internal Compensation
Low Cost



PRODUCT DESCRIPTION

The AD517 is a high accuracy monolithic op amp featuring extremely low offset voltages and input currents. Analog Devices' thermally-balanced layout and superior IC processing combine to produce a truly precision device at low cost.

The AD517 is laser trimmed at the wafer level (LWT) to produce offset voltages less than 25μV and offset voltage drifts less than 0.5μV/°C unnulled. Superbeta input transistors provide extremely low input bias currents of 1nA max and offset currents as low as 0.25nA max. While these figures are comparable to presently available BIFET amplifiers at room temperature, the AD517 input currents decrease, rather than increase, at elevated temperatures. Open-loop gain in many IC amplifiers is degraded under loaded conditions due to thermal gradients on the chip. However, the AD517 layout is balanced along a thermal axis, maintaining open-loop gain in excess of 1,000,000 for a wide range of load resistances.

The input stage of the AD517 is fully protected, allowing differential input voltages of up to $\pm V_S$ without degradation of gain or bias current due to reverse breakdown. The output stage is short-circuit protected and is capable of driving a load capacitance up to 1000pF.

The AD517 is well suited to applications requiring high precision and excellent long-term stability at low cost, such as stable references, followers, bridge instruments and analog computation circuits.

The circuit is packaged in a hermetically sealed TO-99 metal can, and is available in three performance versions (J, K, and L) specified over the commercial 0 to +70°C range; and one version (AD517S) specified over the full military temperature range, −55°C to +125°C. The AD517S is also available with full processing to the requirements of MIL-STD-883A, Level B.

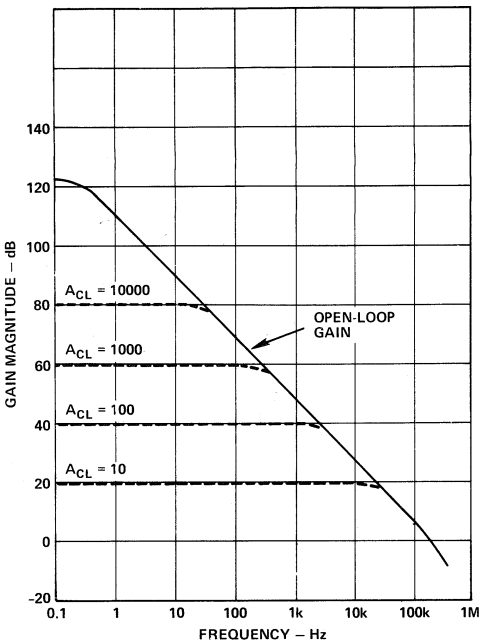
PRODUCT HIGHLIGHTS

1. Offset voltage is 100% tested and guaranteed on all models. Testing is performed using a controlled-temperature drift bath following a 5 minute warm-up period.
2. The AD517 exhibits extremely low input bias currents without sacrificing CMRR (over 100dB) or offset voltage stability.
3. The AD517 inputs are protected (to $\pm V_S$), preventing offset voltage and bias current degradation due to reverse breakdown of the input transistors.
4. Internal compensation is provided, eliminating the need for additional components (often required by high accuracy IC op amps).
5. The AD517 can directly replace 725, 108, and AD510 amplifiers. In addition, it can replace 741-type amplifiers if the offset-nulling potentiometer is removed.
6. Thermally-balanced layout insures high open-loop gain independent of thermal gradients induced by output loading, offset nulling, and power supply variations.
7. Every AD517 is baked for 48 hours at +150°C, temperature cycled from −65°C to +200°C, and subjected to a high G shock test to assure reliability and long-term stability.

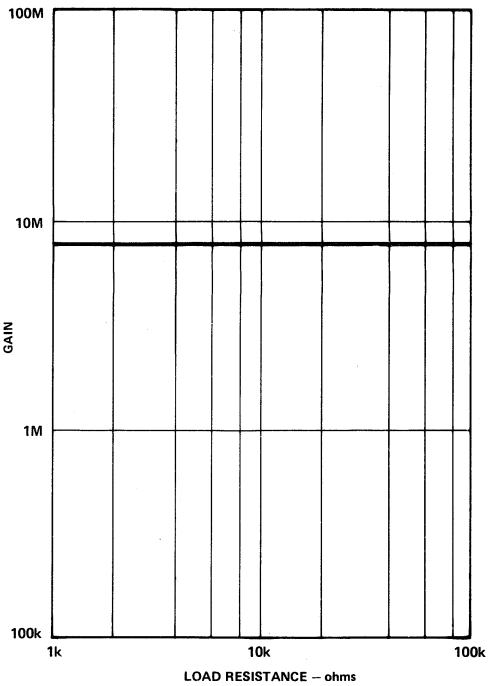
SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	AD517J	AD517K	AD517L	AD517S[1]
OPEN LOOP GAIN				
V_O = ±10V, $R_L \geqslant 2k\Omega$	10^6 min	*	*	*
T_{min} to T_{max}	500,000 min	*	*	250,000
OUTPUT CHARACTERISTICS				
Voltage @ $R_L \geqslant 2k\Omega$, T_{min} to T_{max}	±10V min	*	*	*
Load Capacitance	1000pF	*	*	*
Output Current	10mA min	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	250kHz	*	*	*
Full Power Response	1.5kHz	*	*	*
Slew Rate, Unity Gain	0.10V/μs	*	*	*
INPUT OFFSET VOLTAGE				
Initial Offset, $R_S \leqslant 10k\Omega$	150μV max	50μV max	25μV max	**
vs. Temp., T_{min} to T_{max}	3.0μV/°C max	1.0μV/°C max	0.5μV/°C max	**
vs. Supply	25μV/V max	10μV/V max	**	**
(T_{min} to T_{max})	40μV/V max	15μV/V max	**	20μV/V max
INPUT OFFSET CURRENT				
Initial	1nA max	0.75nA max	0.25nA max	**
T_{min} to T_{max}	1.5nA max	1.25nA max	0.4nA max	2nA max
INPUT BIAS CURRENT				
Initial	5nA max	2nA max	1nA max	**
T_{min} to T_{max}	8nA max	3.5nA max	1.5nA max	10nA max
vs. Temp, T_{min} to T_{max}	±20pA/°C	±10pA/°C	±4pA/°C	**
INPUT IMPEDANCE				
Differential	15MΩ‖1.5pF	20MΩ‖1.5pF	**	**
Common Mode	$2.0x10^{11}\ \Omega$	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	2μV p-p	*	*	*
f = 10Hz	$35nV/\sqrt{Hz}$	*	*	*
f = 100Hz	$25nV/\sqrt{Hz}$	*	*	*
f = 1kHz	$20nV/\sqrt{Hz}$	*	*	*
Current, f = 10Hz	$0.05pA/\sqrt{Hz}$	*	*	*
f = 100Hz	$0.03pA/\sqrt{Hz}$	*	*	*
f = 1kHz	$0.03pA/\sqrt{Hz}$	*	*	*
INPUT VOLTAGE RANGE				
Differential or Common Mode max Safe	$\pm V_S$	*	*	*
Common Mode Rejection, V_{in} = ±10V	94dB min	110dB min	**	**
Common Mode Rejection, T_{min} to T_{max}	94dB min	100dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	±(5 to 22)V
Current, Quiescent	4mA max	3mA max	**	**
TEMPERATURE RANGE				
Operating Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*

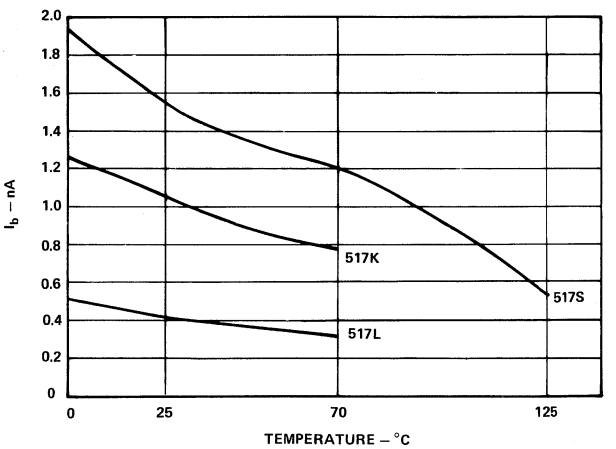
NOTES
*Specifications same as AD517J
**Specifications same as AD517K
Specifications subject to change without notice.
[1] The AD517S is available fully processed and screened to the requirements of MIL-STD-883A, Level B. Consult factory for pricing.



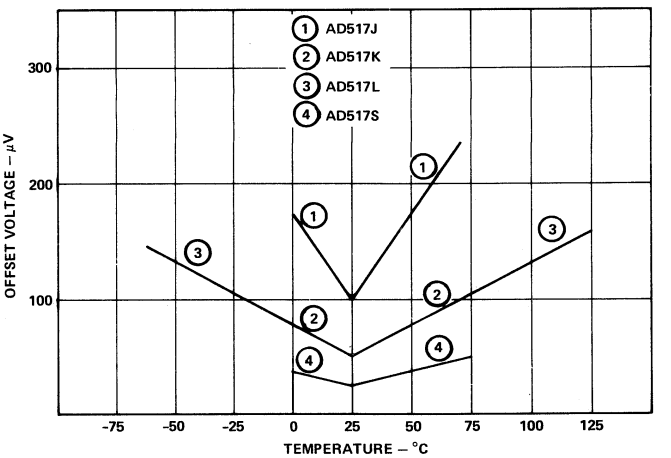
Small-Signal Gain vs. Frequency



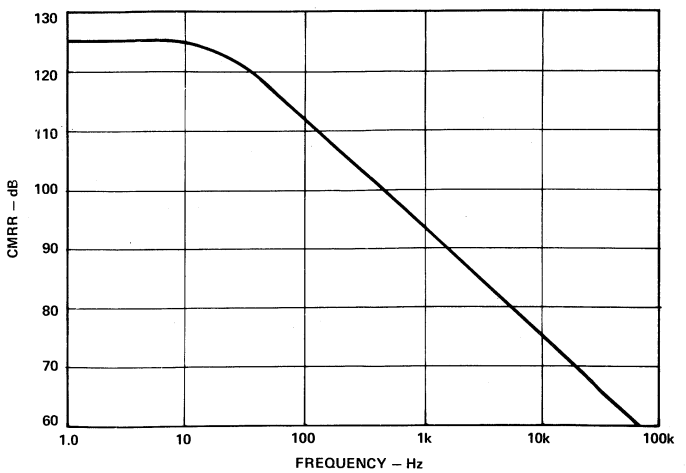
Open-Loop Gain vs. Load Resistance



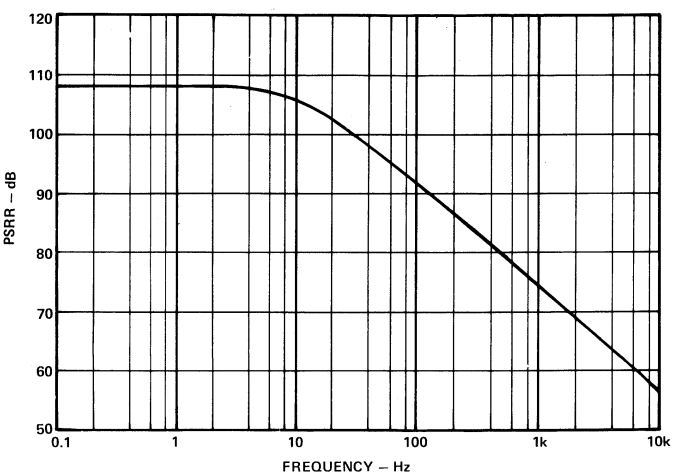
Input Bias Current vs. Temperature



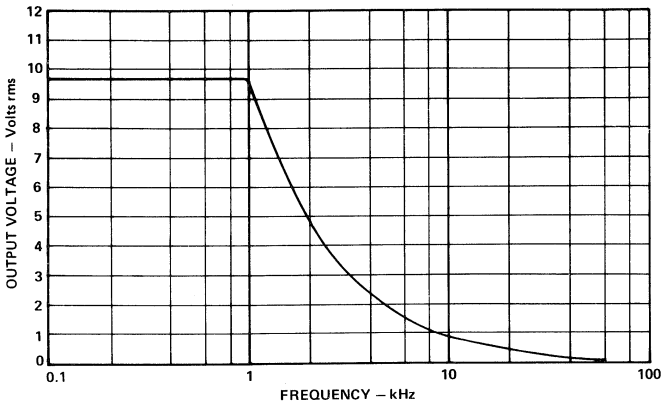
Max Untrimmed Offset Voltage vs. Temperature



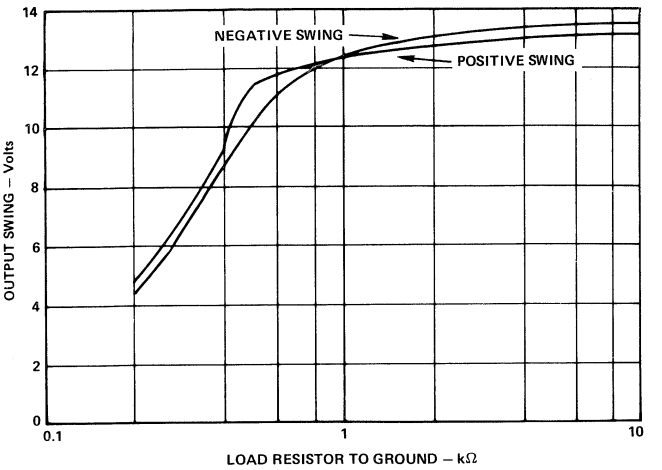
CMRR vs. Frequency



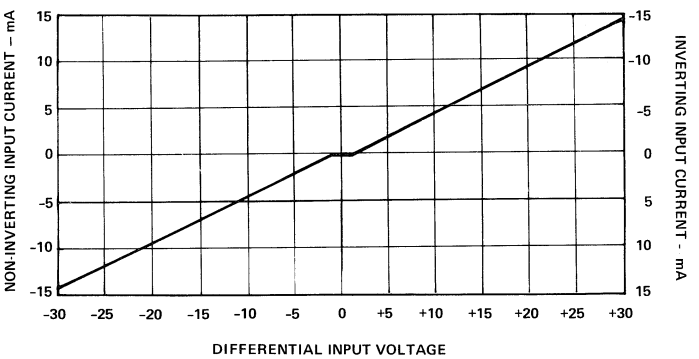
PSRR vs. Frequency



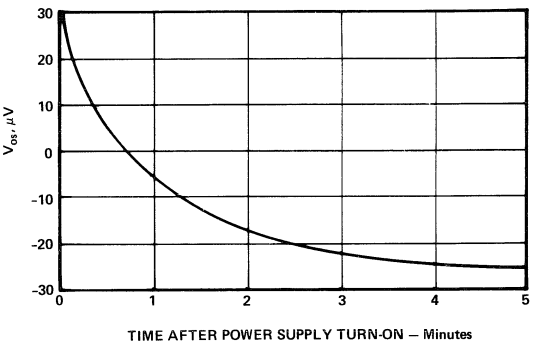
Maximum Undistorted Output vs. Frequency (Distortion ≤ 1%)



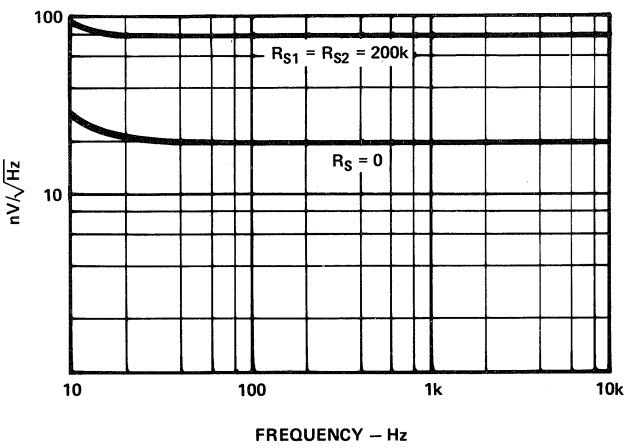
Output Voltage vs. Load Resistance



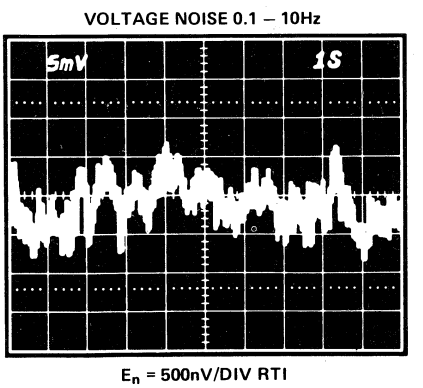
Input Current vs. Differential Input Voltage



Warm-Up Offset Voltage Drift



Total Input Noise Voltage vs. Frequency



Low Frequency Voltage Noise (0.1 to 10Hz)

NULLING THE AD517

The internally-trimmed offset voltage of the AD517 will be low enough for most circuits without further nulling. However, in high precision applications, the AD517 may be nulled using either of the following methods:

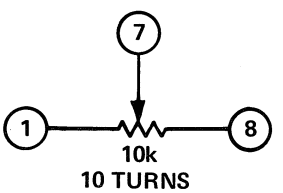
Figure 1A shows a simple circuit using a 10kΩ, ten-turn potentiometer. This circuit allows nulling to within several microvolts.

The circuit of Figure 1B is recommended in applications where nulling to within 1μV is desired. This circuit has the advantage that potentiometer instability effects are reduced by a factor of ten. Values of R_1' and R_2' are calculated as follows:

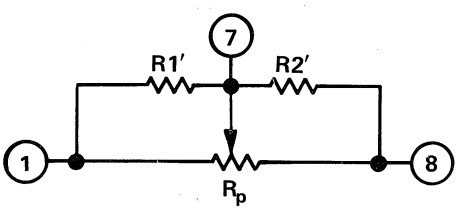
1. Null the offset to zero using a standard 10k pot, as shown in Figure 1A.
2. Measure pot halves R_1 and R_2.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1}, \qquad R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Replace the pot with R_1' and R_2' using the closest value 1% metal film resistors.
5. Use a 100k, ten-turn pot for R_p to complete the nulling.



A. Simple



B. High Precision

Figure 1. Nulling Circuits

AN INSTRUMENT INPUT AMPLIFIER USING THE AD517L

The circuit shown in Figure 2 represents a typical input stage for laboratory instruments and panel meters. The amplifier is non-inverting and offers selectable gains from 1 to 1000 in decade steps.

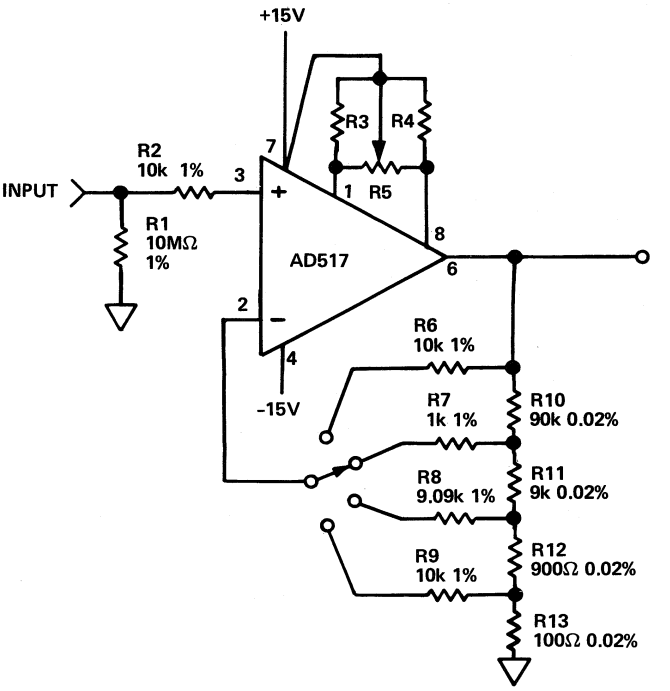


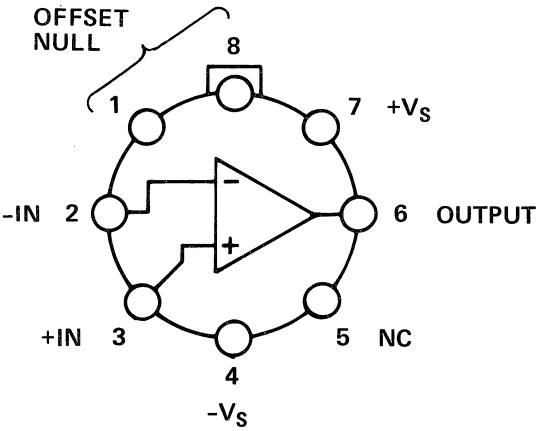
Figure 2. Stable Instrument Input Amplifier

Input impedance of this amplifier is 10 megohms, determined by resistor R_1. The offset nulling network comprised of R_3, R_4 and R_5 is the same one described earlier. If a less precise adjustment can be tolerated, a single 10k potentiometer can be substituted for R_3, R_4 and R_5.

Gain switching is accomplished in the feedback network. The divider consisting of R_{10}, R_{11}, R_{12} and R_{13} determines the gain by dividing the output and returning it to the inverting input of the amplifier. The ratio tolerances of these resistors uniquely determine the gain of the amplifier. The impedance seen by the inverting input is held constant at 10k ohms by R_6, R_7 R_8 or R_9 depending on the gain selected. Since input bias currents flow through equal resistances, the offset voltages produced will cancel each other. The input offset currents will produce an insignificant offset voltage on the order of 1 microvolt. If this offset is nulled out at the highest gain selected, it will be nulled on all ranges.

The AD517 offers excellent temperature stability in this circuit. Once the offset has been zeroed, the error produced by offset current drift will remain quite low due to the extremely low offset current drift of the AD517. A FET-input op amp would not work well in this application, since the input offset currents would double for each 10°C increase in temperature, soon exceeding the input offset currents of the AD517.

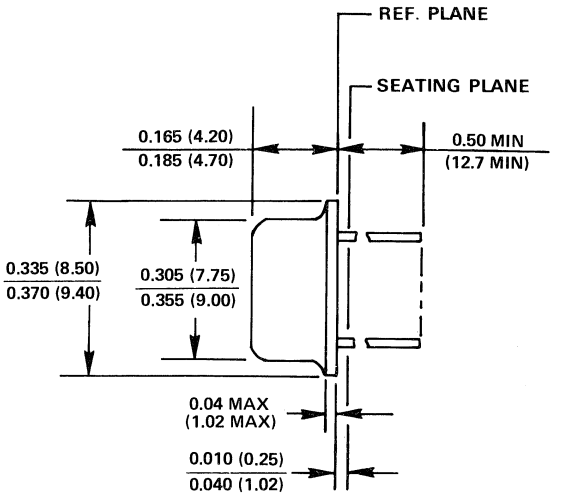
PIN CONFIGURATION



TOP VIEW

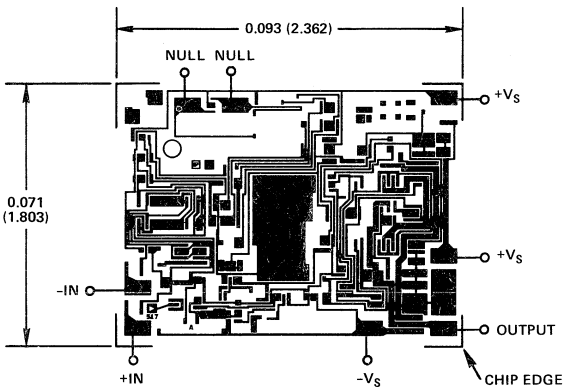
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

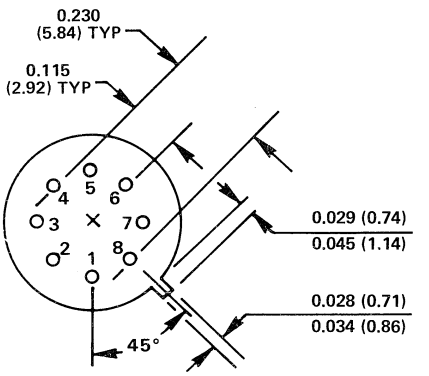


CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).



THE AD517 IS AVAILABLE IN LASER-TRIMMED CHIP FORM. THE CHIP CAN BE GUARANTEED TO J-LEVEL PERFORMANCE. CONSULT FACTORY FOR APPLICATION AND PRICING DETAILS.



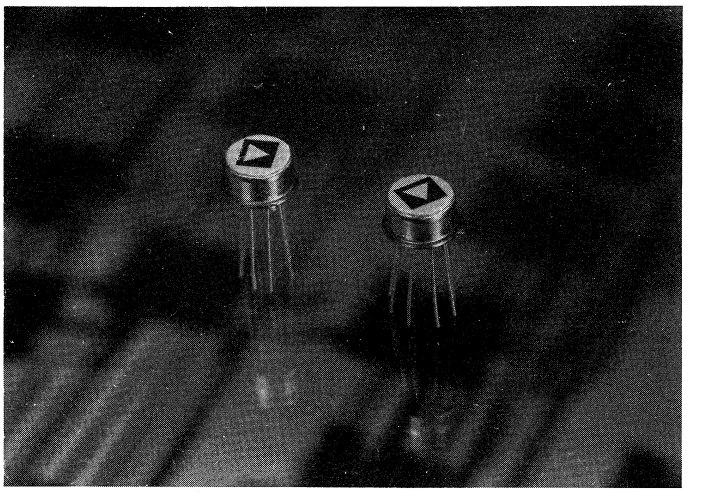
TO-99

ANALOG DEVICES

Low Cost, High Speed, IC Operational Amplifier

AD518

FEATURES
- Low Cost
- High Slew Rate: 70V/μs
- Wide Bandwidth: 12MHz
- 60° Phase Margin (At Unity Gain Crossover)
- Drives 300pF Load
- Guaranteed Low Offset Drift:
  - 15μV/°C Max (AD518K)
- Pin Compatible With 118-Type Op Amp Series
- MIL-STD-883 Availability



PRODUCT DESCRIPTION

The AD518J, AD518K, and AD518S are high speed precision monolithic operational amplifiers designed for applications where slew rate and wide bandwidth are required, but low cost and ease of use are essential. The devices are internally compensated for unity gain applications with a 60° phase margin to insure stability, a minimum unity gain slew rate of 50V/μs, and a typical bandwidth of 12MHz. In addition, in inverting applications external feedforward compensation may be added to increase the slew rate to over 100V/μs, and nearly double the bandwidth. If desired, settling time to 0.1% can be reduced to under 1μs with a single external capacitor.

The AD518's dc performance is consistent with its precision dynamic characteristics. The devices feature offset voltages below 2mV, maximum offset drifts of 15μV/°C, and offset currents below 50nA max.

The high slew rate, fast settling time, ease of use, and low cost of the AD518 make it ideal for use with D/A and A/D converters, as well as active filters, sample-and-hold circuits, and as a general purpose, fast, wideband amplifier. The AD518 is supplied in the TO-99 package. The AD518J and AD518K are specified for operation over the 0 to +70°C temperature range; the AD518S for operation from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD518 offers the user high speed performance and flexibility previously unavailable at low cost . . . . . .
   - Internal compensation for unity gain applications
   - Capability to increase slew rate to over 100V/μs and double the bandwidth by an external feedforward technique
   - Capability to reduce settling time to under 1μs to 0.1% with a single external capacitor
   - Differential input capability
2. The phase margin of the AD518, uncompensated at the unity gain crossover frequency, is 60°, providing unconditional stability for all conditions. This conservative phase margin represents a clear improvement over that of the 118 series IC op amps currently available.
3. The static performance of the AD518 is consistent with its excellent dynamic performance, providing offset voltage drift under 15μV/°C, CMRR of 80dB, and offset current below 50nA.
4. Every AD518 is stored for 40 hours at +200°C, temperature cycled 10 times from −65°C to +150°C, and subjected to a high G shock test to insure reliability and long-term stability.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

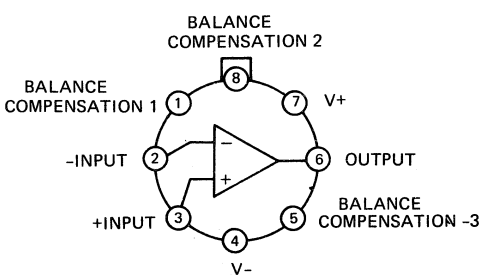
PARAMETER	AD518J	AD518K	AD518S
OPEN LOOP GAIN			
$R_L \geq 2k\Omega$, V_O = ±10V	25,000 min (100,000 typ)	50,000 min (100,000 typ)	50,000 min (100,000 typ)
@ T_A = min to max	20,000 min	25,000 min	25,000 min
OUTPUT CHARACTERISTICS			
Voltage @ $R_L \geq 2k\Omega$, T_A = min to max	±12V min (±13V typ)	*	*
Current @ V_O = ±10V	±10mA	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	12MHz	*	*
Slew Rate, Unity Gain	50V/μs min (70V/μs typ)	*	*
Settling Time to 0.1% (Single Capacitor Compensation)	800ns	*	*
Phase Margin, Uncompensated at Unity Gain Crossover Frequency	60°	*	*
INPUT OFFSET VOLTAGE			
Initial, $R_S \leq 10k\Omega$	10mV max (4mV typ)	4mV max (2mV typ)	4mV max (2mV typ)
@ T_A = min to max	15mV max	6mV max	6mV max
Avg vs. Temp, T_A = min to max	10μV/°C	15μV/°C max (5μV/°C typ)	20μV/°C max (10μV/°C typ)
Avg vs. Supply, T_A = min to max	65dB min (80dB typ)	80dB min (90dB typ)	80dB min (90dB typ)
INPUT BIAS CURRENT			
Initial	500nA max (120nA typ)	250nA max (120nA typ)	250nA max (120nA typ)
@ T_A = min to max	750nA max	400nA max	400nA max
INPUT OFFSET CURRENT			
Initial	200nA max (30nA typ)	50nA max (6nA typ)	50nA max (6nA typ)
@ T_A = min to max	300nA max	100nA max	100nA max
INPUT IMPEDANCE			
Differential	0.5MΩ min (3.0MΩ typ)	*	*
INPUT VOLTAGE RANGE †			
Common Mode, max safe	±V_S	*	*
Operating, V_S = ±15V	±11.5V	*	*
Common Mode Rejection Ratio	70dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	10mA max (5mA typ)	7mA max (5mA typ)	7mA max (5mA typ)
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*

† The inputs are shunted with back-to-back diodes; if the differential input may exceed ±1 volt, a resistor should be used to limit the input current to 10mA.

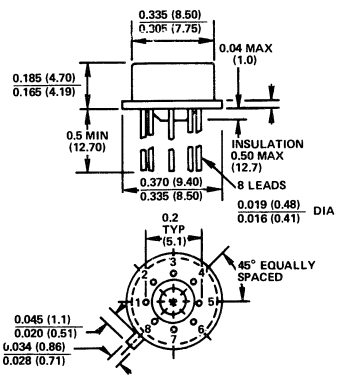
*Specifications same as AD518J.

Specifications and prices subject to change without notice.

PIN CONFIGURATION
Top View



OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).



STABILITY & PHASE MARGIN

Perhaps one of the most meaningful ways to express the relative stability of a closed loop amplifier is in terms of phase margin. Phase margin is measured at that frequency where the open loop gain of the amplifier becomes unity or 0dB. It is the additional amount of phase shift that, if introduced in the loop, would make the loop unstable.

At very low frequencies the gain of most operational amplifiers is generally large. Moreover, the amplifier output signal is very nearly in phase with the differential input signal. This output is, therefore, nearly 180° out of phase with the feedback signal applied to the inverting input. At sufficiently high frequencies the gain of the amplifier begins to decrease as a function of frequency, with the resulting consequence of a lagging phase characteristic. That is, as the gain falls with increasing frequency, the phase of the output signal at a given frequency will lag the phase of the input signal. The phase shift depends most critically on the slope of the gain curve with respect to the logarithm of the frequency at the frequency where the phase is measured. If the gain changes more rapidly than 12dB/octave over a substantial frequency range, the minimum resulting phase shift may exceed 180°.

To insure amplifier stability, it is necessary that the phase shift near the unity gain frequency (12MHz in the AD518) is less than 180°. Moreover, it is generally required that the phase shift be substantially below the critical stability point to insure proper system performance. If the unity gain phase shift approaches 180°, the system will be on the verge of oscillation. As a result, there will be a large peak in the closed loop response near the unity loop gain frequency. This sharply peaked frequency response generally causes an undesirable small signal transient response with a poorly damped overshoot.

The term *phase margin* refers to the difference between 180° and the actual frequency-dependent phase shift at the system unity gain frequency. It is the margin between the actual system phase shift and the critical phase shift at which oscillation will occur. Not only does it indicate the relative immunity to oscillation, but it also gives some indication about the peaking and overshoot that can be expected.

The simple pole or frequency response of a single R-C network has a gain slope of 6dB/octave. This response has an associated phase shift which is asymptotic to −90°. Linear systems which are dominated by this characteristic in their open loop response are stable. They show no overshoot or ringing in their small signal transient response. Additional poles, either above or below the unity loop gain frequency, will add phase shift. As phase shift increases up to a lagging phase of about 120°, representing a 60° phase margin, little or no peaking will result. As the unity gain phase shift increases, peaking becomes more and more evident. For example, as the phase shift reaches 160° (20° of phase margin), between 9 and 10dB of peaking will occur.

The AD518 has been designed for a 60° phase margin at the unity gain crossover frequency, for absolute stability and absence of ringing and overshoot. (Note the transient response of the AD518 in Figure 1.) Note also in Figure 2 that the phase shift at 12MHz, the unity gain crossover frequency, is 120°, representing 60° of phase margin.

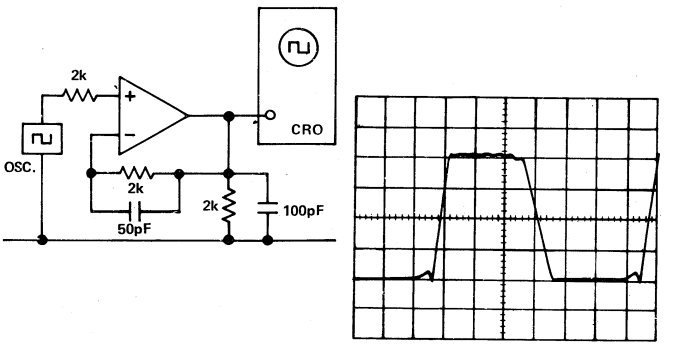


Figure 1. Transient Response of the AD518

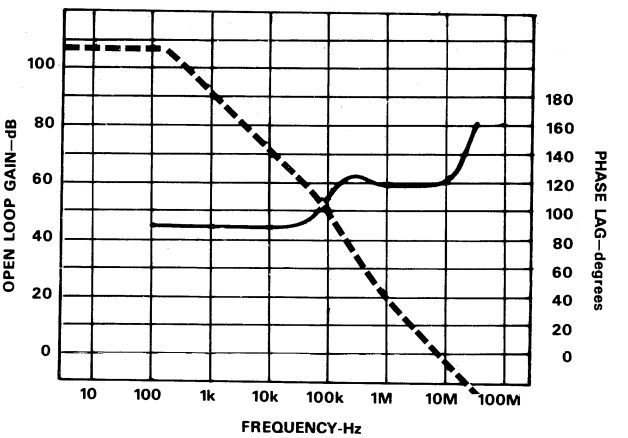


Figure 2. Amplitude and Phase Response of the AD518

THE FLEXIBILITY OF THE AD518

MINIMUM SETTLING TIME APPLICATIONS

For applications where a minimum settling time is desired, the settling time of the AD518 may be reduced significantly by employing the compensation scheme suggested in Figure 3.

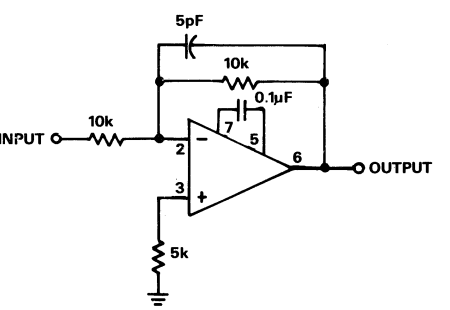


Figure 3. Minimum Settling Time Compensation

Using the 0.1μF capacitor from Pin 5 to V+ (Pin 7), the settling time to 0.1% is reduced from 2μs to 800ns.

HIGHER BANDWIDTH OR
HIGHER SLEW RATE APPLICATIONS

For applications where higher bandwidth is desired, the bandwidth of the AD518 may be increased to nearly 25MHz by using the feedforward technique shown in Figure 4.

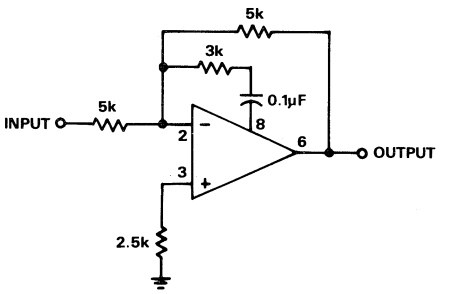


Figure 4. High Bandwidth Configuration

For applications where higher slew rate is desired, the slew rate of the AD518 may be nearly doubled using the technique shown in Figure 5.

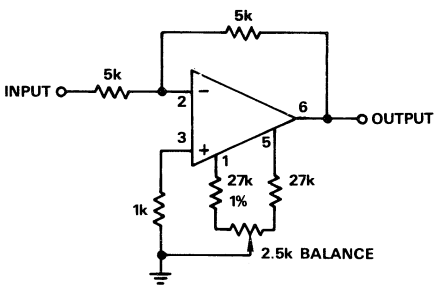


Figure 5. High Slew Rate Configuration

Note that the techniques of Figures 4 and 5 may be used in conjunction with each other to both double the bandwidth to 25MHz and increase the slew rate to 100–140V/μs.

USING THE AD518

The connection scheme employed when using the AD518 is considerably more important than for low frequency, general purpose amplifiers. The primary purpose of the 0.1μF bypass capacitors shown in Figure 6 is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V– 0.1μF capacitor equalizes the supply grounds, while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. This signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal. In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

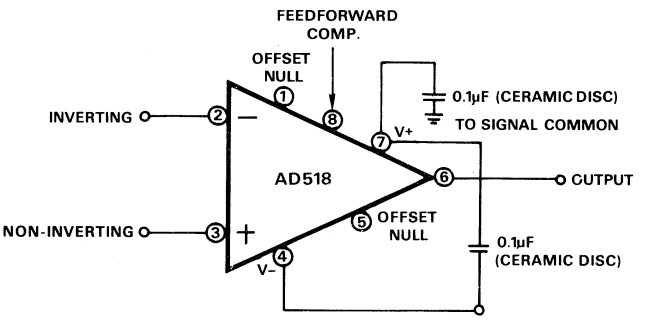
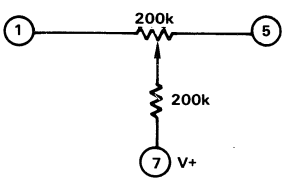


Figure 6. General Purpose Connection Diagram

NULLING THE AD518



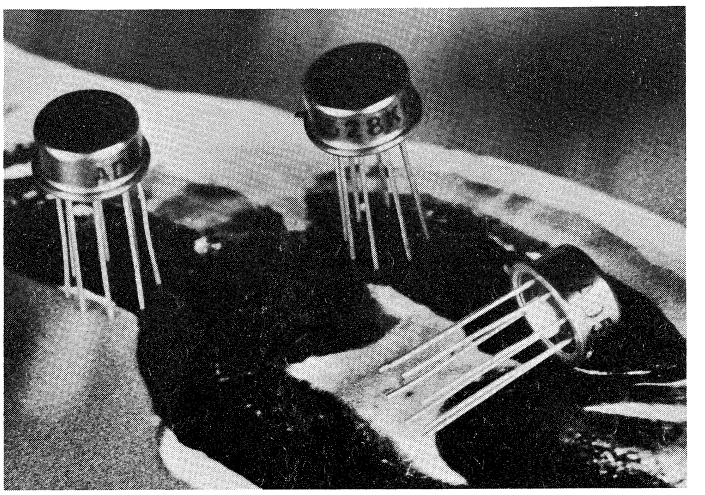
OTHER IC HIGH SPEED AMPLIFIERS AVAILABLE

AD505	Slew Rate of 120V/μs min Bias Current of 25nA max Offset Voltage Drift of 15μV/°C max
AD507	35MHz Gain Bandwidth Slew Rate of 25V/μs min Bias Current of 15nA max Offset Voltage Drift of 15μV/°C max
AD509	Settles to 0.01% in 1μs Settles to 0.1% in 200ns Slew Rate of 100V/μs min

High Speed, Precision, FET-Input Operational Amplifier

AD528

FEATURES
High Slew Rate: 70V/μs
Wide Bandwidth: 10MHz
Low Bias Current: 15pA max (AD528K, S)
Low Offset Voltage: 1mV max (AD528K, S)
Inverting and Non-Inverting Operation
MIL-STD-883 Availability
Low Cost



PRODUCT DESCRIPTION

The AD528J, AD528K and AD528S are high speed, precision FET-input operational amplifiers combining the advantages of very high slew rate and wide bandwidth with the ultra-low input currents only available with FET-input designs. The devices are internally compensated for unity gain applications with a 60° phase margin to insure stability, a minimum unity gain slew rate of 50V/μs, and a typical bandwidth of 10MHz. In addition, in inverting applications external feed forward compensation may be added to increase the slew rate to over 100V/μs, and nearly double the bandwidth. If desired, settling time to 0.1% can be reduced to under 1μs with a single external capacitor.

The AD528 offers the user dc performance previously unavailable in conventional high speed designs. The devices offer maximum bias currents under 15pA, laser-trimmed offset voltages below 1mV, and offset voltage drifts below 25μV/°C.

The high slew rate, wide bandwidth, and low input currents of the AD528 make it ideal for use in sample-hold circuits, A/D, D/A and sampled data systems, and high speed integrators. The AD528 is supplied in the TO-99 package. The AD528J and AD528K are specified for operation over the 0 to +70°C temperature range; the AD528S for operation from -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD528, guaranteeing bias currents of 15pA, offers the user the lowest input current available in a high speed design. In addition, at Analog Devices.....
   - all IC FET op amps meet their published input bias current specs after full warm-up. Conventional high speed IC testing does not allow for self-heating of the chip due to internal power dissipation under operating conditions;
   - all IC FET op amps meet their published input bias current specs at either input. Conventional IC FET op amps generally specify bias current as the average of the two input currents.
2. The AD528 offers the user excellent high speed performance and flexibility.
   - Internal compensation for all gains.
   - Capability to increase slew rate to over 100V/μs and double the bandwidth by an external feed forward technique.
   - Capability to reduce settling time to under 1μs to 0.1% with a single external capacitor.
   - Differential input capability.
3. The phase margin of the AD528, uncompensated at the unity gain crossover frequency, is 60° providing unconditional stability for all applications.
4. Every AD528 is specified for 48 hours at 200°C, temperature cycled 10 times from -65°C to +150°C, and subjected to a high G shock test to insure reliability and long-term stability.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise specified)

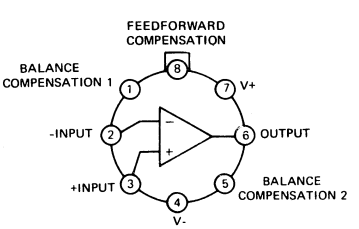
MODEL	AD528J	AD528K	AD528S
OPEN LOOP GAIN			
$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25,000 min (100,000 typ)	50,000 min (100,000 typ)	**
@ T_A = min to max	25,000 min	25,000	**
OUTPUT CHARACTERISTICS			
Voltage @ $R_L \geq 2k\Omega$, T_A = min to max	±10V min	*	*
Current @ $V_O = \pm 10V$	±10mA	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	10MHz	*	*
Slew Rate, Unity Gain	50V/μs min (70V/μs typ)	*	*
Settling Time to 0.1% (Single Capacitor Compensation)	800ns	*	*
Phase Margin, Uncompensated at Unity Gain Crossover Frequency	60°	*	*
INPUT OFFSET VOLTAGE			
Initial, $R_S \leq 10k\Omega$	3mV max (1mV typ)	1mV max (0.3mV typ)	**
@ T_A = min to max	5mV max	2mV max	3mV max
Avg vs Temp, T_A = min to max	50μV/°C max (25μV/°C typ)	25μV/°C max (10μV/°C typ)	**
Avg vs Supply, T_A = min to max	70dB min (90dB typ)	80dB min (90dB typ)	**
INPUT BIAS CURRENT			
Warmed up at 25°C	30pA max (10pA typ)	15pA max (5pA typ)	**
INPUT OFFSET CURRENT			
Warmed up at 25°C	5pA max	2pA max	**
INPUT NOISE			
Voltage, 0.1 to 10Hz	5μV(p-p)	*	*
INPUT IMPEDANCE			
Differential	$10^{12}\Omega \| 6pF$	*	*
INPUT VOLTAGE RANGE			
Differential (Note 1)	±20V	*	*
Common Mode, max safe	$\pm V_S$	*	*
Common Mode Rejection Ratio	70dB min (90dB typ)	80dB min (90dB typ)	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	7mA max (5mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*

*Specifications same as AD528J.
**Specifications same as AD528K.

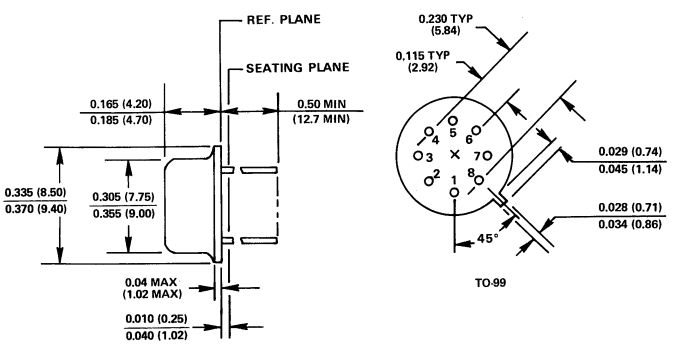
NOTE 1. Defined as voltage between inputs such that neither exceeds ±10V from ground.

Specifications and prices subject to change without notice.

PIN CONFIGURATION
Top View



OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).



USING THE AD528

When designing with the AD528, the user should be aware of the necessity to adhere to the precautions normally observed when using FET op amps, as well as those observed when using fast bipolar designs.

THE AD528 AS A HIGH SPEED OP AMP

Phase Margin. The AD528 is internally compensated for unconditional stability at all gains. Perhaps one of the most meaningful ways to express the stability of a closed loop amplifier is in terms of its phase margin. Phase margin is measured at the frequency where the open loop gain of the amplifier becomes unity or 0dB. It is the additional amount of phase shift that, if introduced in the loop, would make the loop unstable. The AD528 has been designed for a 60° phase margin at the unity gain crossover frequency for absolute stability and absence of ringing and overshoot. Note the transient response of the AD528 in Figure 1. Note also in Figure 2 that the phase shift at 10MHz, the unity gain crossover frequency, is 120° representing 60° of phase margin.

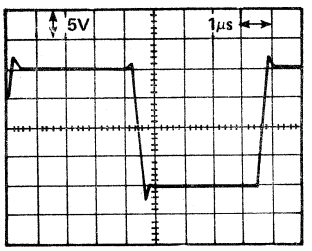


Figure 1. Transient Response of the AD528

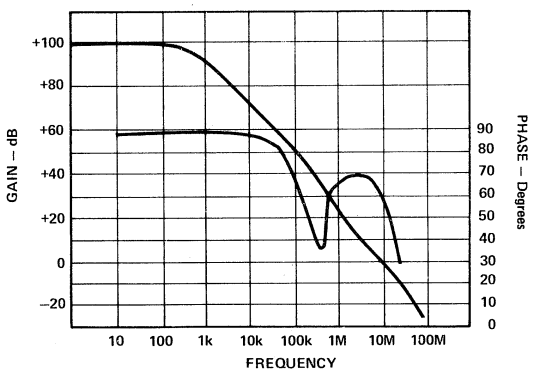


Figure 2a. Small Signal Amplitude and Phase Response

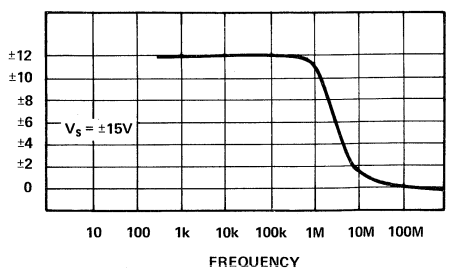


Figure 2b. Large Signal Amplitude and Phase Response

Connecting the AD528. The connection scheme employed when using the AD528 is considerably more important than for low frequency, general purpose amplifiers. The primary purpose of the 0.1μF bypass capacitors shown in Figure 3 is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V– 0.1μF capacitor equalizes the supply grounds, while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. This signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

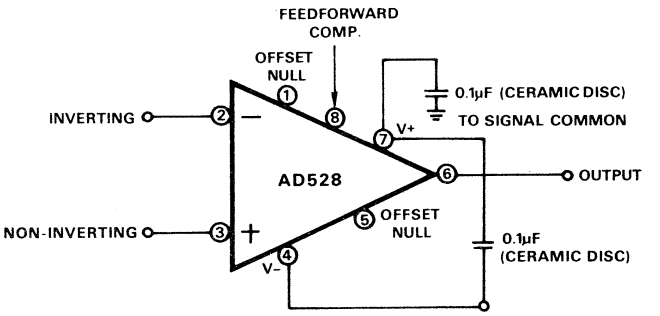


Figure 3. General Purpose Connection Diagram

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal. In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

Neutralizing Input Capacitance. The common mode capacitance at each input is approximately 6pF. If large input or feedback resistors are used, as is often the case with FET op amps, a 6–10pF capacitor should be added in parallel with the larger resistor to cancel the pole which is introduced by the input capacitance. For precision, fast settling applications, it may be desirable to use a trimmer capacitor to optimize the response.

Capacitive Loading. The AD528 can drive 100pF capacitive loads; for larger capacitive loads, an isolation resistor, as shown in Figure 4 is recommended.

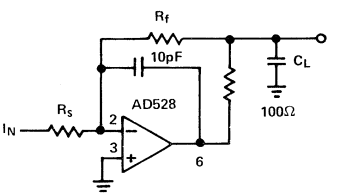


Figure 4. Isolating a Capacitive Load Up To 500pF

THE AD528 AS A FET OP AMP

1. The AD528 meets its published input bias current and offset voltage spec after full warm-up. Conventional IC testing does not pick up self-heating of the chip due to internal power dissipation. This can cause up to an 8X increase in bias and offset currents.
2. The input bias current of the AD528 is specified as a maximum at either input, not as an average of the bias current at both terminals.
3. The gain of many IC FET op amps decreases by an order of magnitude when nulled. The AD528 guarantees a minimum gain with V_{OS} nulled and unnulled.

4. The laser-trimmed offset voltages below 1mV preclude the necessity for further nulling in most applications. If any small adjustments are required, there will be a very minimal effect on the offset drift coefficient.

THE FLEXIBILITY OF THE AD528

MINIMUM SETTLING TIME APPLICATIONS

For applications where a minimum settling time is desired, the settling time of the AD528 may be reduced significantly by employing the compensation scheme suggested in Figure 5.

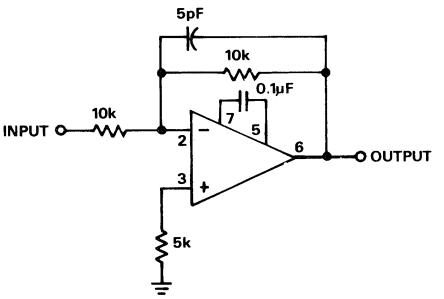


Figure 5. Minimum Settling Time Configuration

Using the 0.1μF capacitor from Pin 5 to V+ (Pin 7), the settling time to 0.1% is reduced from 2μs to 800ns.

HIGHER BANDWIDTH OR HIGHER SLEW RATE APPLICATIONS

For applications where higher bandwidth is desired, the bandwidth of the AD528 may be increased to nearly 25MHz by using the feedforward technique shown in Figure 6.

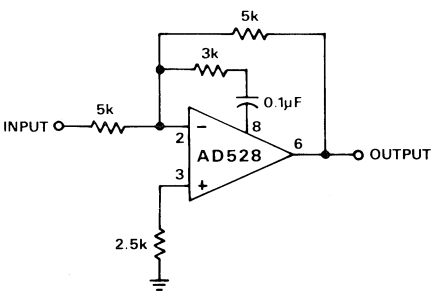


Figure 6. High Bandwidth Configuration

For applications where higher slew rate is desired, the slew rate of the AD528 may be nearly doubled using the technique shown in Figure 7.

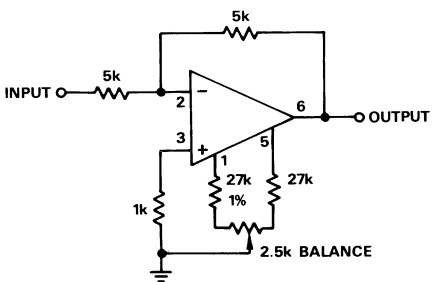


Figure 7. High Slew Rate Configuration

Note that the techniques in Figures 6 and 7 may be used in conjunction with each other to both double the bandwidth to 25MHz and increase the slew rate to 100–140V/μs.

NOISE PERFORMANCE OF THE AD528

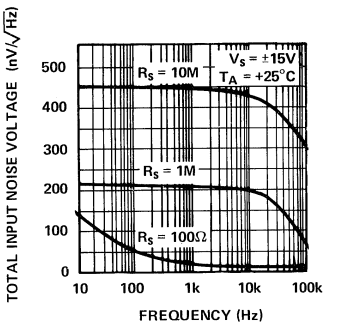


Figure 8. Total Input Noise Voltage vs. Frequency

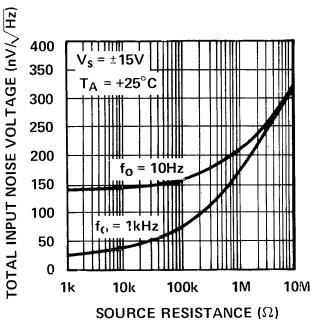
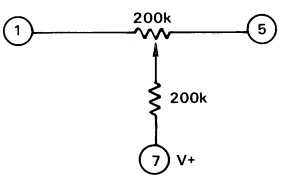


Figure 9. Total Input Noise vs. Source Resistance

NULLING THE AD528



OTHER IC HIGH SPEED AMPLIFIERS AVAILABLE

AD505 Slew Rate of 120V/μs min
Bias Current of 25nA max
Offset Voltage Drift of 15μV/°C max

AD507 35MHz Gain Bandwidth
Slew Rate of 25V/μs min
Bias Current of 15nA max
Offset Voltage Drift of 15μV/°C max

AD509 Settles to 0.01% in 1μs
Settles to 0.1% in 200ns
Slew Rate of 100V/μs min

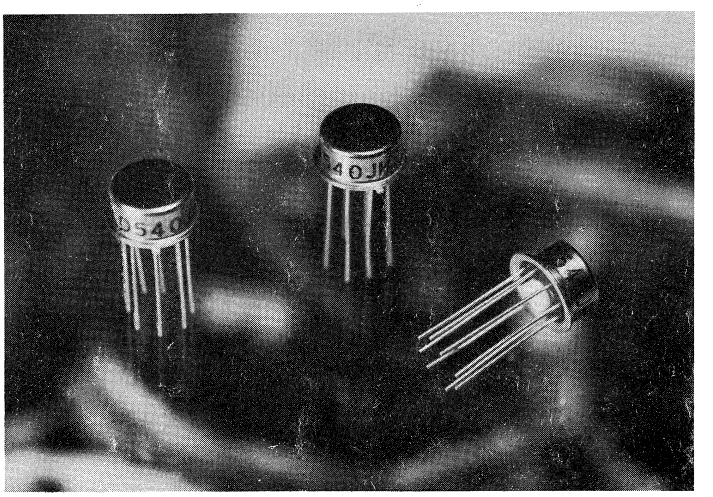
AD518 Slew Rate of 50V/μs min
Internally Compensated For All Gains
Low Cost

ANALOG DEVICES

High Accuracy, Low Cost, FET-Input Operational Amplifier

AD540

FEATURES
Low Cost
Low I_b: 25pA max (K)
Low V_{os}: 20mV max (K)
Low V_{os} Drift: 25μV/°C max (K)
High Differential Input Voltage Capability: ±20V



PRODUCT DESCRIPTION

The AD540 is the lowest cost, high accuracy FET-input op amp available which provides the user with low bias currents, high overall performance, and accurately specified predictable operation. The device offers maximum bias currents as low as 25pA, offset voltages below 20mV, maximum offset voltage drift below 25μV/°C and a minimum gain of 50,000.

All devices are free from latchup and are short-circuit protected. No external compensation is required as the internal 6dB/octave roll-off provides stability in closed loop applications.

The AD540 is suggested for all FET-input amplifier requirements where low cost is of prime importance. Its performance is comparable to modular FET op amps, but its IC construction reduces the price significantly below that of modules.

All versions of the AD540 are supplied in the hermetically-sealed, 8-pin, TO-99 package. The AD540J and AD540K are specified for 0 to +70°C applications, while the AD540S is offered for operation over the full military temperature range of -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD540 op amp meets specified input bias current and offset voltage values after full warm-up. Conventional high speed IC testing does not allow for self-heating of the chip due to internal power dissipation under operating conditions.
2. The bias currents of the AD540 are specified as a maximum for either input. Conventional IC FET op amps generally specify bias currents as the average of the two input currents.
3. Unlike many FET-input op amps, the AD540 allows a maximum differential input voltage of ±20V dc. Standard "bootstrapped" FET-input op amps permit maximum differential input voltages of only about ±3V.
4. Offset nulling of the AD540 is accomplished without affecting the operating current of the FET's and results in relatively small changes in temperature drift characteristics. The additional drift induced by nulling is only ±2.0μV/°C per millivolt of nulled offset, compared to several times this for other IC FET op amps.
5. The gain of the AD540 is measured with the offset voltage nulled. Nulling a FET-input op amp can cause the gain to decrease below its specified limit. The gain of the AD540 is fully guaranteed with the offset voltage both nulled and unnulled.
6. To maximize the reliability inherent in IC construction, every AD540 is stored for 40 hours at +150°C, temperature cycled from -65°C to +125° and receives a high impact shock test.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD540J	AD540K	AD540S
OPEN LOOP GAIN (Note 1)			
V_{out} = ±10V, $R_L \geqslant 2k\Omega$	20,000 min	50,000 min	**
T_A = min to max	15,000 min	25,000 min	**
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±13V typ)	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±12V min (±14V typ)	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	100kHz	*	*
Slew Rate, Unity Gain	6.0V/μs	*	*
INPUT OFFSET VOLTAGE (Note 2)	50mV max	20mV max	**
vs. Temperature	75μV/°C max	25μV/°C max	50μV/°C max
vs. Supply, T_A = min to max	400μV/V max	300μV/V max	**
INPUT BIAS CURRENT			
Either Input (Note 3)	50pA max	25pA max	**
INPUT IMPEDANCE			
Differential	$10^{10}\Omega \| 2pF$	*	*
Common Mode	$10^{11}\Omega \| 2pF$	*	*
INPUT VOLTAGE RANGE			
Differential (Note 4)	±20V	*	*
Common Mode	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{in} = ±10V	70dB min	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Quiescent Current	7mA max (3mA typ)	*	*
TEMPERATURE RANGE			
Operating, Rated Performance	0 to +70°C	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*

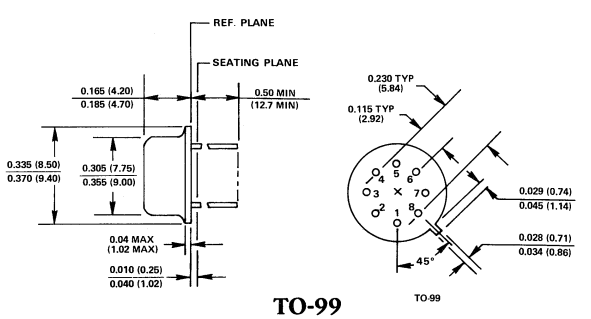
NOTE:
1. Open Loop Gain is specified with V_{os} both nulled and unnulled.
2. Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
3. Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
4. Defined as voltage between inputs, such that neither exceeds ±10V from ground.

* Specifications same as AD540J.
** Specifications same as AD540K.

Specifications and prices subject to change without notice.

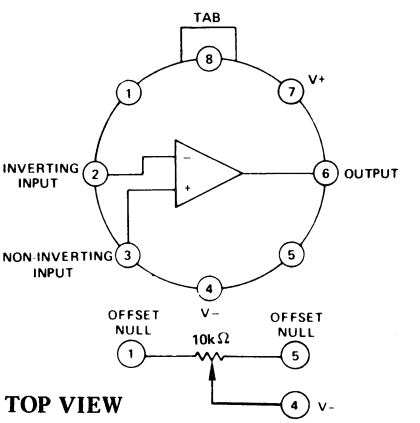
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-99

PIN CONFIGURATION



TOP VIEW

APPLYING THE AD540

The AD540 is especially designed for low cost applications involving the measurement of low level currents or small voltages from high impedance sources in which bias current can be a primary source of error. Input bias current contributes to error in two ways: (1) in current measuring configurations the bias current limits the resolution of a current signal; (2) the bias current produces a voltage offset which is proportional to the value of input resistance (in the case of an inverting configuration) or source impedance (when the non-inverting "buffer" connection is used). The AD540 FET-input operational amplifier is, therefore, of use where small currents are to be measured or where relatively low voltage drift is necessary despite large values of source resistance.

APPLICATIONS CONSIDERATIONS

BIAS CURRENTS. Most IC FET op amp manufacturers specify maximum bias currents as the value immediately after turn-on. Since FET bias currents double every 10°C and since most FET op amps have case temperature increases of 15°C to 20°C above ambient, initial "maximum" readings may be only ¼ of the true warmed-up value. Furthermore, most IC FET op amp manufacturers specify I_b as the average of both input currents, sometimes resulting in twice the maximum bias current appearing at the input being used. The total result is that 8X the expected bias current may appear at either input terminal in a warmed-up operating unit.

The AD540 specifies maximum bias current at either input after warm-up, thus giving the user the values he expected.

IMPROVING BIAS CURRENT BEYOND GUARANTEED VALUES. Bias currents can be substantially reduced in the AD540 by decreasing the junction temperature of the devices. One technique to accomplish this is to reduce the operating supply voltage. This procedure will decrease the power dissipation of the device, which will in turn result in a lower junction temperature and lower bias currents. The supply voltage effect on bias current is shown in Figure 1.

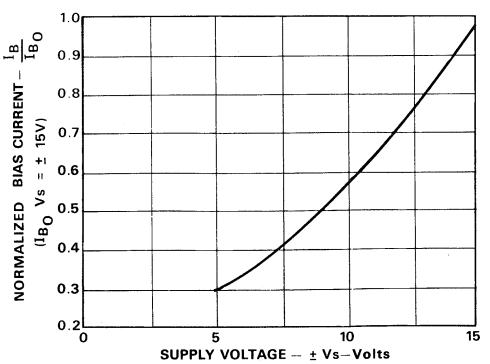


Figure 1. Normalized Bias Current vs. Supply Voltage

Operation of the AD540K at ±5V reduces the warmed-up bias current by 70% to a typical value of 8pA.

A second technique is the use of a suitable heat sink. Wakefield Engineering Series 200 heat sinks were selected to demonstrate this effect. The characteristic bias current vs. case temperature above ambient is shown in Figure 2. Bias current has been normalized with unity representing the 25°C free air reading. Note that the use of the Model 209 heat sink reduces warmed-up bias current by 60% to 10pA in the AD540K.

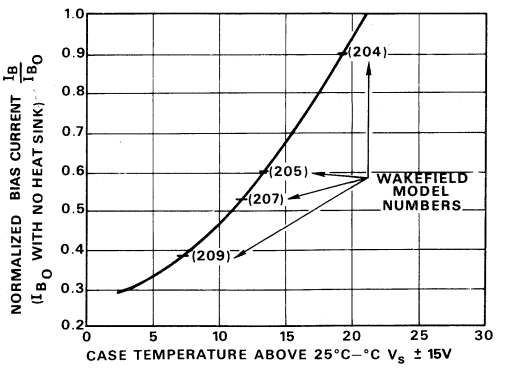


Figure 2. Normalized Bias Current vs. Case Temperature

Both of these techniques may be used together for obtaining lower bias currents. Remember that loading the output can also affect the power dissipation.

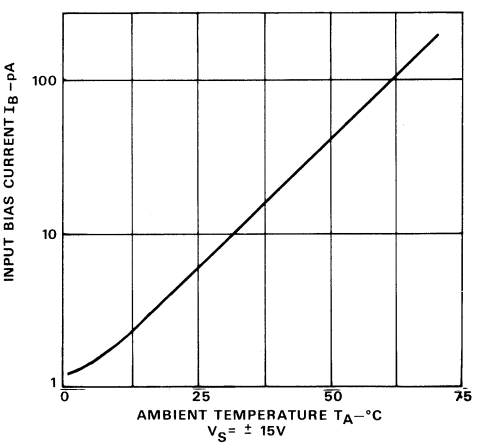


Figure 3. Input Bias Current vs. Temperature

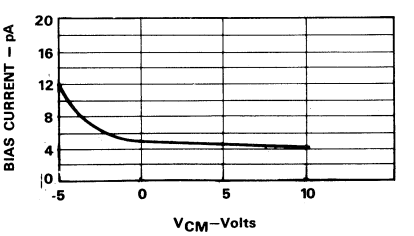


Figure 4. Bias Current vs. Common Mode Voltage.

INPUT CONSIDERATIONS. Unlike some FET-input operational amplifiers, the AD540 accommodates differential input voltages of up to ±20V....without any degradation in bias current. In certain time-dependent applications, such as charge amplifiers and integrators, large differential input voltages temporarily occur which may exceed the rated value of a typical FET op amp (approximately ±3V differential).

By utilizing un-bootstrapped FET's at the inputs, the AD540 assures the user of expected performance at large differential input voltages....without the use of protective diodes or resistors.

OFFSET VOLTAGE DRIFT. Most commercially available IC FET op amps are nulled by adjusting the FET operating currents, causing the offset voltage temperature coefficients to vary 3 to 6$\mu V/^{\circ}C$ per millivolt of offset nulled. Thus a conventional FET op amp with 20mV initial offset, when nulled may display an additional offset drift of 60 to 120$\mu V/^{\circ}C$, in addition to its nulled value.

The AD540 achieves nulling without disturbing the operating currents of the FET's, thus allowing a substantial reduction in drift. Figure 5 graphically displays the offset drift performance of the AD540, nulled and unnulled. As can be seen, nulling the device can result in either positive or negative offset drifts given by the slope $\Delta V_{OS}/\Delta T$. The nulled curves represent the maximum changes in drift, indicating performance considerably better than many other IC FET op amps which null V_{OS} by varying the operating currents of the FET's.

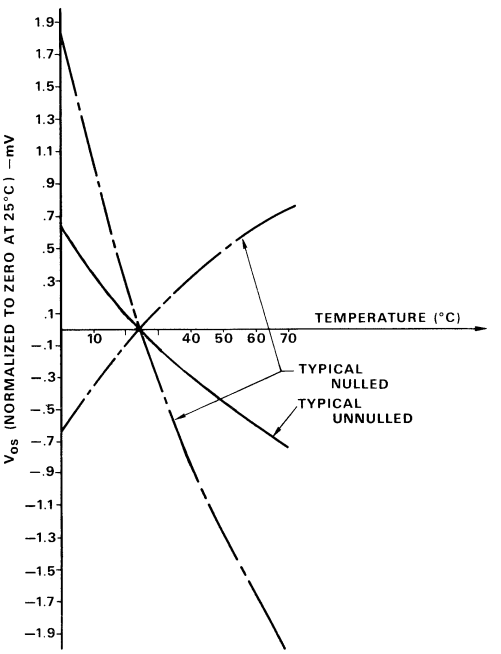


Figure 5. V_{OS} vs. Temperature

NOISE PERFORMANCE. The noise spectral density vs. frequency for the AD540 is given in Figure 6. The curve shows approximately 300nV/$\sqrt{Hz}$ at 10Hz, declining in a 1/f fashion (1/f for power, 1/$\sqrt{f}$ for voltage) to approximately 12nV/$\sqrt{Hz}$ at higher frequencies.

Current noise in the AD540 is approximately 0.001pA/$\sqrt{Hz}$ at low frequencies. Above 300Hz, the current noise generated by the op amp increases at a 3dB/octave rate, determined by $\omega e_n C_{in}$, where e_n = spectral noise density and C_{in} = input capacitance. In most practical applications, the current noise from source or feedback resistors will be larger than the low frequency current noise from the amplifier.

At high frequencies, the total circuit current noise is equal to $\omega e_n C$, where C is the sum of all input and feedback capacitors. In well-shielded circuits, C is usually 10 to 100pF, so that the $\omega e_n C$ can be a significant factor. Thus the user should attempt to minimize C.

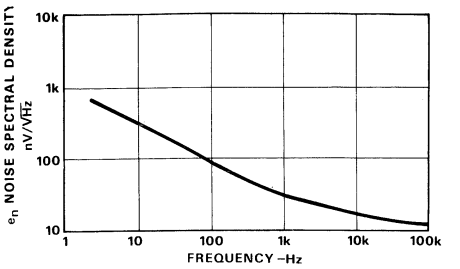


Figure 6. Noise Spectral Density vs. Frequency

DYNAMIC PERFORMANCE. The AD540 is internally compensated to achieve a –3dB bandwidth of 1MHz (see Figure 7). At unity gain the full power bandwidth is 50kHz minimum, and typically 100kHz. Slew rates are 3V/μs minimum and 6V/μs typical (see Figure 8 and Figure 9).

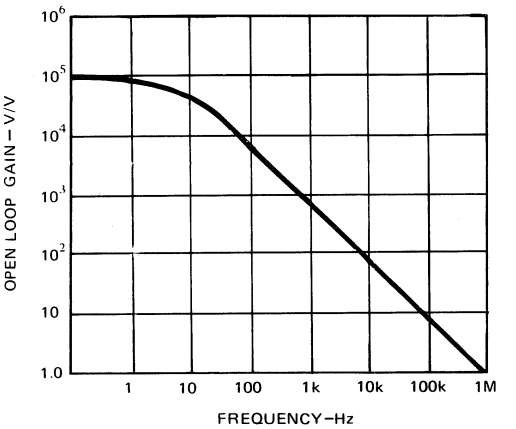


Figure 7. Small Signal Gain vs. Frequency

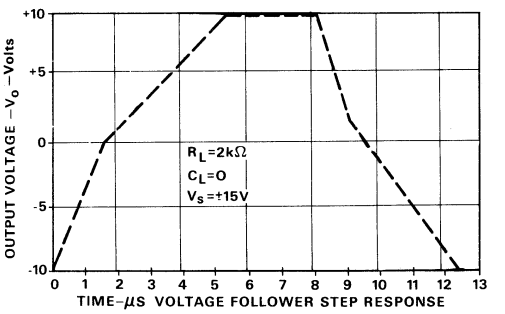


Figure 8. Voltage Follower Step Response

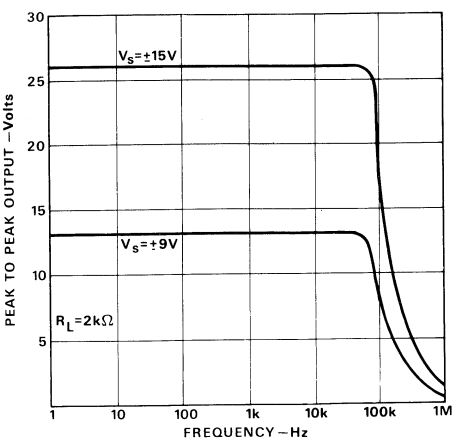


Figure 9. P-P Output vs. Frequency

Lowest Cost High Accuracy IC Op Amps

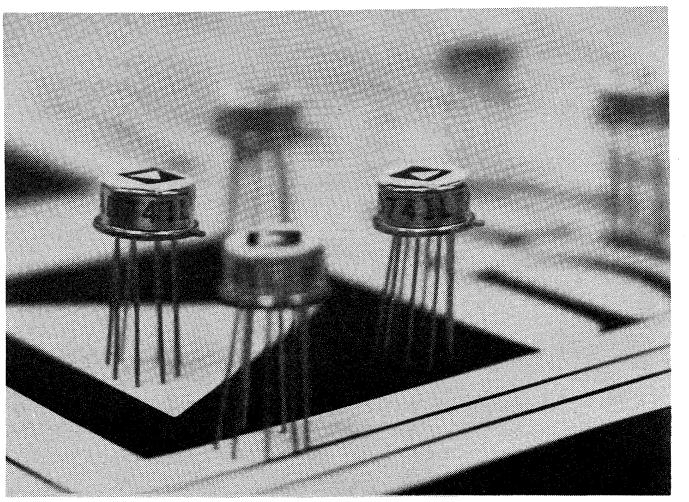
AD741 J,K,L,S

FEATURES

Precision Input Characteristics
- Low V_{OS}: 0.5mV max (L)
- Low V_{OS} Drift: 5μV/°C max (L)
- Low I_b: 50nA max (L)
- Low I_{OS}: 5nA max (L)
- High CMRR: 90dB min (K, L)

High Output Capability
- A_{OL} = 25,000 min, 1kΩ load (J, S)
  T_{min} to T_{max}
- V_O = ±10V min, 1kΩ load (J, S)

Low Cost



GENERAL DESCRIPTION

The Analog Devices AD741J, AD741K, AD741L and AD741S are specially tested and selected versions of the popular AD741 operational amplifier. Improved processing and additional electrical testing guarantee the user precision performance at a very low cost. The AD741J, K and L substantially increase overall accuracy over the standard AD741C by providing maximum limits on offset voltage drift, and significantly reducing the errors due to offset voltage, bias current, offset current, voltage gain, power supply rejection, and common mode rejection (see Error Analysis). For example, the AD741L features maximum offset voltage drift of 5μV/°C, offset voltage of 0.5mV max, offset current of 5nA max, bias current of 50nA max, and a CMRR of 90dB min. The AD741S offers guaranteed performance over the extended temperature range of −55°C to +125°C, with max offset voltage drift of 15μV/°C, max offset voltage of 4mV, max offset current of 25nA, and a minimum CMRR of 80dB.

HIGH OUTPUT CAPABILITY

Both the AD741J and AD741S offer the user the additional advantages of high guaranteed output current and gain at low values of load impedance. The AD741J guarantees a minimum gain of 25,000, swinging ±10V into a 1kΩ load from 0 to +70°C. The AD741S guarantees a minimum gain of 25,000, swinging ±10V into a 1kΩ load from −55°C to +125°C.

All devices feature full short circuit protection, high gain, high common mode range, and internal compensation. The AD741J, K and L are specified for operation from 0 to +70°C, and are available in both the TO-99 and mini-DIP packages. The AD741S is specified for operation from −55°C to +125°C, and is available in the TO-99 package.

GUARANTEED ACCURACY

The vastly improved performance of the AD741J, AD741K, AD741L and AD741S provides the user with an ideal choice when precision is needed and economy is a necessity. An error budget is calculated for all versions of the AD741 (see further); it is obvious that these selected versions offer substantial improvements over the industry-standard AD741C and AD741. A typical circuit configuration (see Figure 1) is assumed, and the various errors are computed using maximum values over the full operating temperature range of the devices. *The results indicate a factor of 8 improvement in accuracy of the AD741L over the AD741C, a factor of 5 improvement using the AD741K, and a factor of 2.5 improvement using the AD741J. The AD741S, similarly, achieves a factor of 3.5 improvement over the standard AD741.* Note that the total error has been determined as a sum of component errors, while in actuality, the total error will be much less. Also, while the circuit used for the error analysis is only one of a multitude of possible applications, it effectively demonstrates the great improvement in overall 741 accuracy achievable at relatively low cost with the AD741J, K, L or S.

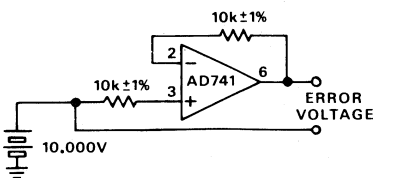


Figure 1. Error Budget Analysis Circuit

SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

MODEL	AD741J	AD741K	AD741L	AD741S
OPEN LOOP GAIN				
R_L = 1kΩ, V_O = ±10V	50,000 min (200,000 typ)			*
R_L = 2kΩ, V_O = ±10V		50,000 min (200,000 typ)	50,000 min (200,000 typ)	
Over Temp Range, T_{min} to T_{max}, same loads as above	25,000 min	*	*	*
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 1kΩ, T_{min} to T_{max}	±10V min (±13V typ)			*
Voltage @ R_L = 2kΩ, T_{min} to T_{max}		±10V min (±13V typ)	±10V min (±13V typ)	
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1MHz	*	*	*
Full Power Response	10kHz	*	*	*
Slew Rate, Unity Gain	0.5V/μs	*	*	*
INPUT OFFSET VOLTAGE				
Initial, $R_S \leq$ 10kΩ (adjustable to zero)	3mV max (1mV typ)	2mV max (0.5mV typ)	0.5mV max (0.2mV typ)	2mV max (1mV typ)
T_{min} to T_{max}	4mV max	3mV max	1mV max	*
Avg vs Temperature (untrimmed)	20μV/°C max	15μV/°C max (6μV/°C typ)	5μV/°C max (2μV/°C typ)	15μV/°C max (6μV/°C typ)
vs Supply, T_{min} to T_{max}	100μV/V max (30μV/V typ)	15μV/V max (5μV/V typ)	15μV/V max (5μV/V typ)	*
INPUT OFFSET CURRENT				
Initial	50nA max (5nA typ)	10nA max (2nA typ)	5nA max (2nA typ)	10nA max (2nA typ)
T_{min} to T_{max}	100nA max	15nA max	10nA max	25nA max
Avg vs Temperature	0.1nA/°C	0.2nA/°C max (0.02nA/°C typ)	0.1nA/°C max (0.02nA/°C typ)	0.25nA/°C max (0.1nA/°C typ)
INPUT BIAS CURRENT				
Initial	200nA max (40nA typ)	75nA max (30nA typ)	50nA max (30nA typ)	75nA max (30nA typ)
T_{min} to T_{max}	400nA max	120nA max	100nA max	250nA max
Avg vs Temperature	0.6nA/°C	1.5nA/°C max (0.6nA/°C typ)	1nA/°C max (0.6nA/°C typ)	2nA/°C max (0.6nA/°C typ)
INPUT IMPEDANCE				
Differential	1MΩ	2MΩ	2MΩ	2MΩ
INPUT VOLTAGE RANGE (Note 1)				
Differential, max safe	±30V	*	*	*
Common Mode, max safe	±15V	*	*	*
Common Mode Rejection, $R_S \leq$ 10kΩ, T_{min} to T_{max}, V_{in} = ±12V	80dB min (90dB typ)	90dB min (100dB typ)	90dB min (100dB typ)	*
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	±(5 to 22)V	±(5 to 22)V	±(5 to 22)V
Current, Quiescent	3.3mA max (2.0mA typ)	2.8mA max (1.7mA typ)	2.8mA max (1.7mA typ)	2.8mA max (2.0mA typ)
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

*Specifications same as AD741J.

Specifications subject to change without notice.

ERROR BUDGET ANALYSIS

PARAMETER	AD741C SPEC (0 to +70°C)	AD741C ERROR	AD741J SPEC (0 to +70°C)	AD741J ERROR	AD741K SPEC (0 to +70°C)	AD741K ERROR	AD741L SPEC (0 to +70°C)	AD741L ERROR	AD741 SPEC (−55°C to +125°C)	AD741 ERROR	AD741S SPEC (−55°C to +125°C)	AD741S ERROR
Gain *(Error = $10V_{in}/G$)*	15,000	660μV	25,000[1]	400μV	25,000	400μV	25,000	400μV	25,000	400μV	25,000[1]	400μV
I_b *(Error = I_b x resistor mismatch)*	800nA	160μV	400nA	80μV	120nA	24μV	100nA	20μV	1500nA	300μV	250nA	50μV
I_{os} *(Error = I_{os} x 10kΩ)*	300nA	3000μV	100nA	1000μV	15nA	150μV	10nA	100μV	500nA	5000μV	25nA	250μV
$\Delta V_{os}/\Delta T$ *(Error = $\Delta V_{os}/\Delta T$ x ΔT)*	25μV/°C[2]	1125μV	20μV/°C	900μV	15μV/°C	675μV	5μV/°C	225μV	25μV/°C[2]	2500μV	15μV/°C	1500μV
CMRR *(Error = 10V/CMRR)*	70dB	3300μV	80dB	1000μV	90dB	330μV	90dB	330μV	70dB	3300μV	80dB	1000μV
PSRR *(assume a ±5% power supply variation)*	150μV/V	450μV	100μV/V	300μV	15μV/V	45μV	15μV/V	45μV	150μV/V	450μV	100μV/V	300μV
TOTAL		8.7mV		3.7mV		1.6mV		1.1mV		12.0mV		3.5mV

[1] AD741J and AD741S...Open Loop Gain is guaranteed with a 1kΩ load.
[2] AD741C and AD741...$\Delta V_{OS}/\Delta_T$ is not guaranteed (for complete specifications, contact the factory for data sheet).

INPUT CHARACTERISTICS

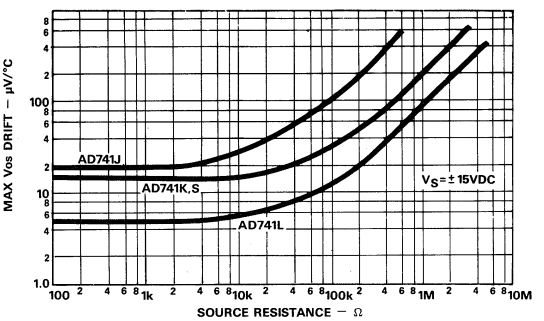


Figure 2. Max Equivalent Input Offset Drift vs. Source Resistance

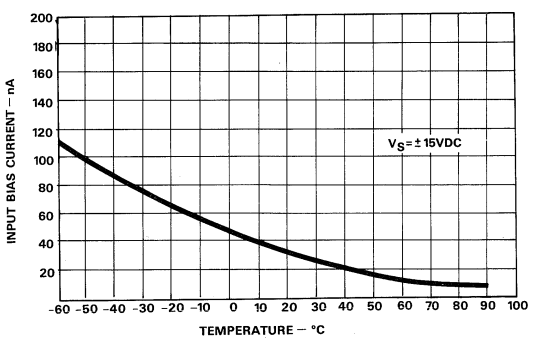


Figure 3. Input Bias Current vs. Temperature

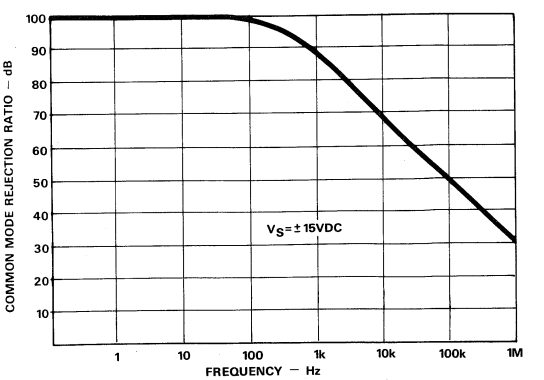


Figure 4. Common Mode Rejection vs. Frequency

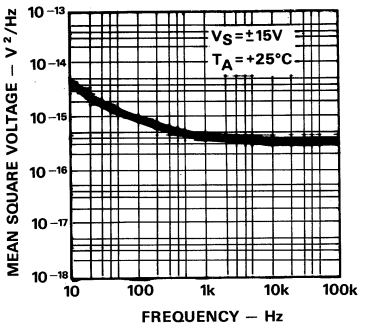


Figure 5. Input Noise Voltage vs. Frequency

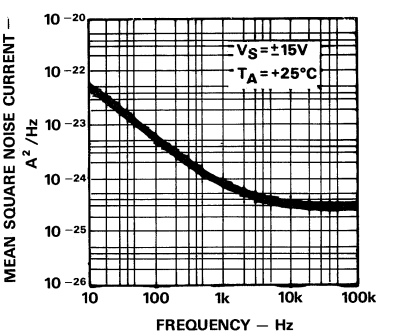


Figure 6. Input Noise Current vs. Frequency

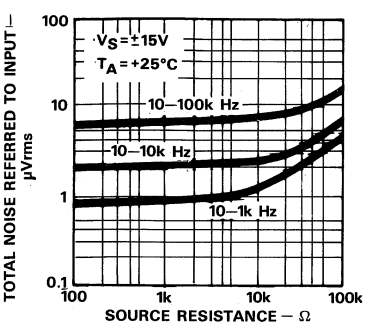


Figure 7. Broadband Noise vs. Source Resistance

OUTPUT CHARACTERISTICS

The AD741J and AD741S are specially selected for high output current capability. High efficiency output transistors, thermally balanced chip design and precise short circuit current control insure against gain degradation at high current levels and temperature extremes. The AD741J guarantees a minimum gain of 25,000, swinging ±10V into a 1kΩ load from 0 to +70°C. The AD741S guarantees minimum gain of 25,000, swinging ±10V into a 1kΩ load from −55°C to +125°C. The AD741K and AD741L are guaranteed with the standard 2kΩ load.

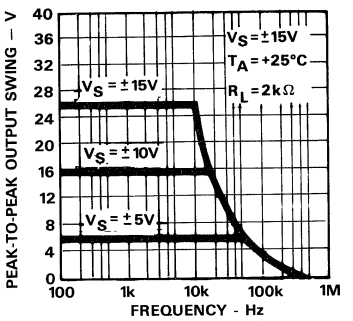


Figure 8. Output Voltage Swing vs. Frequency

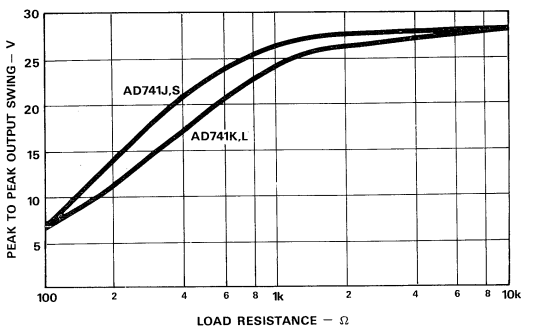


Figure 9. Output Voltage Swing vs. Load Resistance

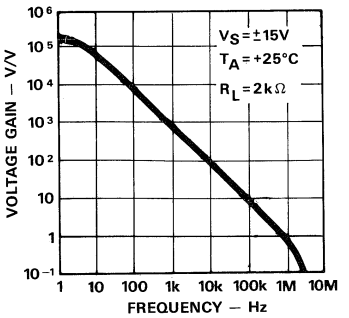
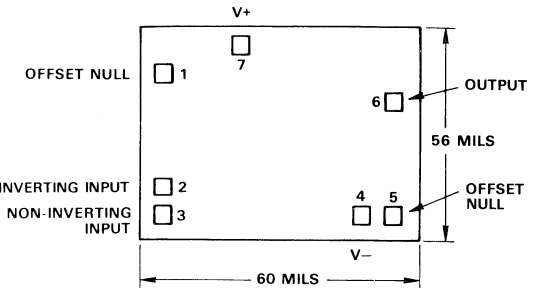


Figure 10. Open Loop Gain vs. Frequency

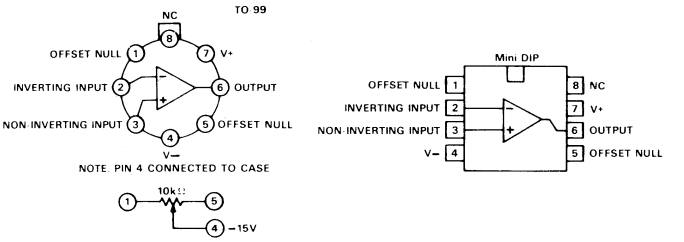
BONDING DIAGRAM

All versions of the AD741 are available in chip or wafer form, fully tested at +25°C. Because of the critical nature of using unpackaged devices, it is suggested that the factory be contacted for specific information regarding price, delivery and testing.



CONNECTION DIAGRAMS

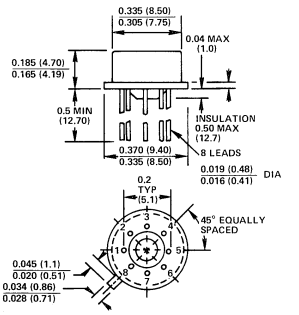
(Top View)



(H package) (N package)

PHYSICAL DIMENSIONS

Dimensions shown in inches and (mm).



MIL-STANDARD-883

The AD741S is available with 100% screening to MIL-STD-883, Method 5004, Class A, B, or C. Consult the factory for pricing and delivery.

ORDERING GUIDE

MODEL	TEMP. RANGE	ORDER NUMBER
AD741J	0°C to +70°C	AD741J*
AD741K	0°C to +70°C	AD741K*
AD741L	0°C to +70°C	AD741L*
AD741S	−55°C to +125°C	AD741SH

*Add Package Type Letter; H = TO-99, N = Mini-DIP.

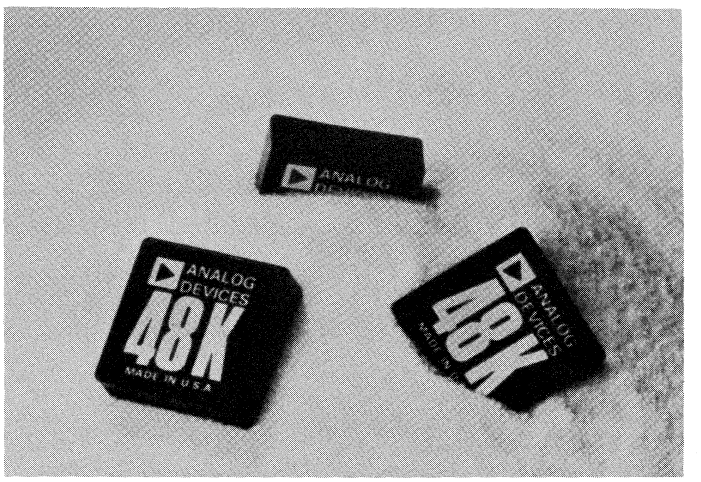
ANALOG DEVICES

Fast Settling Differential FET Op Amp

MODEL 48

FEATURES
- Fast Settling: 500ns max
- Fast Slew Rate: 125V/μs
- Wide Bandwidth: 15MHz
- High Common Mode Rejection: 83dB min
- High Gain: A_0 = 100,000
- Low Drift: 15μV/°C (48K)

APPLICATIONS
- Stable Unity Gain Buffer to 15MHz
- Sample Hold Circuits
- Ultra Fast Current Source
- High Speed Integrator



GENERAL DESCRIPTION

The model 48 is an ultra fast, FET input differential op amp that should be considered where settling time, slew rate, bandwidth and good thermal stability are critical requirements. Characterized by a -6dB/octave rolloff to frequencies exceeding 15MHz, the model 48's dynamic response consists of a guaranteed slew rate of 110V/μs and settles to 0.01% in 500μs, max. For dc performance, the model 48 has open loop gain of 100,000 min, and common mode rejection at a full ±10V of 15,000 min (83dB). Maximum offset drifts of 50μV/°C (48J) and 15μV/°C (48K) complete the performance profile, proving this amplifier to be an excellent choice for both high speed analog and digital applications.

Packaged in a small 1 1/8" x 1 1/8" x 0.4" case, the model 48 requires little space, runs cool (9mA of quiescent current) and is competitively priced at $57 in unit quantities (48J)

FAST SETTLING APPLICATIONS

A/D and D/A converters, multiplexers and other sampling circuits require fast settling output amplifiers. Since system conversion speed is most often dictated by the settling time of the amplifier, model 48, with a guaranteed 500ns settling time to 0.01%, makes it an excellent choice.

D/A CURRENT TO VOLTAGE CONVERTER

Current to voltage converters for D/A applications place severe requirements on the op amp's slew rate, open loop gain and offset drift. Model 48 meets these requirements with smooth settling to 0.01% in 500ns, open loop gain of 100,000 and offset drift of 15μV/°C (48K).

SETTLING TIME VS SIGNAL LEVEL

Shown in Figure 1 is a graph of settling time for various step inputs and the test circuit used to obtain this data. Settling time varies in a nonlinear fashion with input level, error band, and polarity of input step. The worst case settling is that which is specified at ±10V.

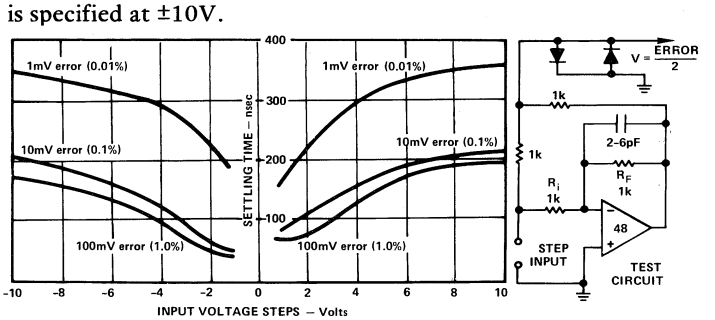


Figure 1. Settling Time for Various Input Steps

SETTLING TIME VS R_F AND C_L

Settling time of an amplifier is also influenced by the value of the gain resistors selected and the amount of capacitive loading. Model 48 is stable even when driving cap loads, C_L, up to 1000pF, but to obtain optimum settling time this value of capacitance should be held as low as possible. The effects of C_L and R_F on settling time are shown in Table 1.

TABLE 1. 0.1% SETTLING TIME VS R_F, C_L

$R_F = R_i$ (Ω)	t_s (ns)	Cap Load (pF)
1k	350	6
10k	420	6
50k	560	6
2k	320	100
2k	420	200
2k	1100	500

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	48J (K)
OPEN LOOP GAIN	
DC Load 500 ohms	100,000 min
RATED OUTPUT[1]	
Voltage, 500 ohm Load	±10V min
Current	±20mA min
Maximum Load Capacitance	1000pF
FREQUENCY RESPONSE	
Unity Gain	15MHz
Full Power	1.5MHz min
Slew Rate, Non-Inverting	90V/μs min
Slew Rate, Inverting	110V/μs min
Overload Recovery	0.5μs
SETTLING TIME, UNITY GAIN, 0.01%	
Non-Inverting	500ns max
Inverting, $R_f = R_i = 2k\Omega$	500ns max
SETTLING TIME, UNITY GAIN, 0.1%	
Inverting, $Z_f = 1k\Omega \| 3.3pF$	300ns max
Inverting, $Z_f = 1k\Omega \| 3.3pF$	250ns
Noninverting, $Z_f = 1k\Omega \| 3.3pF$	250ns
INPUT OFFSET VOLTAGE	
Initial @ +25°C	Adjust to Zero
Trim Potentiometer	1k ohm
With 499 ohm Fixed Trim Resistor	±2mV
vs. Temp (0 to +70°C)	±50μV/°C max (±15μV/°C max)
vs. Time	250μV/month
vs. Supply	±15μV/%
INPUT BIAS CURRENT	
Initial @ +25°C	-50pA max (-25pA max)
At +85°C	2nA (1nA)
INPUT IMPEDANCE	
Differential	$10^{11}\Omega \| 3.5pF$
Common Mode	$10^{11}\Omega \| 3.5pF$
INPUT NOISE	
Voltage, 0.01 to 1Hz	2μV p-p
5Hz to 50kHz	3μV rms
Current, 0.01 to 1Hz	0.1pA p-p
INPUT VOLTAGE RANGE	
Differential	±15V
Common Mode, 1% Error	±11V
COMMON MODE REJECTION	
±10V dc	15,000 min
±10V dc	30,000
POWER SUPPLY[2]	
Voltage, Rated Specifications	±15V
Operating	±(12 to 18)V
Current, Quiescent	9mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C
MECHANICAL	
Weight	15 grams
Trimpot	1kΩ, ADI #79PR1k
Mating Socket	AC1010

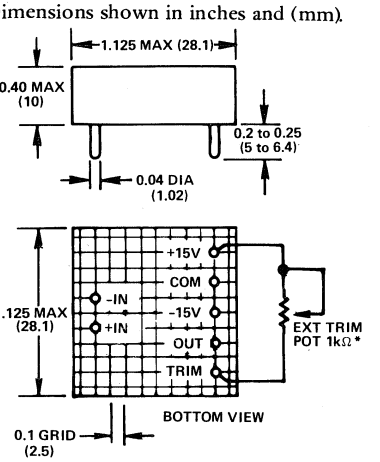
[1] Short circuit protected to ground.

[2] Recommend ADI model 904, ±15V @ 50mA.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

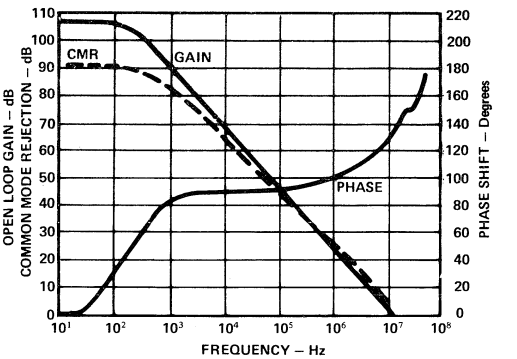
Dimensions shown in inches and (mm).



Mating Socket AC1010

*Analog Devices Model 79PR1k

OPEN LOOP GAIN, PHASE & CMRR VS FREQUENCY



KEY SPECS FOR ADI FAST SETTLING FET OP AMPS

Model	48J	46J	44J	45J	
Settling to 0.01% (max)	500	300	1000	1000	ns
Slew Rate	125	1000	75	75	V/μs
Bandwidth	15	40	10	10	MHz
Output @ 10V	20	100	20	20	mA
Drift	50	75	50	50	μV°C
CMR min @ 10V	83	72	80	74	dB
Gain (min)	100k	25k	100k	50k	

CONSIDERATIONS FOR HIGH SPEED APPLICATIONS

Components: Use gain resistors of 2kΩ or less to reduce effects of stray capacitance. Use metal film resistors for low capacitance and inductance.

Wiring: Run separate signal and power grounds terminating at a common point at the power supply common (preferably). Keep all leads as short as possible to reduce noise pickup and inductive effects.

Fast Settling, Wideband, 100mA Output, FET Amplifiers

MODELS 50 & 51

FEATURES
Fast Settling: 200ns max, 0.05% (50J/K)
100ns max, 0.1% (50J/K)
100mA Output: dc to 8MHz (50J/K)
dc to 6MHz (51A/B)
All Hermetically Sealed Semiconductors (51A/B)
-55°C to +125°C Temperature Range (51A/B)
100MHz Gain Bandwidth (50J/K)

APPLICATIONS
A to D Input Amplifier
D to A Current Converter
Video Pulse Amplifier
CRT Deflection Amplifier
Wideband Current Booster

GENERAL DESCRIPTION

Models 50 and 51 are ultra fast, wideband differential FET amplifiers, designed for applications requiring fast settling time with high output current in closed loop gain configurations of 2 or greater. Model 50 offers guaranteed settling time of 100ns maximum to ±0.1% accuracy and 200ns maximum to ±0.05% accuracy. Model 51 features all hermetically sealed semiconductors for greater reliability and wide operating temperature range (-55°C to +125°C) with guaranteed settling times of 140ns maximum to ±0.1% and 250ns maximum to ±0.05%.

Model 50 is available in two input voltage drift selections, model 50J is ±50μV/°C max, model 50K is ±15μV/°C max. Other outstanding features of models 50J/K are 100MHz gain bandwidth product, slew rate of 500V/μs and output current of ±100mA from dc to 8MHz.

Model 51 is also available in two input voltage drift selections; model 51A is ±50μV/°C max, model 51B is ±20μV/°C max. Models 51A/B offer 80MHz gain bandwidth product, slew rate of 400V/μs and ±100mA output current from dc to 6MHz. Both models 50 and 51 offer significant improvement over previous designs with lower input voltage noise (6μV rms, 5Hz to 2MHz bandwidth), particularly important in display system D/A converter applications.

FAST SETTLING APPLICATIONS

D/A converters require fast settling output amplifiers since conversion speed is often dictated by the settling time of the amplifier. Models 50 and 51 offer fast settling time performance at closed loop gains from 2 to 6. This characteristic is extremely important for D/A applications requiring fast current to voltage conversion from less than ideal current sources.

The circuit shown in Figure 1 is that of a typical current to voltage converter. The output of the D/A converter is often considered an ideal current source ($R_{out} = \infty$) which is converted to a voltage by the amplifiers' feedback resistor. Although it may appear that in this application the amplifier is being operated in a closed loop gain of 1, a closer look at the D/A's specifications may show an output impedance of 800 to 2500 ohms. For this condition, the amplifier is operated in a closed loop gain of 2 to 6. This is then the range of gains over which settling time is important.

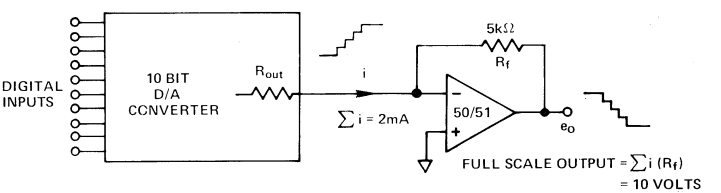


Figure 1. High Speed Current to Voltage Buffer

High speed amplifiers typically suffer significant degradation in settling time when operated in closed loop gains greater than unity. Model 50, with 100MHz gain bandwidth and model 51 with 80MHz gain bandwidth achieve fast settling time since they are far from the point of bandwidth limitations. For example, at a gain of 4, model 50 has a bandwidth of 20MHz, which represents a time constant of 8ns. For 0.1% settling, the bandwidth limitation is 6.9 time constants or approximately 55ns.

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	50J	50K	51A	51B
OPEN LOOP GAIN				
DC, Load = 100 ohm	88dB min	*	94dB min	**
DC, Load = 2k ohm	94dB min	*	97dB min	**
RATED OUTPUT[1]				
Voltage, $R_L \geq 100\Omega$	±10V min	*	*	*
Current	±100mA min	*	*	*
Impedance, Open Loop dc	200Ω	*	*	*
Load Capacitance,				
Inverting	100pF max	*	*	*
Noninverting	50pF max	*	*	*
FREQUENCY RESPONSE				
Small Signal, Unity Gain	70MHz	*	56MHz	**
Small Signal, -3dB, Unity Gain	100 MHz	*	80MHz	**
Full Power	8MHz min	*	6MHz min	**
Slew Rate, Noninverting	400V/μs, min	*	300V/μs, min	**
Slew Rate, Inverting	500V/μs, min	*	400V/μs, min	**
Overload Recovery	200ns	*	*	*
SETTLING TIME				
Inverting, Gain = 2				
±0.1%, ±10 Volt Step	100ns max	*	140ns max	**
±0.05%, ±10 Volt Step	200ns max	*	250ns max	**
Noninverting, Gain = 2				
±0.1%, ±10 Volt Step	150ns max	*	200ns max	**
±0.05%, ±10 Volt Step	300ns max	*	400ns max	**
INPUT OFFSET VOLTAGE				
Initial, @ +25°C	Adjust to Zero	*	*	*
Trim Potentiometer[2]	1kΩ	*	*	*
With 499Ω Fixed Resistor	±3mV	*	*	*
vs. Temperature	±50μV/°C max	±15μV/°C max	±50μV/°C max	±20μV/°C max
vs. Supply Voltage	±15μV/%	*	*	*
vs. Time	±500μV/month	*	*	*
Warm up Drift, 20 Minutes	±2mV	*	*	*
INPUT BIAS CURRENT				
Initial, @ +25°C	(0, -) 2nA max	*	*	*
vs. Temperature	Double/+10°C	*	*	*
vs. Supply Voltage	10pA/%	*	*	*
INPUT DIFFERENCE CURRENT				
Initial, @ +25°C	±100pA	*	*	*
vs. Temperature	Double/+10°C	*	*	*
INPUT IMPEDANCE				
Differential	$10^{10}\Omega \| 3.5$pF	*	*	*
Common Mode	$10^{10}\Omega \| 3.5$pF	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	5μV, p-p	*	*	*
5Hz to 2MHz	6μV, rms	*	*	*
Current, 0.1Hz to 10Hz	1pA, p-p	*	*	*
INPUT VOLTAGE RANGE				
Common Mode Voltage	±10V min	*	*	*
Max Safe Differential Voltage	$\pm V_S$	*	*	*
Common Mode Rejection, CMV = ±10V	60dB, min	*	*	*
Common Mode Rejection, CMV = ±5V	70dB, min	*	*	*
POWER SUPPLY				
Voltage, Rated Performance[3]	±15V dc	*	*	*
Voltage, Operating	±(12 to 18)V dc	*	*	*
Current, Quiescent	±40mA	*	*	*
TEMPERATURE RANGE				
Rated Specifications	0 to +70°C	*	-25°C to +85°C	**
Operating[4]	-25°C to +85°C	*	-55°C to +125°C	**
Storage	-55°C to +125°C	*	*	*
MECHANICAL				
Case Size	1.8" x 1.2" x 0.6"	*	*	*
Weight, grams	31	*	*	*
Mating Socket	AC1034	*	*	*

982 407

*Specifications same as Model 50J.

**Specifications same as Model 51A.

[1] Short circuit protected to ground.

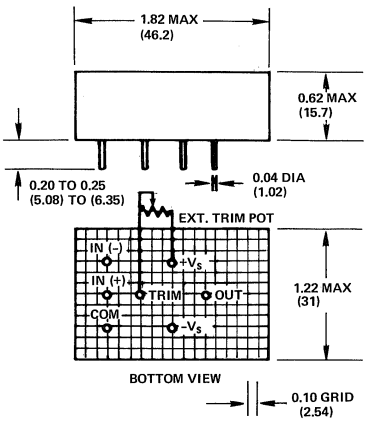
[2] Analog Devices' part number 79PR1K

[3] Recommended ADI Model 920, ±15V @ 200mA

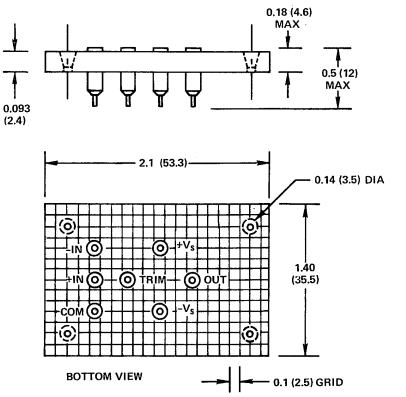
[4] Models 51A and 51B have an operating temperature range of -55°C to +100°C when operating in the differential mode.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET AC1034



OTHER FAST AMPLIFIERS AVAILABLE

Models 44, 45 and 48, each available with two drift selections (J, K), offer fast settling of 1μs max (0.5μs, 48) to 0.01%. They provide ±10 volts output at 20mA with input drifts of 50μV/°C (J) and 15μV/°C (K) max. Unity gain response is 10MHz (15MHz, 48) with 1MHz (1.5MHz, 48) full power output.

ECONOMY – Select models 45J/K. Good performance for inverting or noninverting (±5V CMV) designs.

FOLLOWER – Select models 44J/K for guaranteed 80dB CMR (CMV ±10V). Excellent as buffer for A to D's, sample-hold multiplexer.

FAST SETTLING – Select models 48J & K for settling to 0.01% in 500ns - small package – 1" x 1".

Figure 2 illustrates 0.1% and 0.05% settling time performance achievable from models 50 and 51 over closed loop gains from 1 to 10. Both models offer dramatic improvement over previous designs.

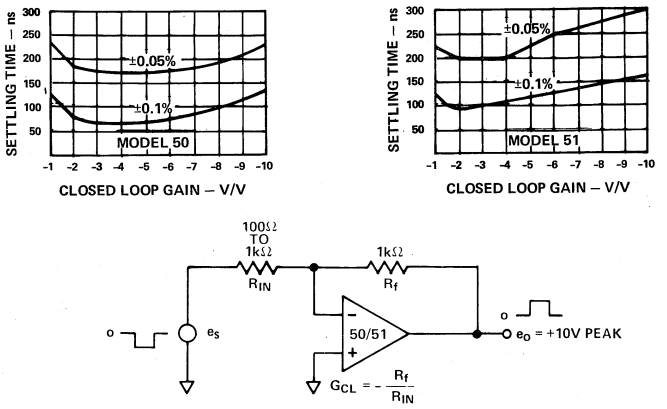


Figure 2. Settling Time versus Closed Loop Gain

SLEW RATE VS. CLOSED LOOP GAIN

Unlike most high speed amplifiers, models 50 and 51 do not require high input drive voltage to achieve fast slew rate and rise time. For small signals and closed loop gains of 2 or greater, models 50 and 51 can slew faster than amplifiers having slew rate specifications of 1000V/μs and greater. This is a consequence of the method used throughout industry to specify slew rate and the fact that slew rate is determined by the initial error signal at the summing junction and the transconductance of the amplifier. If either of these two factors is reduced, slew rate is reduced.

Figure 3 illustrates the higher slew rate sensitivity of mdels 50 and 51 by plotting slew rate versus initial error signal along with model 46, a popular 1000V/μs industry standard. These curves illustrate that for error signals of less than 2.5V, model 50 has a higher slew rate than model 46; for error signals less than 2V, model 51 has a higher slew rate compared to model 46.

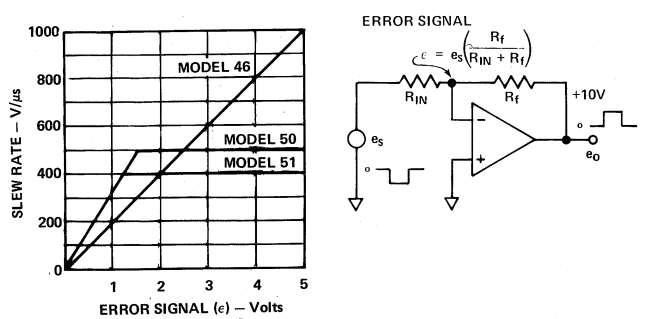


Figure 3. Slew Rate vs. Error Signal

As an example of the faster performance available from models 50/51, Figure 4 compares the response of model 50 and 46 to a 100ns pulse in an inverting, gain of 4 circuit. Model 50 is twice as fast as model 46 with a risetime (10%–90%) of 18ns compared to model 46's risetime of 38ns. Models 50 and 51 therefore, can be faster in many applications than model 46 and other fast amplifiers in the 1000V/μs category.

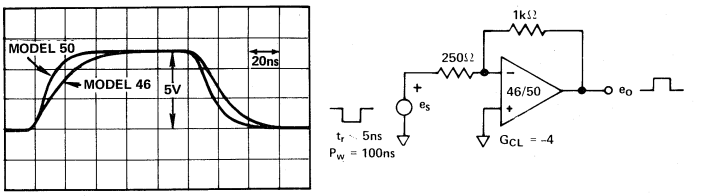


Figure 4. Pulse Response, Model 46/Model 50

SETTLING TIME VS. SIGNAL SWING

The curves in Figure 5 illustrate models 50/51 settling time error versus input signal level. These curves are useful as a design aid for bracketing settling time versus step input level. Settling time is defined as that time required for the output signal to settle within a specified error band about its final value in response to a perfect input step. During the settling time cycle, the output signal initially displays a propagation delay, a rise time, and a time period to settle into the specified error band.

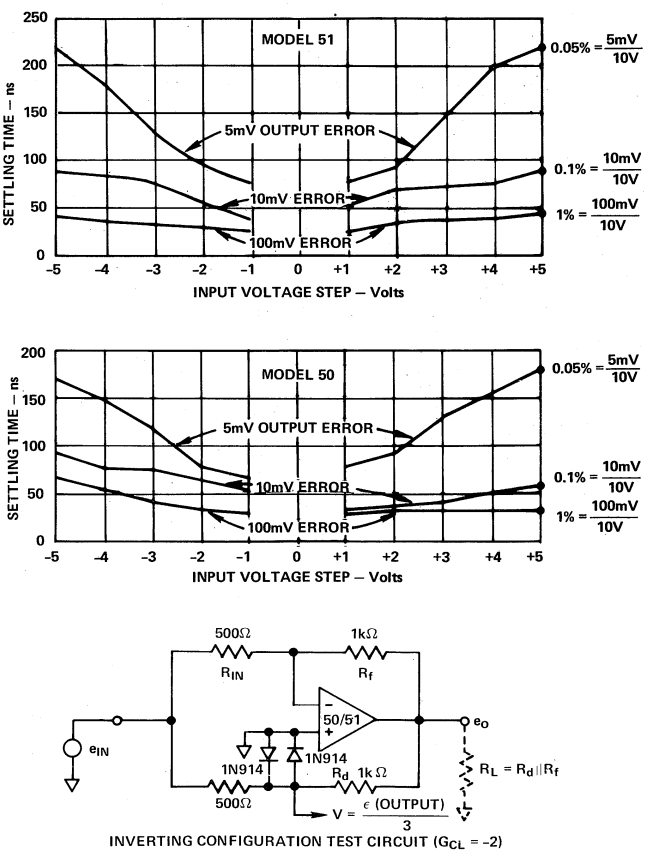


Figure 5. Settling Time Error vs. Input Level

Percentage settling time error is calculated by forming the ratio of output error to output voltage step. Shown in Figure 5 are 1%, 0.1% and 0.05% error points for a ±10V output step. The settling times for these errors are read off the vertical axis.

Because of nonlinear factors, extrapolation of settling times from one set of conditions to another becomes very difficult, if not impossible. This point becomes very apparent, in Figure 5, when reviewing settling time as a function of input signal swing.

FREQUENCY RESPONSE

The frequency performance of model 50, shown in Figure 6, is characterized by a useful small signal bandwidth of up to 80MHz and a common mode rejection of 70dB rolling off at 10kHz. The frequency performance of model 51, shown in Figure 7 is characterized by a useful small signal bandwidth of up to 60MHz and a common mode rejection of 70dB rolling off at 10kHz. Although the gain roll-off for both models 50 and 51 is running at -6dB per octave, implying a single pole response, the phase angle above 10MHz reveals the presence of higher order poles just beyond unity gain cross-over.

Whereas the design is developed to stagger these breaks for greater phase margin, it is not uncommon to encounter parasitic effects arising from stray capacitance and tight loop gain when designing in the amplifier. It is essential, therefore, to take certain precautions in selecting the value of gain resistors, load terminations and wiring techniques when applying wideband amplifiers.

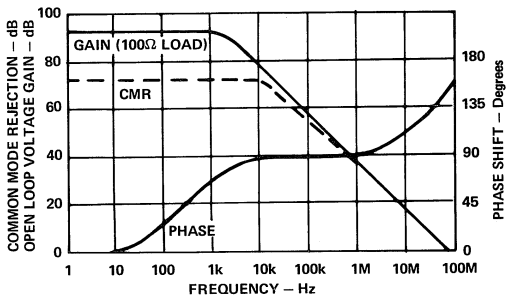


Figure 6. Model 50 Frequency Response

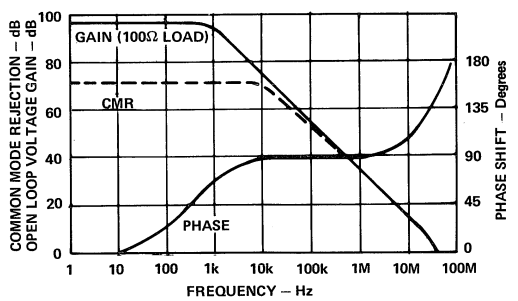


Figure 7. Model 51 Frequency Response

UNITY GAIN APPLICATIONS

Models 50 and 51 have been optimized for fast settling inverting applications, such as current to voltage conversion at the output of D/A converters. In these configurations the high speed amplifier is usually operating in a noise gain of about 5. (Noise Gain = 1 + R_f/R_{out} of D/A). They have also been designed as fast noninverting amplifiers and offer excellent performance at noise gains of 2 or higher. For unity gain applications the circuits shown in Figure 8 and Figure 9 are recommended.

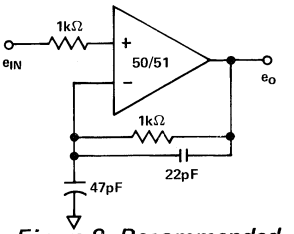


Figure 8. Recommended Circuit for Unity Gain Noninverting Buffer

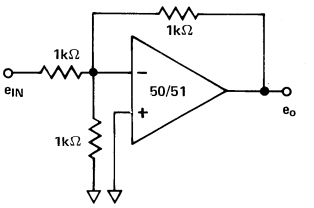


Figure 9. Recommended Circuit for Unity Gain Inverter

ADDITIONAL LOAD CAPACITANCE

If circuit applications require that load capacitances greater than 100pF be driven, then stability may be assured by using the load isolation circuit of Figure 10. The available output swing will be reduced by the drop across the 10Ω resistor. A 4.7pF feedback capacitor should suffice to insure stability for 1000 to 1500pF loads. Larger values of load capacitance will require increasing either the feedback capacitor or the 10Ω resistor.

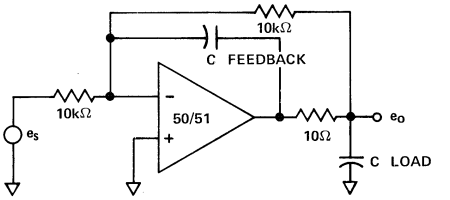


Figure 10. Isolation of Load Capacitance

COMPONENT SELECTION AND WIRING

As with all fast op amp designs, great care must be taken in designing and packaging these circuits to realize their ultimate capability. Unfortunately, what has been painstakingly gained in design can often be lost through misapplication. To assist the user, several elements of good design are presented for his consideration when applying these amplifiers.

CIRCUIT WIRING

It is of utmost importance that care be taken in laying out signal and power ground circuits to avoid extraneous voltage pick-up in the ground signal paths. Keep all leads short to minimize stray inductance and capacitance at the input terminals.

Stray effects at the input tend to cause excessive ringing while output strays destabilize the amplifier roll-off resulting in possible oscillations. Be sure to resistively decouple monitoring instruments such as oscilloscopes since their input capacitance can affect measurements also.

Power supply lead length is not as critical since models 50 and 51 use 1μF bypass supply capacitors internally. When mounting on a pc card, the designer should consider using a ground plane about the input and feedback terminals for line driving applications. Where the source or load signals are remote to the amplifier, consider using properly terminated coax cable. Don't overlook sockets or printed circuit mounting boards as possible sources of dielectric absorption. Avoid pole-zero mismatches in any feedback networks used with the amplifier.

COMPONENTS

Metal film resistors are preferred over wire-wounds because of their lower capacitance and inductance. Good selections are now available with excellent accuracies and temperature coefficients. Diodes are preferably hot carrier types for the fastest-settling applications. 1N914 types are suitable for more routine uses. Capacitors in critical locations should be polystyrene, teflon, or polycarbonate, to minimize dielectric absorption.

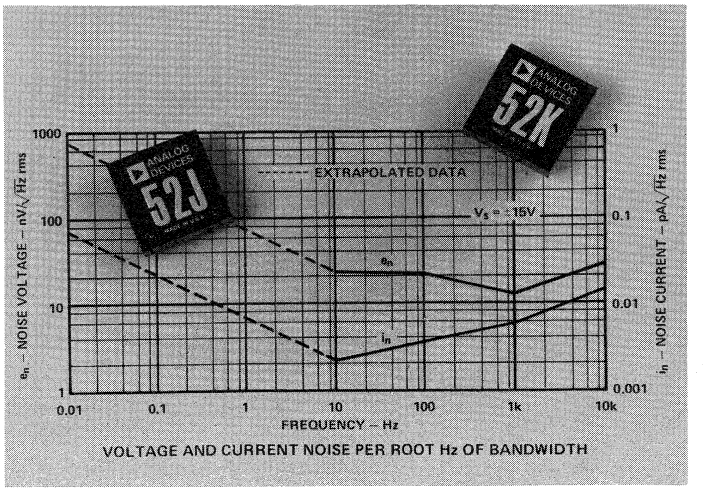
ANALOG DEVICES

Low Noise, Low Drift Precision FET Amplifier

MODEL 52

FEATURES
Guaranteed Low Noise 1.5μV p-p max (0.01 to 1Hz)
Low Voltage Drift: 1μV/°C max (52K)
Low Bias Current: 3pA, max
High CMR: 100dB, min
High Voltage Gain: 120dB, min
Wide Power Supply Range: ±9V to ±18V
Excellent Long Term Stability: 5μV/month
Fast Thermal Response

APPLICATIONS
Low Level Instrumentation Preamp
High Impedance Precision Buffer
Long Term Integrator
Current to Voltage Converter
Precision Voltage Regulator
Preamp for 16 Bit Resolution V/F Converters



VOLTAGE AND CURRENT NOISE PER ROOT Hz OF BANDWIDTH

GENERAL DESCRIPTION
Model 52, a low noise, high accuracy FET input operational amplifier was designed for handling microvolt signals from high impedance (>100kΩ) sources. It features guaranteed low voltage noise (1.5μV p-p max, 0.01 to 1Hz bandwidth) with low input offset voltage drift (3μV/°C max, 52J; 1μV/°C max 52K). Unlike most available low drift amplifiers, model 52 voltage drift is unaffected by trimming the initial offset voltage (0.5mV max). The low input bias current (3pA max) is held constant over the entire ±10V common mode voltage range. High voltage gain (120dB, min) and high CMR (100dB, min) complete the performance profile. Model 52 is an excellent choice for high accuracy, high resolution linear signal processing applications.

By incorporating a new low noise N-channel monolithic FET input stage, thermal stability, voltage noise and differential signal performance are improved to a level previously obtainable only in the best bipolar amplifier designs. Model 52 is an excellent choice to replace chopper stabilized amplifiers where significant sources of error are introduced from zero beating, "chopper spikes" and ground loop currents.

The guaranteed accuracy performance of model 52 suggests critical applications such as low noise, low drift "front-end" preamplifiers for A to D converters and DVM's. For high impedance buffering applications, model 52 offers low input bias current, high linear common mode rejection, complete protection from input transients (offset voltage and bias current will not degrade due to reverse breakdown) and freedom from latch up when the common mode voltage range is exceeded. Model 52 is supplied in a reliable, compact epoxy module package. Output is protected from shorts to ground and/or supply voltage and is capable of driving up to 0.01μF load capacitance.

IMPROVED OFFSET VOLTAGE STABILITY
Model 52 has been designed for the lowest possible input voltage drift over the 0 to +70°C temperature range. In most operational amplifier designs, trimming is accomplished by unbalancing the current in the input stage. This trimming technique introduces an additional 2 to 12μV/°C for each millivolt of E_{OS} that is nulled. To provide performance consistent with low offset voltage drift, model 52 incorporates a three-point trim (see connection diagram) whereby a compensating voltage is introduced without unbalancing the input stage currents. By virtue of this trim scheme, there is no degradation in T.C. when E_{OS} is nulled and the specified performance is achieved.

IMPROVED NOISE PERFORMANCE
Input noise limits signal resolution in low level signal processing applications. The FET input stage of model 52 reduces noise current significantly from that of bipolar amplifiers, permitting high source impedance applications. Model 52 also offers voltage noise levels appreciably below that of other FET amplifiers. To illustrate the excellent low noise performance of model 52, Figure 1 shows typical input voltage noise in a 0.01 to 1Hz bandwidth. Noise is typically less than 1μV p-p and is free of noise spikes.

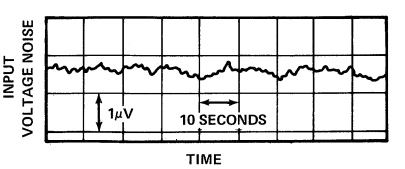


Figure 1. Voltage Noise 0.01 to 1Hz Bandwidth

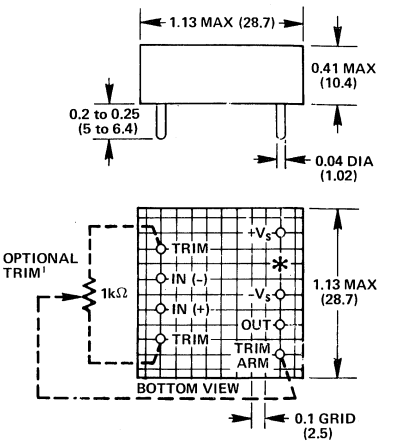
SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	52J	52K
OPEN LOOP GAIN		
DC 2kΩ Load	120dB Min (130dB Typ)	*
RATED OUTPUT[1]		
Voltage, 2kΩ Load	±10V min	*
Current	±5mA min	*
Maximum Load Capacitance	0.01μF	*
Impedance, Open Loop	75Ω	*
FREQUENCY RESPONSE		
Unity Gain, Small Signal	500kHz	*
Full Power	4kHz min	*
Slew Rate	0.25V/μs min	*
Overload Recovery	130μs	*
Settling Time, ±0.1%, ±10V Step	100μs	*
Settling Time, ±0.01%, ±10V Step	150μs	*
INPUT OFFSET VOLTAGE		
Initial[2], @ +25°C	±500μV max	*
With External Trim Potentiometer	Adjustable to Zero	*
vs. Temperature (0 to +70°C)	±3μV/°C max	±1μV/°C max
vs. Supply Voltage	±2μV/%	*
vs. Time	±5μV/Month	*
Warm-Up Drift, 5 Minutes	±5μV	*
INPUT BIAS CURRENT		
Initial, @ +25°C	-3pA max (-1pA typ)	*
vs. Temperature (0 to +70°C)	x2/+10°C	*
vs. Supply Voltage	±0.01pA/%	*
INPUT DIFFERENCE CURRENT		
Initial, @ +25°C	±1pA	*
vs. Temperature (0 to +70°C)	x2/+10°C	*
INPUT IMPEDANCE		
Differential	$10^{12}\Omega \| 3.5pF$	*
Common Mode	$10^{12}\Omega \| 3.5pF$	*
INPUT NOISE		
Voltage, 0.01Hz to 1Hz	1.5μV p-p max (1μV p-p typ)	*
10Hz to 10kHz	3μV rms max (2μV rms typ)	*
f = 1Hz	$70nV/\sqrt{Hz}$ rms	*
f = 10Hz	$25nV/\sqrt{Hz}$ rms	*
f = 100Hz	$20nV/\sqrt{Hz}$ rms	*
f = 1kHz	$13nV/\sqrt{Hz}$ rms	*
Current, 0.01Hz to 1Hz	0.1pA p-p	*
f = 1Hz	$7fA/\sqrt{Hz}$ rms	*
f = 10Hz	$2.5fA/\sqrt{Hz}$ rms	*
f = 100Hz	$3.5fA/\sqrt{Hz}$ rms	*
f = 1kHz	$6fA/\sqrt{Hz}$ rms	*
INPUT VOLTAGE RANGE		
Common Mode Voltage	±10V min	*
Common Mode Rejection, CMV = ±10V	100dB min (106dB typ)	*
Max Safe Differential Voltage	$\pm V_S$	*
POWER SUPPLY		
Voltage, Rated Performance	±15V	*
Voltage, Operating	±(9 to 18)V	*
Current, Quiescent	±5mA	*
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Case Size	1.12" x 1.12" x 0.4"	*
Weight	16g	*
Mating Socket	AC1008	*

*Specifications same as model 52J.
[1] Protected for short circuit to ground.
[2] With no external trim potentiometer connected.
[3] Recommended power supply, ADI model 904, ±15V @ 50mA output
Specifications subject to change without notice.

OUTLINE DIMENSIONS

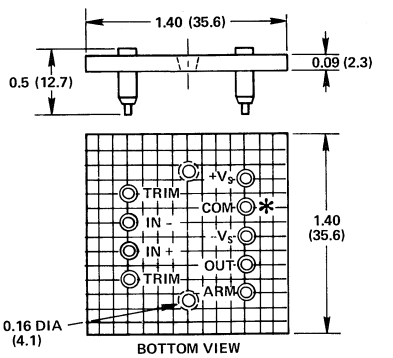
Dimensions shown in inches and (mm).



[1] Optional 1kΩ external trim pot, Analog Devices Model 79PR1K. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim pins left open, input offset voltage will be ±0.5mV, maximum.

*Common Supply connection not required.

MATING SOCKET AC1008



*No connection required on Model 52.

FREQUENCY RESPONSE

From the plot of Open Loop Voltage Gain and Phase Shift (see Figure 2) versus Frequency, it can be seen that model 52 is stable for all closed loop gains. Even at the crossover frequency of 500kHz, model 52 has a phase margin of 75°.

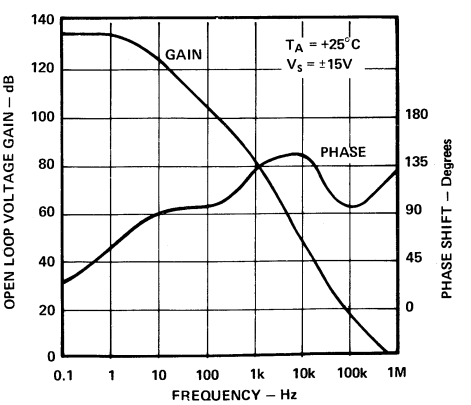


Figure 2. Open Loop Frequency Response

ANALOG DEVICES

High Voltage Differential FET Amplifier

MODEL 171

FEATURES
- High Output Voltage: ±140V
- High CMR: 100dB min
- Operates With a Wide Range of Power Supplies
- High CMV: $\pm(|V_S| - 10V)$

APPLICATIONS
- High Voltage Compliance Current Source
- High Voltage Follower With Gain
- High Voltage Integrator
- Diff. Amp for High CMV Bridge Applications
- Reference Power Supply

GENERAL DESCRIPTION

Model 171 is a high performance FET input op amp designed for operation over a wide range of supply voltages. This module features an output range of ±15V to ±140V at 10mA, a minimum CMRR of 100dB and a high common mode voltage rating of $\pm(V_S - 10V)$ min. DC offset is less than ±1mV, and maximum drift of either ±50 or ±15μV/°C is available in the J or K versions. Bias current is less than 50pA (171J) or 20pA (171K), doubling per +10°C increase of temperature. The model 171 also features small signal bandwidth of 3MHz for unity gain, full-power bandwidth of 15kHz, and slew rate of 10V/μs. These operating characteristics make model 171 an excellent choice for high voltage buffer applications, followers with gain, off-ground signal measurements and reference power supplies.

Excellent power supply rejection of 7μV/V enables model 171 to be powered by inexpensive, low regulation supplies, without sacrificing any of the 171's inherent high performance. The supplies also need not be symmetrical. Any combination of power supply voltages between the limits of 15 to +300V for the positive side and 15 to -300V for negative side is acceptable provided the total voltage across the amplifier is within the range of 30 to 300V.

Model 171's output is completely short circuit protected by the use of a current limit scheme. This type of protection provides a short circuit output that is only slightly greater than the rated output current for normal operation. With this design the module and external circuitry are protected, internal heat dissipation and the associated high temperature rise are limited, and added reliability is built in.

POWER SUPPLY VOLTAGES

Model 171 offers the flexibility of operating with an extensive range and combination of power supply voltages. Figure 1 shows a chart of permissible combinations of supply voltages for the 171. The model 171 maintains its normal operating characteristics when using asymmetrical power supply configurations.

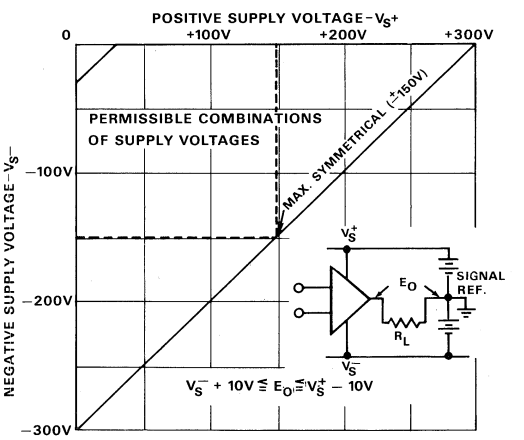


Figure 1. Power Supply Voltage Combinations

SPECIFICATIONS (typical @ +25°C and ±125V unless otherwise noted)

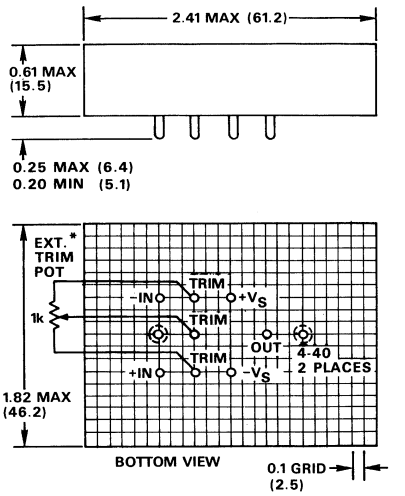
MODEL	171J	171K
OPEN LOOP GAIN	10^6 min	*
RATED OUTPUT		
Voltage	$\pm(\|V_S\|-10V)$ min	*
Current	±10mA min	*
Maximum Load Capacitance	1000pF	*
FREQUENCY RESPONSE		
Unity Gain, Small Signal	3MHz	*
Slewing Rate	10V/μs min	*
Full Power	15kHz min	*
Settling Time to ±0.1%, ±10V Step	25μs	*
Overload Recovery	5μs	*
INPUT OFFSET VOLTAGE		
Initial Offset, +25°C[1]	±1mV	*
Avg. vs. Temp (0 to +70°C)	±50μV/°C max	±15μV/°C max
vs. Supply Voltage	±7μV/V	*
vs. Time	±250μV/mo	*
INPUT BIAS CURRENT		
Initial Bias, +25°C	-50pA max	-20pA max
vs. Temp (0 to +70°C)	x 2/10°C	*
Difference Current	±10pA	±5pA
INPUT IMPEDANCE		
Differential	$10^{11}\Omega\|\|3.5$pF	*
Common Mode	$10^{11}\Omega\|\|3.5$pF	*
INPUT NOISE		
Voltage, 0.01 to 1.0Hz	4μV p-p	*
10Hz to 10kHz	2.5μV rms	*
5Hz to 50kHz	6μV rms	*
INPUT VOLTAGE RANGE		
Common Mode Voltage	$\pm(\|V_S\|-10V)$ min	*
Common Mode Rejection	100dB min	*
Common Mode Rejection	114dB	*
Max Safe Differential Voltage	$\pm V_S$	*
POWER SUPPLY		
Voltage, Rated Specification	±25 to ±150V dc	*
Voltage, Operating	±15 to ±150V dc	*
Current, Quiescent	±6mA	*
TEMPERATURE RANGE		
Rated Specification	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-40°C to +100°C	*
MECHANICAL		
Case Size	2.41" x 1.82" x 0.61"	*
Weight	80g	*
Mating Socket	AC1037	*

*Specifications same as 171J

[1] No external trim connection required.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



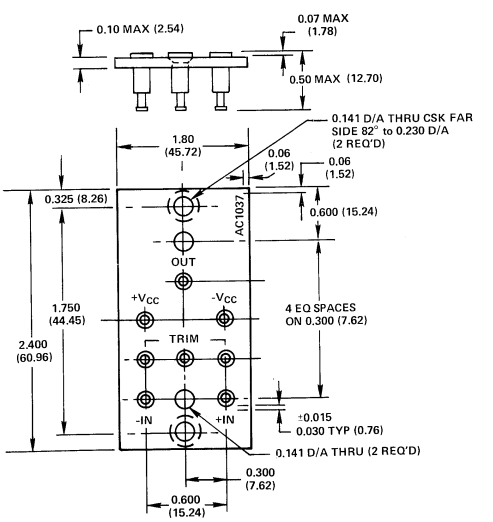
NOTES:

1. Pins: 0.040 $^{+0.002}_{-0.000}$ dia., spherical radius on ends, half-hard brass: gold plated.
2. Markings next to pins and grid are for reference only and do not appear on unit.

*Available from Analog Devices – #79PR1K

MATING SOCKET

Dimensions shown in inches and (mm).



MATING SOCKET AC1037

As shown in Figure 1, the model 171 requires at least ±15 volts applied across it in order to operate properly. The 171 may be operated from a single floating supply voltage by using the power supply offsetting scheme shown in Figure 2. When this configuration is used, the 171 is capable of operating over its specified input and output voltage range.

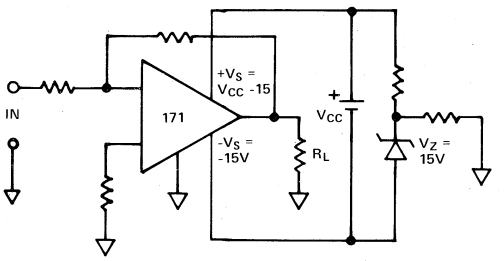


Figure 2. Single Supply Operation

FREQUENCY RESPONSE

Figure 3 shows a plot of open loop gain and phase shift as a function of frequency for model 171. It can be seen that the model 171 is stable for all closed loop gains. At the crossover frequency, model 171 typically displays a phase margin of 85°.

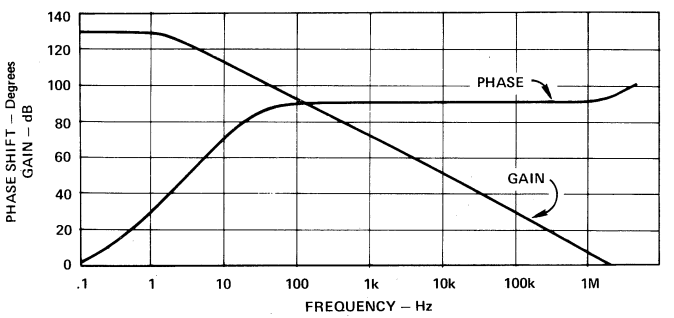


Figure 3. Gain and Phase Shift vs. Frequency

The open loop dc gain of the model 171 does not change appreciably as the power supply voltage is varied (see Figure 4). Open loop gain is typically greater than 106dB over the full power supply voltage range. Figures 3 and 4 show that excellent closed loop accuracy is assured over a great range of frequency and supply voltage when using the 171.

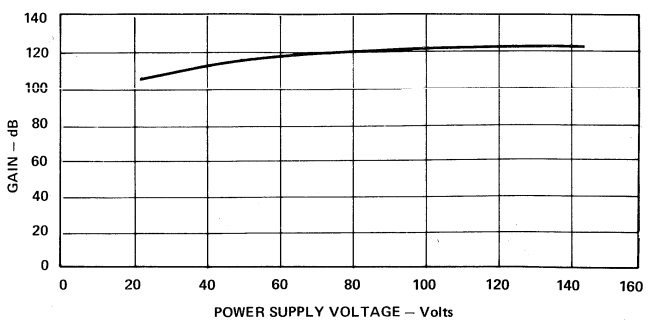


Figure 4. Open Loop dc Gain vs. Power Supply Voltage

COMMON MODE REJECTION RATIO

Common mode rejection is an important parameter in measurements requiring the amplification of small differential signals riding on high common-mode voltage levels. Model 171 is characterized by a minimum CMR of 100dB over its specified power supply voltage range. For the 171, CMR increases above this minimum value as the power supply voltage is raised. Figure 5 shows CMR as a function of supply voltage for model 171. The 171 also is capable of handling common-mode voltages up to 140 volts (with maximum supply voltages).

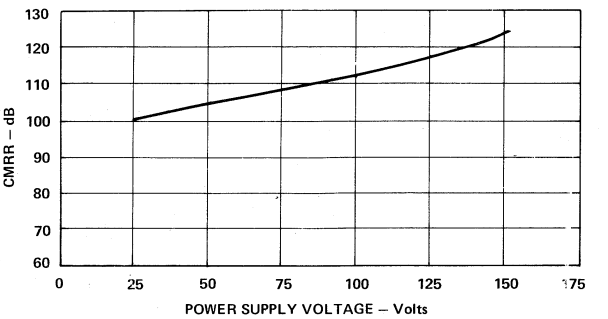


Figure 5. CMRR vs. Power Supply Voltage

OFFSET VOLTAGE

Model 171 provides excellent power supply rejection of 7μV/V and guaranteed input offset voltage drift of 15μV/°C (171K). The combination of these two characteristics, along with its gain and common mode performance, help make the model 171 an accurate and stable source of high voltage signals. Figure 6 shows input offset vs. power supply voltage for the 171. Supply rejection is fairly constant and is not dependent upon the power supply voltage level.

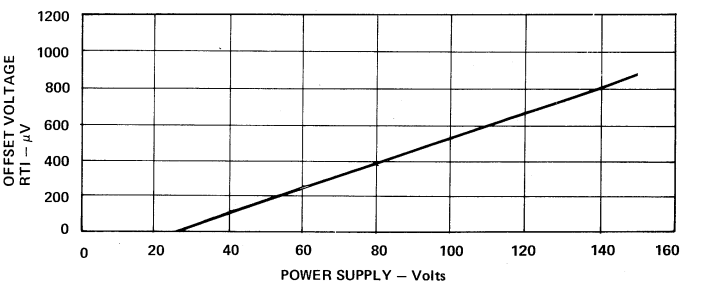


Figure 6. Input Offset Voltage vs. Power Supply Voltage

BIAS CURRENT

The input bias current for the model 171 is specified to be 50pA, max for the J version and 20pA, max for the K version. These specifications are guaranteed over the normal range of common mode voltage. Bias current is a function of CMV and decreases as the CMV approaches zero volts. Figure 7 shows bias current vs. CMV for model 171K. Notice that with zero CMV the bias current is typically less than 3pA.

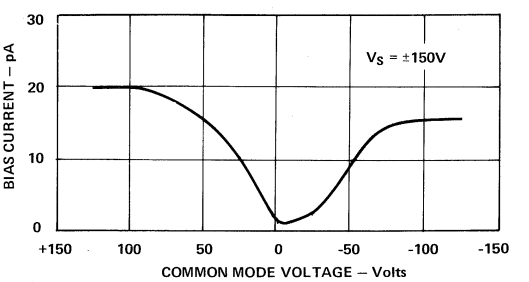


Figure 7. Bias Current vs. CMV for Model 171K

APPLICATIONS

There are many moderate-to-high voltage applications for which the model 171 FET-input op amp is useful. Typical classes of applications include:

1. Retrofit and auxiliary applications in existing analog computing systems utilizing a standard ±100V signal-voltage range.
2. Use as low-noise buffers and input amplifiers in differential or non-inverting applications with signals derived from high-voltage sources.
3. Applications for which high output voltage is needed, e.g., wide-range precision reference sources. piezoelectric crystal drivers, etc.
4. Applications with moderate signal levels in systems subject to wide variation of supply voltage.

Model 171's excellent performance characteristics, including high supply rejection, high input impedance, low noise, tolerance of capacitive load, and protection against output short circuits, make it ideal for all these classes of application.

In addition, there is one more class that is a bit unusual. For an amplifier to be safe against short-circuits, it must not only be self-protected, it must also protect the supply that feeds it. The 171 is programmed to draw a maximum short-circuit current slightly greater than the 10mA maximum load current plus its quiescent current. Therefore, model 171 is the ideal choice for applications where a fail-safe current load that is essentially independent of supply voltage is needed.

APPLICATIONS – PROGRAMMABLE REFERENCE VOLTAGE SOURCE

The operating specifications of the model 171 make it ideally suited for use as a low-cost, high voltage reference power supply. When coupled with an appropriate D/A converter, the 171 can also function as a 12 bit programmable voltage source. Such a network, utilizing Analog Devices DAC12QZ converter, is shown in Figure 8. This system offers the versatility of binary or BCD coding and unipolar or bipolar output. Programmable levels of ±50V or ±100V are available by setting the output level on the D/A converter. The model 171 supply voltages can also be varied depending on the desired reference output levels. Gain control and offset control can be used, as shown in Figure 8. This type of reference supply network can be used in such applications as generation of calibration voltages (circuit or instrument testing) and low current control signal levels. Trim resistors are used in this circuit to precisely adjust the full scale and zero levels of the reference output.

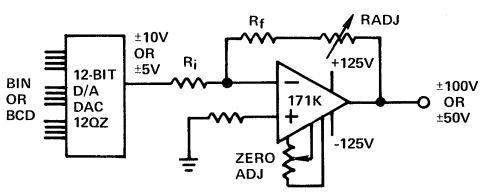


Figure 8. Programmable Power Supply

An expanded application for model 171 in a programmable voltage source for a mass spectrometer is shown in Figure 9.

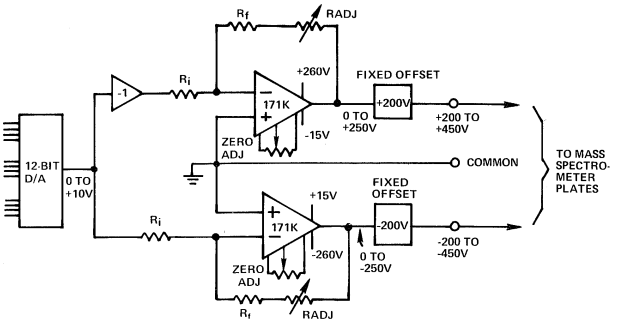


Figure 9. Programmable Mass Spectrometer Voltage Source

NONLINEAR CIRCUITS HANDBOOK

In addition to its linear devices, Analog Devices also offers a comprehensive line of nonlinear function modules (multipliers, dividers, rms to dc converters, etc.). These function modules provide essential building blocks in systems that process information in industrial applications. In order to further the understanding of function modules, Analog Devices has issued the Nonlinear Circuits Handbook. This handbook is an invaluable source of information on principles, circuitry, performance specifications, testing and application of the class of devices used in nonlinear applications. The handbook helps identify design situations for which nonlinear devices will offer the best solution and provides the fundamentals and guidelines necessary for the proper selection and use of function modules. The Nonlinear Circuits Handbook is available from Analog Devices

OTHER AMPLIFIERS

- High Performance FET – model 52: low noise (1.5μV p-p, 1Hz BW), low drift (1μV/°C, 5 2K) low bias (3pA max), CMRR = 80dB min
- Wideband – model 48: 15MHz (unity gain), low noise 2μV p-p, 1Hz BW, 300ns settling, 15μV/°C drift (max)
- Wideband, Fast Settling – model 50: 70MHz (unity gain), 100mA output, 15μV/°C drift (max, 50K)
- Chopper Stabilized – model 261: guaranteed low noise (1μV p-p max, 1Hz BW), ±0.1μV/°C drift (max, 261K)
- Economy Electrometer – model 42: lowest bias (75fA, 42K)
- High Output Current – model 50: 100mA output, wideband (10MHz, f_p), 80ns settling

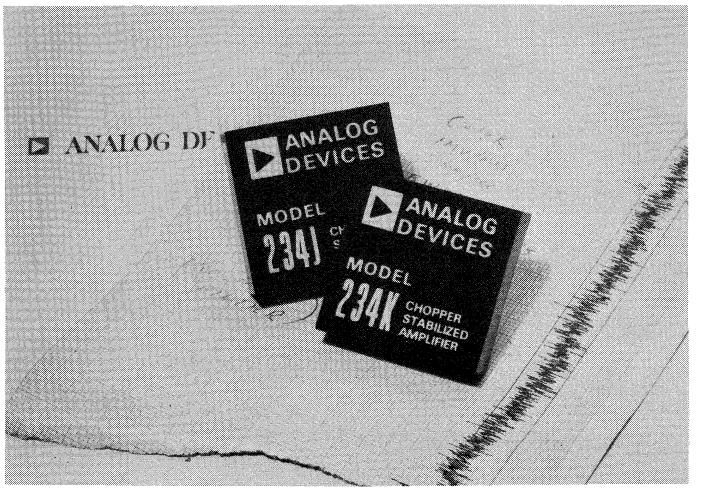
ANALOG DEVICES

Low Noise-Wideband Chopper Stabilized Amplifier

MODEL 234

FEATURES
Low Drift: 0.1μV/°C, 1pA/°C (Model 234L)
Offset Stability: 2μV per month
Submicrovolt Noise: 0.7μV p-p (0.01 to 1Hz B.W.)
Fast Response: 2.5MHz B.W., 4μs settling (0.01%)
Low Cost Module
Small Size: 1½" x 1½" x 0.4"

APPLICATIONS
Precision Wideband Amplification
Current and Voltage Summation
High Speed Integration
Reference Buffering
Controlled Current Source
Bridge Amplifier



GENERAL DESCRIPTION

Analog Devices' model 234 is a high performance chopper stabilized op amp which significantly improves on the noise and bandwidth performance of previous designs. Available with drift of 0.1μV/°C, the model 234 features 0.7μV p-p input noise and 2.5MHz unity gain bandwidth to satisfy many demanding requirements for a premium amplifier at less than premium prices.

Incorporating MOSFET choppers and discrete components (vs. IC op amps) for the main and stabilizing amplifier channels, this inverting design is virtually free of input chopper spikes and offers reduced modulation ripple for quieter wideband performance. These characteristics are especially desirable when operating from high source impedances (above 100kΩ) at wide bandwidths. To illustrate the improvements in noise and bandwidth performance, over previous Analog Devices' designs, comparative data is set forth in the following sections comparing models 232 and 233 with 234.

Other model 234 specifications include: gains of 10^7 V/V, 4μs settling time to 0.01% (20kΩ load, 10V) and three selections for voltage drift: 1μV/°C (234J), 0.3μV/°C (234K), and 0.1μV/°C (234L). Available in a compact plug-in module (1½" x 1½" x 0.4"), model 234 is competitively priced for new OEM designs and is recommended as a pin compatible replacement for upgrading the performance of most existing designs. The use of premium discrete components throughout assures repeatable unit-to-unit performance for best results at lower costs.

APPLICATIONS

In general, the model 234 inverting amplifier should be considered where long term stability of offset voltage must be maintained with time and temperature for precision designs, or wherever carefree operation of instruments and remote circuits is essential. Typical applications include low drift amplification of wideband microvolt signals, integration of low duty-cycle pulse trains and fast analog computing for general purpose designs. Low input noise and stable offset voltages also make model 234 an ideal preamp for precision low frequency applications such as DVM's, 12 to 16 bit A to D converters, and for error amplifiers in servo and null detector systems.

IMPROVED NOISE AND BANDWIDTH PERFORMANCE

The improved performance of model 234 accrues from the use of discrete components throughout, coupled with low noise front-end circuits, all carefully packaged and shielded to minimize pickup and intermodulation effects. Chopper modulation ripple, as shown in Figure 1, is significantly reduced over an earlier design, model 232, for most wideband applications.

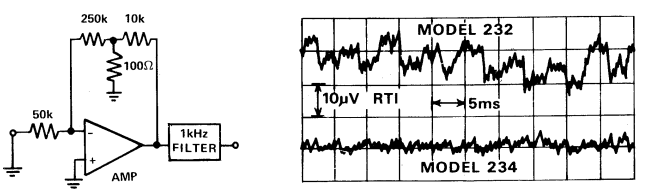


Figure 1. Comparative Input Noise (RTI) Performance in a dc to 1kHz Bandwidth

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	234J	234K	234L
OPEN LOOP GAIN			
DC, 2k ohm load	10^7 V/V min	*	*
RATED OUTPUT			
Voltage	±10V min	*	*
Current	±5mA min	*	*
Load Capacitance Range	0–1000pF min	*	*
FREQUENCY			
Unity Gain, Small Signal	2.5MHz	*	*
Full Power Response	500kHz min	*	*
Slew Rate	30V/μs	*	*
SETTLING TIME to 0.01%			
20kΩ load, 10V step (Figure 2)	4μs	*	*
INPUT OFFSET VOLTAGE			
Initial Offset[1] @ +25°C	±50μV max	±20μV max	±20μV max
vs. Temp, 0 to +70°C	±1.0μV/°C max	±0.3μV/°C max	±0.1μV/°C max
vs. Supply Voltage	±0.2μV/%	*	*
vs. Time	±2μV/month	*	*
vs. Turn On, 10 sec to 10 min	±3μV	*	*
INPUT BIAS CURRENT			
Initial, @ +25°C	±100pA max	*	*
vs. Temp, 0 to +70°C	±4pA/°C max	±2pA/°C max	±1pA/°C max
vs. Supply Voltage	±0.5pA/%	*	*
INPUT IMPEDANCE			
Inverting Input to Signal Ground	300k ohms	*	*
INPUT NOISE			
Voltage, 0.01 to 1Hz	0.7μV p-p	*	*
0.1 to 10Hz	1.5μV p-p	*	*
10Hz to 10kHz	2μV rms	*	*
Current, 0.01 to 1Hz	2pA p-p	*	*
0.1 to 10Hz	4pA p-p	*	*
INPUT VOLTAGE RANGE			
(-) Input to Signal Ground	±15V max	*	*
POWER SUPPLY (V dc)[2]			
Rated Performance	±15V @ 5mA	*	*
Operating	±(12 to 18)V	*	*
TEMPERATURE RANGE			
Rated Specifications	0 to +70°C	*	*
Operating	-25°C to +85°C	*	*
Storage	-25°C to +100°C	*	*

*Specifications same as model 234J.

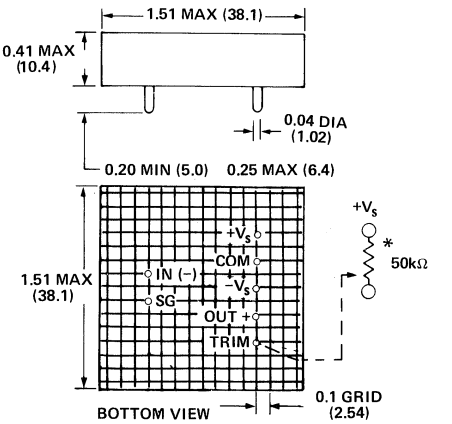
[1] Externally adjustable to zero.

[2] Recommended power supply, Analog Devices model 904, ±15V @ 50mA

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

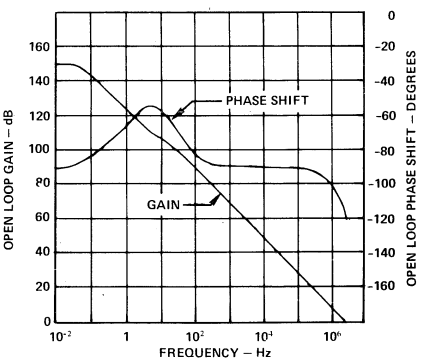


NOTES:

*Optional Trim Pot Analog Devices Model 79PR50k
Connect Trim Terminal to Common if Trim Pot is not used.

1. SG (SIGNAL GROUND) Tied to Common.
2. Mating Socket AC1010
3. Weight: 27 grm

OPEN LOOP GAIN AND PHASE SHIFT



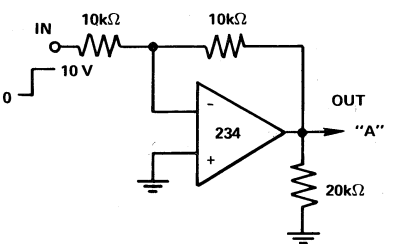


Figure 2. Settling Time Test Circuit Using Scope Comparator Preamp at "A"

Shown below are plots of typical input voltage and input current noise over the frequency range of 0.01Hz to 10Hz. Particular care has been exercised in the design of this amplifier to reduce the noise level to that commensurate with the low drift performance obtained by chopper stabilization.

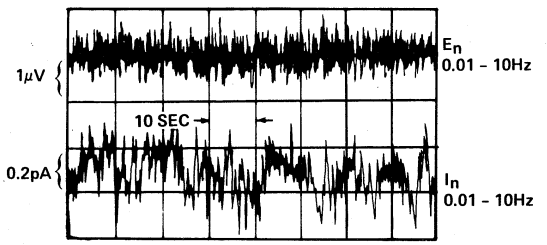


Figure 3. Model 234 Voltage and Current Noise

INPUT IMPEDANCE CONSIDERATIONS

The maximum input impedance for inverting amplifiers of all types is limited by bias current, bias current drift, and noise current. These currents flowing through the source impedance will increase the total error and noise when the input impedance exceeds E/I, where E is a given type of voltage error and I is the corresponding current error. Figure 4 is a plot of total offset voltage, total voltage drift and total noise vs. input resistance for the model 234. Up to 100,000 ohms, the model 234 provides relatively constant levels of offset, noise, and drift. Above this resistance level, the bias current effects become more predominant.

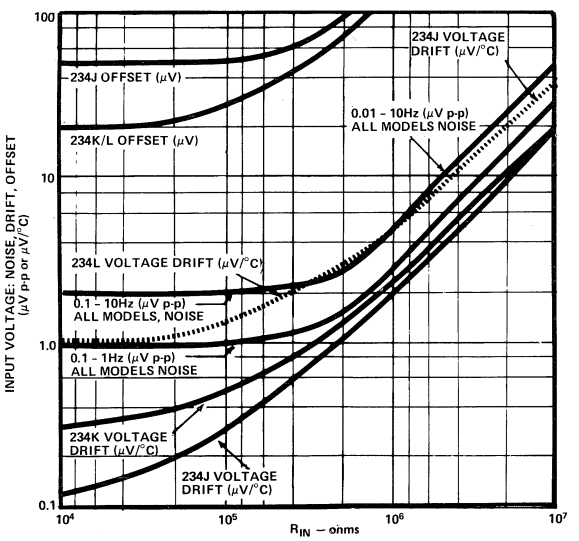


Figure 4. Uncompensated Offset, Drift and Noise vs. R_{in}

INITIAL OFFSET ADJUSTMENT

A valuable characteristic of the model 234 is the low offset voltage without external trim. The specification is 50μV maximum for the model 234J, and 20μV maximum for the models 234K and 234L. In many applications there will be no need to zero the offset since it is so low. In such cases the trim terminal may either be left open, or grounded, whichever is more convenient for the user. If voltage offset adjustment is desired, it may be done with a potentiometer or selected fixed resistor network, as shown in the outline drawing on previous page.

Input bias current flowing through the input resistor(s) creates additional voltage offset, particularly with input resistances exceeding 500,000 ohms. For circuits where the total input and source resistance remain relatively constant, the entire offset may be zeroed out with the voltage offset adjustment. No additional drift will occur with the model 234 when voltage trimming is used to compensate for the offset effects of input bias current.

The circuit of Figure 5 should be used to compensate for bias current offsets when using the model 234 as a current to voltvoltage converter. The potentiometer-resistor network provides a compensating bias current to cancel the amplifier's own input bias current. The offset voltage trim may be used but is not necessary when using this technique.

When the amplifier is used with a widely varying input resistance and minimum offset is desired, the voltage and current trim potentiometers should be used. The voltage offset should be zeroed with a low value (e.g. 1k ohm) resistor connected from the inverting input to ground. The offset current adjustment should be made with the maximum expected value of R_i connected between the input and ground.

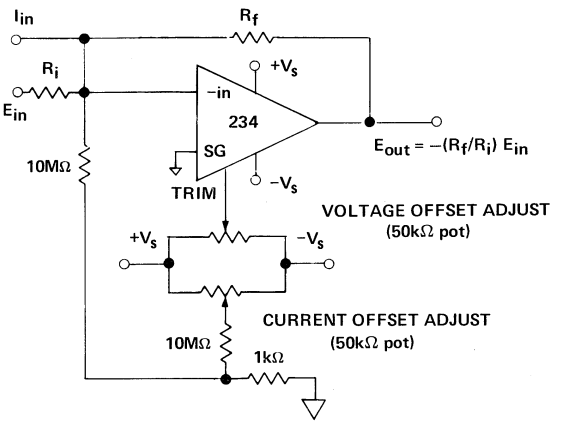


Figure 5. Offset Current Voltage Cancellation

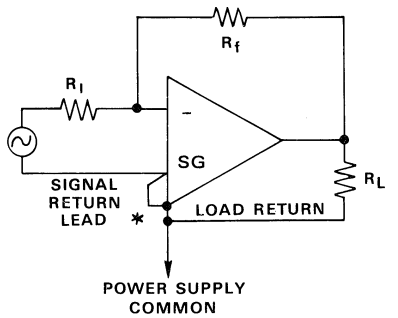
INVERTING OPERATION

The model 234 is designed for use in the inverting mode. It is important that the SG (equivalent to +in) terminal be kept at the same potential as the amplifier's "common" terminal. Any voltage difference between these points is similar to a common mode voltage, and performance cannot be guaranteed under such conditions. The model 234 is also an excellent amplifier for measurement and conversion of low level current sources to proportionate voltages. With offset current externally zeroed, input currents of ten to twenty picoamperes can be amplified and converted to a voltage source for further processing.

SHIELDING, PICKUP AND GROUNDS

A special feature of the model 234 is the internal electrostatic static shield. This prevents not only pickup of extraneous signals by the module but also prevents radiation of chopper noise by the module. One precaution is to insure that noise sources are shielded from the inverting input. The user should

also insure that ground loops do not occur which can add extraneous signals when amplifying from microvolt or millivolt sources. Figure 6 illustrates the proper connections to avoid ground loops.



* SIGNAL RETURN AND LOAD RETURN SHOULD BE CONNECTED TO POWER COMMON AS CLOSE TO AMPLIFIER PINS AS POSSIBLE

Figure 6. Ground Connection

INTERMODULATION CONSIDERATIONS

If noise at medium frequencies (to 400Hz) finds its way into the input circuits of carrier amplifiers (chopper amplifiers and the chopper-stabilizing portions of chopper-stabilized amplifiers), it tends to "beat" with the chopper frequency and produce sum and difference frequencies. The "sum" frequencies are unimportant, because they are usually filtered out; the noise frequency is usually unimportant because it, too, is filtered out. But the difference frequencies (which can include dc) usually interfere directly with the low-level low-frequency signal information.

There are precautions that can be taken by the manufacturer to minimize such interference occurring within the devices themselves; but the user must also be aware of the need for precautions, especially in performing low-level measurements in the presence of:

1. input signals containing high-frequency normal-mode noise components (such as unfiltered carrier from a measuring device)
2. ripple coupled in from power supplies
3. stray electromagnetic radiation at line frequencies, especially if it is rich in harmonics.

This noise may be introduced to the amplifier at either improperly guarded input leads or at the power supply terminals. These effects may be minimized by using shielded supplies which have low ripple and low source impedances at the line harmonics. Properly shielding the input leads, as well as locating the amplifier as far from sources of 60Hz (or 50Hz) magnetic fields, is also recommended for best performance. Mechanical orientation of the amplifier package and layout of signal grounds may also be used to minimize EMI effects.

If a "beat" does occur, it usually manifests itself as a slowly varying offset signal at the output of the amplifier, usually below 20Hz. To examine the extent of this equivalent offset noise voltage in a system, an oscilloscope should be used to monitor the amplifier output with the input signal point shorted to ground. As another test, a low level signal may be applied at the input of the final circuit configuration to determine the intermodulation rejection capability of the design. In this test, the signal frequency should be swept through the modulation frequency point to observe output signal peaking. A low pass output filter, at approximately 40Hz, should be used when making these tests.

THE "T" NETWORK

High gains and high input impedance to an inverting amplifier normally require excessively large feedback resistors. For example, an input impedance of 1,000,000 ohms and a gain of 100 require a feedback resistor of 100 Megohms. Such a resistor is relatively expensive, particularly for low tolerance units. Furthermore, one picofarad of stray capacitance across this single resistor would reduce 3dB bandwidth to 1590Hz, and resistive leakage across PC boards may become a problem. The "T" network in Figure 7 is a means of minimizing these problems. If the ratio R_f/R_i is at least 5 to 1, there will be no measurable change in other performance characteristics. If the ratio is lower, for instance, 1 to 1, the effective drift and noise gain will be doubled, compared to the signal gain. A general rule is to make the ratio R_f/R_i approximately equal to the ratio R_2/R_1. This normally results in reasonable values of resistance for R_f, and a minimal increase in noise and drift gains compared to the standard two resistor circuit. An additional advantage of the "T" network is variable gain without the necessity of connecting a switch or potentiometer directly to the highly sensitive inverting input terminal. This avoids serious noise pickup problems. In such a hookup, R_1 is the variable element.

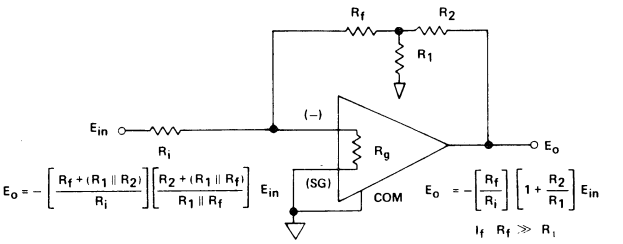


Figure 7. "T" Network

OVERLOAD RECOVERY

The overload recovery circuit shown in Figure 8 will prevent the input circuitry from becoming saturated. This circuit, connected externally, will allow the amplifier to recover from overload in less than 0.5μs. Without this circuit overload recovery will require up to 5 seconds.

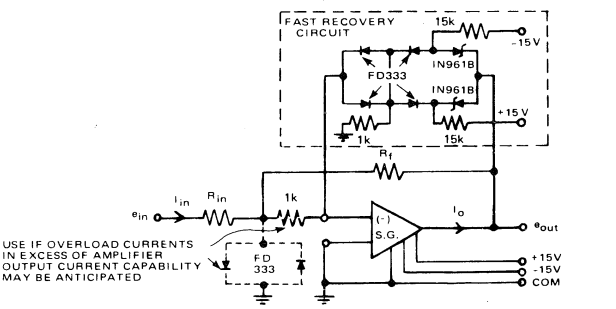


Figure 8. Overload Recovery Circuit

HIGH SOURCE IMPEDANCE CIRCUITS

When required to operate from source impedances above 100kΩ, the model 234, with inherently lower input current noise and spikes, offers dramatic improvements over previous designs. (See Figure 9)

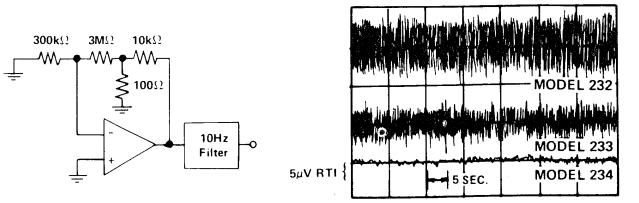


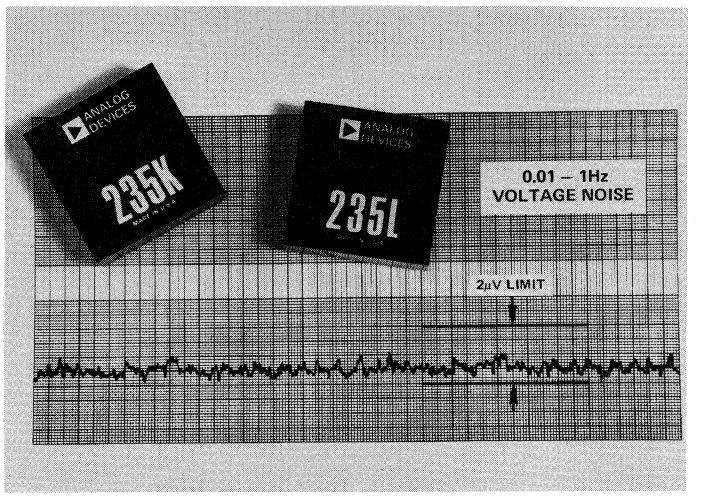
Figure 9. Comparative Input Noise (RTI) Performance in a dc to 10Hz Bandwidth

Economy, Guaranteed Low-Noise Chopper Stabilized Amplifier

MODEL 235

FEATURES
Low Cost
Ultra-Low Noise: 0.5μV p-p, 1Hz BW (2μV, max)
Very Low Drift: 0.1μV/°C max, 0.5pA/°C max (235L)
Excellent Long Term Stability: 5μV/yr
Low Profile: 0.5" Height

APPLICATIONS
Precision Integrator
Picoamp Current Measurements
Microvolt Voltage Measurements
Bridge Amplifier
Balance Scales and Weighing Instruments



GENERAL DESCRIPTION

Analog Devices' model 235 is a chopper stabilized inverting op amp that delivers premium performance at economy prices. It is pin-compatible with existing, more expensive modules, allowing designers to upgrade systems while realizing significant cost savings.

Foremost among model 235's electrical specifications is its outstanding noise performance of 0.5μV p-p (f = 0.01 to 1Hz) with a guaranteed maximum limit of 2μV in a 1Hz BW. Low voltage noise combined with low current noise (10pA p-p, 1Hz BW) yields low input noise for source impednaces up to several hundred-thousand ohms. The 235 also offers low voltage and current drift as a function of both temperature (0.1μV/°C max, 0.5pA/°C max, 235L) and time (5μV/yr). This combination of noise and drift performance makes model 235 ideally suited for demanding applications such as balance scales and weighing instruments requiring high accuracy and excellent long-term stability without the use of "front panel" balance pots or periodic internal adjustment.

Model 235 has been designed to virtually eliminate intermodulation problems caused by "beating" against power line frequencies. The chopper's ultra-stable oscillator is precisely set at the factory to a frequency that minimizes interactions with harmonics of 50, 60 and 400Hz power lines.

For new and upgraded designs, model 235 sets the benchmark for economy chopper performance.

APPLICATIONS

The model 235 inverting amplifier should be considered when long term stability must be maintained with time and temperature, and wherever maintenance-free operation of instruments and remote circuits is essential. Typical applications include amplification of microvolt signals, precision integration and analog computing. Low input noise and stable offset voltages make model 235 an ideal preamp for precision low frequency applications such as DVM's, 12 to 16 bit A to D converters, and error amplifiers in servo and null detector systems.

GUARANTEED NOISE PERFORMANCE

The excellent 1Hz voltage noise performance of model 235 (Figure 1) results from careful selection of critical design components during manufacturing. Selection permits 1Hz voltage noise to be maintained very near the typical specification (0.5μV p-p).

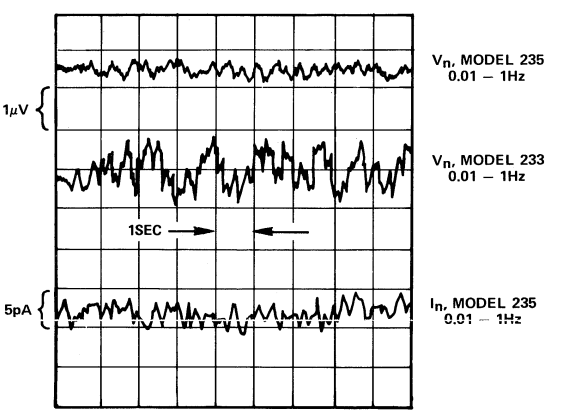


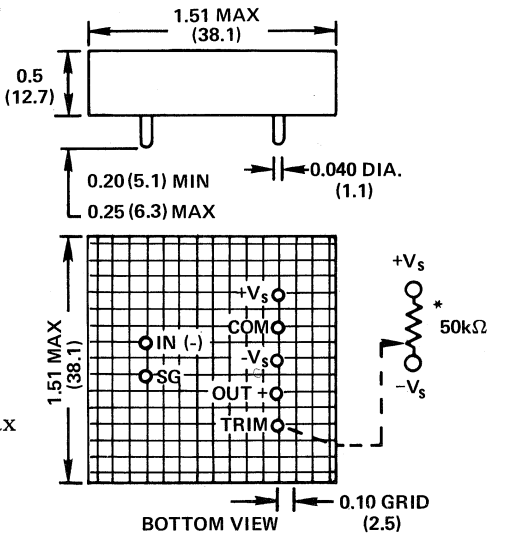
Figure 1. Model 235 Voltage and Current Noise. Model 233 Voltage Noise Shown for Comparison

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	235J	235K	235L
OPEN LOOP GAIN			
DC, 2k ohm load	5 x 10^7V/V min	*	*
RATED OUTPUT			
Voltage	±10V min	*	*
Current	±5mA min	*	*
Load Capacitance Range	0.01μF	*	*
FREQUENCY			
Unity Gain, Small Signal	1MHz	*	*
Full Power Response	5kHz min	*	*
Slew Rate	0.3V/μs min	*	*
Overload Recovery	10 sec	*	*
INPUT OFFSET VOLTAGE			
Initial Offset,[1] @ +25°C	±25μV max	±25μV max	±15μV max
vs. Temp, 0 to +70°C	±0.5μV/°C max	±0.25μV/°C max	±0.1μV/°C max
vs. Supply Voltage	±0.1μV/%	*	*
vs. Time	±5μV/year	*	*
vs. Turn On, 10 sec to 10 min	±3μV	*	*
INPUT BIAS CURRENT			
Initial, @ +25°C	±100pA max	±50pA max	±50pA max
vs. Temp, 0 to +70°C	±1pA/°C max	±0.5pA/°C max	±0.5pA/°C max
vs. Supply Voltage	0.2pA/%	*	*
INPUT IMPEDANCE			
Inverting Input to Signal Ground	300k ohms	*	*
INPUT NOISE			
0.01 to 1Hz, typ	0.5μV p-p		
0.01 to 1Hz, max	—	2μV p-p	2μV p-p
0.1 to 10Hz	3.5μV p-p	*	*
10Hz to 10kHz	5μV rms	*	*
Current, 0.01 to 1Hz	10pA p-p	*	*
0.1 to 10Hz	30pA p-p	*	*
INPUT VOLTAGE RANGE			
(-) Input to Signal Ground	±15V max	*	*
POWER SUPPLY (V dc)[2]			
Rated Performance	±15V @ 5mA	*	*
Operating	±(12 to 18)V	*	*
TEMPERATURE RANGE			
Rated Specifications	0 to +70°C	*	*
Operating	-25°C to +85°C	*	*
Storage	-55°C to +125°C	*	*

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



NOTES:

*Optional Trim Pot Analog Devices Model 79PR50k
Connect Trim Terminal to Common if Trim Pot is not used.

1. SG Should Be Tied to Common.
2. Mating Socket AC1010
3. Weight: 27 grams.

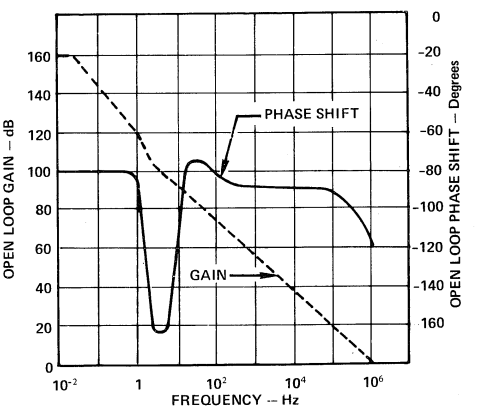


Figure 2. Open Loop Gain and Phase Shift vs. Frequency

*Specifications same as model 235J.

[1] Externally adjustable to zero.

[2] Recommended power supply, Analog Devices model 904, ±15V dc @ 50mA

Specifications subject to change without notice.

Model 235's low frequency noise characteristics complement its very low drift performance to yield exemplary stability and accuracy for a chopper stabilized amplifier. A plot of noise as a function of bandwidth for model 235 is shown in Figure 3.

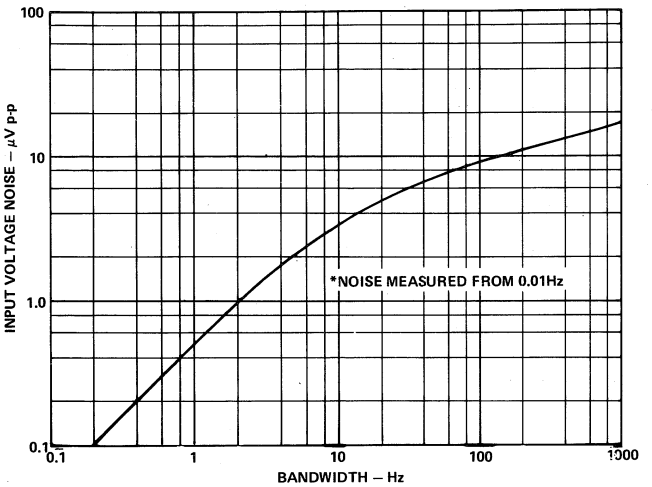


Figure 3. Input Voltage Noise vs. Bandwidth for Model 235

INPUT IMPEDANCE CONSIDERATIONS

Maximum input impedance for inverting amplifiers of all types is limited by bias current, bias current drift, and noise current. These currents flowing through the source impedance increase total error and noise as the input impedance increases. Figure 4 is a plot of total offset voltage, voltage drift and noise vs. input resistance for the model 235.

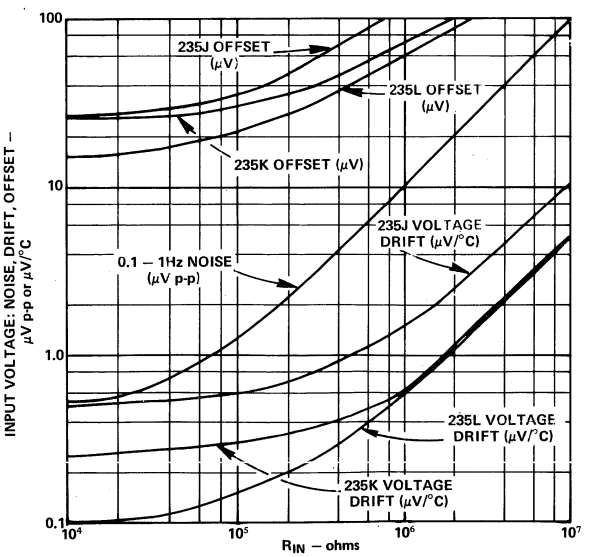


Figure 4. Uncompensated Offset, Drift and Noise vs. R_{IN}

INITIAL OFFSET ADJUSTMENT

Model 235 has low, untrimmed offset voltage specifications of 25μV max for the J and K versions, and 15μV max for the L version. In many applications there will be no need to further trim the offset. In such cases the trim terminal may either be left open, or grounded. If voltage offset adjustment is desired, it may be done with a potentiometer or selected fixed resistor network, as shown in the outline drawing. For circuits where the total input and source resistance remain relatively constant, the entire offset may be zeroed out with the voltage offset adjustment.

The circuit of Figure 5 should be used to compensate for bias current offset when using the model 235 as a current to voltage converter. The potentiometer-resistor network provides a compensating bias current to cancel the amplifier's own input bias current.

When the amplifier is used with a widely varying input resistance and minimum offset is desired, the voltage and current trim potentiometers should be used. The voltage offset should be zeroed with a low value (e.g. 1k ohm) resistor connected from the inverting input to ground. The offset current adjustment should be made with the maximum expected value of R_i connected between the input and ground.

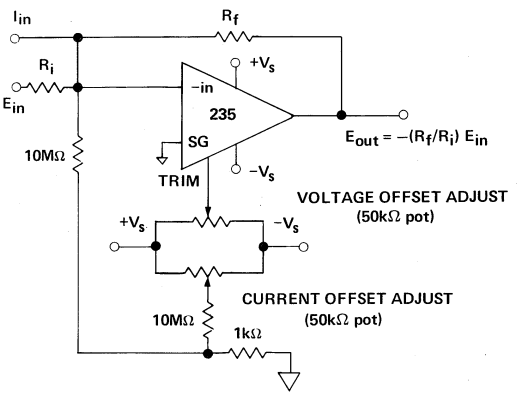


Figure 5. Offset Current Voltage Cancellation

INVERTING OPERATION

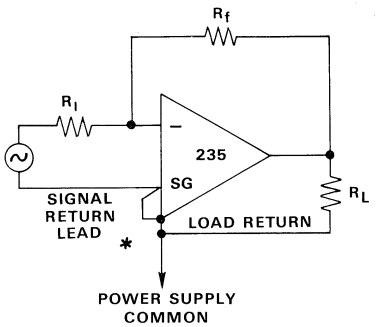
The model 235 is designed for use in the inverting mode. It is important that the SG (equivalent to +in) terminal be kept at the same potential as the amplifier's "common" terminal. Any voltage difference between these points is similar to a common mode voltage, and performance cannot be guaranteed under such conditions. The model 235 is also an excellent amplifier for measurement and conversion of low level current sources to proportionate voltages. With offset current externally zeroed, input currents of ten to twenty picoamperes can be amplified and converted to a voltage source for further processing.

SHIELDING, PICKUP AND GROUNDS

Model 235 has an internal electrostatic shield that prevents pickup of extraneous signals and radiation of chopper noise by the module. One precaution is to insure that noise sources are shielded from the inverting input. The user should also insure that ground loops do not occur which can add extraneous signals when amplifying from microvolt or millivolt sources. Ground loop errors most often occur when the power supply current is allowed to flow through the input (signal) ground connection. When this happens, a voltage drop is developed across the power supply leads which appears as a voltage generator in series with the signal source, and as error at the output. This is effectively eliminated by insuring that the signal return lead does not carry the power supply current. Figure 6 illustrates the proper connection.

Another source of error is the small voltages developed by the junction of dissimilar metals encountered in the external connections to the amplifier. Normally insignificant, these "therm-

ocouple" effects may approach the magnitude of the drift specifications of the 235. Careful attention to interconnection layout design will minimize these errors.



* SIGNAL RETURN AND LOAD RETURN SHOULD BE CONNECTED TO POWER COMMON AS CLOSE TO AMPLIFIER PINS AS POSSIBLE

Figure 6. Ground Connection

INTERMODULATION CONSIDERATIONS

If noise at medium frequencies finds its way into the input circuits of carrier amplifiers (chopper amplifiers and the chopper-stabilizing portions of chopper-stabilized amplifiers), it may "beat" with the chopper frequency and produce sum and difference frequencies. The "sum" and noise are unimportant, because they are usually filtered out. But the difference frequencies (which can include dc) usually interfere directly with the low-level low-frequency signal information. These effects can be examined with an oscilloscope.

Model 235 employs specially designed internal shielding and a stable, factory-set oscillator frequency to drastically reduce problems caused by interference from 50, 60 and 400Hz power lines. The user can take further precautions to eliminate intermodulation problems by:

1. Properly shielding input and power supply leads.
2. Using shielded supplies with low ripple and source impedance at the line harmonic frequencies.
3. Avoiding ground loops and locating the amplifier far from interference sources.

THE "T" NETWORK

High gains and high input impedance to an inverting amplifier normally require excessively large feedback resistors. Such a resistor is relatively expensive, particularly for low tolerance units. Furthermore, any stray capacitance across this single resistor significantly reduces bandwidth. The "T" network in Figure 7 minimizes these problems. If R_f/R_i is at least 5:1, there will be no measurable change in other performance characteristics. If the ratio is lower, the effective drift and noise gain will be increased compared to the signal gain. As a general rule, make the ratio R_f/R_i approximately equal to R_2/R_1. This results in reasonable values of resistance for R_f, and a minimal

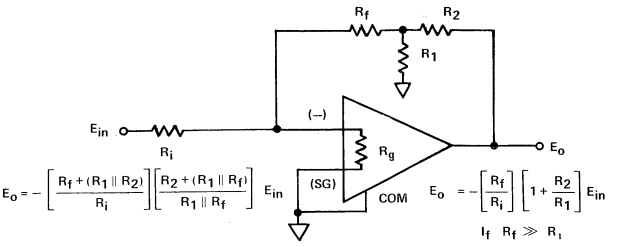


Figure 7. "T" Network

increase in noise and gain drift compared to the standard two resistor circuit. The "T" network also permits gain to be varied, by changing R_1, without the necessity of connecting a switch or potentiometer directly to the highly sensitive inverting input terminal.

OVERLOAD RECOVERY

The overload recovery circuit shown in Figure 8 will prevent the input circuitry from becoming saturated. This circuit, connected externally, will allow the amplifier to recover from overload in less than 0.5μs. Without this circuit overload recovery will require up to 10 seconds.

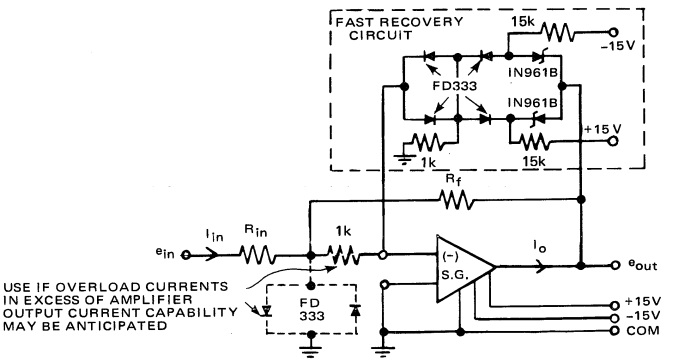


Figure 8. Overload Recovery Circuit

MODEL 234 WIDEBAND CHOPPER

The forte of model 235 is low frequency applications requiring high accuracy and highest stability. For wideband designs, the model 234 chopper is the recommended amplifier. The 234 has very good drift specifications coupled with outstanding bandwidth (2.5MHz unity gain, 500kHz full power) and wideband noise performance (1.5μV p-p, f = 0.1 to 10Hz and 2μV rms, f = 10 to 10kHz).

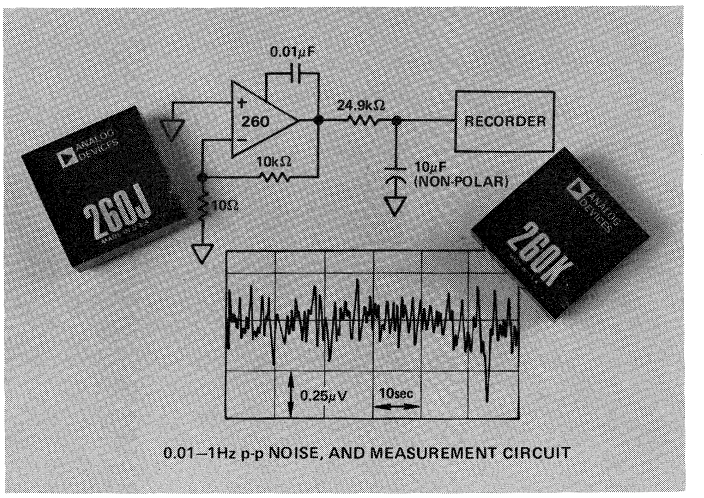
Model 234 is preferred for designs of wideband microvolt signal processors, low duty cycle pulse train integrators and fast analog computers.

Low Noise Non-Inverting Chopper Amplifier

MODEL 260

FEATURES
- Non-Inverting Input
- $10^9\,\Omega$ Common Mode Impedance
- Protected MOSFET Chopper
- Ultra Low Drift $0.1\mu V/^\circ C$, max (260K)
- Low Voltage Noise of $0.4\mu V$ p-p (0.01 to 1Hz)
- Low Current Noise of 4pA p-p (0.01 to 1Hz)
- Low Cost

APPLICATIONS
- Microvolt & Millivolt Measurements
- Meter & Recorder Preamplifier
- Semiconductor Strain Gage Amplifier
- Biological Sensors
- Potentiometer Buffer



0.01–1Hz p-p NOISE, AND MEASUREMENT CIRCUIT

GENERAL DESCRIPTION

Model 260 is a low cost non-inverting chopper amplifier featuring ultra low drift of $0.1\mu V/^\circ C$ (261K), open loop gain of greater than 5 million V/V and low noise performance of $0.4\mu V$ p-p in a 0.01 to 1Hz bandwidth. It is ideally suited for low level pre-amplifier applications where high input impedance and low noise are essential.

NON-INVERTING VS. INVERTING OPERATION

The major limitation of the standard inverting type chopper stabilized amplifier is due to the practical limit on input impedance resulting from input bias current characteristics. If one attempts to obtain 10^7 ohms input impedance by using a 10^7 ohm input resistor with an inverting amplifier, this resistor will convert input current drifts of $0.5pA/^\circ C$ into equivalent voltage drifts of $5\mu V/^\circ C$. It will also add Johnson Noise of $2.5\mu V$ p-p/$\sqrt{Hz}$ to the amplifier's input. These results negate the advantage of selecting the chopper-stabilized amplifier in the first place. Noise current will similarly increase the input uncertainty: inverting amplifier input noise currents of 10pA become $100\mu V$ noise voltages (referred to input). Furthermore, uncompensated initial bias currents of 50pA cause additional offsets of $500\mu V$. Due to the non-inverting configuration of the model 260, these limitations are avoided. The input bias current (with its drift and noise) flows only through the signal source impedance, effectively eliminating the multiplication of drift and noise and offset caused by the input resistor in the inverting configuration.

CHOPPER VS. CHOPPER-STABILIZED

Most conventional ultra-stable amplifiers are chopper-stabilized to achieve low drift. In these units, the higher frequency signal components are separated and directly amplified, while the low frequency and dc components are separately chopped, amplified, demodulated, and then summed with the high frequency components in an output stage. This method provides wide bandwidth and excellent performance at the expense of increased cost and complexity. Since many requirements for ultra-low drift amplification involve only dc and low frequency signals, the additional high frequency amplifier stage found in most chopper-stabilized amplifiers has been eliminated from the model 260. This design approach has made it possible to achieve a practical non-inverting configuration, which retains the advantages of low cost and small size. The input stage of the model 260 chops the signal at a 500Hz rate, resulting in a maximum useful -3dB bandwidth of about 100Hz. For increased flexibility in meeting specific design requirements, terminals are provided for an external compensation capacitor, which determines the amplifier's gain-bandwidth product.

INPUT IMPEDANCE

One of the prime advantages of the non-inverting amplifier is the capability of bootstrapping the input impedance up to the level of the common mode impedance. For the model 260, this means that the 80kΩ open loop input resistance will be multiplied by the open loop gain times the feedback factor. With a typical open loop gain of 20×10^6, closed loop gains of up to 1600 will allow the user to realize $10^9\,\Omega$ input resistance. Even at a gain of 10,000, the effective input resistance will be over 100 megohms. (i.e.,) $(80k\Omega)\,\frac{20 \times 10^6}{10^4} = 160M\Omega$

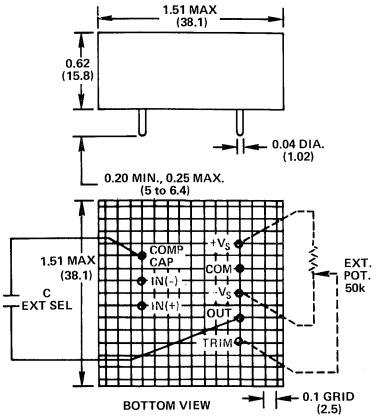
SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

Model	260J	260K
OPEN LOOP GAIN		
DC rated load	$5x10^6$ min	
RATED OUTPUT		
Voltage	±10V min	*
Current	±5mA min	*
Load Capacitance Range	0 to 0.001μF	*
FREQUENCY RESPONSE[1]		
Small Signal, -3dB	100Hz	*
Full Power Response	2-50Hz min	*
Slewing Rate	100V/sec min	*
Overload Recovery	300ms	*
INPUT OFFSET VOLTAGE		
External Trim Pot[2]	50kΩ	*
Initial Offset, +25°C	±25μV max	*
Avg vs Temp (0 to +70°C)	±0.3μV/°C max	±0.1μV/°C max
Supply Voltage	±0.1μV/%	*
Time	±½μV/month	*
Warm-up Drift	<3μV in 20 minutes	*
INPUT BIAS CURRENT		
Initial Bias, +25°C, + Input	±300pA max	*
Avg vs Temp (0 to +70°C)	±10pA/°C max	*
Initial Bias, +25°C, - Input	±3nA max	*
Avg vs Supply Voltage	±3pA/%	*
INPUT IMPEDANCE		
Differential	80kΩ‖0.01μF	*
Common Mode	10^9 Ω‖0.02μF	*
INPUT NOISE		
Voltage, 0.01 to 1Hz, p-p	0.4μV	*
0.01 to 10Hz, p-p	1.0μV	*
Current, 0.01 to 1Hz, p-p	4pA	*
0.01 to 10Hz, p-p	10pA	*
INPUT VOLTAGE RANGE		
Common Mode Voltage	±0.33V min	±1.0V min
Common Mode Rejection	300,000	*
Max Safe Differential Voltage	±20V	*
Max Safe Common Mode Voltage	±20V	*
POWER SUPPLY[3]		
Voltage, Rated Specification	±(14 to 16)V	*
Voltage, Operating	±(13 to 18)V	*
Current, Quiescent	±7mA	*
TEMPERATURE RANGE		
Rated Specifications	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Case Size	1.5" x 1.5" x 0.62"	*
Mating Socket	AC1022	*
Weight	1.75 oz. (50g)	*

[1] See selectable bandwidth, and Figure 1 and Figure 2.
[2] Ground trim terminal if trim potentiometer is not used.
[3] Recommended power supply, ADI model 904, ±15V @ 50mA output
*Specifications same as for model 260J.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SELECTABLE BANDWIDTH

The model 260 uses an external compensation capacitor to determine the gain-bandwidth product. Its value may be chosen to allow the use of the maximum 100Hz -3dB bandwidth, at any given value of closed loop gain. By using a larger value of compensation capacitance, the bandwidth can be limited to any desired value below 100Hz. The minimum value of the required compensation capacitor, in μF, is 1000/GB, where G is the desired closed-loop dc gain, and B is the -3dB bandwidth. For example, the minimum value of recommended capacitance (for 100Hz bandwidth to -3dB) is 10/G. Shown in Figure 1 are curves of the amplifier's response for various closed loop gains while using values of capacitance appropriate for maintaining 100Hz (-3dB) bandwidth. Figure 2 illustrates the model 260's open loop response with various values of the compensation capacitor. It is recommended that the capacitor be polycarbonate, mylar, mica, glass or polystyrene.

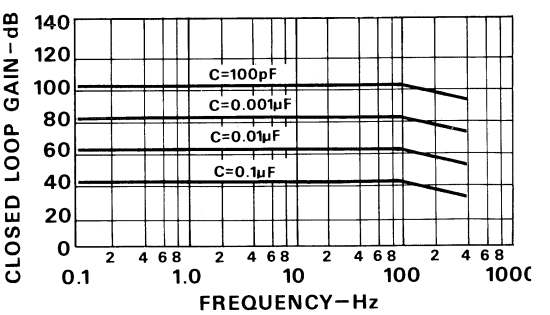


Figure 1. Compensation vs. Gain for 100Hz Bandw

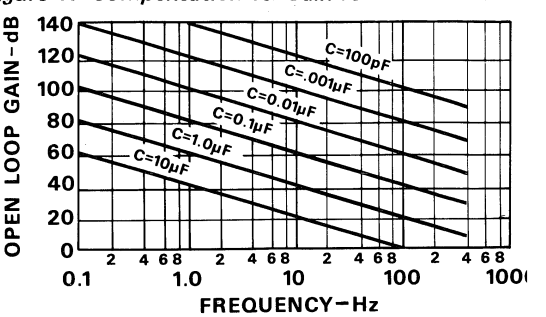


Figure 2. Open Loop Response vs. Compensation

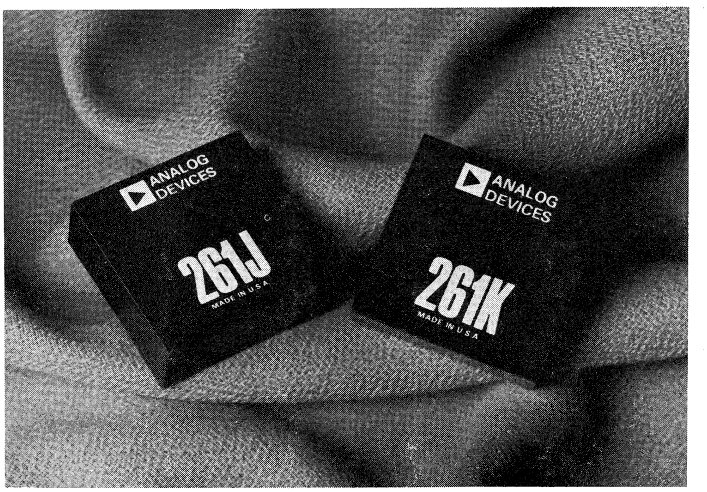
ANALOG DEVICES

Low Noise Non-Inverting Chopper Amplifier

MODEL 261

FEATURES
- Non-Inverting Input
- $10^9\Omega$ Common Mode Impedance
- Protected MOSFET Chopper
- Ultra Low Drift 0.1μV/°C, Max (261K)
- Guaranteed Low Noise of 0.4μVp-p (0.01 to 1Hz)
- Low Cost

APPLICATIONS
- Microvolt & Millivolt Measurements
- Meter & Recorder Preamplifier
- Semiconductor Strain Gage Amplifier
- Biological Sensors
- Potentiometer Buffer



GENERAL DESCRIPTION

Model 261 is a low cost non-inverting chopper amplifier featuring ultra low drift of 0.1μV/°C, open loop gain of greater than 10 million V/V and guaranteed low noise performance of 0.4μV p-p max in a 0.01 to 1Hz bandwidth. It is ideally suited for low level pre-amplifier applications where high input impedance and low noise are essential.

Model 261 also offers a solution to beat frequency problems caused by a low frequency carrier mixing with harmonics of the ac line. Its carrier frequency of 3500Hz is nearly a decade higher than that of models previously available. The required harmonic of the ac line that could cause interference with a 3500Hz carrier has negligible energy content and beat frequencies are eliminated. As a further protection against interfering signals, model 261 has been completely shielded internally. This protective shield reduces interference due to RF signals, as well as carrier signals from adjacent chopper amplifiers.

Still another advantage of the 261 due to its higher chopper frequency and shielded design is an output signal that is free from both distortion and chopper spikes. The result is a design that can process low level signals while maintaining low distortion and high signal to noise ratios.

CHOPPER VS. CHOPPER-STABILIZED

Most conventional ultra-stable amplifiers are chopper-stabilized to achieve low drift. In these units, the higher frequency signal components are separated and directly amplified, while the low frequency and dc components are separately chopped, amplified, demodulated, and then summed with the high frequency components in an output stage. This method provides wide bandwidth and excellent performance at the expense of increased cost and complexity. Since many requirements for ultra-low drift amplification involve only dc and low frequency signals, the additional high frequency amplifier stage found in most chopper-stabilized amplifiers has been eliminated from the model 261. This design approach has made it possible to achieve a practical non-inverting configuration, which retains the advantages of low cost and small size. The input stage of the model 261 chops the signal at a 3500Hz rate, resulting in a maximum useful -3dB bandwidth of about 100Hz. For increased flexibility in meeting specific design requirements, terminals are provided for an external compensation capacitor, which determines the amplifier's gain-bandwidth product.

INPUT IMPEDANCE

One of the prime advantages of the non-inverting amplifier is the capability of bootstrapping the input impedance up to the level of the common mode impedance. For the model 261, this means that the 40kΩ open loop input resistance will be multiplied by the open loop gain times the feedback factor. With a typical open loop gain of 40×10^6, closed loop gains of up to 1600 will allow the user to realize $10^9\Omega$ input resistance. Even at a gain of 10,000, the effective input resistance will be over 100 megohms. (i.e.) $(40k\Omega)\frac{40 \times 10^6}{10^4} = 160M\Omega$

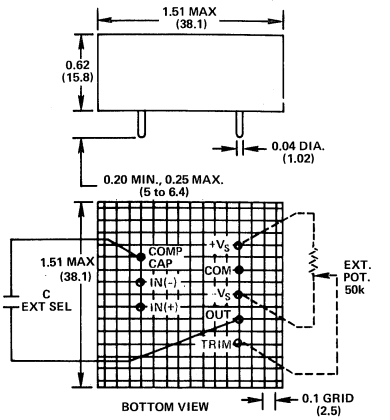
SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

Model	261J	261K
OPEN LOOP GAIN		
DC rated load	10^7 V/V min	
RATED OUTPUT		
Voltage	±10V min	*
Current	±5mA min	*
Load Capacitance Range	0 to 0.001μF	*
FREQUENCY RESPONSE[1]		
Small Signal, -3dB	100Hz	*
Full Power Response	2-50Hz min	*
Slewing Rate	100V/sec min	*
Overload Recovery	300ms	*
INPUT OFFSET VOLTAGE		
External Trim Pot[2]	50kΩ	*
Initial Offset, +25°C	±25μV max	*
Avg vs Temp (0 to +70°C)	±0.3μV/°C max	±0.1μV/°C max
Supply Voltage	±0.1μV/%	*
Time	±½μV/month	*
Warm-Up Drift	<3μV in 20 minutes	*
INPUT BIAS CURRENT		
Initial Bias, +25°C, + Input	±300pA max	*
Avg vs Temp (0 to +70°C)	±10pA/°C max	*
Initial Bias, +25°C, - Input	±10nA max	*
Avg vs Supply Voltage	±3pA/%	*
INPUT IMPEDANCE		
Differential	40kΩ||0.01μF	*
Common Mode	10^9 Ω||0.02μF	*
INPUT NOISE		
Voltage, 0.01 to 1Hz, p-p	0.4μV max	*
0.01 to 10Hz, p-p	1.0μV max	*
Current, 0.01 to 1Hz, p-p	8pA	*
0.01 to 10Hz, p-p	20pA	*
INPUT VOLTAGE RANGE		
Common Mode Voltage	±0.5V min	±1.0V min
Common Mode Rejection	300,000	*
Max Safe Differential Voltage	±20V	*
Max Safe Common Mode Voltage	±20V	*
POWER SUPPLY[3]		
Voltage, Rated Specification	±(14 to 16)V	*
Voltage, Operating	±(13 to 18)V	*
Current, Quiescent	±7mA	*
TEMPERATURE RANGE		
Rated Specifications	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Case Size	1.5" x 1.5" x 0.62"	*
Mating Socket	AC1022	*
Weight	1.75 oz. (50g)	*

[1] See applications information.
[2] Ground trim terminal if trim potentiometer is not used.
[3] Recommended power supply, ADI model 904, ±15V @ 50mA output
*Specifications same as for model 261J.
Specifications subject to change without notice.

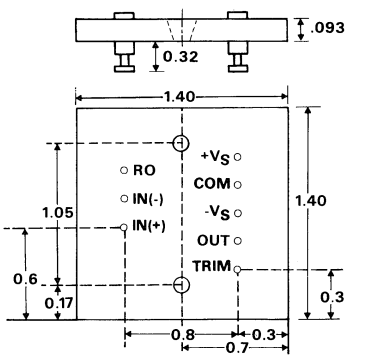
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Notes
1. Epoxy Case.
2. Pins 0.04 Dia. $\frac{+0.002}{-0.000}$ half hard Brass, Gold plated
3. Amplifier mates with socket AC1022
4. Trim potentiometer ADI part number 79PR50K.
5. Markings do not appear on unit.
6. Trim terminal should be grounded if potentiometer is not used.
7. See Note 1 below for cap value. Use Polycarbonate, Mylar, Mica, Glass, or Polystyrene capacitor for best performance.

MATING SOCKET AC1022



Notes
1. R.O. is connection for compensation capacitor.
2. Bottom View Shown.
3. Mounting holes 0.141 Dia., countersunk 82° to 0.23" Dia.
4. All in line pins spaced 0.2".
5. Dimensions in inches.
6. Markings printed on socket.

OTHER ULTRA LOW DRIFT, LOW NOISE AMPLIFIERS

Model 43K: This ultra low noise differential FET amplifier has guaranteed noise performance of 2μV p-p max in a 10Hz B.W. and 3μV rms max in a 50kHz B.W. Drift is 5μV/°C max.

Model 235: Chopper stabilized amplifier has noise of less than 1μV p-p and drift is only 0.1μV/°C (235L)

Model 184: A chopperless differential input amplifier with 0.25μV/°C drift and 1MHz bandwidth. Noise is 1μV p-p in a 0.01 to 1Hz B.W. and 4μV rms in a 50kHz B.W.

NON-INVERTING VS. INVERTING OPERATION

The major limitation of the standard inverting type chopper stabilized amplifier is due to the practical limit on input impedance resulting from input bias current characteristics. If one attempts to obtain 10^7 ohms input impedance by using a 10^7 ohm input resistor with an inverting amplifier, this resistor will convert input current drifts of 0.5pA/°C into equivalent voltage drifts of 5μV/°C. It will also add Johnson Noise of 2.5μV p-p/$\sqrt{\text{Hz}}$ to the amplifier's input. These results negate the advantage of selecting the chopper-stabilized amplifier in the first place. Noise current will similarly increase the input uncertainty: inverting amplifier input noise currents of 10pA become 100μV noise voltages (referred to input). Furthermore, uncompensated initial bias currents of 50pA cause additional offsets of 500μV. Due to the non-inverting configuration of the model 261, these limitations are avoided. The input bias current (with its drift and noise) flows only through the signal source impedance, effectively eliminating the multiplication of drift and noise and offset caused by the input resistor in the inverting configuration. These benefits of the model 261 are shown graphically in Figure 1. When required input impedance is more than 300,000 ohms, the model 261 gives increasingly superior performance. One additional advantage is that the gain-setting precision resistors can be low-cost low value resistors instead of the more costly high resistance values.

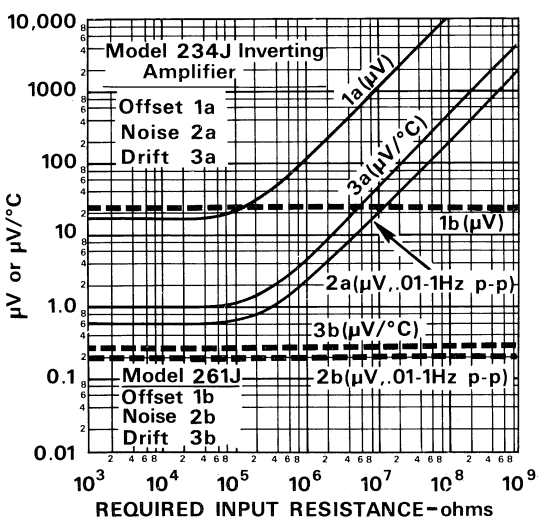


Figure 1. Offset, Drift, & Noise vs. Required Input Resistance

NON-INVERTING AMPLIFIER SELECTION CRITERIA

(Model 261 vs. chopperless amplifiers)

In selecting an amplifier for low drift, one of the major considerations is the effect of source resistance. For low values of source resistance, the total offset (or drift) for differential amplifiers is essentially equal to the amplifier's offset (or drift) voltage. At the value of source resistance equal to the ratio of offset voltage to difference current, or offset voltage drift to difference current drift, the respective current is contributing an error equal to its corresponding voltage error. For values of source resistance larger than this calculated value, the current error's contribution will be dominant. In this section, model 261's drift and offset are compared with two low drift chopperless differential amplifiers, one with FET input, the other with bipolar input.

Fixed Source Resistance. If source resistance is fixed, bipolar chopperless amplifiers not having internal bias current drift compensation can benefit by the use of a compensating resistor in series with the (-) input. Under these conditions, Figure 2 shows a comparison of total drift /°C vs. source resistance for the model 261K, the model 184L low drift bipolar amplifier, and the model 52K low drift FET amplifier. For source resistances up to 200,000 ohms, the model 261 gives the lowest temperature drift. Total drift (R.T.I.) is equal to:

$$\triangle E_{in}/\triangle T = \triangle E_{os}/\triangle T + R_S\ (\triangle I_{os}/\triangle T) \text{ (Models 184, 52)}$$

$$\triangle E_{in}/\triangle T = \triangle E_{os}/\triangle T + R_S\ (\triangle I_b/\triangle T) \text{ (Model 261)}$$

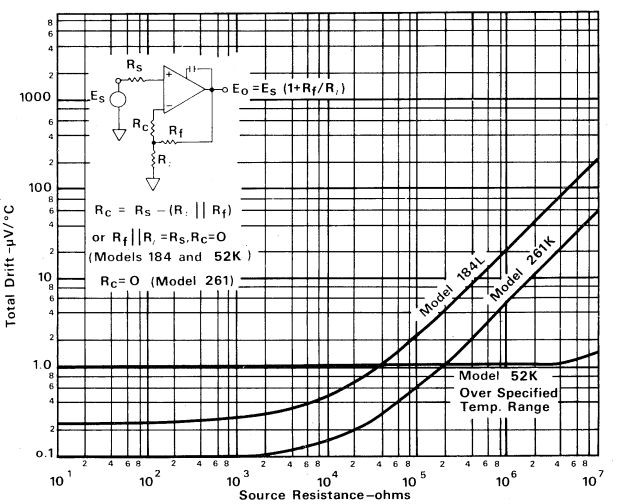


Figure 2. Offset Drift vs. Fixed Source Resistance

Variable Source Resistance. For situations where the source resistance can vary over a significant range, for instance when the amplifier's source is a multiturn potentiometer, a different set of conditions apply. The effective drift current to be considered for differential chopperless amplifiers is now the Input Bias Current/°C, rather than the Input Difference Current/°C (I_{os}/°C). A two to one improvement in drift for the model 184 can be obtained if the bias current balancing resistor (R_C in Figure 3) is made equal to the mean value of the source resistance. Under these conditions, drift will be approximately:

$$\triangle E_{in}/\triangle T = \triangle E_{os}/\triangle T + \tfrac{1}{2}\ (R_S \text{ max} - R_S \text{ min})\ (\triangle I_b/\triangle T) + R_C\ (\triangle I_{os}/\triangle T) \text{ (Models 184, 52K)}$$

$$\triangle E_{in}/\triangle T = \triangle E_{os}/\triangle T + (R_S \text{ max})\ (\triangle I_b/\triangle T) \text{ (Model 261)}$$

Figure 3 shows the total drift for a source resistance varying from zero to the chosen value, for models 52K, 184L and 261K. For values up to 200,000 ohms the model 261 again gives the lowest total temperature drift.

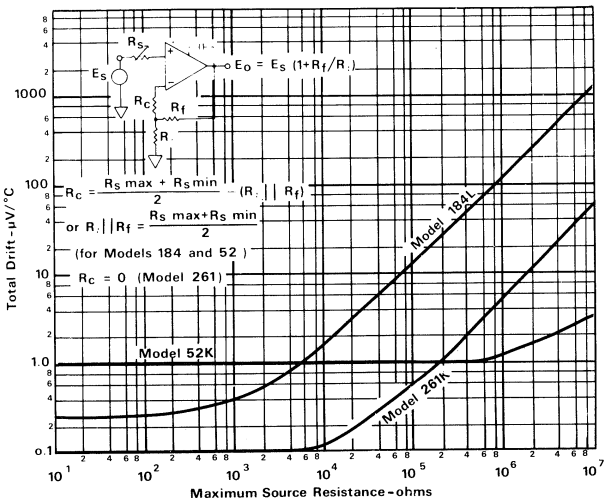


Figure 3. Offset Drift vs. Variable Source Resistance

INITIAL OFFSET

An initial offset voltage will develop due to bias current flowing through the source impedance. For fixed source impedances, this offset may be zeroed out in differential chopperless amplifiers not having internal bias current drift compensation by the use of the series compensating resistor, R_C shown in Figure 4. This offset should not be nulled out by adjusting the amplifier's offset trim because this will increase the offset voltage drift. With the model 261, however, all offsets may be zeroed out by means of the trim potentiometer. For variable source impedances, the offset should be zeroed out with the source impedance at its mean value. Figure 4 is a plot of the maximum offset which will occur with a given range of R_S variations, assuming the offsets are zeroed when operating with the mean value of R_S. Initial offset due to R_S is $I_b/2$ (R_S max - R_S min).

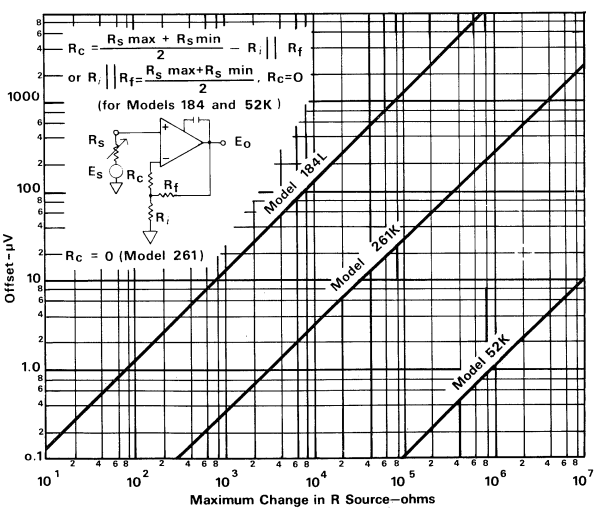


Figure 4. Offset vs. $\triangle R_S$

LONG TERM DRIFT

Offset voltage of any amplifier will show some change with time, due to normal component aging. It is important to realize that the published drift for amplifiers does not accumulate linearly with increasing time. For example, the voltage drift of the model 261 is specified as ±½µV/month (a calculated figure believed to be quite conservative). For calculation of random long term drift, a rule of thumb is that one should multiply drift by the square root of the time factor increase. For the model 261, this yields a conservative long term drift of less than 2µV per year.

NOISE

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. This is particularly important whenever high source impedances are encountered, since current noise through the source impedance will appear as an additional voltage noise, combining with the basic amplifier voltage noise and Johnson noise of the resistor. The sum of these noise sources will then be amplified along with the desired signal. For this reason, special care has been taken to reduce noise voltage and current to a level far below that of comparable chopper amplifiers. The one Hertz bandwidth noise voltage and current are 0.4µV p-p max and 8pA p-p respectively. For 10Hz bandwidth, corresponding values are 1µV p-p max and 20pA p-p. Figure 5A is a graph of noise vs. bandwidth for both current and voltage. Figure 5B is a spectral density plot for determining spot noise at any frequency. Figure 6 is a plot of peak to peak noise which will be encountered for these bandwidths, as a function of source resistance.

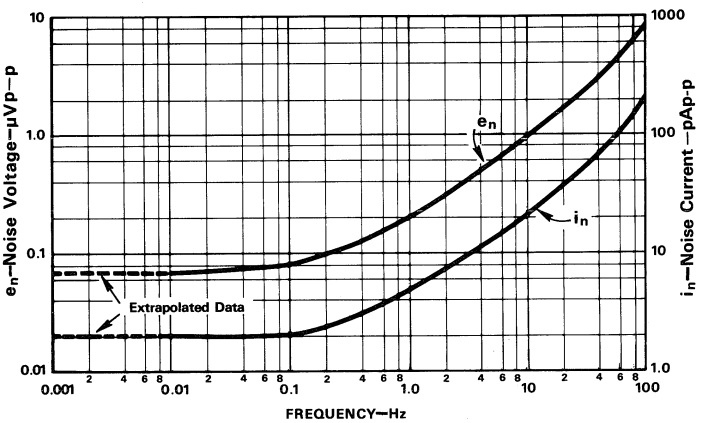


Figure 5A. Noise Current and Voltage vs. Bandwidth. Measured from 0.01Hz.

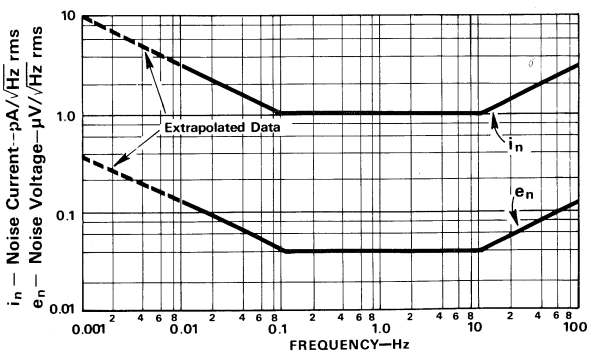


Figure 5B. Spectral Density of Current and Voltage

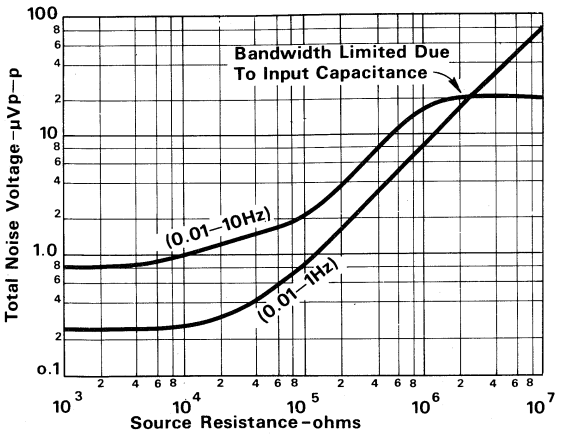


Figure 6. Total Noise vs. Source Resistance

preserving polarity information. The drift of the input stage is not present in the demodulated signal since it was not chopped by the input network. The demodulated signal is filtered and further amplified by the integrator connected output dc amplifier.

Using the system just described, the reamining drift and offset, referred to the amplifier input, is equal to the output dc amplifier stage input drift and offset divided by the ac-coupled amplifier's gain. If the output stage integrated circuit amplified had a 100μV/°C drift, and the ac-coupled amplifier gain is 1000, then the drift, referred to the input will be 0.1μV/°C (the specification for the model 261K). The same considerations apply for offset voltage, accounting for its low value and the excellent long term stability of this amplifier.

The chopping signal is generated by a standard multivibrator. The frequency is not critical, and the multivibrator circuit is protected against latch-up.

HOW THE MODEL 261 OPERATES

As shown in Figure 7, the model 261 consists of five specific circuit functions. The input signal is fed through a resistor to the MOSFET Chopper. When the MOSFET is off (high resistance), the error signal appears at the input to the ac-coupled amplifier. When the MOSFET transistor is on (low resistance), the input to this amplifier is reduced to near zero. The difference between the on and off voltages at the amplifier is a square wave of amplitude slightly less than the error voltage. The attenuating effect of the MOSFET Chopper's "on" resistance is negligible. For example, if the attenuation were as much as 10%, the only effect would be to lower the potential open loop gain of the amplifier by the same amount.

The ac-coupled amplifier, consisting primarily of a linear integrated circuit, amplifies the resulting chopper error signal. Its output is capacitively coupled into a synchronous demodulator which reconstructs the low frequency-dc input signal,

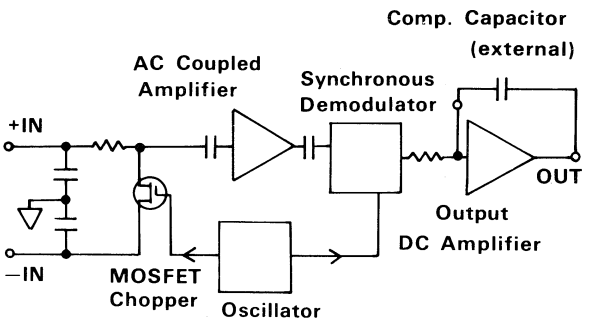


Figure 7. Model 261 Block Diagram

APPLICATION NOTES

Measurement of small signals or accurate handling of larger signals always requires care. Model 261 was specifically designed to minimize the problems raised by dc drift. To obtain best results, it is necessary to maintain good engineering practice and to observe a few requirements for optimizing performance of this precision instrument.

OFFSET VOLTAGE AND CURRENT TRIM

With the trim terminal connected to common, initial offset voltage of the model 261 is less than 25μV. An additional offset voltage is developed by the flow of the input bias current through the resistance of the signal source. With a 10,000 ohm source resistance and worst case bias current of 300pA, the maximum additional offset voltage would be only 3μV. For many applications, these offset voltages may be ignored, and the expense of a trim potentiometer and its adjustment is avoided. If the application requires lower offsets, an external 50,000 ohm trim potentiometer may be connected to zero the offset voltages, as shown previously. This trimming operation will not affect the drift or noise characteristics of the model 261.

INVERTING AND DIFFERENTIAL INPUT OPERATION

The input current to the amplifier's (–) terminal is less than ±10nA. Differential input operation of the amplifier is allowable, but the impedance from the inverting terminal to ground should not exceed 5000 ohms, and the common mode voltage range for best performance should not be exceeded. For purely inverting applications the user should select Analog Devices' models 234 or 235 chopper stabilized amplifiers, which are optimized for inverting operation.

SELECTABLE BANDWIDTH

For practical low-frequency applications, the model 261 uses an external compensation capacitor to determine the gain-bandwidth product. Its value may be chosen to allow the use of the maximum 100Hz –3dB bandwidth, at any given value of closed loop gain. By using a larger value of compensation capacitance, the bandwidth can be limited to any desired value below 100Hz, as required by the application. The minimum value of the required compensation capacitor, in μF, is 1000/GB, where G is the desired closed-loop dc gain, and B is the –3dB bandwidth. For example, the minimum value of recommended capacitance (for 100Hz bandwidth to –3dB) is

10/G. Shown in Figure 8 are curves of the amplifier's response for various closed loop gains while using values of capacitance appropriate for maintaining 100Hz (-3dB) bandwidth. Figure 9 illustrates the amplifier's open-loop response with various values of the compensation capacitor. It is recommended that the capacitor be polycarbonate, mylar, mica, glass or polystyrene for best performance.

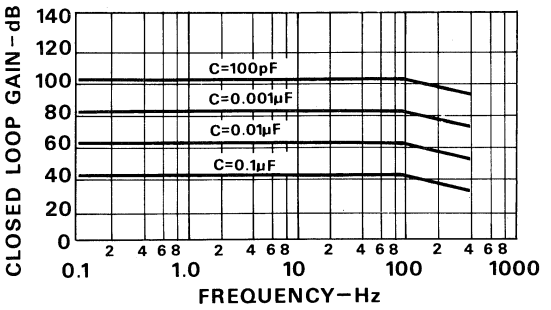


Figure 8. Compensation vs. Gain for 100Hz Bandwidth

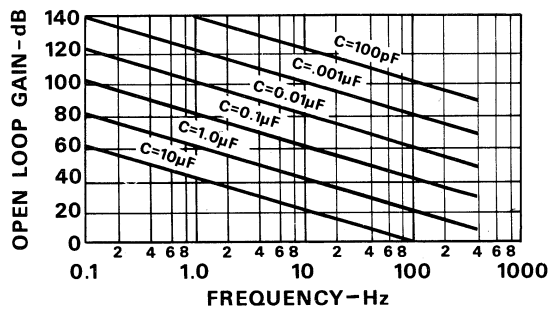


Figure 9. Open Loop Response vs. Compensation

FULL POWER RESPONSE

Full power output at any frequency can be obtained only with closed loop gains exceeding 10. This is due to the common mode voltage limitation described below.

The maximum full power output frequency is 50Hz, and will be obtained when using compensation capacitors of less than 0.013μF. For larger compensation capacitors, f_p is given by the formula:

$$f_p \text{ (Hz)} = 0.66/C \text{ (}\mu\text{F)}$$

When using a low gain, for instance 10, the maximum f_p will be 0.66Hz due to the 1.0μF required compensation capacitor for this closed loop gain. Under such conditions the user may wish to employ the compensation circuit of Figure 10. This will increase f_p to 5Hz (for a gain of 30). For higher gains, an increase in f_p will be obtained (with the same circuit), although the rise in f_p will not be proportionately as large.

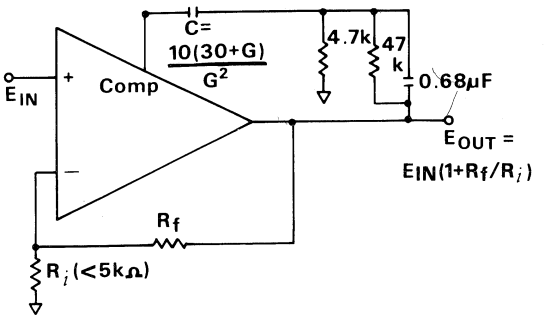


Figure 10. Compensation for Increased f_p

COMMON MODE CONSIDERATIONS

In the model 261, the maximum safe input voltage, both differential and common mode, exceeds ±20 volts. However, in order to maintain the specified Common Mode Rejection Ratio of 300,000 it is necessary that common mode voltage be limited to ±1.0 volts for the model 261K and ±0.5 volts for the model 261J. These values will not be exceeded by normal input signal swings if the amplifiers closed loop gain exceeds 10 and 20, respectively. Since most applications will use this amplifier at gains of 100 or more, the specified common mode range should prove entirely adequate.

COMMON MODE REJECTION

Model 261 is designed to provide high stability, high gain and low noise in non-inverting applications where the high input impedance minimizes input signal attenuation. Although operation as a differential amplifier is possible, it is not recommende

In the non-inverting mode, there is a source of error due to the common mode voltage; however this error term can be completely ignored since the error due to open loop gain will dominate.

INVERTING INPUT TERMINAL RESISTANCE (R_i)

An attempt should be made to maintain low resistance from the inverting input terminal to ground. This will prevent the negative input's bias current from degrading the offset performance of the amplifier. This restriction in no way relates to the source resistance seen by the positive (non-inverting) input terminal.

ANALOG DEVICES

Ultra Low Bias Current Varactor Bridge Operational Amplifiers

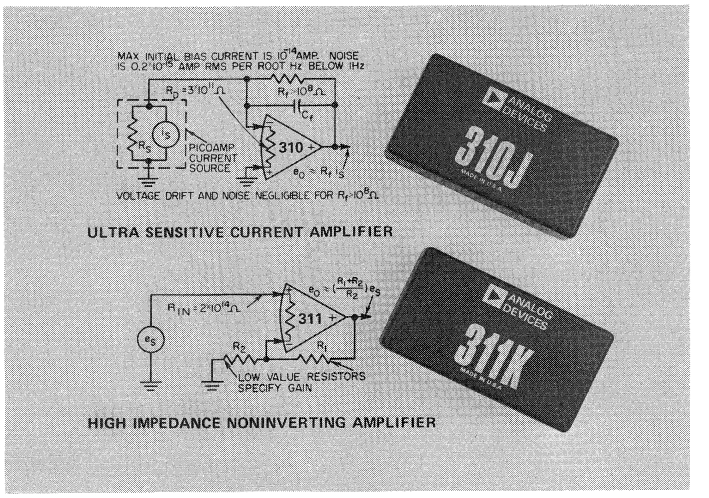
MODELS 310, 311

FEATURES

Guaranteed Low Bias: 10^{-14} A max
Low Voltage Drift: 10μV/°C max (310K, 311K)
Versatility: Noninverting, model 311J/K
Inverting, model 310J/K
High Input Impedance: $10^{14}\Omega$ (311J, 311K)

APPLICATIONS

Femtoammeter
Electrometer
Long-Time Integrator
Small-Rate Differentiator
Flame Current Detector
Phototube Amplifier
Log Compressor
pH Meter



GENERAL DESCRIPTION

The Analog Devices' models 310 and 311 are operational amplifiers with extremely low input bias currents and high input impedances. As such, they are applicable to a large number of *electrometer* amplifier applications which have traditionally been fulfilled (not without difficulty) by vacuum electrometer tubes. These specialized requirements are characterized by extremely high source impedances or where infinitesimal currents must be measured or amplified. Because of varactor bridge inputs, the all solid state 310 and 311 amplifiers are ideally suited to this type of requirement. Voltage drifts are small, noise is minimized, and the cost is low. In principle, the operation of varactor bridge amplifiers is similar to that of vibrating reed electrometers (parametric), but also includes the inherent advantages of solid state design.

VOLTAGE SOURCE OR CURRENT SOURCE?

Model 310 – The model 310 is designed such that the high quality signal input is the *inverting* input terminal, and is most appropriate for measurements of *current* signals. This type of signal source is common to gas chromatograph flame detectors, photomultiplier tubes, radiation detectors, etc. The inverting model 310 is also useful for logarithmic compression over an extremely wide dynamic range and in the construction of very-long-time-constant integrators or differentiators. Input signals from picoamps to milliamps may be accommodated with femtoamp current resolution.

Model 311 – The 311 is similar to the 310 but the high quality input is the positive or *non-inverting* input. It is primarily intended for measurement of voltages from very high source impedances. Such sources are found in the glass electrodes of pH cells and other scientific measurement apparatus. Another such source is charge stored on the plates of a capacitor, as is found in long-time track-and-hold applications.

Table 1. Comparison of Electrometer Types

TYPE	VARACTOR BRIDGE	VIBRATING CAPACITOR	MOSFET	ELECTROMETER TUBES
I–Stability	good	excellent	good	good
V-Stability	excellent	excellent	fair	poor
Bandwidth	narrow	narrow	wide	wide
Overload Protection	easy	easy	difficult	–
CMR	excellent	excellent	fair	poor
Microphonics	fair	fair	good	poor
Warm-Up	fast	fast	fast	slow
Size	small	large	small	large
Price	low	high	medium	medium

The chart above shows the relative advantages of various electrometer types. The best performance possible is given by the vibrating reed electrometer. It should be remembered, however, that this is a large, expensive laboratory instrument not generally suitable for instrument construction.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

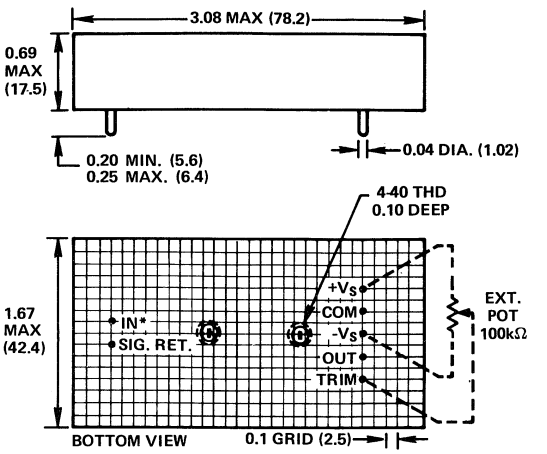
MODEL	310J/K	311J/K
OPEN LOOP GAIN		
DC 2kΩ Load	10^5 min	*
RATED OUTPUT		
Voltage, 2kΩ Load	±10V min	*
Current	±5mA min	*
Load Capacitance	up to 1nF	*
FREQUENCY RESPONSE		
Unity Gain, Small Signal	2kHz	*
Full Power Response	7Hz min	*
Slew Rate	0.4V/ms min	*
Overload Recovery	10ms	*
INPUT OFFSET VOLTAGE		
Initial, @ +25°C	±10mV max	*
With External Trim Pot	Adj. to zero	*
vs. Temp (0 to +70°C) max	±30μV/°C (J)	±30μV/°C (J)
	±10μV/°C (K)	±10μV/°C (K)
vs. Supply Voltage	±100μV/%	*
vs. Time	±100μV/mo	*
Warm-Up Drift	75μV (15 min)	*
INPUT BIAS CURRENT		
Initial Bias, +25°C		
Inverting Input	±10fA[2] max	±1nA max
Non-Inverting Input	±1nA max	±10fA max
vs. Temp (Signal Input Only)[1]	x 2/+7°C	*
vs. Supply Voltage (Signal Input Only)	±2fA/%	*
INPUT IMPEDANCE		
Differential	$3 \times 10^{11}\Omega \| 30pF$	*
Inverting Input (To Common)	–	$10^9\Omega \| 20nF$
Non-Inverting Input (To Common)	–	$10^{14}\Omega \| 2pF$
INPUT NOISE		
Voltage, 0.01 to 1Hz	10μV p-p	*
1 to 100Hz	10μV rms	*
Current, 0.01 to 1Hz	1fA p-p	*
1 to 100Hz	2fA rms	*
COMMON MODE CHARACTERISTICS		
Max Safe Differential Voltage	±300V	*
Max Common Mode	NA	±25V
Common Mode Rejection @ ±25V	NA	10^5
POWER SUPPLY		
Voltage, Rated Performance	±15V	*
Voltage, Operating	±(12 to 18)V	*
Current, Quiescent	+15, -6mA max	*
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +85°C	*
MECHANICAL		
Case Size	3" x 1.6" x 0.69"	*
Mating Socket	AC1017	*
Socket Shield	AC1118	*

[1] Negative input for 310, positive input for 311.
[2] 1fA (femtoamp) = 10^{-15}A.
*Specifications same as 310J/K.

Specifications subject to change without notice.

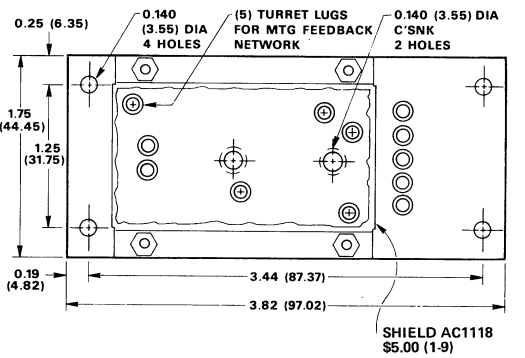
OUTLINE DIMENSIONS

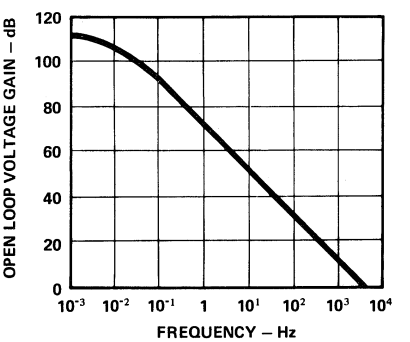
Dimensions shown in inches and (mm)



* = INVERTING INPUT (-IN), MODEL 310
NONINVERTING INPUT, (+IN), MODEL 311
WEIGHT: 150 grams

MATING SOCKET
AC1017





Open Loop Frequency Response

APPLICATION CONSIDERATIONS

The relatively large capacitance between inputs of varactor bridge amplifiers is a cause for stability problems when large feedback resistors are used. These stability problems can usually be cured at the expense of bandwidth by judiciously adding an external capacitor.

For the current amplifier (Figure 1) this capacitor, C_f, is added in parallel with R_f. A value of 0 to 5pF for C_f is normally required for the 310, but to optimize bandwidth a square wave should be applied at the input and C_f should be adjusted for the desired output transient response. Where bandwidth is not required, C_f should be increased to limit the bandwidth and thus reduce noise.

Note that bandwidth is sacrificed when C_f is made arbitrarily large since bandwidth is proportional to $1/R_fC_f$.

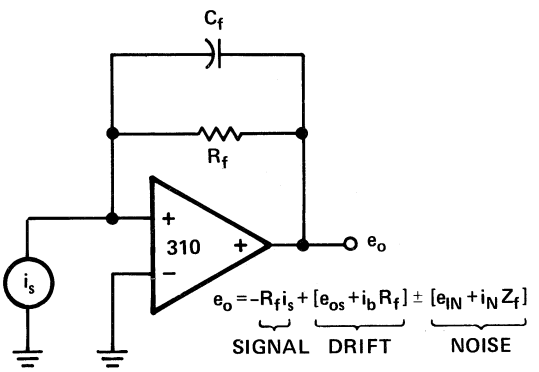


Figure 1. Improving Closed Loop Stability Inverting Configuration

To improve stability for the noninverting amplifier (Figure 2), a capacitor C_i is required from the plus input to ground. Although the value for C_i depends primarily on the source impedance, R_S, in most cases a few picofarads should be adequate. In this configuration the use of C_i degrades bandwidth since R_S and C_i form a low pass filter and reduce the dynamic input impedance.

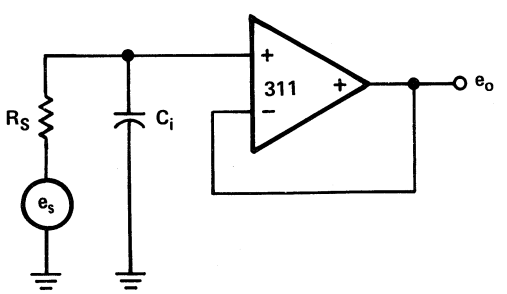


Figure 2. Improving Closed Loop Stability Noninverting Configuration

Remember when choosing a capacitor type that the leakage resistance of the capacitor can be very critical. The capacitor chosen should have at least 10^{14} ohms insulation. The type SX polystyrene capacitor manufactured by Mallory is suitable.

LEAKAGE RESISTANCE

In working with picoamp signals and/or impedance values in the range from 10^7 to 10^{11} ohms, attention to insulation and guarding techniques is extremely important. For example, a leakage resistance of 10^{14} ohms from the 15 volt power supply to the negative input of the 310 will cause a 150fA error current which is 15 times greater than the 10fA bias current guaranteed for this amplifier. The insulation resistance of most commercial wire, connectors, printed circuit boards, switches and other interconnection devices fall considerably short of 10^{14} ohms, particularly on a humid day. Teflon and ceramic are about the only reliable insulators in applications where one is serious about measuring fractions of picoamps or in obtaining maximum input impedance. Teflon wire and ceramic switches are available with acceptance insulator properties.

Analog Devices offers mating sockets for model 310 and model 311 amplifiers which use teflon-insulated receptacles.

HIGH VALUE RESISTORS

Frequently very large resistance values are required with the 300 series. Metal film resistors are recommended. One source of these resistors is Electra Mfg. Co.* which specializes in metal film resistors which are available up to 10^7 ohms. A source for higher value resistors is Victoreen.** This firm offers special carbon resistors up to 10^{14} ohms. The high value carbon resistors have a relatively large temperature coefficient, about 1000ppm, and the tolerance of resistance values is 1 to 10%. Moreover, these devices also have a substantial voltage coefficient, which means that the resistance will vary with applied voltage, particularly for large voltages; also, the long term stability is poor. As a rule, degradation in performance increases with increasing resistance value.

By contrast, metal film resistors have much better coefficients, about 100ppm, accuracy to 0.1%, and better long term stability.

From this discussion it is apparent that smaller errors due to feedback resistors are obtained with lower resistance values. Figure 3 shows a technique for circumventing the use of very large value resistors for a current amplifier.

This circuit multiplies the effective value of R_1, by the ratio $(R_2 + R_3)/R_2$. For example, if one requires a sensitivity of 10mV/pA, the value for R_f in Figure 1 (Inverting Configuration) would be 10^{10} ohms. However, in Figure 3, the same sensitivity is obtained when $R_1 = 10^8$ ohms and $(R_2 + R_3)/R_2 = 100$. Reasonably well behaved resistors of 10^8 are available.

*Address: 3151 Fiberglas Rd., Kansas City, Kansas 66115.
**Address: 10101 Woodland Ave., Cleveland, Ohio 44114.

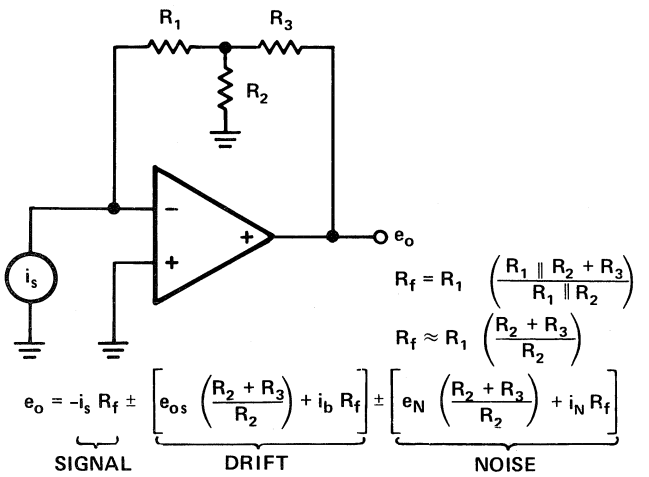


Figure 3. Current Amplifier with Voltage Divider Feedback

On the other hand, the noise and drift of the circuit in Figure 3 is greater than that of Figure 1 for a given sensitivity. This follows from the fact that voltage noise and drift are amplified by the ratio $(R_2 + R_3)/R_2$ when referred to the output. We can see this by comparing the output noise and drift equation of Figure 1 and 3 for a given sensitivity (that is, $R_f = R_1(R_2 + R_3)/R_2$ and assuming $R_1 >> R_2$ and source resistance is infinite).

Johnson noise from the feedback resistor is also greater for the configuration of Figure 3 than for Figure 1.

IMPROVED LARGE SIGNAL RESPONSE

The full power response, slewing rate and/or open loop gain of the model 310 and 311 can be improved by cascading an inexpensive op amp like our model 118 or possibly an integrated circuit like the AD308 to the output. In this way, the output voltage swing of the 310 or 311 is decreased so that the full power response and slewing rate limitations are proportionally improved; and the 310 or 311 can be operated near unity gain, so maximum loop gain is available. To avoid stability problems, it is simpler to connect the output amplifier separately (that is, not inside the feedback loop of the 310 or 311) with a closed loop gain of 10 to 100.

RFI AND OTHER NOISE PROBLEMS

Since the input circuit of the varactor bridge amplifier operates at a high frequency carrier signal, a low frequency beat signal can appear in the output due to pick up of radio broadcast signals near the carrier frequency or due to interference between the oscillators of multiple amplifiers connected in a single system.

In general, properly shielded wiring will eliminate RFI pickup; however, one or more additional steps can be taken to further improve any such problems: (See Figure 4)

1) Decouple the power supply leads at or near the amplifier terminals.
2) Add a one megohm resistor in series with the minus input of the 310. (Unfortunately this will reduce the signal bandwidth by about a factor of 10).
3) Add a filter network to the non-inverting input of the 311.

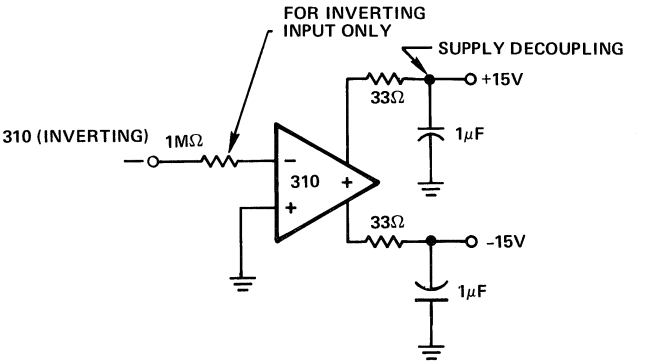


Figure 4A. Improving RFI Noise - 310

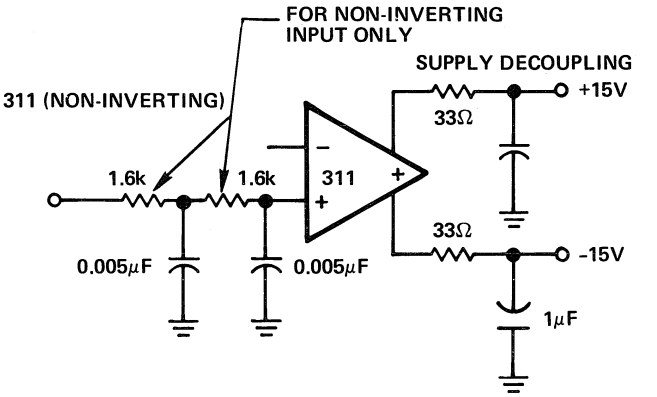


Figure 4B. Improving RFI Noise - 311

Feedback through the power supply will be the major source of interference for multiple amplifier connections. This can be remedied by running separate leads from the power supply to each amplifier and by connecting a 1μF tantalum capacitor from the plus and minus supply terminals to common on each amplifier. Ground loops may also cause a problem, which can usually be solved by experimenting with the grounding system – keeping the grounds for each amplifier completely separate. Where a common source is used to feed several amplifiers, you should first experimentally work out the best grounding scheme and as a last resort add a one megohm resistor in series with each amplifier input and suffer the resulting loss of bandwidth.

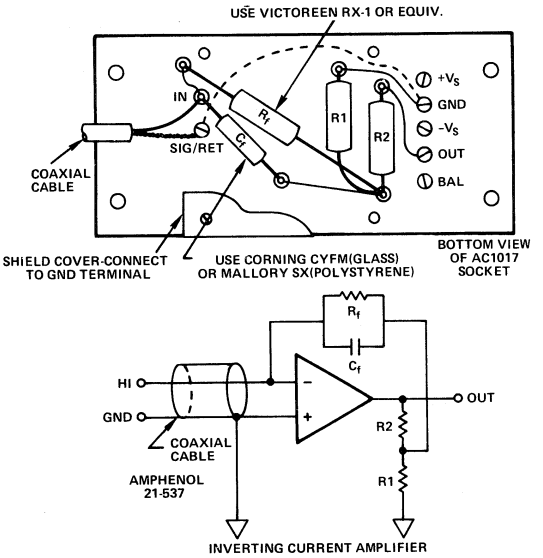
INSTALLATION NOTES

Because of the phenomenal sensitivity of models 310 and 311, they must be installed and used with more care than is required for more conventional operational amplifiers.

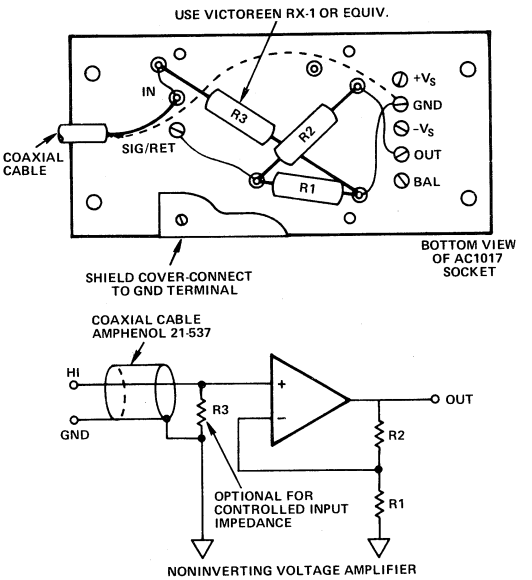
Insulation and shielding of all components and wiring associated with the "hot" input terminal (inverting input of model 310, non-inverting input of model 311) must be near perfect. Insulators of clean teflon are preferable, but polyethylene, or glass types are also suitable. Dirt and moisture do not adhere to teflon, but if required it may be cleaned with methy alcohol.

Models 310 and 311 are enclosed in metal-shielded cases. The mating socket provides stand-off insulators for mounting resistors and/or capacitors connected to the hot input. A metal shield model AC1118 is also available for complete shielding of the circuitry. Where the hot input terminals must be connected to a signal source outside the shield, a coaxial cable with a graphite coating between insulation and braid should be used. This type is required to minimize the generation of noise currents due to any changes in the relative position of shield and conductor. Amphenol type 21-537 is suitable.

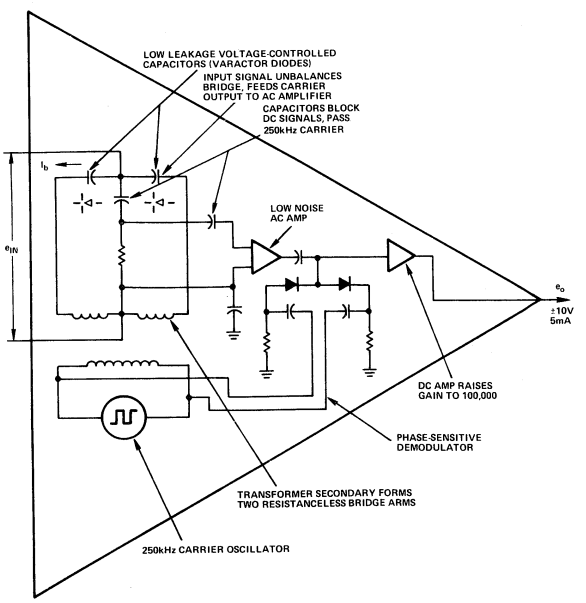
Changes in capacity across a high-impedance voltage source cause voltage fluctuations. For this reason, wiring should be rigid, as short as possible, and spaced as far from other objects as possible. Similarly, current fluctuations result from the motion of a conductor in an electrostatic field. The same precautions are effective.



Connection Diagram for Model 310
Used with AC1017 Socket



Connection Diagram for Model 311
Used with AC1017 Socket



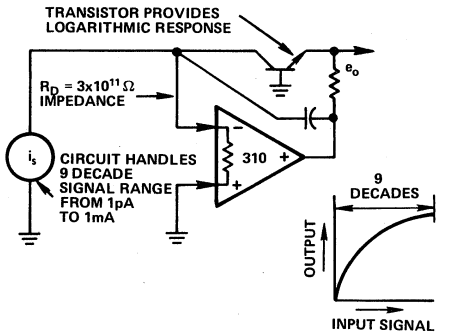
HOW VARACTOR BRIDGE AMPLIFIERS WORK

Amplifier input, e_{IN}, varies varactor capacitances, unbalances bridge, and develops pump voltage output proportional to bridge unbalance.

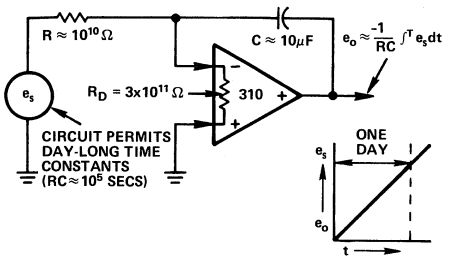
After low noise ac amplification, the output pump voltage is phase-sensitively demodulated to restore correct polarity, then further boosted by the dc amplifier.

Final output is a replica of the original signal, amplified by the open loop gain.

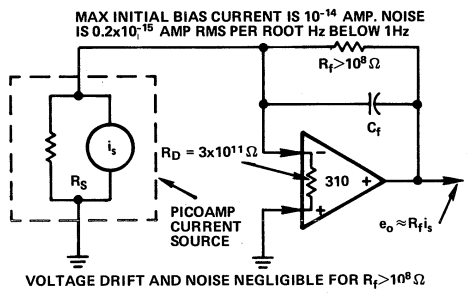
Matched low leakage varactors inherently eliminate 1/f noise, give excellent offset and drift specs, and provide 3×10^{11} ohms differential input impedance. Transformer coupling is responsible for the amplifier's advanced common mode characteristics.



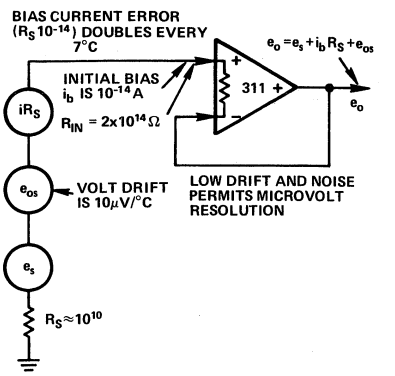
Nine Decade Logarithmic Amplifier



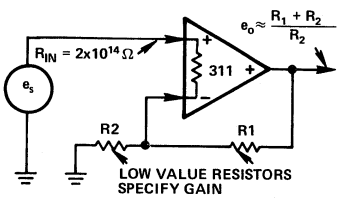
Long Term Integrator



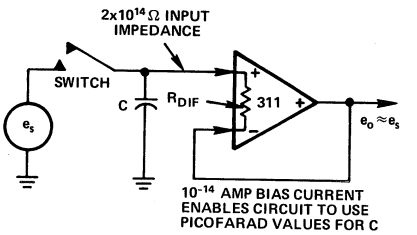
Ultra Sensitive Current Amplifier



Ultra High Impedance Buffer



High Impedance Noninverting Amplifier



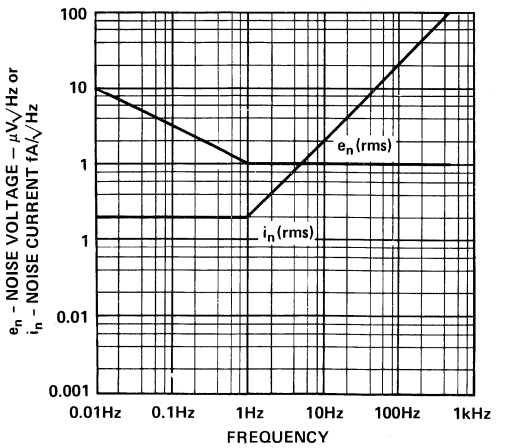
Low Capacitance Sample-Hold Amplifier

MODEL 310 (INVERTING)

Applications where the high sensitivity of the 310 as a current amplifier is important include flame detectors, photomultiplier tubes, semiconductor testing, ionization detectors, vacuum gauges and reactor controls. The low bias current of the 310 is also useful in long term, high accuracy integrators or as a nine decade logarithmic amplifier.

MODEL 311 (NONINVERTING)

The model 311 is primarily useful as a high input impedance voltage follower for unloading high source impedances. Typical applications are sample-and-hold and pH amplifiers and/or measuring other chemical reactions.



Calculated Noise Per Root Hertz

Instrumentation Amplifiers

An instrumentation amplifier is a committed "gain block" that measures the difference between the voltages existing at its two input terminals, amplifies it by a precisely set gain – usually from 1V/V to 1000V/V or more – and causes the result to appear between a pair of terminals in the output circuit. Referring to Figure 1,

$$V_S - V_R = G\,(V^+ - V^-)$$

An ideal instrumentation amplifier responds only to the *difference* between the input voltages. If the input voltages are equal ($V^+ = V^- = V_{CM}$, the *common-mode voltage*), the output of the ideal instrumentation amplifier will be zero.

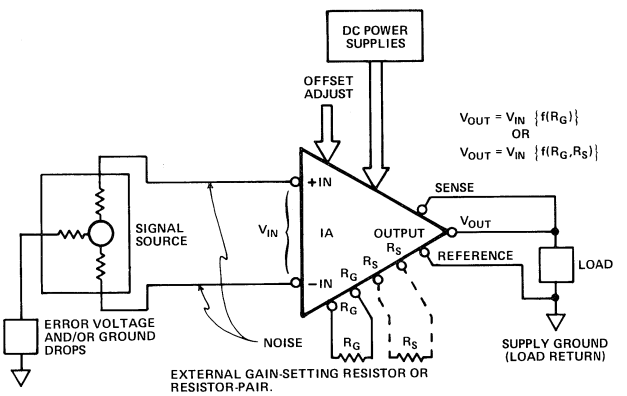


Figure 1. Basic Instrumentation Amplifier Functional Diagram

An amplifier circuit which is optimized for performance as an instrumentation-amplifier gain block has high input impedance, low offset and drift, low nonlinearity, stable gain, and low effective output impedance. It is commonly used for applications which capitalize on these advantages. Examples include: transducer amplification – for thermocouples, strain-gage bridges, current shunts, and biological probes, preamplification of small differential signals superimposed on high common-mode voltages, signal conditioning and (moderate) isolation for data acquisition, and signal translation for differential and single-ended signals wherever the common "ground" is noisy or of questionable integrity.

Instrumentation-amplifier modules and IC's are usually chosen in preference to user-assembled op-amp circuitry, because they offer optimized, specified performance in low-cost, easy-to-use, compact packages. If the application calls for high common-mode voltages (typically, voltages in excess of the amplifier supply voltage), or if isolation impedances must be very high (e.g., $10^{10}\,\Omega$, with galvanic isolation, as in medical and industrial applications), the designer should consult the *Isolator* section of this catalog, starting on page 125.

SPECIFYING INSTRUMENTATION AMPLIFIERS

The instrumentation amplifier chosen for a given application will be the lowest-cost device that satisfies the performance and environmental requirements. A Selection Guide to Analog Devices instrumentation amplifiers recommended for new designs is provided on page 108. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; they are listed on page 599. Data sheets are available upon request. It is essential that the designer have a firm understanding of the specifications of instrumentation amplifiers and of the contributions of the various sources of error to the total error. The data sheets provide much useful application data on these devices, as well as examples of basic error analyses.

Definitions of the key specifications follow a brief discussion of instrumentation-amplifier architectures. For more-complete information on the fundamentals and applications of instrumentation amplifiers, a number of publications are available from Analog Devices upon request.[1,2,3]

INSTRUMENTATION-AMPLIFIER ARCHITECTURE

All Analog Devices instrumentation amplifiers have two high-impedance input terminals, a set of terminals for gain-setting resistance, an "output" terminal, and a pair of feedback terminals, labeled *sense* and *reference*, as well as a set of power-supply terminals and offset-trim terminals.

Two basic circuit concepts are employed. The AD522, 606, and 610 use variations of the well-known three-op-amp configuration (Figure 2), consisting of a differential input-output gain stage and a subtractor stage. Gain ($\geqslant$1V/V) is set by the choice of a single external gain-setting resistor, R_G. Its nominal value is $\frac{400{,}000}{G-1}\,\Omega$, for the 606 and the 610, and $\frac{200{,}000}{G-1}\,\Omega$, for the AD522. When the *sense* (V_S) feedback terminal is connected to the output terminal and the *reference* terminal (V_R) is connected to power common, the output voltage appears between the output terminal and power common.

[1] "Application Guide to Precision Measurement Using Instrumentation and Isolation Amplifiers" (Summer, 1978)

[2] "Isolation and Instrumentation Amplifiers Designer's Guide, 1978 edition

[3] "A User's Guide to IC Instrumentation Amplifiers," by J. Riskin, 1978

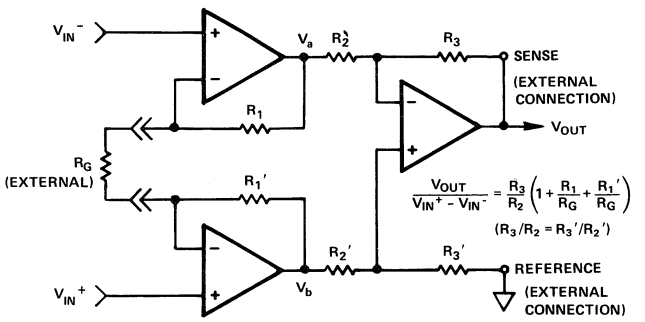


Figure 2. "Classic" 3 Op Amp Instrumentation Amplifier

The second circuit approach, employed in the case of the monolithic AD521 (Figure 3), employs two differential-input follower pairs to generate the currents, $\frac{V_1 - V_2}{R_G}$, and $\frac{V_S - V_R}{R_S}$. The current difference is applied to a control amplifier, and, with the feedback loop closed (for example, V_S to the output terminal and V_R to system ground or the supply midpoint), the currents are servoed to be equal, and the nominal gain is thus equal to the ratio, R_S/R_G, making possible a wide range of gain, including gains of less than unity.

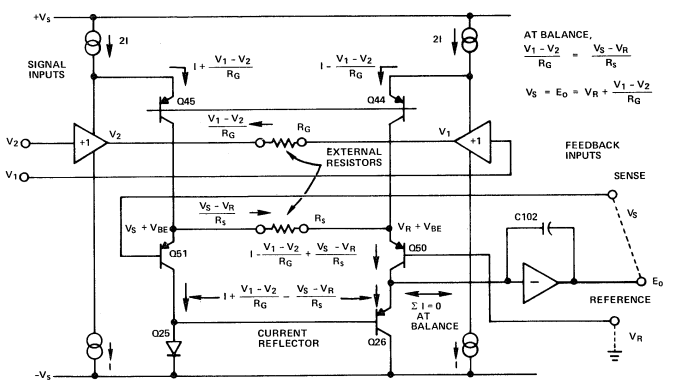


Figure 3. Simplified Schematic Diagram of the AD521 Instrumentation Amplifier

The V_S and V_R terminals may be used for remote sensing — to establish precise outputs in the presence of line drops; they may be used with an inside-the-loop booster follower to obtain power amplification without loss of accuracy; and they may be used to establish an output current that is precisely proportional to the difference signal. A voltage applied to the V_R terminal will bias the output by a predetermined amount. It is important always to maintain very low impedance (in relation to the specified V_S and V_R input impedances), when driving the V_S and V_R inputs, in order not to introduce common-mode, gain, and/or offset errors. In devices using the 3-amplifier configuration, the V_R terminal is sometimes used for "tweaking" common-mode rejection.

SPECIFICATIONS

Specification tables are generally headed by the legend: "specifications are typical at $V_S = \pm 15V$, $T_A = +25°C$, and rated load, unless otherwise noted." This tells the user that these are the normal operating conditions under which the device is tested. Deviations from these conditions might degrade (or improve) performance. When deviations from the "normal" conditions are likely (such as a change in temperature), the significant effects are usually indicated within the specs. "Typical" means that the manufacturer's characterization process has shown this number to be "average," but individual devices vary.

Specifications not discussed in detail are self-explanatory and require only a basic knowledge of electronic measurements. Such specs are not uniquely applicable to instrumentation amps.

GAIN These specifications refer to the linear transfer function of the device; for example, the AD522 gain equation is: $G = 1 + \frac{200{,}000}{R_G}$ V/V. The value of R_G for a given gain value is:

$R_G = \frac{200{,}000}{G - 1}\Omega$. For example, if G is to be 100 V/V,

$R_G = 2020.2$ ohms.

Gain Range Specified at 1 to 1000, for example, the device may work at higher gains (1 V/V is minimum, except for the AD521), but the manufacturer does not specify performance outside the range. In practice, noise and drift may make higher gains impractical for a given device.

Equation Error (or "Gain Accuracy") The number given by this specification describes deviation from the gain equation when R_G is at its nominal value. The user can trim the gain or compensate for gain error elsewhere in the overall system. Systems using microprocessors (or computers, or other digital "intelligence") can be made self-calibrating, to take into account the lumped gain errors of all the stages in the analog portion of the system, from transducer to a/d converter.

Nonlinearity (or Gain Nonlinearity) Nonlinearity is defined as the deviation from a straight line on the plot of output vs. input. The magnitude of linearity error is the maximum deviation from a "best straight line," with the output swinging through its full-scale range. Nonlinearity is usually specified in percent of full-scale output range.

Gain vs. Temperature These numbers give the deviations from the gain equation as a function of temperature.

SETTLING TIME is defined as that length of time required for the output voltage to approach and remain within a certain (±)

tolerance of its final value. It is usually specified for a fast step that will drive the output through its full-scale range and includes slewing time. Since several factors contribute to the overall settling time, fast settling to 0.1% does not necessarily mean proportionally fast settling to 0.01%, nor is settling time necessarily proportional to gain. Principal contributing factors include slew-rate limiting, underdamping (ringing), and thermal gradients ("long tails").

VOLTAGE OFFSET Voltage offset and common-mode rejection (see below) specifications are often considered the key figures of merit for instrumentation amplifiers. While initial offset can be adjusted to zero, shifts in offset voltage with time and temperature introduce errors. Systems that involve "intelligent" processors can correct for offset errors in the whole measurement chain, but such applications are still relatively infrequent; in most applications, the instrumentation amplifier's contribution to system offset error must be defined.

Voltage offset and offset drift in instrumentation amplifiers are functions of gain.[4] The offset, measured at the output, is equal to a constant plus a term proportional to gain. For an amplifier with specified performance over a gain range from 1 to 1000, the constant is essentially the offset at unity gain, and the proportionality term (or slope) is equal to the change in output offset between G = 1 and G = 1000, divided by 999. To refer offset to the input (RTI), divide the total output offset by the gain. Since offset at a gain of 1000 is dominated by the proportional term, the slope is often called the "RTI offset, G = 1000." At any value of gain, the offset is equal to the unity-gain offset plus the product of the gain and the "RTI offset, G = 1000".

The same considerations apply to the offset drift. For example, the maximum RTI drift of the AD522B is specified at 25μV/°C at G = 1, 2μV/°C at G = 1000, and $(\frac{25}{G} + 2)$ μV/°C at any arbitrary gain in the range. Thus, the output drift is (25 + 2G)μV/°C at any gain, G, in the range. The data sheets provide offset-vs.-gain plots, but the function is easily computed in the manner described above.

Voltage offset as a function of power supply level is also specified RTI at one or more gain settings.

INPUT BIAS AND OFFSET CURRENTS Input bias currents are those currents needed to bias the input transistors of a dc amplifier or to supply the junction-leakage of FET's. FET-input devices have lower bias currents than those using bipolar transistors, but FET leakage currents increase dramatically with temperature, approximately doubling every 11°C. Since bias currents can be considered as a source of voltage offset (when multiplied by source resistance), the change in bias currents is of more concern than the magnitude of the bias currents. Input offset current is the difference between the two input bias currents.

Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying outputs of "floating" sources, such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to common. If a dc return path is impracticable, an *isolator* must be used (see page 126).

COMMON-MODE REJECTION (CMR) is a measure of the change in output voltage when both inputs are changed by equal amounts. CMR is usually specified for a full-range common-mode voltage change (CMV), at a given frequency, and a specified imbalance of source impedance (e.g. 1kΩ source unbalance, at 60Hz). CMR is a logarithmic expression of the *common-mode rejection ratio* (CMRR): CMR = 20 $\log_{10}$ (CMRR). The common-mode rejection ratio is defined as the ratio of the signal gain, G, to the ratio of common mode signal appearing at the output to the input CMV.

In most instrumentation amplifiers, the CMR increases with gain, because the front-end configuration does not amplify common-mode signals, and the amount of common-mode signal appearing at the output stary relatively constant as the signal gain (G) increases.

However, at higher gains, amplifier bandwidth decreases. Since differences in phase shift through the differential input stage will show up as common-mode errors, CMR becomes more frequency-dependent at high gains.

[4] There is a good explanation of the specification of offset in instrumentation amplifiers in ANALOG DIALOGUE 6–2 (1972), p. 14

Selection Guide
Instrumentation Amplifiers

	606J/K/L/M Module	AD522A/B/S Hybrid IC	610J/K/L Module	AD521J/K/S Monolothic IC
Nominal Gain Range	1 to 10,000V/V	1 to 1000	1 to 10,000V/V	1 to 1000V/V
Gain Tempco, ppm/°C	±15 max	2 max, G = 1 50 max, G = 1000	±15 max	3/3/15, G = 1 53/53/415, G = 1000
Nonlinearity, max (G = 100)	0.002%	0.01%/0.005%/0.005%	0.01%	0.2%
Offset Tempco RTI, μV/°C				
G = 1	200/150/100/75 max	50/25/100 max	200/150/150	400/150/150 max
G = 1000	2/1/0.5/0.25 max	6/2/6 max	3/1/0.5 max	15/5/5 max
I_{BIAS}, nA max	+60	±25/15/25	+60	80/40/40
I_{BIAS} Tempco	-0.2nA/°C	±100/50/100pA/°C	-0.2nA/°C	1/0.5/0.5nA/°C max
I_{OS}, nA	±1	±20/10/20 max	±5	20/10/10 max
I_{OS} Tempco, pA/°C	±20	±100/50/100	±20	250/125/125 max
Noise, RTI, 0.1Hz - 10Hz, μV p-p				
G = 1	40(0.01 – 10Hz)	15	50(0.01 – 10Hz)	225
G = 1000	1 max (0.01 – 10Hz)	1.5	2.5/2/2 max (0.01 – 10Hz)	0.5
CMR at rated CMV				
1kΩ Unbalance, Frequency:	DC to 100Hz	DC to 30/10/1Hz*	DC to 100Hz	DC to 60Hz
G = 1, dB min	60	75/80/75	60	70/74/74
G = 10, dB min	80	90/95/90	80	90/94/94
G = 100, dB min	86	100	86	100/104/104
G = 1000, dB min	90	100/110/100	90	100/110/110
Small-Signal Frequency Range (±1% Gain Error), typ.				
G = 100	100kHz (-3dB)	3kHz, -3dB	100kHz (-3dB)	24kHz
Settling Time to 0.1%, ±10V Output Step				
G = 100	30μs	5ms	30μs	10μs
Temperature Range†	C	I/I/M	C	C/C/M
Page	117	113	121	109

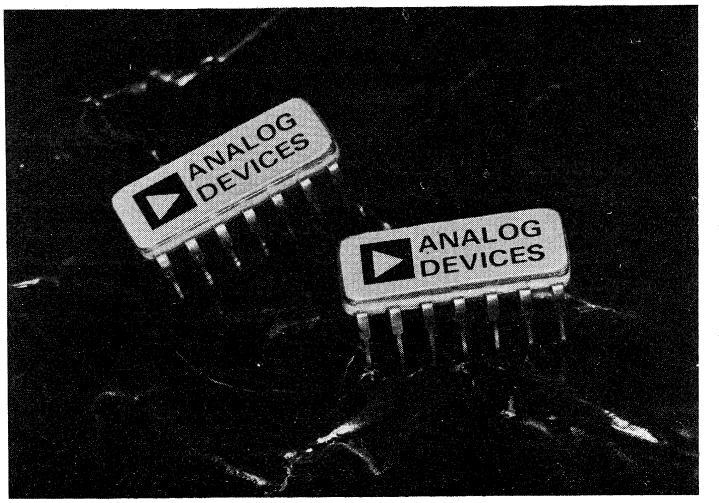
*G = 1 to 1000, DC to 60Hz: 75/80/75dB for A/B/S
†C: 0 to +70°C, I: -25°C to +85°C; M: -55°C to +125°C

Integrated Circuit Precision Instrumentation Amplifier

AD521

FEATURES

Programmable Gains from 0.1 to 1000
Floating Differential Inputs
High CMRR: 110dB min
Complete Input Protection, Power ON and Power OFF
Functionally Complete with the Addition of Two Resistors
Internally Compensated
Gain Bandwidth Product: 40MHz
Output Current Limited: 25mA
Extremely Low Cost



PRODUCT DESCRIPTION

The AD521 is the second generation, low cost, monolithic IC instrumentation amplifier developed by Analog Devices. A true instrumentation amplifier, the AD521 is a controlled gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521, like its predecessor the AD520, should not be confused with an operational amplifier, even though several manufacturers (including Analog Devices) offer op amps that can be used as building blocks in variable gain instrumentation amplifier circuits. An op amp is merely a high gain component requiring the addition of external feedback to complete the amplification function. Because of the limitations of resistor matching in the external feedback circuit and the relatively low input impedance resulting from the input resistors, an instrumentation amplifier circuit designed around op amps frequently provides less than satisfactory performance. Since the AD521 is a complete amplification circuit which does not depend upon external resistor matching for input/output isolation it maintains its high CMRR (110dB min) in any application. In addition, the high impedance inputs are fully protected against over voltages up to 15V greater than the supply voltage.

The AD521 can be operated at gains from 0.1 to greater than 1000 with the addition of only two programming resistors. Excellent dc characteristics are realized through the device's inherently low offset and gain drift and optional one-pot nulling. Dynamic performance is also outstanding with a gain bandwidth product of 40MHz, full peak response of 100kHz and a 10V/μs slew rate.

The AD521 IC instrumentation amplifier is available in three different versions, depending on accuracy and operating temperature range: the economical "J" specified from 0 to +70°C, the low drift "K", also specified from 0 to +70°C and the "S", guaranteed over the full MIL-temperature range, -55°C to +125°C. All versions are packaged in a 14 pin DIP.

PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
3. The AD521 is fully protected for input levels up to 15V beyond the supply voltage and 30V differential at the inputs.
4. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
5. Offset nulling can be achieved with an optional trim pot.
6. The AD521 offers superior dynamic performance with a gain bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5μs to 0.1% of a 10V step.
7. Every AD521 is baked for 40 hours at +150°C and temperature cycled ten times from -65°C to +150°C.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = 25°C unless otherwise specified)

MODEL	AD521J	AD521K	AD521S
GAIN			
Range (For Specified Operation. Note 1)	1 to 1000	*	*
Equation	$G = R_S/R_G V/V$	*	*
Error from Equation	(±0.25−0.004G)%	*	*
Nonlinearity (Note 2)			
1≤G≤1000	0.1% max	*	*
Gain Temperature Coefficient	±(3 ±0.05G)ppm/°C	*	±(15 ±0.4G)ppm/°C
OUTPUT CHARACTERISTICS			
Rated Output	±10V, ±10mA min	*	*
Output at Maximum Operating Temperature	±10V @ 5mA min	*	*
Impedance	0.1Ω	*	*
DYNAMIC RESPONSE			
Small Signal Bandwidth (±3dB)			
G = 1	>2MHz	*	*
G = 10	300kHz	*	*
G = 100	200kHz	*	*
G = 1000	40kHz	*	*
Small Signal, ±1.0% Flatness			
G = 1	75kHz	*	*
G = 10	26kHz	*	*
G = 100	24kHz	*	*
G = 1000	6kHz	*	*
Full Peak Response (Note 3)	100kHz	*	*
Slew Rate, 1≤G≤1000	10V/μs	*	*
Settling Time (any 10V step to within 10mV of Final Value)			
G = 1	7μs	*	*
G = 10	5μs	*	*
G = 100	10μs	*	*
G = 1000	35μs	*	*
Differential Overload Recovery (±30V Input to within 10mV of Final Value) (Note 4)			
G = 1000	50μs	*	*
Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5)			
G = 1000	10μs	*	*
VOLTAGE OFFSET (may be nulled)			
Input Offset Voltage (V_{os_1})	3mV max (2mV typ)	1.5mV max (0.5mV typ)	**
vs. Temperature	15μV/°C max (7μV/°C typ)	5μV/°C max (1.5μV/°C typ)	**
vs. Supply	3μV/%	*	*
Output Offset Voltage (V_{os_0})	400mV max (200mV typ)	200mV max (30mV typ)	**
vs. Temperature	400μV/°C max (150μV/°C typ)	150μV/°C max (50μV/°C typ)	**
vs. Supply (Note 6)	$0.005V_{os_0}$/%	*	*
INPUT CURRENTS			
Input Bias Current (either input)	80nA max	40nA max	**
vs. Temperature	1nA/°C max	500pA/°C max	**
vs. Supply	2%/V	*	*
Input Offset Current	20nA max	10nA max	**
vs. Temperature	250pA/°C max	125pA/°C max	**
INPUT			
Differential Input Impedance (Note 7)	$3 \times 10^9 \Omega \| 1.8pF$	*	*
Common Mode Input Impedance (Note 8)	$6 \times 10^{10} \Omega \| 3.0pF$	*	*
Input Voltage Range for Specified Performance	±10V	*	*
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	*	*
Voltage at either input (Note 10)	V_S ±15V	*	*
Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance			
G = 1	70dB min (74dB typ)	74dB min (80dB typ)	**
G = 10	90dB min (94dB typ)	94dB min (100dB typ)	**
G = 1000	100dB min (104dB typ)	104dB min (114dB typ)	**
G = 1000	100dB min (110dB typ)	110dB min (120dB typ)	**
NOISE			
Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10)	$\sqrt{(0.5G)^2 + (150)^2}\,\mu V$	*	*
RMS RTO, 10Hz to 10kHz	$\sqrt{(1.2G)^2 + (30)^2}\,\mu V$	*	*
Input Current, rms, 10Hz to 10kHz	15pA(rms)	*	*
REFERENCE TERMINAL			
Bias Current	3μA	*	*
Input Resistance	10MΩ	*	*
Voltage Range	±10V	*	*
Gain to Output	1	*	*
POWER SUPPLY			
Operating Voltage Range	±5 to ±18	*	*
Quiescent Supply Current	5mA max	*	*
TEMPERATURE RANGE			
Specified Performance	0 to +70°C	*	−55°C to +125°C
Operating	−25°C to +85°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*

*Specification same as AD521J.
**Specification same as AD521K.

Specifications and prices subject to change without notice.

NOTES:

1. Gains below 1 and above 1000 are realized by simply adjusting the gain setting resistors. For best results, input voltage should be restricted to ±10V for gains equal to or less than 1.

2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output of ±9 volts to 18 volts. With a combination of high gain and ±10 volt output swing, distortion may increase to as much as 0.3%.

3. Full Peak Response is the typical frequency below which the amplifier will produce full output swing.

4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10μs pulse at a 1kHz rate. (When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, and an added thermal time constant, but will not damage the device.)

5. Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is 30V, 10μs pulse at a 1kHz rate. (When a common mode signal greater than V_S - 0.5V) is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, and an added thermal time constant, but will not damage the device.)

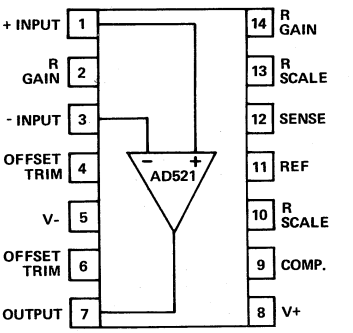
6. Output Offset Voltage versus Power Supply Change is a constant 0.005 times the unnulled output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.

7. Differential Input Impedance is the impedance between the two inputs.

8. Common Mode Input Impedance is the impedance from *either* input to the power supplies.

9. Maximum Input Voltage (differential or at either input) is 30V when using ±15V supplies. A more general specification is that neither input may exceed either supply (even when V_S = 0) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)

10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise observed during 2 of 3 separate 10 second periods with the test circuit of Figure 6.



TOP VIEW

Figure 1. AD521 Pin Configuration

TO-116

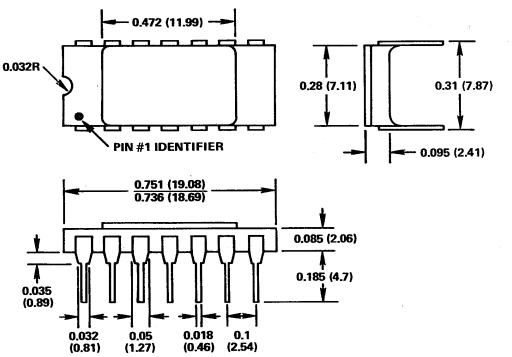


Figure 2. Physical Dimensions. Dimensions shown in inches and (mm).

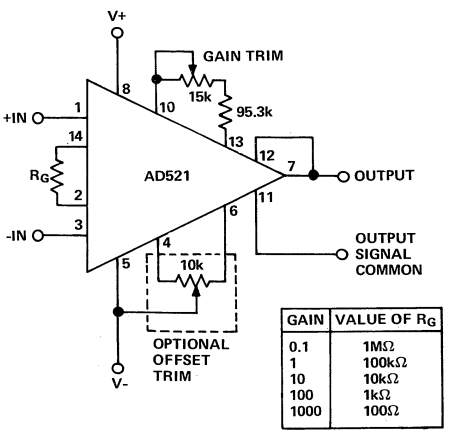


Figure 3. Operating Connections for AD521

INPUT OFFSET AND OUTPUT OFFSET

When specifying offsets and other errors in an operational amplifier, it is often convenient to refer these errors to the inputs. This enables the user to calculate the maximum error he would see at the output under any gain or circuit configuration. An op amp with 1mV of input offset voltage, for example, would produce 1V of offset at the output in a gain of 1000 configuration.

In the case of an instrumentation amplifier, where the gain is controlled in the amplifier, it is more convenient to separate errors into two categories. Those errors which simply add to the output signal and are unaffected by the gain, can be classi-

fied as output errors. Those which act as if they are associated with the input signal, such that their effect at the output is proportional to the gain, can be classified as input errors.

As an illustration, a typical AD521 might have a +30mV output offset and a -0.7mV input offset. In a unity gain configuration, the *total* output offset would be +29.3mV or the sum of the two. At a gain of 100, the output offset would be -40mV or: 30mV + 100(-0.7mV) = -40mV.

By separating these errors, one can evaluate the total error independent of the gain settings used, similar to the situation with the input offset specifications on an op amp. In a given gain configuration, both errors can be combined to give a total error with respect to either the input or output by the following formulae:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain x input error) + output error

As shown in Figure 4, the gain range on the AD521 can be extended considerably by adding an attenuator in the sense terminal feedback path (as well as adjusting the ratio, R_S/R_g). Since the sense terminal is the inverting input to the output amplifier, the additional gain to the output is controlled by R_1 and R_2. This gain factor is $1 + R_2/R_1$.

Where offset errors are critical, a resistor equal to the parallel combination of R_1 and R_2 should be placed between pin 11 and V_{REF}. This minimized the offset errors resulting from the input currents at the sense terminal flowing in R_1 and R_2. Note that gain changes introduced by changing the R_1/R_2 attenuator will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

When a predetermined output offset is desired, V_{REF} can be placed in series with pin 11. This offset is then multiplied by the gain factor $1 + R_2/R_1$ as shown in the equation of Figure 4.

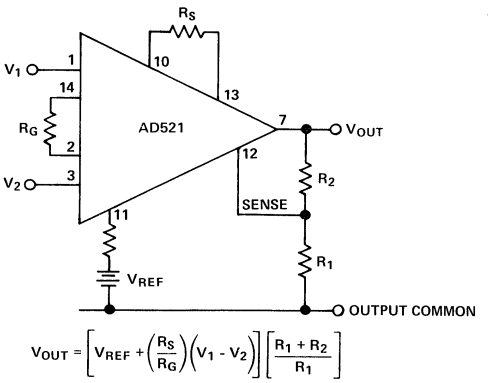


Figure 4. Circuit for utilizing some of the unique features of the AD521. Note that gain changes introduced by changing R_1 and R_2 will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

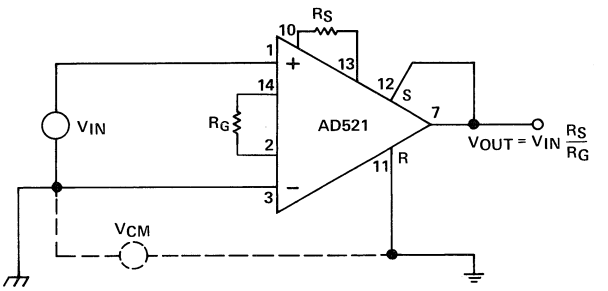


Figure 5. Ground loop elimination. The reference input, Pin 11, allows remote referencing of ground potential. Differences in ground potentials are attenuated by the high CMRR of the AD521.

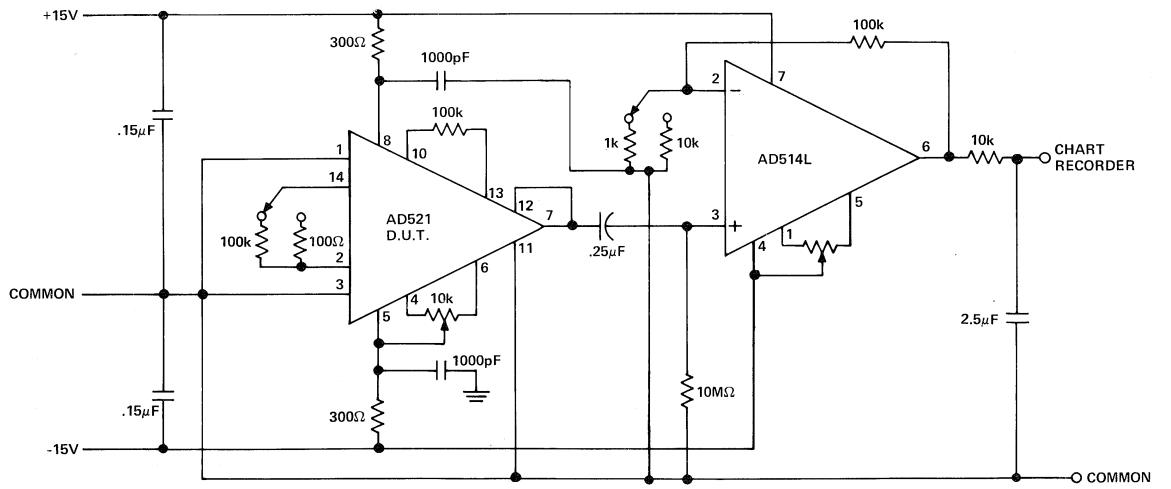


Figure 6. Test circuit for measuring peak to peak noise in the bandwidth 0.1Hz to 10Hz. Typical measurements are found by reading the maximum peak to peak voltage noise of the device under test (D.U.T.) for 3 observation periods of 10 seconds each.

High Accuracy Data Acquisition Instrumentation Amplifier

AD522

FEATURES

Performance

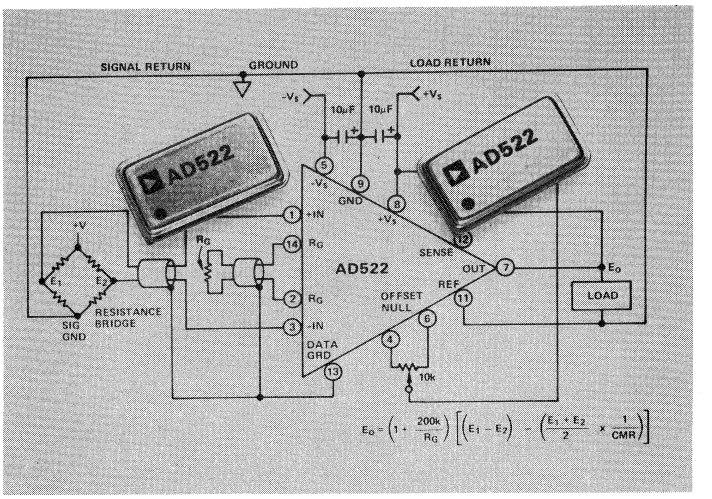
- Low Drift: 2.0μV/°C (AD522B)
- Low Nonlinearity: 0.005% (G = 100)
- High CMRR: >110dB (G = 1000)
- Low Noise: 1.5μV p-p (0.1 to 100Hz)
- Low Initial V_{OS}: 100μV (AD522B)
- Hermetically-Sealed, Electrostatically Shielded DIP

Versatility

- Single-Resistor Gain Programmable: $1 \leqslant G \leqslant 1000$
- Output Reference and Sense Terminals
- Data Guard for Improving ac CMR

Value

- Internally Compensated
- No External Components except Gain Resistor
- Active Trimmed Offset, Gain, and CMR
- Low Cost



PRODUCT DESCRIPTION

The AD522 is a precision IC instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low voltage drift, and low noise makes the AD522 suitable for use in many 12-bit data acquisition systems.

An instrumentation amplifier is usually employed as a bridge amplifier for resistance transducers (thermistors, strain gauges, etc.) found in process control, instrumentation, data processing, and medical testing. The operating environment is frequently characterized by low signal-to-noise levels, fluctuating temperatures, unbalanced input impedances, and remote location which hinders recalibration.

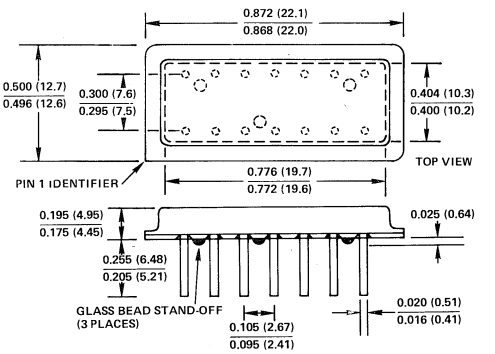
The AD522 was designed to provide highly accurate signal conditioning under these severe conditions. It provides output offset voltage drift of less than 10μV/°C, input offset voltage drift of less than 0.5μV/°C, CMR above 80dB at unity gain (110dB at G = 1000), maximum gain nonlinearity of 0.001% at G = 1, and typical input impedance of $10^9\Omega$.

This excellent performance is achieved by combining a proven circuit configuration with state-of-the-art manufacturing technology which utilizes active laser trimming of tight-tolerance thin-film resistors to achieve low cost, small size and high reliability. This combination of high value with no-compromise performance gives the AD522 the best features of both monolithic and modular instrumentation amplifiers, thus providing extremely cost-effective precision low-level amplification.

The AD522 is available in three versions with differing accuracies and operating temperature ranges; the "A", and "B" are specified from –25°C to +85°C, and the "S" is guaranteed over the military/aerospace temperature range of -55°C to +125°C. All versions are packaged in a hermetically-sealed, electrostatically shielded 14-pin DIP and are supplied in a pin configuration similar to that of the popular AD521 instrumentation amplifier.

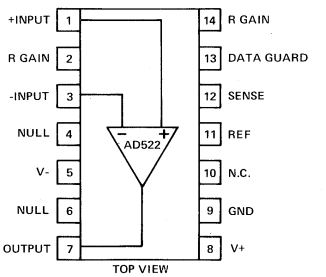
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



14-PIN DUAL-IN-LINE

PIN CONFIGURATION



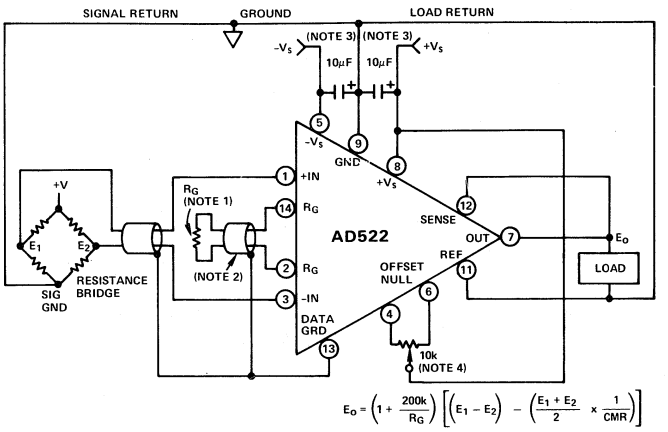
SPECIFICATIONS (typical @ $+V_S = \pm 15V$, $R_L = 2k\Omega$ & $T_A = +25^\circ C$ unless otherwise specified)

MODEL	AD522A	AD522B	AD522S
GAIN			
Gain Equation	$1 + \frac{2\ (10^5)}{R_g}$	*	*
Gain Range	1 to 1000	*	*
Equation Error			
G = 1	0.2% max	0.05% max	**
G = 1000	1.0% max	0.2% max	**
Nonlinearity, max (see Fig. 4)			
G = 1	0.005%	0.001%	**
G = 100	0.01%	0.005%	**
vs. Temp, max			
G = 1	2ppm/°C (1ppm/°C typ)	*	*
G = 1000	50ppm/°C (25ppm/°C typ)	*	*
OUTPUT CHARACTERISTICS			
Output Rating	±10V @ 5mA	*	*
DYNAMIC RESPONSE (See Fig. 6)			
Small Signal (-3dB)			
G = 1	300kHz	*	*
G = 100	3kHz	*	*
Full Power GBW	1.5kHz	*	*
Slew Rate	0.1V/μs	*	*
Settling Time to 0.1%, G = 100	0.5ms	*	*
to 0.01%, G = 100	5ms	*	*
to 0.01%, G = 10	2ms	*	*
to 0.01%, G = 1	0.5ms	*	*
VOLTAGE OFFSET			
Offsets Referred to Input			
Initial Offset Voltage (adjustable to zero)			
G = 1	±400μV max (±200μV typ)	±200μV max (±100μV typ)	±200μV max (±100μV typ)
vs. Temperature, max (see Fig. 3)			
G = 1	±50μV/°C (±10μV/°C typ)	±25μV/°C (±5μV/°C typ)	±100μV/°C (±10μV/°C typ)
G = 1000	±6μV/°C	±2μV/°C	±6μV/°C
$1 < G < 1000$	$\pm(\frac{50}{G} + 6)\mu V/^\circ C$	$\pm(\frac{25}{G} + 2)\mu V/^\circ C$	$\pm(\frac{100}{G} + 6)\mu V/^\circ C$
vs. Supply, max			
G = 1	±20μV/%	*	*
G = 1000	±0.2μV/%	*	*
INPUT CURRENTS			
Input Bias Current			
Initial max, +25°C	±25nA	±15nA	±25nA
vs. Temperature	±100pA/°C	±50pA/°C	±100pA/°C
Input Offset Current			
Initial max, +25°C	±20nA	±10nA	±20nA
vs. Temperature	±100pA/°C	±50pA/°C	±100pA/°C
INPUT			
Input Impedance			
Differential	$10^9\ \Omega$	*	*
Common Mode	$10^9\ \Omega$	*	*
Input Voltage Range			
Minimum Differential Input	±10V	*	*
Maximum Differential Input	±20V	*	*
Maximum Common Mode, Linear	±10V	*	*
Maximum Common Mode Input	±15V	*	*
Common Mode Rejection Ration, Min @ ±10V, 1kΩ Source Imbalance (see Fig. 5)			
G = 1 (dc to 30Hz)	75dB (90dB typ)	80dB (100dB typ)	75dB (90dB typ)
G = 10 (dc to 10Hz)	90dB (100dB typ)	95dB (110dB typ)	90dB (110dB typ)
G = 100 (dc to 3Hz)	100dB (110dB typ)	100dB (120dB typ)	100dB (120dB typ)
G = 1000 (dc to 1Hz)	100dB (120dB typ)	110dB (>120dB typ)	100dB (>120dB typ)
G = 1 to 1000 (dc to 60Hz)	75dB (88dB typ)	80dB (88dB typ)	*
NOISE			
Voltage Noise, RTI (see Fig. 4)			
0.1Hz to 10Hz (p-p)			
G = 1	15μV	*	*
G = 1000	1.5μV	*	*
10Hz to 10kHz (rms)			
G = 1	15μV	*	*
TEMPERATURE RANGE			
Specified Performance	-25°C to +85°C	*	-55°C to +125°C
Operating	-55°C to +125°C	*	*
Storage	-65°C to +150°C	*	*
POWER SUPPLY			
Power Supply Range	±(5 to 18)V	*	*
Quiescent Current, max @ ±15V	±10mA	±8mA	±8mA

*Specifications same as AD522A.
**Specifications same as AD522B.
Specifications subject to change without notice.

GENERAL APPLICATION CONSIDERATIONS

Figure 1 illustrates the AD522 wiring configuration when used in a typical bridge amplifier application. In any low-level, high impedance, noise-dominated environment, proper shielding and grounding are requisite for optimum performance; a recommended technique is shown.



NOTES:
1. GAIN RESISTOR R_G SHOULD BE <5ppm/°C (VISHAY TYPE RECOMMENDED).
2. SHIELDED CONNECTIONS TO R_G RECOMMENDED WHEN MAXIMUM SYSTEM BANDWIDTH AND AC CMR IS REQUIRED, AND WHEN R_G IS LOCATED MORE THAN SIX INCHES FROM AD522. NO INSTABILITIES ARE CAUSED BY REMOTE R_G LOCATIONS. WHEN NOT USED, THE DATA GUARD PIN CAN BE LEFT UNCONNECTED.
3. POWER SUPPLY FILTERS ARE RECOMMENDED FOR MINIMUM NOISE IN NOISY ENVIRONMENTS.
4. NO TRIM REQUIRED FOR MOST APPLICATIONS. IF REQUIRED, A 10kΩ, 25ppm/°C, 25 TURN TRIM POT (SUCH AS VISHAY 1202-Y-10k) IS RECOMMENDED.

Figure 1. Typical Bridge Application

Direct coupling of the AD522 inputs makes it necessary to provide a signal ground return for input amplifier bias currents. This can be achieved by direct connection as shown, or through an indirect path of less than 1MΩ resistance such as other system interconnections.

To minimize noise, shielding should be provided for the input leads and gain resistor connections. A passive data guard is provided to improve ac common mode rejection by "bootstrapping" the capacitance of the input cabling, thus minimizing differential phase shift. This will also reduce degradation of system bandwidth.

Balanced design eliminates the need for external bypass capacitors for most applications. If, however, the power supplies are remotely located (farther than 10 feet or so) or if they are likely to carry more than a few millivolts of noise, local filtering will enable the user to retain optimal performance.

Reference and sense pins are provided to permit remote load sensing. These points can also be used to trim the device CMR, add an output booster, or to offset the output to a reference level. These applications are illustrated in following sections.

It is good practice to place R_G within several inches of the AD522. Longer leads will increase stray capacitance and cause phase shifts that will degrade CMR at higher frequencies. For frequencies below 10Hz, a remote R_G is generally acceptable; no stability problems are caused. Bear in mind that a leakage impedance of 200MΩ between R_G pins will cause an 0.1% gain error at G = 1. Unity gain is not trimmable.

TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS (See Figure 1 and Table 1)

A floating transducer with a 0 to 1 volt output has a 1kΩ source imbalance. A noisy environment induces a one volt 0 to 60Hz common mode signal in the ground return. This signal must be amplified to interface with a data acquisition system calibrated for a 0 to 10 volt signal range. The operating temperature range is 0 to +50°C and an AD522B is to be used. Table 1 lists error sources and their effect on system accuracy.

The total effect on absolute accuracy is less than ±0.2%, allowing adjustment-free 8-bit operation. In computer or microprocesser controlled data-acquisition systems, automatic recalibration can nullify gain and offset drifts leaving noise, distortion and CMR as the only error sources. In this case, full 12-bit operation is achieved.

Gain Errors: Absolute gain errors can be nulled by trimming R_G. Gain drift is a linear effect, not detrimental to resolution and is caused by the change in value of internal resistors over the operating temperature range. An "intelligent" system can correct for these errors with an automatic calibration cycle. Gain nonlinearity never exceeds 0.002% at G = 10.

Offset Drift & Pins Current Errors: Special care has been taken in the design of the AD522 input stage to minimize offset drift. Unless transducer impedances are unbalanced by more than 2kΩ, errors caused by offset current drift are negligible compared to offset voltage drift. Although initial offset voltages are laser-nulled for most applications, provisions have been made to allow further adjustment to correct for initial system offset. In this example, all offset drifts amount to ±0.014% and do not effect resolution (can be corrected with an automatic calibration cycle).

CMR and Noise Errors: Common mode rejection and noise performance of instrumentation amplifiers are critical because

Error Source	Specification	Effect on Absolute Accuracy, % of F.S.	Effect on Resolution % of F.S.
Gain Nonlinearity	±0.002% max, G = 10 (from Spec. Sheet and Fig. 4)	±0.002	±0.002
Voltage Drift	$\frac{25\mu V/°C}{Gain}$ + 2.0μV/°C = 4.5μV/°C R.T.I. = 0.00055%/°C (from Spec. Sheet)	±0.011	---
CMR	86dB (from Spec. Sheet, CMR vs. F vs. G, typical curve)	±0.005	±0.005
Noise, R.T.O. (0.1 to 100Hz)	15μV (p-p) R.T.O. (from Spec. Sheet, Noise vs. G typical curve)	±0.0015	±0.0015
Offset Current Drift	±50pA/°C x 1k source imbalance (Spec. Sheet) = ±50μV/°C = ±1.25μV R.T.I.	±0.000125	---
Gain Drift (add 10ppm/°C for external R_G)	60ppm/°C (Spec. Sheet)	±0.15	---

Table 1. Error Sources

these errors can not be corrected by calibration. Common mode rejection of the AD522 is active laser-trimmed to the limits of thin-film resistor stability. Further trimming could improve CMR on a short term basis, but regular readjustment would be necessary to maintain this improvement (see Figure 2). In this example, untrimmed CMR and noise cause a total error of ±0.0065% of full scale and are the major contributors to resolution error.

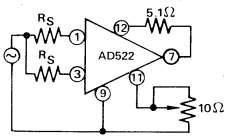


Figure 2. Optional CMR Trim

PERFORMANCE CHARACTERISTICS

Offset Voltage and Current Drift: The AD522 is available in four drift selections. Figure 3 is a graph of maximum RTO offset voltage drift vs. gain for all versions. Errors caused by offset voltage drift can thus be determined for any gain. Offset current drift will cause a voltage error equal to the product of the offset current drift and the source impedance unbalance.

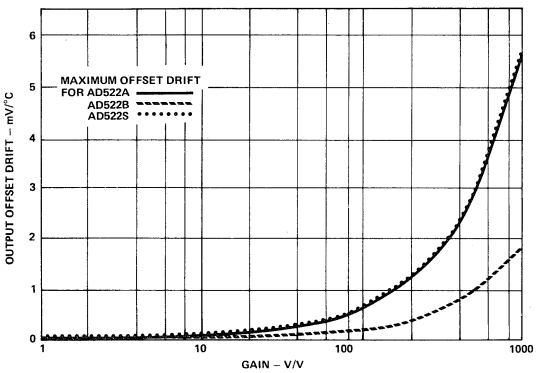


Figure 3. Output Offset Drift (RTO) vs. Gain

Gain Nonlinearity and Noise: Gain nonlinearity increases with gain as the device loop-gain decreases. Figure 4 is a plot of typical nonlinearity vs. gain. The shape of the curve can be safely used to predict worst-case nonlinearity at gains below 100. Noise vs. gain is shown on the same graph.

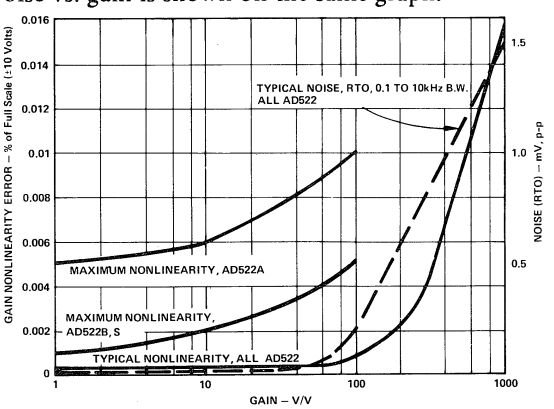


Figure 4. Gain Nonlinearity and Noise (RTO) vs. Gain

Common Mode Rejection: CMR is rated at ±10V and 1kΩ source imbalance. At lower gains, CMR depends mainly on thin-film resistor stability but due to gain-bandwidth considerations, is relatively constant with frequency to beyond 60Hz. The dc CMR improves with increasing gain and is increasingly subject to phase shifts in limited bandwidth high-gain amplifiers. Figure 5 illustrates CMR vs. Gain and Frequency.

Dynamic Performance: Settling time and unity gain bandwidth are directly proportional to gain. As a result, dynamic performance can be predicted from the well-behaved curves of Figure 6.

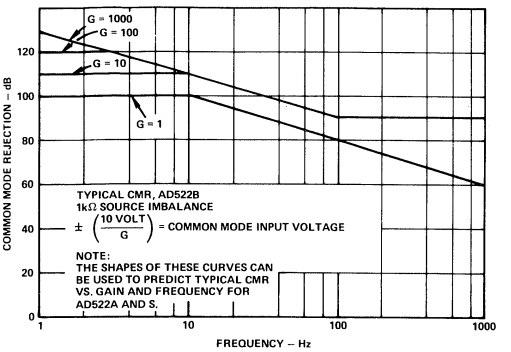


Figure 5. Common Mode Rejection vs. Frequency and Gain

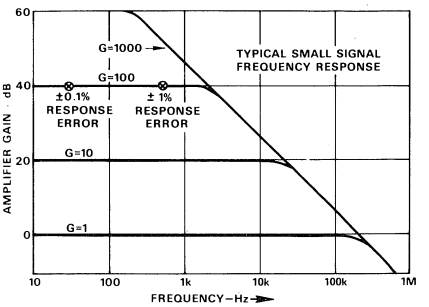


Figure 6. Small Signal Frequency Response (-3dB)

SPECIAL APPLICATIONS

Offset and Gain Trim: Gain accuracy depends largely on the quality of R_G. A precision resistor with a 10ppm/°C temperature coefficient is advised. Offset, like gain, is laser-trimmed to a level suitable for most applications. If further adjustment is required, the circuit shown in Figure 1 is recommended. Note that good quality (25ppm) pots are necessary to maintain voltage drift specifications.

CMR Trim: A short-term CMR improvement of up to 10dB at low gains can be realized with the circuit of Figure 2. Apply a low-frequency 20/G volt peak-to-peak input signal to *both* inputs through their equivalent source resistances and trim the pot for an ac output null .

Sense Output: A sense output is provided to enable remote load sensing or use of an output current booster. Figure 7 illustrates these applications. Being "inside the loop", booster drift errors are minimized. When not used, the sense output should be tied to the output.

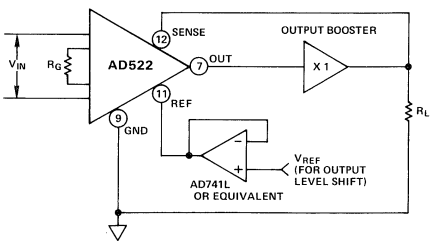


Figure 7. Output Current Booster and Buffered Output Level Shifter

Reference Output: The reference terminal is provided to permit the user to offset or "level shift" the output level to a datum compatible with his load. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset. Furthermore, any reference source resistance will unbalance the CMR trim by the ratio $10k/R_{ref}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 10,000 = 80dB). A buffer amplifier can be used to eliminate this error, as shown in Figure 7, but the drift of the buffer will add to output offset drift. When not used, the reference terminal should be grounded.

ANALOG DEVICES

Precision, Low Drift, Low Noise, Wide Band Instrumentation Amplifier

MODEL 606

FEATURES
Bandwidth Virtually Constant: 100kHz @ G = 100V/V
Guaranteed Low Noise: 1.0μV p-p max (10Hz BW)
Low Drift: ¼μV/°C (606M) – Nonlinearity: 0.002%
Settling Time: 50μs to 0.01% (G = 100V/V)
High CMR: 100dB (G = 100V/V) – CMV: ±10V min

VERSATILITY
Adjustable Gain (Single Resistor) 1 to 10,000 V/V
Output Offset & Remote Sense Terminals

APPLICATIONS
Bridge Amplifiers, Strain Gages, Thermistors, Probes
Data Acquisition & Switch Gain Designs
Precision Current Amplifiers (Floating or Grounded Loads)
Recorder Preamplifiers
High Speed Differential & Buffer Amplifiers

GENERAL DESCRIPTION

The model 606 combines the best attributes of fast instrumentation amplifier designs with the accuracy of slower models to produce the industry's fastest high accuracy model. Featuring virtually constant bandwidth (100kHz @ G = 100) over a gain range of 1 to 10,000V/V, model 606 is available in four low RTI offset drift grades; ¼, ½, 1 and 2μV/°C max (G = 1000V/V). Model 606 offers precision performance with gain nonlinearity error of 0.002% (max), making it possible to hold total amplifier errors well below 0.1% over a 20°C temperature range. Add to this its 12kHz full power response (independent of gain) and 50μs settling to 0.01% and the model 606 approaches the premium performance of rack and panel data amplifier designs, but at a fraction of their cost.

In addition to the above specifications, input voltage noise is specified as less than 1μV p-p (10Hz bandwidth, RTI, G = 1000V/V) making model 606 the first instrumentation amplifier on the market to offer guaranteed low voltage noise. Wideband noise (10Hz to 10kHz bandwidth) is 1.5μV rms max (RTI, G = 1000V/V).

Model 606 offers 20pA/°C current drift and 100MΩ input impedance for use with source impedances up to 100kΩ. Using precision components throughout, this novel design achieves excellent time and temperature gain stability of 6ppm/month and 15ppm/°C, respectively, thereby assuring carefree long-term performance.

Other features include output offset and remote sense terminals for developing power booster and current amplifier configurations for grounded or floating loads. The reference terminal also may be used for level shifting the output for comparator circuits and chart recorders.

APPLICATIONS: INSTRUMENTATION AND DATA ACQUISITION

Available in a compact 2 x 2 x 0.4 inch module, model 606 may be applied as a high impedance differential preamplifier to accurately recover low millivolt signals carried on noisy lines or at high CMV levels. These conditions are commonly experienced in biomedical, aerospace and harsh industrial environments when processing various transducer and control signals. Consider using model 606 also for recorder preamps, bridge and null detector amplifiers and, in general, for designs requiring high CMR and high input impedance even under gain changes.

For high speed data acquisition systems and for amplifying fast transient phenomena, the wideband model 606 may be used as a fixed gain amplifier at the signal site or combined with switch gain networks to develop a semi-programmable gain amplifier as shown in the figure below.

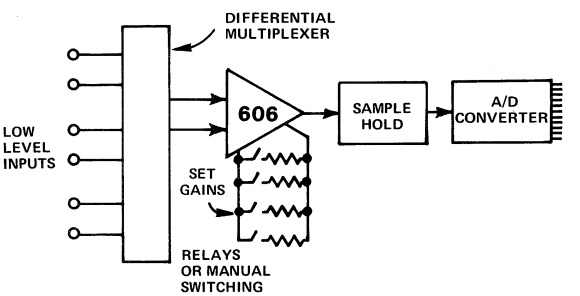


Figure 1. Multiple Input Data Acquisition System

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

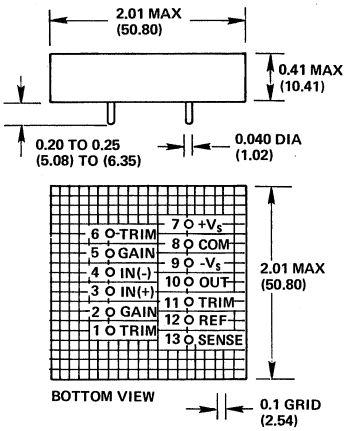
Model		606J|606K|606L|606M				
GAIN						
Gain Range		1 to 10,000V/V				
Gain Equation		G = 1 + (400kΩ/Rg)				
vs. Temperature		±15ppm/°C max				
vs. Time		±6ppm/mo				
Gain Accuracy, G = 100		±0.1% max				
Gain Nonlinearity, G = 100		±0.002% max				
OFFSET VOLTAGE						
Total Offset Voltage, Referred to Input[1]						
Initial, @ +25°C		Adjust to Zero				
Warm Up Drift, 10 minutes, G = 1000		±5μV				
vs. Temperature, G = 1 (max)		±200	±150	±100	±75	μV/°C
G = 1000 (max)		±2	±1	±½	±¼	μV/°C
At other Gains (max)		$\pm\left[2 \pm \frac{200}{G}\right]$	$\pm\left[1 \pm \frac{150}{G}\right]$	$\pm\left[\frac{1}{2} \pm \frac{100}{G}\right]$	$\pm\left[\frac{1}{4} \pm \frac{75}{G}\right]$	μV/°C
vs. Supply, G = 1000		±3μV/V				
At other Gains		$\pm\left[3 \pm \frac{500}{G}\right]$ μV/V				
FREQUENCY RESPONSE						
Small Signal Bandwidth,						
±1% Gain Accuracy,	G = 100	20kHz				
-3dB Gain Accuracy,	G = 100	100kHz				
	G = 10,000	5kHz				
Slew Rate		0.8V/μs				
Full Power		12kHz				
Settling Time, G = 100, ±10V Output Step						
±0.1%		30μs				
INPUT NOISE						
Voltage, G = 1000						
0.01Hz to 10Hz		1μV p-p max				
10Hz to 10kHz		1.5μV rms max				
f = 10Hz		15nV/√Hz rms				
Current, G = 1000						
0.01Hz to 10Hz		60pA p-p				
10Hz to 10kHz		30pA rms				
OUTPUT NOISE						
Voltage, G = 1						
0.01Hz to 10Hz		40μV p-p				
10Hz to 10kHz		50μV rms				
INPUT VOLTAGE RANGE						
Linear Differential Input		±10V min				
Max Differential Input		±Vs				
Common Mode Voltage		±10V min				
CMR, CMV = ±10V, dc to 100Hz,						
1kΩ Source Imbalance,	G = 1	60dB min (70dB typ)				
	G = 10	80dB min (90dB typ)				
	G = 100	86dB min (100db typ)				
	G = 1000	90dB min (106dB typ)				
INPUT IMPEDANCE						
Differential		10^9Ω||3pF				
Common Mode		10^9Ω||3pF				
INPUT BIAS CURRENT						
Initial, @ +25°C		+60nA max				
vs. Temperature		-0.2nA/°C				
INPUT DIFFERENCE CURRENT						
Initial, @ +25°C		±1nA				
vs. Temperature		±20pA/°C				
RATED OUTPUT[2]						
Voltage, 2kΩ Load		±10V min				
Current		±5mA min				
Impedance, dc to 100Hz, G = 100		0.1Ω				
Maximum Load Capacitance		0.1μF				
REFERENCE TERMINAL						
Impedance		200kΩ				
Output Offset Range		±10V min				
POWER SUPPLY[3]						
Voltage, Rated Performance		±15V dc				
Voltage, Operating		±(9 to 18)V dc				
Current, Quiescent		±2.5mA				
TEMPERATURE RANGE						
Rated Performance		0 to +70°C				
Operating		-25°C to +85°C				
Storage		-55°C to +125°C				
CASE SIZE		2" x 2" x 0.4"				

[1] Refer to Figure 3.
[2] Protected for shorts to ground and/or either supply voltage
[3] Recommended power supply, ADI model 904, ±15V @ 50mA output

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

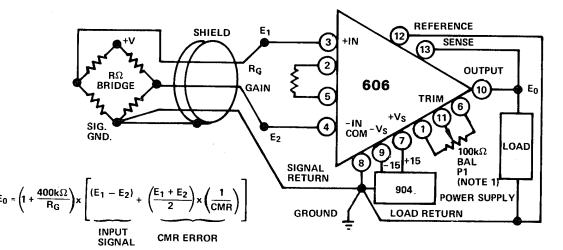


1. **Weight — 52 grams**
2. **Mating Socket AC1040**

INTERCONNECTION DIAGRAM & SHIELDING TECHNIQUES

The figure below illustrates the basic hook-up diagram for voltage amplification in a simple bridge circuit along with several basic equations relating gain, CMV and input-output relationships. A recommended shielding and grounding technique for preserving the excellent amplifying characteristics of model 606 is shown. An error budget is presented on the next page.

Because model 606 is direct coupled, a ground return path for amplifier bias currents must be provided either by direct connection (as shown) or by an implicit ground path having up to 1MΩ resistance between signal ground and amplifier common (pin 8). The sensitive input and gain setting terminals should be shielded from noise sources for best performance, especially at high gains.



NOTE
TRIM POT, P1, 100K OHMS, ADI PART NUMBER 79PR100K (100PPM/°C, 15 TURN CERMET)

Figure 2. Typical Bridge Application

BRIDGE APPLICATION (SEE FIGURE 2)

The model 606 has been conservatively specified using min-max values as well as typicals to allow the designer greater freedom in developing accurate error budgets for predictable performance. In most cases, errors of 0.1% (max) total error (0.03% typical) are easily achieved using model 606 over a ±10°C temperature range as illustrated by the following example:

Error Analysis (Refer to Figure 2)

Error	% of F.S. (10V)	Calculation
Gain Nonlinearity	0.002%	Specified @ 10V F.S.
Gain Drift	0.015%	0.0015%/°C x 10°C
Offset Drift		
Amplifier Offset	0.05%	0.5mV/°C (RTO) x Δ T x 1/10V
Current Offset	0.0006%	20pA/°C x G x ΔT x 300 x 1/10V
Power Supply Change	0.00045%	0.1% x 0.45μV/% x G x 1/10V
Noise	0.01%	Specified (10Hz B.W.)
Total Output Error	0.078% max (0.03% typical)	

Assuming 606L is used, G = 1000, ΔT = ±10°C, with 300Ω, 10V bridge

The error calculations are based on the following considerations:

Gain Errors: Absolute gain errors become negligible by trimming R_G. Gain nonlinearity is 0.002% max at 10V F.S. This value usually can be maintained at less than full scale swings by calibrating gain at the maximum anticipated output voltage, i.e., ±5V out @ G = 1000. Gain drift and time stability contribute 0.015% error, with long term effects becoming negligible.

Offset Drift & Bias Current Errors: The importance of having low offset drift in model 606 is evident in this error term, since offset drift usually predominates and is crucial in high accuracy designs, even where temperature changes are moderate. Initial amplifier offset is zeroed using the balance pot.

Bias current, flowing through the 300Ω source impedance, will develop offset voltages which are trimmed to zero during initial balance. In general, the 20pA/°C current drift error produces less than 2.0μV/°C equivalent drift for up to 100kΩ bridges. For the 300Ω bridge, drift error is 0.0006%. Supply voltage rejection also introduces an equivalent offset which is nulled out with initial balance. Line voltage and temperature changes may be 0.1% adding a negligible error of 0.00045%.

CMR & Noise Errors: Since the CMV is virtually constant at 5V, the CMR error appears as an output offset which is nulled out with initial balance. However, for other applications, with widely varying CMV, high CMR is essential for low errors. The CMR for model 606 is specified for CMV = ±10V and source imbalance of 1kΩ and requires no trimming to achieve values of 90dB min (G = 1000).

The input noise at G = 1000 contributes less than 0.01% in a 10Hz bandwidth and may be reduced by heavier filtering for lower frequency applications.

PERFORMANCE CHARACTERISTICS

Input Offset Voltage Drift: Model 606 is available in four drift selections; ¼, ½, 1 and 2μV/°C (max, RTI, G = 1000V/V). Total input drift is composed of two sources, (input and output stage drifts) and is gain dependent. The curves of Figure 3 illustrate worst case total input drift over the gain range from 1 to 10,000 for models 606J and 606M. Drift is further guaranteed at G = 1V/V and G = 1000V/V.

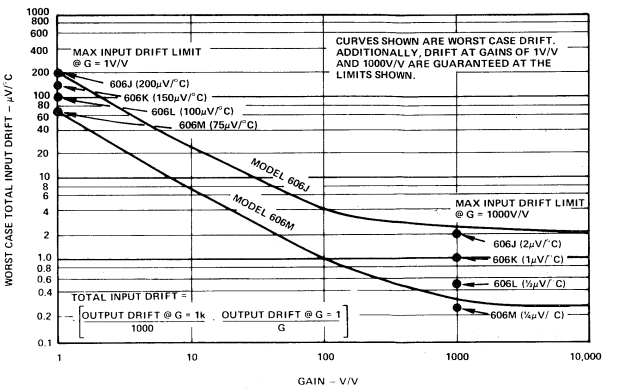


Figure 3. Total Input Offset Drift (Worst Case) vs. Gain

Improved Noise Performance: Model 606 offers a new level of performance in voltage noise by guaranteeing maximum RTI noise of 1μV p-p (G = 1000 V/V, 10Hz BW). The input rms voltage noise density is shown in Figure 4.

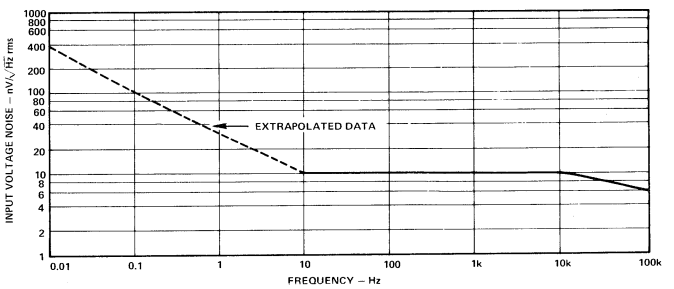


Figure 4. Voltage Noise Per Root Hz of Bandwidth (G = 1000)

Gain Nonlinearity: Nonlinearity is presented as a % of 10V full scale; e.g. 0.2mV RTO for 0.002%. At reduced outputs, nonlinearity may be maintained or improved by trimming the gain resistor, R_G, at the maximum expected output voltage. Since nonlinearity improves at gains above 100 V/V, highest possible gain should be used in the application.

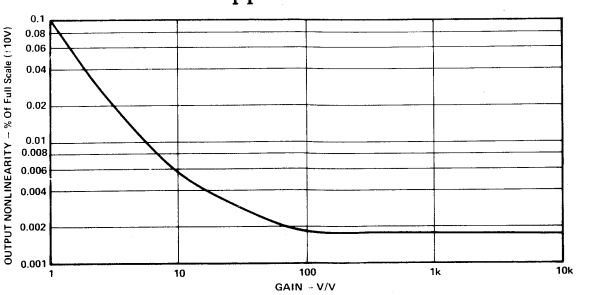


Figure 5. Nonlinearity Error vs. Gain

Common Mode Rejection: CMR is rated at ±10V CMV and 1kΩ source imbalance. As a function of frequency, CMR response is maintained flat from dc to approximately 100Hz (see Figure 6) for all gains from 1 to 10,000. CMR is typically 10dB above the specified minimum.

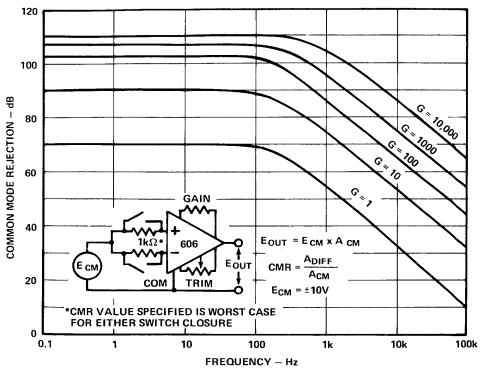


Figure 6. Common Mode Rejection vs. Frequency And Gain

Bandwidth and Settling Time: Bandwidth (−3dB) is relatively constant with gain (see Figure 7 below) and is approximately 100kHz at a gain of 100V/V, increasing to 200kHz at G = 10 V/V. Below 5V/V, gain starts peaking at about 10kHz. Full power response and slew rate are 12kHz and 0.8V/μs (typ) respectively, independent of gain. Settling time response to ±10V step output is relatively constant and gain insensitive, except for gains below 5V/V. Settling time to 0.01% accuracy is 50μs; for 0.1% accuracy, 30μs.

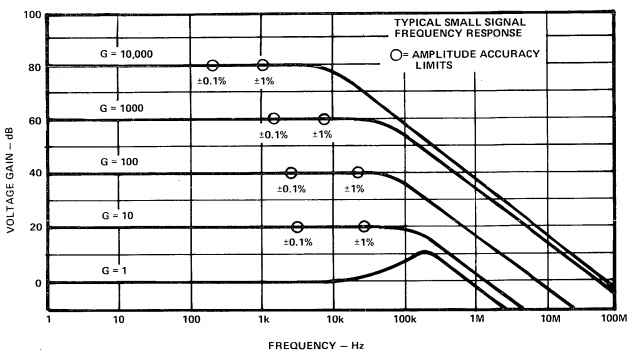


Figure 7. Small Signal Frequency Response

OPERATING INSTRUCTIONS

Install model 606 as shown in the diagram of Figure 2. Gain, offset trim and use of reference and sense terminals are described below.

Gain Adjustment: Gain accuracy and drift are a direct function of R_G tolerance. Use recommended types for best performance. A fine trim may be used in series or in parallel with R_G to improve accuracy. To avoid gain peaking vs. frequency, stray capacitance at these terminals should be less then 0.5pF x Gain. Gain should be set at that output level requiring greatest accuracy.

Balance Procedure: During initial balance, short the sense terminal to load high and the reference terminal to load low respectively. With gain set at the desired value, adjust the output offset for a null, using P1, with input leads shorted to signal ground through their source impedances. This adjusts for amplifier offset, bias current and power supply effects simultaneously. If several gains are to be used, adjust P1 for null, per above, at max gain initially and then switch to min gain. Apply a correction voltage to the reference terminal to reduce output offset and then switch back to max gain. Readjust P1 for a new null. Repeat process until desired null is achieved.

USE OF REFERENCE TERMINAL

Normally tied to load low, the reference terminal (pin 12) may be connected to a stable reference voltage, E_{REF}, to permit adjustment of the output level between ±10V, independent of initial offset adjustments. Source impedance of E_{REF} will be critical to CMR rating since the impedance at pin 12 is 200kΩ and forms a balanced bridge network around the output amplifier stage. (Typically a 60Ω imbalance can result in a CMR of 69dB; 200kΩ/60Ω = 69dB). The use of a buffer amplifier, as shown below, will eliminate these difficulties. Reference source stability becomes critical when operating at low gains since any shifts may be referred to the input as RTI offset errors; i.e. $\Delta E_{REF}/G$ = Offset Error (RTI).

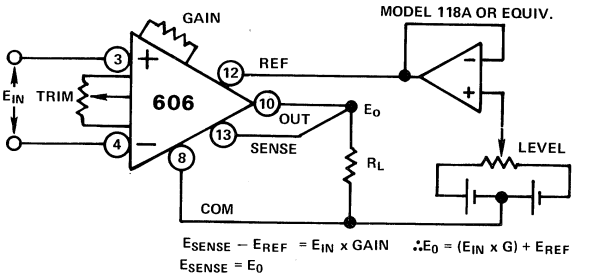


Figure 8. Output Level Control

USE OF REMOTE SENSE AND REFERENCE TERMINALS

The output sense point (pin 13), may be used to include a power booster for increased voltage or current output. When connected as shown below, the booster is contained within a feedback loop of model 606, thereby overcoming booster drift and similar error terms.

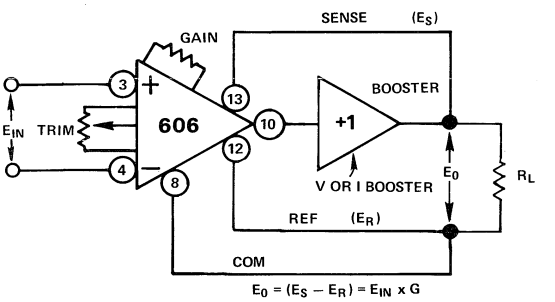


Figure 9. External Booster Connection

Current Feedback Circuits: The sense and reference terminals are also useful for driving currents to either floating or grounded loads as shown below (Figure 10). For floating loads, the reference terminal is grounded; for grounded loads, the sense terminal is connected to the output. The current sense resistor, R_S, is usually below 5 ohms, typically 1 ohm. Special care must be taken in the current control configuration to avoid voltage saturation when driving reactive loads; $E_o = IR + L\,(dI/dt)$.

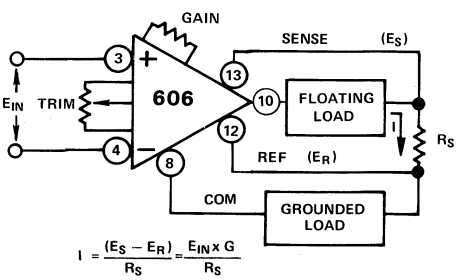


Figure 10. Current Feedback for Floating or Grounded Loads

Economy, Wideband, Low Noise, Low Drift Instrumentation Amplifier

MODEL 610

FEATURES

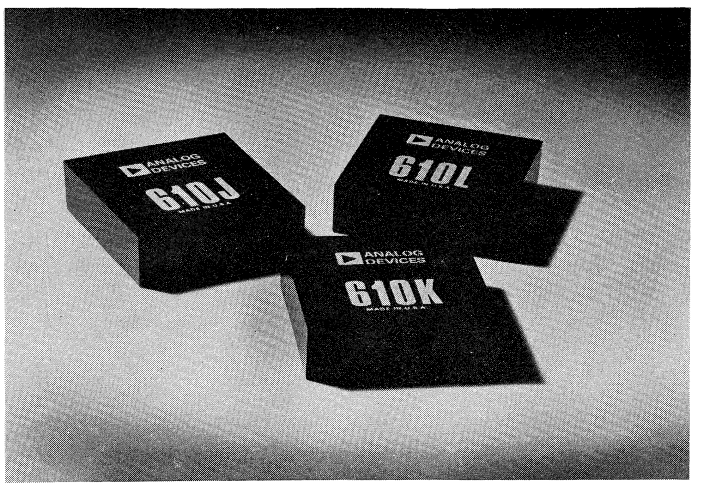
Bandwidth Virtually Constant: 100kHz @ G = 100V/V
Guaranteed Low Noise: 2μV p-p max (610L)
Low Drift: 0.5μV/°C max (610L)
Nonlinearity: 0.01% max
CMR: 86dB min — CMV: ±10V

VERSATILITY

Adjustable Gain (Single Resistor) 1 to 10,000V/V
Output Offset & Remote Sense Terminals

APPLICATIONS

OEM Designs, Lab and Field Instruments
Bridge Amplifiers, Strain Gages, Thermistors, Probes
Data Acquisition & Switch Gain Designs
Precision Current Amplifiers (Floating or Grounded Loads)
Biologic Probes
High Speed Differential & Buffer Amplifiers



GENERAL DESCRIPTION

Analog Devices' model 610 combines high performance with low price to set an outstanding standard of value for this class of instrumentation amplifier. The 610 features guaranteed low noise performance: 2.5μV rms, max (610J) and 2μV rms, max (610K, L) for f = 10Hz to 10kHz. Other noteworthy guaranteed specifications include 0.01% max nonlinearity (610J, K, L), 0.5μV/°C max offset drift (610L), and 15ppm max gain error (610J, K, L). When coupled with 86dB (min) CMR (G = 100, CMV = ±10V) the model 610's performance characteristics enable it to maintain total amplifier errors below 0.2% over a +20°C temperature range. Other salient features of the 610 include virtually constant bandwidth (100kHz @ G = 100) and very low power consumption (90mW). The model 610 is the component of choice when considering instrumentation amplifiers to meet the cost and performance objectives of OEM designs.

In addition to the above specifications, the model 610 offers the versatility of adjustable gain, remote output sensing and output offset. Amplifier gain can be controlled between 1 and 10,000 with a single external resistor. Output offset and remote sensing terminals may be employed to develop power booster and current amplifier circuit configurations for both grounded and floating leads. The reference terminal may also be used to provide level shifting of the output for comparative circuits and chart recorders.

The combination of these special features greatly increases the utility of model 610 and allows it to be employed in a broad scope of applications. By selecting the 610, the designer can realize a savings in components that might otherwise be required to perform the functions already built into this amplifier. Among the competition, the model 610 is alone at offering these capabilities at such a low price.

APPLICATIONS: INSTRUMENTATION AND DATA ACQUISITION

The combination of low cost and very good performance provided by model 610 offers exceptional quality and value to the OEM designer. This compact module may be applied as a high impedance differential preamplifier to accurately recover millivolt signals carried on noisy lines or high CMV levels. These environmental conditions are frequently encountered in biomedical, aerospace and industrial applications when processing transducer and control signals. Consideration should be given to model 610 for designs, such as bridge and null detector circuits, which require high CMR and high input impedance even under changes in gain. Model 610 is also an ideal component for use in lab and field instruments.

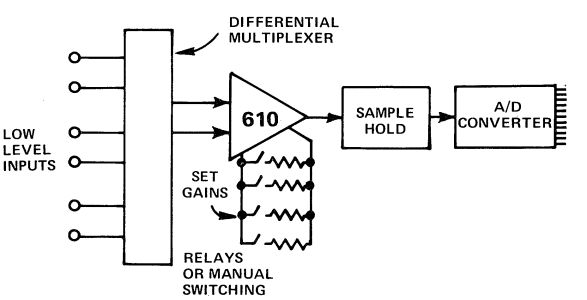


Figure 1. Multiple Input Data Acquisition System

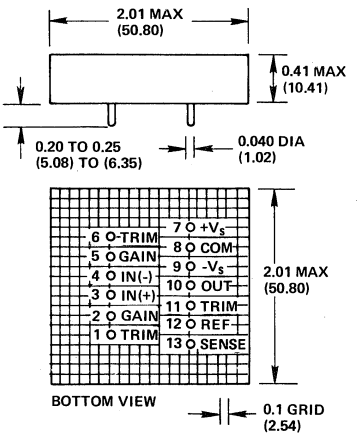
SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

Model	610J | 610K | 610L
GAIN	
Gain Range	1 to 10,000V/V
Gain Equation	G = 1 + (400kΩ/Rg.)
vs. Temperature	±15ppm/°C max
vs. Time	±0.001%/mo.
Gain Accuracy, G = 100	±0.1% max
Gain Nonlinearity, G = 100	±0.01% max
OFFSET VOLTAGE	
Input Offset Voltage	
Initial (@ +25°C)	Adjust to Zero
vs. Temperature, G = 1000	±3 | ±1 | ±½μV/°C max
vs. Supply, G = 1000	±3μV/V
Output Offset Voltage, G = 1	
vs. Temperature	±200|±150|±150μV/°C
FREQUENCY RESPONSE	
Small Signal Bandwidth	
±1% Gain Accuracy, G = 100	20kHz
-3dB Gain Accuracy, G = 1	1MHz
G = 100	100kHz
Slew Rate	0.8V/μs
Full Power	12kHz
Settling Time, G = 100, ±10V Output Step	
±0.1%	30μs
INPUT NOISE	
Voltage, G = 1000	
0.01Hz to 10Hz	2.5|2|2μV p-p max
10Hz to 10kHz	2.5|2|2μV rms
Current, G = 1000	
0.01Hz to 10Hz	60pA p-p
10Hz to 10kHz	30pA rms
OUTPUT NOISE	
Voltage, G = 1	
0.01Hz to 10Hz	50μV p-p
10Hz to 10kHz	50μV rms
INPUT VOLTAGE RANGE	
Linear Differential Input	±10V min
Max Differential Input	±V_S
Common Mode Voltage	±10V min
CMR, CMV = ±10V, dc to 100Hz	
1k Source Imbalance, G = 1	60dB min (70dB typ)
G = 1000	90dB min (106dB typ)
INPUT IMPEDANCE	
Differential	10^9Ω||3pF
Common Mode	10^9Ω||3pF
INPUT BIAS CURRENT	
Initial, @ +25°C	+60nA max
vs. Temperature	-0.2nA/°C
INPUT DIFFERENCE CURRENT	
Initial, @ +25°C	±5nA
vs. Temperature	±20pA/°C
RATED OUTPUT[1]	
Voltage, 2kΩ Load	±10V min
Current	±5mA min
Impedance dc to 100Hz, G = 100	0.1Ω
REFERENCE TERMINAL	
Impedance	200kΩ
Output Offset Range	±10V min
POWER SUPPLY[2]	
Voltage, Rated Performance	±15V dc
Voltage, Operating	±(12 to 18)V dc
Current, Quiescent	±3mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C
CASE SIZE	2" x 2" x 0.4"

[1] Protected for shorts to ground or either supply voltage.
[2] Recommended power supply, ADI model 904, ±15V @ 50mA output
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

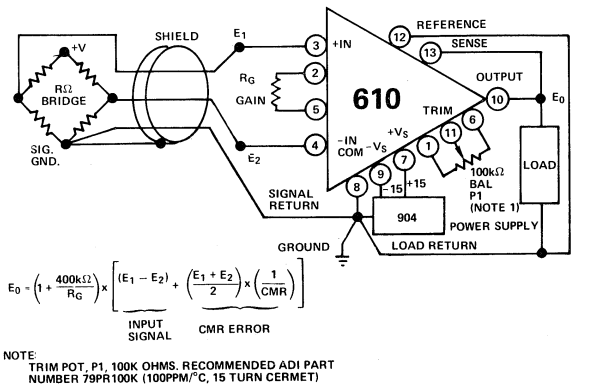


NOTES:
1. Weight — 52 grams
2. Mating Socket AC1040

INTERCONNECTION DIAGRAM & SHIELDING TECHNIQUES

The figure below illustrates the basic hook-up diagram for voltage amplification in a simple bridge circuit along with several basic equations relating gain, CMV and input-output relationships. A recommended shielding and grounding technique for preserving the excellent amplifying characteristics of model 610 is shown. An error budget is presented on next page.

Because model 610 is direct coupled, a ground return path for amplifier bias currents must be provided either by direct connection (as shown) or by an implicit ground path having up to 1MΩ resistance between signal ground and amplifier common (pin 8). The sensitive input and gain setting terminals should be shielded from noise sources for best performance, especially at high gains.



NOTE:
TRIM POT, P1, 100K OHMS. RECOMMENDED ADI PART NUMBER 79PR100K (100PPM/°C, 15 TURN CERMET)

Figure 2. Typical Bridge Application

For data acquisition systems and for amplifying transient phenomena, the model 610 may be used as a fixed gain amplifier at the signal site or combined with switch gain networks to develop a semi-programmable gain amplifier as shown in Figure 1.

BRIDGE APPLICATION: ERROR BUDGET ANALYSIS (See Figure 2)

Model 610 specifications employ min-max values as well as typicals to allow the designer wider latitude in formulating accurate error budgets for predictable operation. Total errors of 0.1% max (0.04% typical) are possible in most cases when the model 610 is used over a ±10°C temperature range. The error analysis computations in the table below illustrate the performance of the 610:

Error	% of F.S. (10V)	
Gain Nonlinearity	0.02%	Specified @ 10V f.s.
Gain Drift	0.015%	0.0015% x 10°C
Offset Drift		
Amplifier Offset	0.05%	0.5mV/°C (RTO) x ΔT x 1/10V
Current Offset	0.006%	200pA/°C x G x ΔT x 300 x 1/10V
Power Supply Change	0.0004%	0.2% x 0.2μV/% x G x 1/10V
Noise	0.01%	Specified (10Hz B.W.)
Total Output Error	0.100% max (0.04% typical)	

Assuming: 610L is used, G = 1000, ΔT = ±10°C, with 300Ω, 10V bridge.

Computations of errors are based on the following considerations:

Offset Drift and Bias Current Errors: This error term demonstrates the importance of low offset drift offered in model 610. Offset drift is usually the dominant error component and a low value for this parameter is critical in high accuracy designs, even over moderate temperature ranges.

Bias current flowing through the 300Ω source impedance, will develop offset voltages which are trimmed to zero during initial balance. The 200pA/°C current drift error produces less than 1μV/°C equivalent drift for up to 10kΩ bridges; drift error is 0.003% for the 300Ω bridge. Supply voltage rejection also introduces an equivalent offset which is nulled out with initial balance. Line voltage and temperature changes may be 0.2%, adding a negligible error of 0.0004%.

Gain Errors: By trimming R_G absolute gain errors can be made negligibly small. Gain nonlinearity is 0.02% max (0.01% typical) at 10V f.s. This value usually can be maintained at lesser than full scale swings by calibrating gain at the maximum anticipated output voltage, i.e. ±5V out @ G = 1000. Gain drift and time stability contribute 0.015% error, with long term effects becoming negligible.

CMR & Noise Errors: Since the CMV is virtually constant at 5V, the CMR error appears as an output offset which is nulled out with initial balance. However, for other applications, with widely varying CMV, high CMR is essential for low errors. The CMR for model 610 is conservatively specified and requires no trimming to achieve values of 120dB min (G = 1000). Use of the reference or sense terminal does not degrade CMR as with most other designs. The input noise at G = 1000 contributes about 0.01% in a 10Hz bandwidth which may be reduced by heavier filtering for lower frequency applications.

PERFORMANCE CHARACTERISTICS

Input Offset Voltage Drift: Model 610 offers a selection of three drift specifications; 3, 1 and ½μV/°C (max, RTI, G = 1000V/V). Total input drift is a gain dependent phenomenon and is composed of two sources (input and output stage drifts). Figure 3 shows worst case total drift over the gain range of 1 to 10,000.

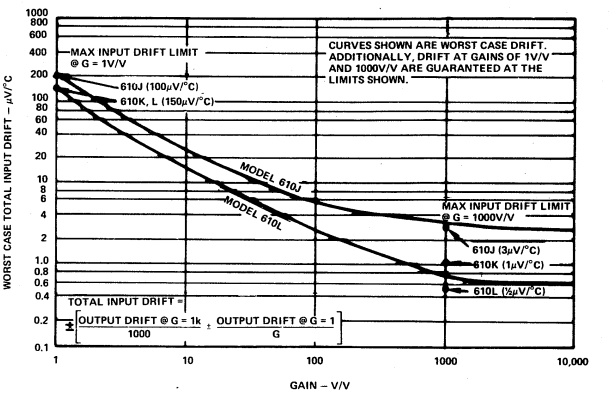


Figure 3. Total Input Offset Drift (Worst Case) vs. Gain

Gain Nonlinearity and Output Noise: Nonlinearity is specified as a percent of full scale (10V), e.g. 1mV RTO for 0.01%. By trimming gain at the maximum expected output voltage, nonlinearity may be maintained or improved for lower output levels. Also, as indicated in Figure 4, nonlinearity is minimum for gains above 100V/V. Thus the highest possible gain should be used when nonlinearity is a critical parameter.

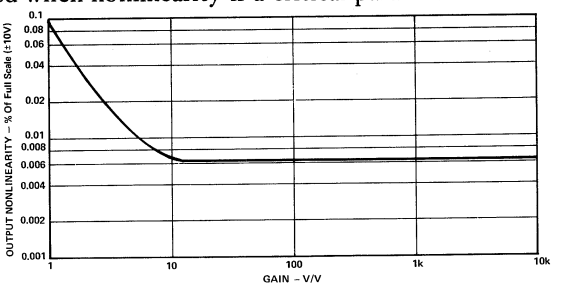


Figure 4. Nonlinearity Error vs. Gain

As one would expect, total output voltage noise increases with gain. Figure 5 shows noise density as a function of amplifier bandwidth.

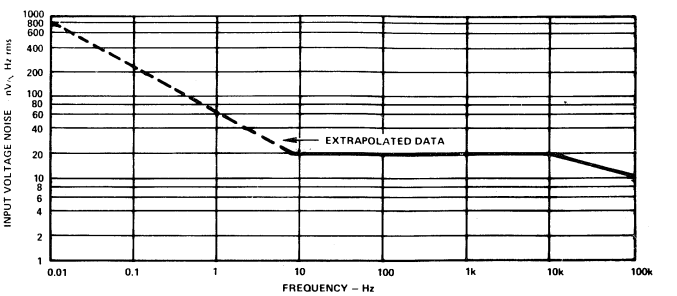


Figure 5. Voltage Noise per Root Hz of Bandwidth (G = 1000)

Common Mode Rejection: CMR is specified at ±10V CMV and 1kΩ source imbalance over the frequency range of dc to 100Hz. In this frequency band, CMR response is flat for all gains from

1 to 10,000 (see Figure 6). For model 610, CMR is typically 10dB above the specified minimum.

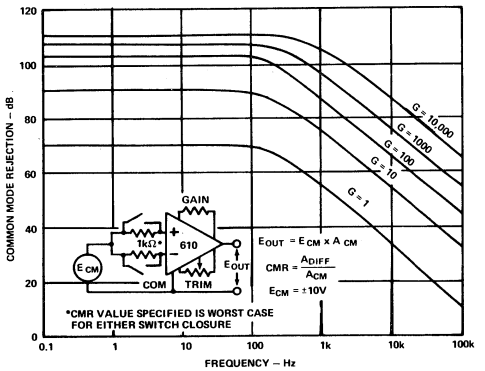


Figure 6. Common Mode Rejection vs. Frequency and Gain

Bandwidth and Settling Time: Bandwidth (−3dB) is relatively constant with gain (see Figure 7 below) and is approximately 100kHz at a gain of 100V/V, increasing to 200kHz at G = 10 V/V. Below 5V/V, gain starts peaking at about 10kHz. Full power response and slew rate are 12kHz and 0.8V/μs (typ) respectively, independent of gain. Settling time response to ±10V step output is relatively constant and gain insensitive, except for gains below 5V/V. Settling time to 0.01% accuracy is 50μs; for 0.1% accuracy, 30μs.

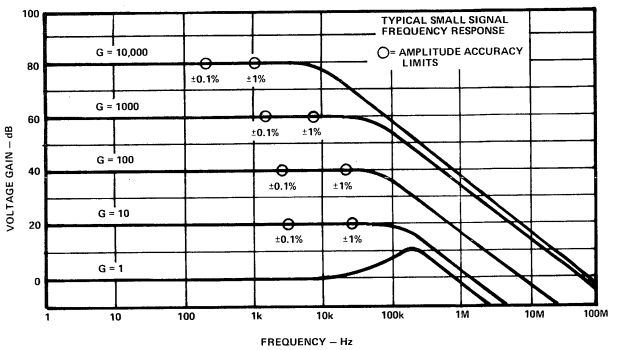


Figure 7. Small Signal Frequency Response

OPERATING INSTRUCTIONS

Install model 610 as shown in the diagram of Figure 2. Gain, offset trim and use of reference and sense terminals are described below.

Gain Adjustment: Gain accuracy and drift are a direct function of R_G tolerance. Use recommended types for best performance. A fine trim may be used in series or in parallel with R_G to improve accuracy. To avoid gain peaking vs. frequency, stray capacitance at these terminals should be less than 0.5pF x Gain . Gain should be set at that output level requiring greatest accuracy.

Balance Procedure: During initial balance, short the sense terminal to load high and the reference terminal to load low respectively. With gain set at the desired value, adjust the output offset for a null, using P1, with input leads shorted to signal ground through their source impedances. This adjusts for amplifier offset, bias current and power supply effects simultaneously. If several gains are to be used, adjust P1 for null, per above, at max gain initially and then switch to min gain. Apply a correction voltage to the reference terminal to reduce output offset and then switch back to max gain. Readjust P1 for a new null. Repeat process until desired null is achieved.

Current Feedback Circuits: The sense and reference terminals are also useful for driving currents to either floating or grounde loads as shown below (Figure 8). For floating loads, the refer ence terminal is grounded; for grounded loads, the sense terminal is connected to the output. The current sense resistor, R_S, is usually below 5 ohms, typically 1 ohm. Special care must be taken in the current control configuration to avoid voltage satu ation when driving reactive loads; $E_o = IR + L\ (dI/dt)$.

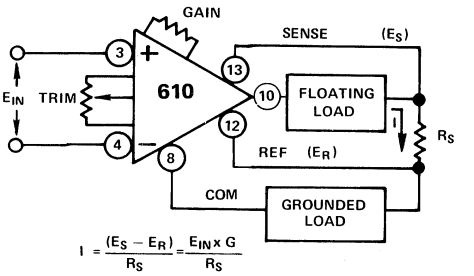


Figure 8. Current Feedback for Floating or Grounded Loads

USE OF REFERENCE TERMINAL

Normally tied to load low, the reference terminal (pin 12) may be connected to a stable reference voltage, E_{REF}, to permit adjustment of the output level between ±10V, independent of initial offset adjustments. Source impedance of E_{REF} will be critical to CMR rating since the impedance at pin 12 is 200kΩ and forms a balanced bridge network around the output amplifier stage. (Typically a 60Ω imbalance can result in a CMR of 69dB; 200kΩ/60Ω = 69dB). The use of a buffer amplifier, as shown below, will eliminate these difficulties. Reference source stability becomes critical when operating at low gains since any shifts may be referred to the input as RTI offset errors; i.e. $\Delta E_{REF}/G$ = Offset Error (RTI).

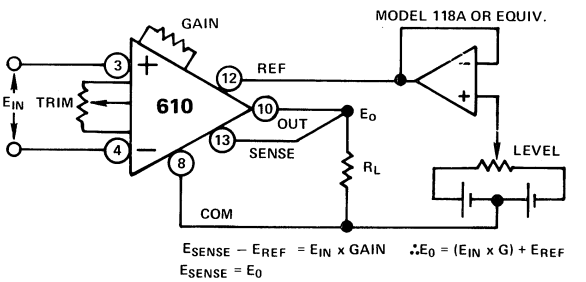


Figure 9. Output Level Control

USE OF REMOTE SENSE AND REFERENCE TERMINALS

The output sense point (pin 13), may be used to include a power booster for increased voltage or current output. When connected as shown below, the booster is contained within a feedback loop of model 610, thereby overcoming booster drif and similar error terms.

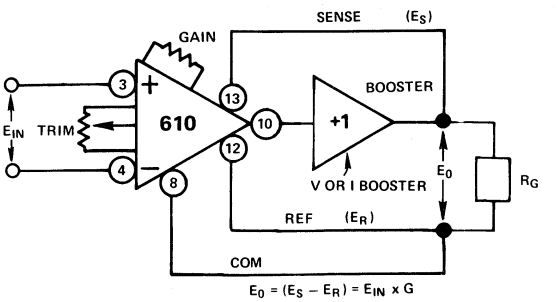


Figure 10. External Booster Connection

Isolation Amplifiers

Orientation
Isolation Amplifiers

The *isolation amplifier* (or *isolator*) has an input circuit that is galvanically isolated from the power supply and the output circuit. Isolators are intended for applications requiring safe, accurate measurement of dc and low-frequency voltage or current in the presence of high common-mode voltage (to thousands of volts) with high CMR, line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements where dc and line-frequency leakage must be maintained at levels well below certain mandated minima.* Principal applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment, and industrial process-control systems.

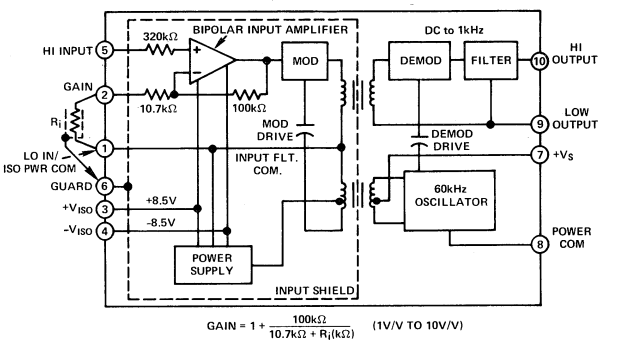
Analog Devices Isolators described in this catalog use electromagnetically coupled high-frequency carrier techniques for communication of power to and signals from the input circuit.

CHOOSING AN ISOLATOR

The choice of an isolator depends on the desired *functional characteristics* and the required *specifications*. Functional characteristics include such considerations as number of channels, range of output common-mode (output to power supply), nature of the front-end amplifier (amplification only or general op-amp functioning), and the availability of isolated power for additional external front-end circuitry. Key specifications include performance specs and "absolute max/min" mandated safety specifications. A Selection Guide to isolators recommended for new-equipment design appears on page 128, and definitions of specifications follow this section. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; they are listed on page 599. Data sheets are available upon request. In addition to the useful applications information on the data sheets published here, two publications[1,2], available upon request, provide information useful to the circuit designer.

Functional Characteristics The Figure shows the circuit architecture of a self-contained isolator, Model 284J. The various models differ, but their properties can be discussed in terms of the device shown. An isolator of this type requires power from a two-terminal dc supply. An internal oscillator converts the dc power to ac, which is transformer-coupled to the shielded input section, then converted to dc for the input stage and the auxiliary power output. The ac carrier is also modulated by the amplifier output, transformer-coupled to the output stage, demodulated by a phase-sensitive demodulator (using the oscillator output as the reference), and filtered.

The amplifier in this example is a resistor-protected op amp (actually, the protection works both ways – it protects the amplifier against differential overloads (±6500V pk) and it protects sensitive input sources from supply voltage if the amplifier malfunctions), connected for a programmable gain from 1 to 10V/V, as determined by a single external resistor. Since both input terminals are floating, the amplifier functions effectively as an instrumentation amplifier. All but one of the amplifiers in this series function in the instrumentation-amplifier mode, but with various gain ranges. The 277 is an exception; its input stage is an uncommitted high-gain low-drift, low-noise op amp, and the output terminal of the input stage is available for feedback connections to perform a wide range of single-ended or differential operations. Because of the transformer coupling, the output of these devices is isolated from the input stage.



In the Figure, it can be seen that the demodulator drive is capacitively coupled from the oscillator to the output stage. This permits the output to operate at a dc common-mode potential with respect to power common. An isolator of this type is said to provide *three-port* isolation, because there are three isolated ports: input, power supply, and output. The 275, the 284, the 285, and the 286 have this property. The data sheets carry block diagrams, which show the architecture of each device; 3-port devices, in general, have an output common-mode-voltage spec in the "Rated Output" section. Two-port devices are those in which there is a dc connection between the power supply and the output stage. An example of where a 3-port device might be used: if the isolator power supply is at some distance from the destination (say, a data-acquisition system), line drops could result in common-mode errors if the output were tied to the power supply.

The 284J, as can be seen, is a completely self-contained device. There are applications for which a degree of "unbundling" can lead to economy and improved performance. For example, if there are many input channels to be isolated, economies can be realized by the use of a common oscillator. In addition, the common oscillator makes it possible to avoid the possibility of small errors due to beat frequencies developed by small amounts of crosstalk.

Several synchronized multi-channel devices are available. Model 286 is essentially a 284J with a power amplifier instead of an oscillator. It requires a dc power input and a pair of leads

*Examples of such requirements may be found in UL STD 544 and SWC (Surge Withstand Capability) in IEEE Standard for Transient Voltage Protection 472-1974.

[1] "Application Guide to Precision Measurements with Instrumentation and Isolation Amplifiers" (Spring, 1978)

[2] "Analog Devices Isolation and Instrumentation Amplifiers Designer's Guide" (1978)

for a low-power oscillator input, which can be furnished by a 281 synchronizable oscillator. The 281 will drive from one to 16 286's, and it will also synchronize additional 281's for increments of up to 16 286's per 281. The 288 isolator does not require dc power inputs. Instead, the ac input is furnished from 947/948 matching dc-ac high-frequency drivers. The 947, for example, has eight (isolated) output windings, which provides the carrier signal and input power for as many as eight 288J's. Isolated front-end power is provided by rectification and filtering of the 947 "MOD DRIVE" signal. The result is a very inexpensive high-accuracy multi-channel system.

SPECIFICATIONS

The illustration shows a typical specification block and defines the specifications of key interest.

NONLINEARITY – This is the peak deviation from a best straight line, expressed as a % of peak-to-peak output. Should be considered when signal fidelity is of prime importance.

MAX SAFE DIFFERENTIAL INPUT – Max voltage that can be safely applied across input terminals. Important to consider for fail-safe designs in the presence of high voltages.

CMR, INPUT TO GUARD – Indicates ability to reject differential voltage between signal low and guard. Should be considered in applications where guard cannot be connected directly to signal low.

INPUT NOISE – Total noise, referred to the input. Facilitates comparison with expected signal input levels.

ISOLATED SUPPLY – Dual supply voltages, completely isolated from the input power supply terminals, provide the capability to excite floating input signal conditioners, front-end amplifiers, as well as remote transducers.

MODEL	284J
GAIN (NON-INVERTING)	
Range (50kΩ Load)	1 to 10V/V
Formula (R_i in kΩ)	$G = 1 + \frac{100k\Omega}{10.7k\Omega + R_i}$
Deviation from Formula	±3%
vs. Temperature (0 to +70°C)	±0.0075%/°C
vs. Time	±0.001%/1000 hours
Nonlinearity, ±5V Output (G = 1 to 10V/V)	±0.05%
INPUT VOLTAGE RATINGS	
Linear Differential Range, G = 1V/V	±5V
Max Safe Differential Input	
Continuous	240V rms
Pulse, 10ms Duration, 1 Pulse/10 sec	±6500V pk max
Max CMV, Inputs to Outputs	
ac, 60Hz, 1 minute Duration	2500V rms
Pulse, 10ms Duration, 1 Pulse/10 sec	±2500V pk max
With 510kΩ in series with guard	±5000V pk max
Continuous, ac or dc	±2500V pk
CMR, Inputs to Outputs, 60Hz, $R_S \leq 5k\Omega$	
Balanced Source Impedance	114dB
5kΩ Source Impedance Imbalance	110dB min
CMR, Inputs to Guard, 60Hz	
1kΩ Source Impedance Imbalance	78dB
Max Leakage Current, Inputs to Pwr Com	
@ 115V ac, 60Hz	2.0μA rms max
OFFSET VOLTAGE, REFERRED TO INPUT	
Initial, @ +25°C	±(5 + 20/G)mV
vs. Temperature (0 to +70°C)	
At Gain = 10V/V	±15μV/°C
At Other Gains	±(1 + 150/G)μV/°C
vs. Supply Voltage	±1mV/%
INPUT IMPEDANCE	
Differential	$10^8\Omega \| 150pF$
Overload	320kΩ
Common Mode	$5 \times 10^{10}\Omega \| 20pF$
INPUT DIFFERENCE CURRENT	
Initial, @ +25°C	±7nA max
vs. Temperature (0 to +70°C	±0.1nA/°C
INPUT NOISE	
Voltage, Gain = 10V/V	
0.01Hz to 100Hz	8μV pk-pk
10Hz to 1kHz	10μV rms
Current	
0.01Hz to 100Hz	5pA pk-pk
FREQUENCY RESPONSE, GAIN = 1 to 10V/V	
Small Signal Bandwidth, -3dB	1kHz
Slew Rate	25mV/μs
Full Power, Gain = 1V/V	700Hz
Full Power, Gain = 10V/V	200Hz
ISOLATED POWER SUPPLY	
Voltage/Current	±8.5V dc/±5mA
Accuracy	±5%
Regulation, No Load to Full Load	+0, -15%
CMV, Outputs to Pwr. Com.	±50V pk max
RATED OUTPUT	
Voltage, 50kΩ Load	±5V min
Output Impedance	1kΩ
Output Ripple Noise, 1MHz Bandwidth	5mV pk-pk
POWER SUPPLY, SINGLE POLARITY	
Voltage, Rated Performance	+15V dc
Voltage, Operating	+(8V dc to 15.5V dc)
Current, Quiescent	+10mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C
CASE DIMENSIONS	1.5" x 1.5" x 0.62"

CMV, INPUTS TO OUTPUTS – Voltage that may be safely applied to *both* inputs with respect to outputs or power common. Necessary consideration in applications with high CMV input or when high voltage transients may occur at the input.

CMR, INPUTS TO OUTPUTS – Indicates ability to reject common mode voltages between inputs and outputs. Important when processing small signals riding on high common mode voltages.

LEAKAGE CURRENT – Maximum input leakage current when power-line voltage is impressed on inputs. Vital consideration for patient safety in medical applications.

OFFSET VOLTAGE REFERRED TO INPUT – Total input drift is composed of two sources (input and output stage drifts) and is gain (G) dependent. Referring offsets to the input allows them to be compared to signal levels.

OVERLOAD RESISTANCE – This is the apparent input impedance under conditions of amplifier saturation. It limits differential fault currents.

Selection Guide
Isolation Amplifiers

APPLICATION	PRIMARY CONSIDERATIONS	FEATURES	RECOMMENDED MODEL	PAGE
Industrial and Medical Instrumentation	Lowest Cost High Performance Patient Safety High CMR, CMV	±0.05% Nonlinearity, ±75ppm/°C Gain Drift 2.0μA rms max leakage; Defibrillator Protection Floating Power Supply: ±8.5V dc @ ±5mA min 110dB min CMR @ 60Hz, ±5kV pk CMV (Pulse)	284J	137
Industrial and Medical Instrumentation	Multi-Channel Reliability High CMV, CMR Isolated Supply	External Synchronization; 100kHz Osc – model 281 Meets IEEE SWC Standard and UL 544 Leakage Std 5kV pk pulse differential and Input/Output CMV 110dB min CMR @ 60Hz; ±15V dc @ ±15mA Isolated Supply	286J 281 (Osc)	147
Industrial Instrumentation and Control Systems	Multi-Channel High Accuracy Low Cost Smallest Size	External Synchronization; model 947 or 948 dirver 0.05% max nonlinearity, 100ppm/°C max gain drift, 5μV/°C max input drift, Adjust. Gain, 1 to 1000V/V, 850V dc diff and in/out CMV, 1" x 1" x 0.56"	288J 288K 947 (Driver) 948 (Driver)	153
Industrial Instrumentation and Control Systems	Highest Accuracy Versatility High CMV/CMR Isolated Supply	0.025% max nonlinearity, 1μV/°C max input drift, Uncommitted High Performance Op Amp Front-End 160dB min CMR @ dc; 3.5kV rms CMV (1 min) Floating Power Supply: ±15V dc @ ±15mA min	277J 277K 277A	133
Industrial Instrumentation and Control Systems	High Accuracy Wide Input/Output Range High CMV/CMR Floating Output	0.05% max nonlinearity, 5μV/°C max input drift, ±10V Input/Output Range; 2.5kV dc CMV (Continuous), 120dB min CMR @ 60Hz, Fully Guarded Inputs 3-Port Isolation; 200V dc CMV Outputs to Pwr Com	275J 275K 275L	129
Industrial Instrumentation and Control Systems	High Accuracy Low Impedance Output High CMV/CMR	0.03% max nonlinearity, 5μV/°C max input drift ±10V min Input/Output Range; ±5mA Output Adjustable Gain, 1 to 1000V/V, 3000V rms 60Hz Input/Output Isolation (1 min), 115dB CMR @ 60Hz	285J 285K 285L	143

High CMV, Three Port, High Accuracy, Isolation Amplifier

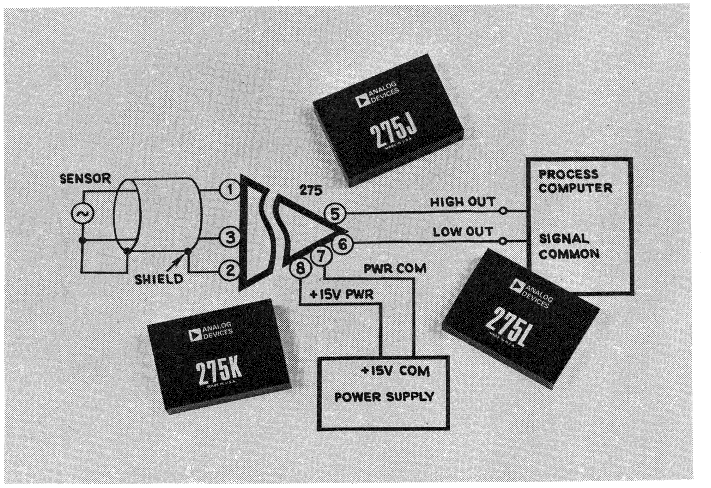
MODEL 275

FEATURES

- 3-Port Isolation with ±2500V CMV
- 120dB min CMR at 60Hz: Fully Guarded Inputs
- ±10V Input/Output Dynamic Range
- Gain Adjustable: 1 to 100V/V, Single Resistor
- Low Nonlinearity Error: ±0.05% max (275L)
- Low Offset Drift: ±5μV/°C max (275L)
- Meets MIL-STD-202E Environmental Testing
- Low Cost

APPLICATIONS

- Process Signal Isolator
- Interface Buffer
- Floating Off-Ground Signal Measurements
- High Voltage Instrumentation Amplifier
- Current Shunt Measurements



GENERAL DESCRIPTION

Model 275 represents a new generation of high performance isolation amplifiers featuring 3-port isolation and improved high accuracy specifications for instrumentation and industrial applications. This new design offers ±2500V total ground isolation between inputs and outputs (or power inputs) as well as ±200V dc isolation between outputs and power inputs. Incorporating a fully guarded input, common mode rejection at 60Hz and 1kΩ source imbalance is guaranteed to be 120dB min with typical performance of 150dB at dc. The low coupling capacitance between inputs and output yields a ground leakage current of less than 8μA at a 115V ac 60Hz. In addition to the high ±2.5kV CMV rating, the differential input is protected for 125V rms (±600V peak) overloads.

Three accuracy selections are available offering guaranteed low nonlinearity error at 20V p-p output; 275L: 0.1% max, 275K: 0.15% max and 275J: 0.2% max. Lower nonlinearity error is also guaranteed at 10V p-p output; 275L: 0.05% max, 275K: 0.1% max, 275J: 0.15% max.

Using modulation techniques with transformer isolation (see Figure 1, Block Diagram) for reliable operation, these new models offer ±10V input and output signal dynamic range.

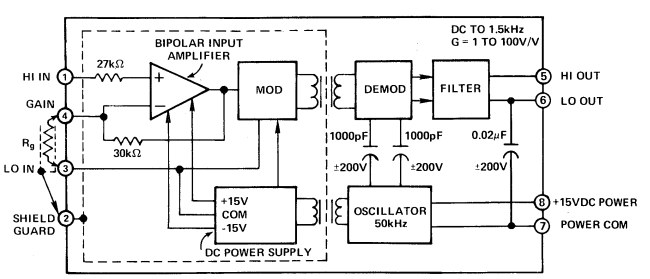


Figure 1. Block Diagram – Model 275

Other unique features of model 275 include single resistor gain adjustment over the range 1 to 100V/V and input offset voltage drift guaranteed for each model; 275L: 5μV/°C max, 275K: 15μV/°C max, and 275J: 25μV/°C max (G = 100V/V). Ideal for portable equipment, model 275 will operate from a single dc supply at any voltage from +12V to +18V, requiring only 15mA current.

Single-resistor gain adjustment, 3-port isolation, high CMV and CMR ratings, as well as input overload protection, combine to make these new isolators an excellent choice for all critical interface applications; high voltage instrumentation, process signal isolators, current shunt measurements, pH control systems and computer interface systems.

HIGH RELIABILITY

Model 275 isolators are conservatively designed, compact, low profile (0.88″ height), epoxy encapsulated modules capable of reliable operation in harsh environments. These models are designed to meet MIL-STD-202E environmental testing; high humidity, vibration, shock, temperature cycling, etc. (see ENVIRONMENTAL SPECIFICATIONS). Model 275 offers excellent noise immunity to EMI/RFI radiation from motors, relays and power line frequencies, thereby enabling measurements to be performed in noisy industrial environments

SPECIFICATIONS (typical @ +25°C and +15V dc unless otherwise noted)

MODEL		275K	275L
GAIN (NON INVERTING)			
Range (50kΩ Load)[1]	1 to 100V/V	*	*
Formula	1 + (30kΩ/R_g)	*	*
Deviation from Formula	-0, +4%	*	*
vs. Temperature[2] (0 to +70°C)	±0.008%/°C max	±0.004%/°C max	±0.004%/°C max
vs. Temperature[2] (0 to +70°C)	±0.015%/°C max	±0.01%/°C max	±0.01%/°C max
Nonlinearity[3], ±5V Output	±0.15% max	±0.1% max	±0.05% max
Nonlinearity[3], ±10V Output	±0.2% max	±0.15% max	±0.1% max
INPUT VOLTAGE RATINGS			
Linear Differential Range	±10V min	*	*
Max Safe Differential Input			
Continuous	125V rms	*	*
Pulse, 5ms Duration, One Pulse/Sec	±600V pk	*	*
Max CMV, Inputs to Outputs/Power Common			
ac, 60Hz, 1 Minute Duration	3000V rms	*	*
Continuous, ac or dc	±2500V pk max	*	*
CMR, Inputs to Outputs, 60Hz, $R_S \leq 5k\Omega$			
Balanced Source Impedance	126dB	*	*
1kΩ Source Impedance Imbalance	120dB min	*	*
CMR, Inputs to Guard, 60Hz			
1kΩ Source Impedance Imbalance	75dB	*	*
Max Leakage Current, Inputs to Common			
115V ac, 60Hz	8μA rms max	*	*
OFFSET VOLTAGE, REFERRED TO INPUT			
Initial, @ +25%°C (Adjustable to Zero)	±(4 + 46/G)mV max	*	*
vs. Temperature (0 to +70°C)			
Gain = 1V/V	±300μV/°C max	±200μV/°C max	±100μV/°C max
Gain = 100V/V	±25μV/°C max	±15μV/°C max	±5μV/°C max
At Other Gains (μV/°C max)	±(23 + 277/G)	±(13 + 187/G)	±(4 + 96/G)
vs. Supply Voltage	±(1 + 50/G)μV/V	*	*
INPUT IMPEDANCE			
Differential	$10^8\Omega$‖3pF	*	*
Overload	27kΩ	*	*
Common Mode	$10^{11}\Omega$‖100pF	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ +25°C	±7nA max	*	*
vs. Temperature (0 to +70°C)	±0.1nA/°C	*	*
INPUT NOISE			
Voltage, Gain = 100V/V			
0.01Hz to 10Hz	5μV p-p	*	*
10Hz to 1kHz	1.5μV rms	*	*
Current			
0.01Hz to 10Hz	1pA p-p	*	*
FREQUENCY RESPONSE			
Small Signal, -3dB, Gain = 100V/V	1.5kHz	*	*
Full Power, 20V p-p Output	300 Hz	*	*
Slew Rate	0.15V/μs	*	*
RATED OUTPUT			
Voltage, 50kΩ Load[4]	±10V min	*	*
Output Impedance	1.5kΩ	*	*
Max CMV, Outputs to Power Inputs			
Peak ac or dc Continuous	±200V	*	*
POWER SUPPLY – SINGLE POLARITY[5]			
Voltage, Rated Performance	+ 15V dc	*	*
Voltage, Operating	+(12 to 18)V dc	*	*
Current, Quiescent	+15mA	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	*
Storage	-55°C to +85°C	*	*
CASE DIMENSIONS	3.5" x 2.5" x 0.88"	*	*

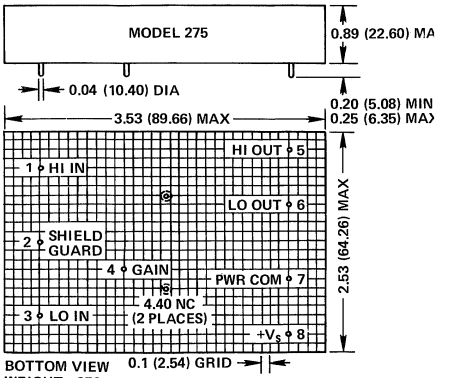
*Specifications same as model 275J

[1] Gains up to 1000V/V may be selected by the user with derated performance.
[2] Gain temperature drift is specified as % of output voltage.
[3] Gain nonlinearity error is specified as % of peak-to-peak output voltage span. (see Figure 2).
[4] For 2kΩ loads, consider model 285 isolation amplifier.
[5] Recommended power supply, ADI model 904, ±15V @ 50mA output

Specifications subject to change without notice.

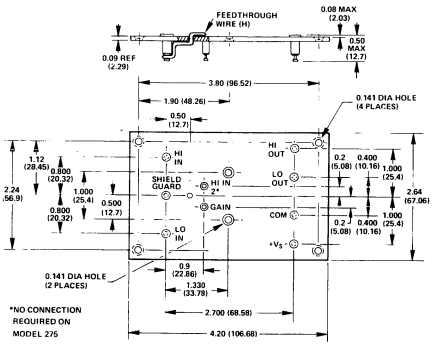
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



WEIGHT: 250 gms.

SHIELDED MOUNTING SOCKET AC1007



BOTTOM VIEW
WEIGHT: 50 gms.

GUARDING TECHNIQUES

Careful design and packaging of model 275 has yielded extremely high CMR and CMV ratings. To preserve the high CMR, care should be taken to keep the capacitance balanced about the input terminals and guard the gain setting resistor, R_g, for gains less than 5V/V. A recommended shielding technique is illustrated in Figure 10, using model AC1007 mounting socket. This socket is recommended to reduce noise, pick-up, and CMR degradation from stray capacitance. Solder feed-through wire (H) to the socket shield pin and copper foil surface. Module will cover shield from further exposure.

Best CMR performance will be achieved by using twisted, shielded cable to reduce inductive and capacitive pickup. To reduce effective cable capacitance, cable shield should be connected to the common mode signal source. This is accomplished by connecting the shield as close as possible to signal low, as shown in Figure 10. To avoid ground loops, signal low or cable shield should never be grounded at more than one point.

such as electric power and electro-chemical plants. When placed between transducers and delicate monitoring equipment (computers, chart recorders, etc.), these isolators will interrupt ground loops, leakage paths and damaging high voltage transients for improved system protection.

ENVIRONMENTAL SPECIFICATIONS

The reliability of instrumentation and control systems is becoming more important as the systems being controlled or measured become more complex and more expensive. To provide the reliability needed to protect plant and personnel during environmental stresses (vibration, humidity, temperature, etc.), model 275 has been designed to meet the environmental requirements of MIL-STD-202E testing, as shown in Table 1. These conditions closely simulate those seen in typical industrial applications. As an additional assurance of high performance reliability, every model 275 is factory tested for CMV rating by application of 1800V rms (2500V peak) between input and output terminals for one minute.

All Units Meet the Requirements of MIL-STD-202E as Outlined Below

TEST	METHOD	CONDITION
High Temperature Storage	108A	D (Non-Operating)
Moisture Resistance	106D	(10 Days)
Solderability	208C	
Thermal Shock	107D	A (5 Cycles)
Terminal Strength	211A	A (Pull Test; 10 lbs)
Temperature Cycling	102A	D (-55°C/+85°C)
Vibration	204C	B (15g Peak)
Barometric Pressure	105C	B (50,000 Feet)

TABLE 1. Environmental Specifications

PERFORMANCE CHARACTERISTICS

Gain Nonlinearity: Nonlinearity error is presented as a % of peak-to-peak output voltage span; e.g. ±0.05% @ 10V p-p output = ±5mV max RTO nonlinearity error. Model 275 is available in three nonlinearity selections; 0.05% (275L), 0.1% (275K) and 0.15% (275J) – max, @ 10V p-p output span. Nonlinearity error is also specified and guaranteed at 20V p-p output span; 0.1%, 0.15% and 0.2% max. The curves of Figure 2 illustrate typical nonlinearity error over the entire output voltage range to 20V p-p (±10V). At output levels less than 10V p-p (±5V), nonlinearity error is typically much better than ±0.1% for both models 275J and 275K. Appropriate gain should be selected for best performance.

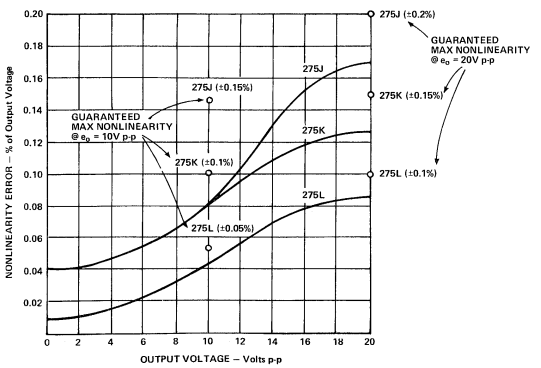


Figure 2. Gain Nonlinearity Error vs. Output Voltage

Common Mode Rejection: CMR is rated at 115V ac, 60Hz and 1kΩ source imbalance for all gains from 1 to 100V/V. CMR typically improves by 10dB above the specified minimum at a gain of 100V/V. As a function of frequency, CMR response approaches 150dB at dc for all gains. (see Figure 3).

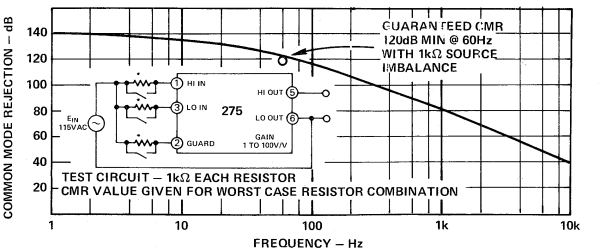


Figure 3. Common Mode Rejection vs. Frequency

Input Offset Voltage Drift: Model 275 is available in three drift selections; 5μV/°C (275L), 15μV/°C (275K), and 25μV/°C (275J) – max, RTI, G = 100V/V. Total input drift is composed of two sources, (input and output stage drifts) and is gain dependent. The curves of Figure 4 illustrate worst case total input drift over the gain range of 1 to 100V/V. Max limits at G = 1V/V and G = 100V/V are also shown.

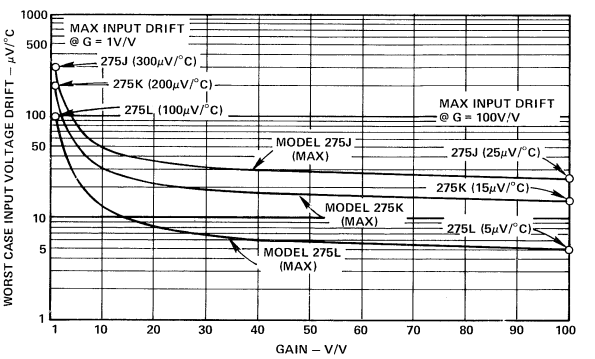


Figure 4. Input Offset Voltage Drift (Worst Case) vs. Gain

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 5. RMS voltage noise is shown in a bandwidth from 0.01Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.01Hz to 1kHz is 10μV p-p @ G = 100V/V. This value is derived by multiplying the rms value at f = 1kHz shown in Figure 5 (1.5μV rms) by 6.6. For best noise performance in particular applications, a low pass filter at the output can be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest (see Figure 10B). Increasing gain will also reduce input noise.

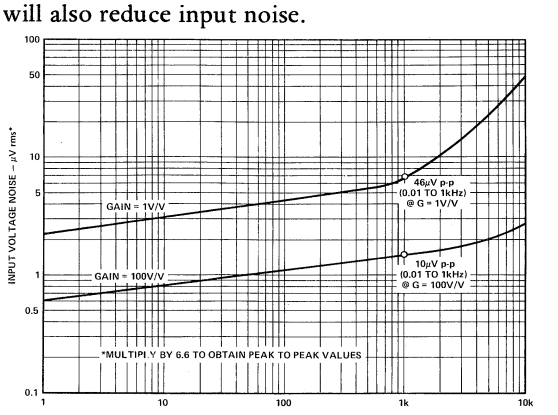


Figure 5. Input Voltage Noise vs. Bandwidth

APPLICATIONS IN INSTRUMENTATION AND PROCESS CONTROL

Interface Buffer Amplifier: Isolators are used in complex industrial systems to control, measure and interface other segments of the manufacturing/process operation and provide protection against damage caused by high voltage transients as well as continuous fault voltages. Model 275's unique three port isolation capability not only provides protection against high input common mode voltages (±2000V dc continuous), but also offers protection against high output common mode voltages (±200V dc continuous, form HI OUT and LO OUT, to POWER COM). In the computer interface application of Figure 6, model 275 will protect both the input sensor and power supply from computer faults causing ac line voltage to simultaneously appear at both output terminals of model 275.

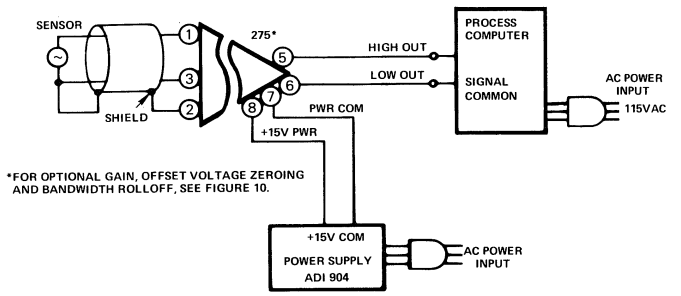


Figure 6. Computer Interface Buffer

Current Shunt Measurements: Model 275's high CMV (±2.5kV) and differential input protection (±600V peak pulse) makes it particularly suitable for measuring SCR gate-to-cathode voltages typical in motor-control circuits (see Figure 7). The isolator's wide bandwidth (dc to 1.5kHz) and single resistor gain adjustment (1V/V to 100V/V) provide the performance required to accurately measure low level current signals from typical 50mV and 100mV shunts.

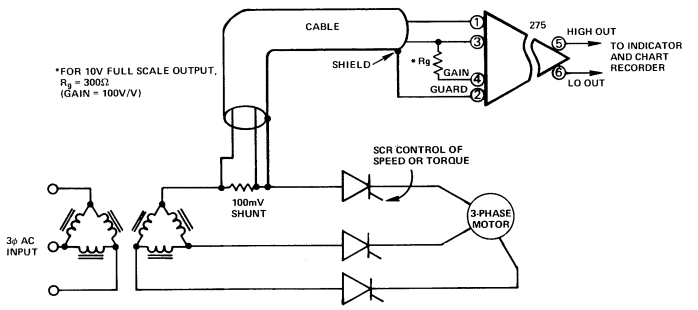
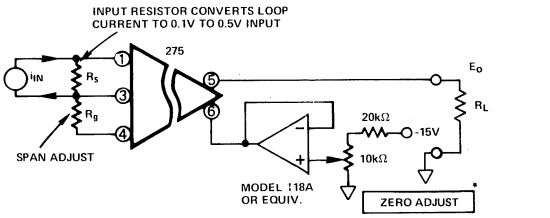


Figure 7. Motor Current Monitor Application

Process Signal Isolator: Model 275 can be easily applied in process control loops to interface standard process signals (e.g. 1 to 5mA, 4 to 20mA, 10 to 50mA, etc.) and convert them to standard, zero based voltage signals (e.g. 0 to +10V). A typical hook-up of model 275 is illustrated in Figure 8, showing input current resistor (R_S), full scale span adjustment (R_g) and a zero adjust pot. The table lists typical values for standard process signals, assuming a 0 to +10V output span is desired. Model 275's high 60Hz CMR rating (120dB min) and high CMV isolation (±2kV dc) permits interfacing with long control loops typical in industrial plant applications.



Loop Current i_{IN}	Input Resistor R_S	Span Resistor R_g	Output Span E_o
1 - 5mA	100Ω	1.24kΩ	0 to +10V
4 - 20mA	25Ω	1.24kΩ	0 to +10V
10 - 50mA	10Ω	1.24kΩ	0 to +10V

Figure 8. Process Signal Isolator, Showing Resistor Values for Typical Process Signal Levels

Bridge Transducer Amplifier: Model 275 offers total ground isolation with simplified two wire hook-up for low-level, floating signal measurements such as remote balanced bridge circuits (see Figure 9). Only differential current flows between the High Input and Low Input terminals of model 275, eliminating a third-wire for bias current return (required with all other types of amplifiers). The 100MΩ differential input impedance of model 275 will not load the bridge circuit. High CMV rating permits the bridge to be floated up to ±2kV dc with respect to power ground.

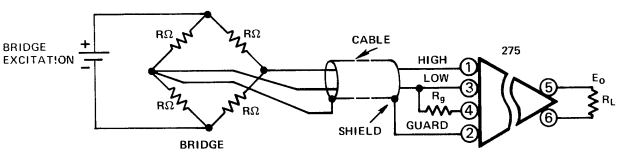


Figure 9. Bridge Transducer Amplifier

ISOLATOR INTERCONNECTION

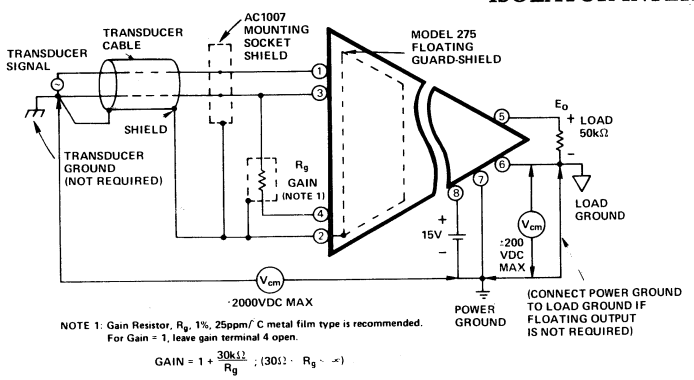


Figure 10A. Transducer, Power, Gain Resistor, and Shielding Interconnection

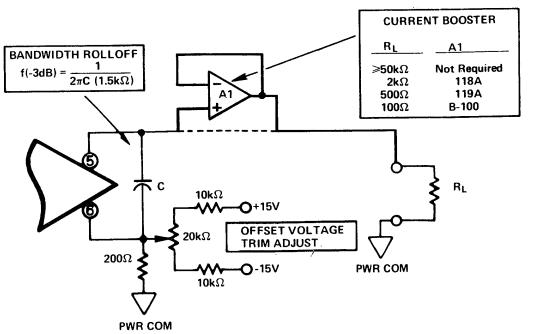


Figure 10B. Optional Connections: Offset Voltage Trim Adjust, Bandwidth (-3dB) Rolloff and Current Booster Amplifier

Precision Isolation Amplifier
High CMV/CMR, ±15V Floating Power

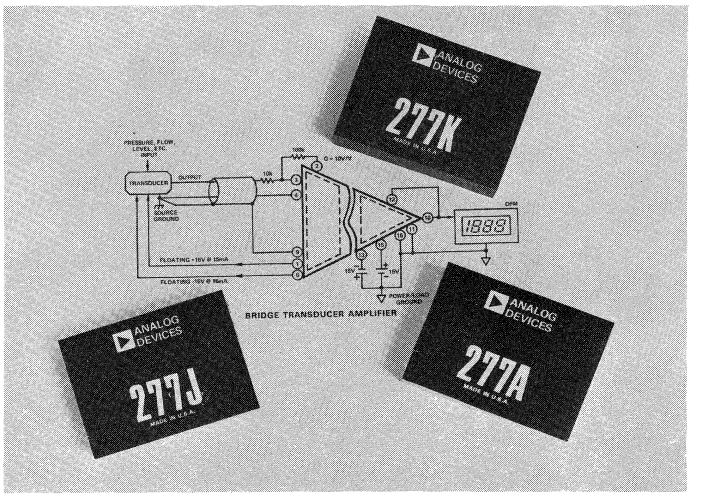
MODEL 277

FEATURES

Versatile Op Amp Front End: Inverting, Non-Inverting, Differential Applications
Low Nonlinearity: 0.025% max, Model 277K
Low Input Offset Voltage Drift: 1μV/°C max, Model 277K
Floating Power Supply: ±15V dc @ ±15mA
High CMR: 160dB min @ dc
High CMV: 3500V_{rms}

APPLICATIONS

Programmable Gain Isolated Amplifier
Isolated Power Source and Amplifier for Bridge Measurements
Instrumentation Amplifier
Instrumentation Grade Process Signal Isolator
Current Shunt Measurements



GENERAL DESCRIPTION

Model 277 is a versatile isolation amplifier which combines a high-performance, uncommitted operational amplifier front end with a precision, isolated output stage and a floating power supply section. This configuration, shown in Figure 1, makes the 277 ideally suited to instrumentation applications where the need for various forms of signal conditioning, high CMV protection and isolated transducer power requirements are encountered.

The input stage is a low drift (±1μV/°C max, model 277K) differential op amp that may be connected for use in inverting, non-inverting and differential configurations. The circuitry employed around the operational amplifier input stage can be designed by the user to suit each application's particular signal processing needs. A full ±10V signal range is available at the output of the front end amplifier.

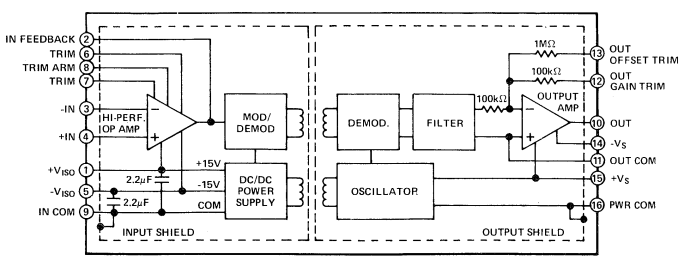


Figure 1. Model 277 Functional Block Diagram

The isolated output stage includes a special modulator/demodulator technique which provides the 277 with 160dB minimum dc common mode rejection between input and output common and an input-to-output CMV rating of 3500V_{rms}. When combined with the output stage's low nonlinearity (0.05%, models 277J/A and 0.025% model 277K), these high CMR and CMV ratings facilitate accurate measurements in the presence of noisy electrical equipment such as motors and relays. In addition, model 277A offers a -25°C to +85°C rated operating temperature range. All versions of model 277 have a ±10 volt output range.

The floating power supply section provides isolated ±15 volt outputs capable of delivering currents up to ±15mA. This feature permits model 277 to power transducers and auxilliary isolated circuitry, thereby eliminating the need for a separate isolated dc/dc converter.

All of the features of the model 277 isolation amplifier are packaged in a compact (3″ x 2.2″ x 0.59″) module. As an assurance of high performance reliability, every model 277 is factory tested for CMV rating by application of 3500V_{rms} (±4900V peak) between input and output common terminals for one minute (meets NEMA and CSA requirements for 660V_{rms} service.) In addition, the 277 has a calculated MTBF of 133,000 hours.

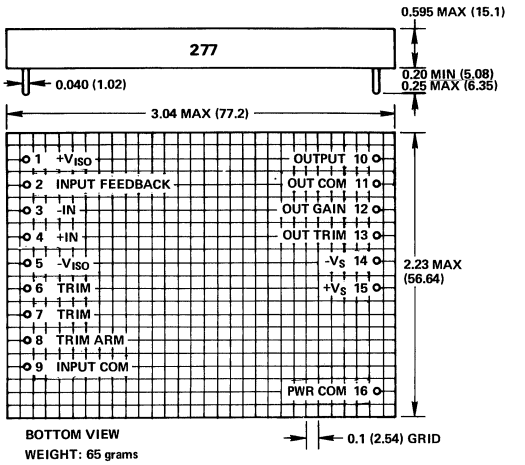
SPECIFICATIONS (typical at +25°C and ±15V unless otherwise noted)

MODEL	277J	277K	277A
INPUT STAGE PERFORMANCE[1,2]			
OPEN LOOP GAIN	106dB min	*	*
INPUT OFFSET VOLTAGE			
Initial, @ +25°C (Adjustable to Zero)	±1.5mV max	*	*
vs. Temperature			
Offset Untrimmed	±5μV/°C max	*	±5μV/°C
Offset Trimmed to Zero	±3μV/°C max	±1μV/°C max	*
vs. Supply Voltage	±30μV/V	*	*
vs. Time	±3.5μV/mo	*	*
INPUT BIAS CURRENT			
Initial, @ +25°C	±20nA max	*	*
vs. Temperature	±50pA/°C	*	*
vs. Supply Voltage	±100pA/V	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ +25°C	±6nA	*	*
vs. Supply Voltage	±50pA/V	*	*
INPUT IMPEDANCE			
Differential	4MΩ	*	*
Common Mode[3]	100MΩ‖4pF	*	*
INPUT NOISE			
Voltage, 0.01Hz to 10Hz	1μV p-p	*	*
10Hz to 1kHz	3μV rms	*	*
Current, 0.01Hz to 10Hz	35pA p-p	*	*
INPUT VOLTAGE RANGE			
Common Mode Voltage[3]	±10V min	*	*
Common Mode Rejection[3], CMV = ±10V, 60Hz	100dB	*	*
Max Safe Differential Voltage	±13V	*	*
ISOLATED POWER SUPPLY[4]			
Voltage/Current[2]	±15V @ ±15mA max	*	*
Load Regulation (No Load – Full Load)	+0, -6%	*	*
Line Regulation	1V/V	*	*
Ripple, Full Load	30mV p-p @ 70kHz	*	*
OUTPUT STAGE PERFORMANCE			
GAIN	1V/V	*	*
Gain Error	±0.5% max	*	*
vs. Temperature	±50ppm/°C max	*	*
Nonlinearity, ±10V Output	±0.05% max	±0.025% max	*
VOLTAGE RATINGS[5]			
Max CMV, Output Com/Input Com			
ac, 60Hz, 1 Minute	$3500V_{rms}$ max	*	*
Nonrecurring Spike (<1 Second)	±5000V pk max	*	*
Peak ac or dc, Continuous	±2500V max	*	*
CMR, Output Com/Input Com[5]			
dc	160dB min	*	*
60Hz	120dB min	*	*
Leak. Cur., Input/output $115V_{rms}$, 60Hz	1μA rms max	*	*
ISOLATION IMPEDANCE[5]			
Input Com/Output Com	$10^{12}Ω‖16pF$	*	*
OUTPUT OFFSET VOLTAGE			
Initial, @ +25°C (Adjustable to Zero)	±10mV max	*	*
vs. Temperature	±100μV/°C max	±50μV/°C max	±100μV/° C max
vs. Supply Voltage	±1mV/V	*	*
vs. Time	±100μV/mo	*	*
FREQUENCY RESPONSE			
Small Signal, -3dB	2.5kHz	*	*
Full Power, 20V p-p Output	1.5kHz	*	*
Settling Time ±10V Step to 0.1%	1ms	*	*
RATED OUTPUT			
Voltage/Current	±10V min @ ±5mA min	*	*
OUTPUT NOISE			
Voltage, 0.01Hz to 10Hz	7μV p-p	*	*
10Hz to 1kHz	25μV rms	*	*
POWER SUPPLY			
Voltage, Rated Performance	±15V dc	*	*
Voltage, Operating	±(14 to 16)V dc	*	*
Current, Quiescent	+35, -5mA	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-25°C to +85°C
Operating	-25°C to +85°C	*	*
Storage	-55°C to +85°C	*	*
CASE SIZE	3.0" x 2.2" x 0.59"	*	*

NOTES:
[1] Current drawn from INPUT FEEDBACK terminal must be ≤5mA.
[2] Total current drawn from IN FEEDBACK and either $+V_{ISO}$ or $-V_{ISO}$ must be ≤15mA.
[3] Input common mode specifications are measured at +IN and -IN terminals with respect to INPUT COM.
[4] Protected for momentary shorts to IN COM.
[5] Isolation specifications are measured at INPUT COM with respect to OUT COM and PWR COM.
*Specifications same as model 277J.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



MATING SOCKET – AC1053

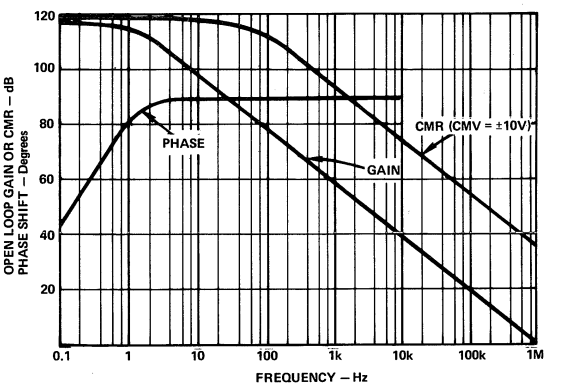


Figure 2. Input Stage Gain, CMR and Phase vs. Frequency

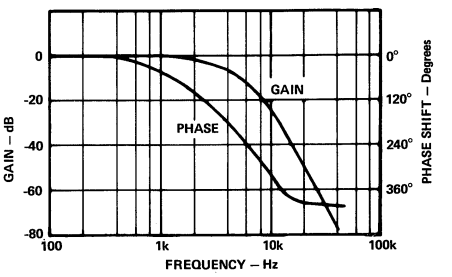


Figure 3. Output Stage Gain and Phase vs. Frequency

PERFORMANCE CHARACTERISTICS

Gain Nonlinearity: Nonlinearity error is expressed as a % of peak-to-peak output voltage span; e.g. ±0.05% @ 10V p-p output = ±5mV max RTO nonlinearity error. Model 277 is available in two maximum nonlinearity grades — ±0.05% (277J/A), ±0.025% (277K).

The nonlinearity of model 277 is virtually independent of output voltage swing. Therefore, the 277 can be used at any level of gain and output signal range up to ±10V while maintaining its excellent linearity characteristics.

Output Voltage Noise: Peak-to-peak output voltage noise is dependent on bandwidth, as shown in Figure 4. The graph shows RTO noise, that is, output noise for a gain of 1V/V through the isolator. For lowest noise performance, a low pass filter at the output can be used to roll-off noise and undesired signal frequencies beyond the bandwidth of interest. As gain increases, voltage noise referred-to-input decreases, resulting in higher input signal to noise ratios. The next section demonstrates how voltage noise, referred-to-input, can be calculated.

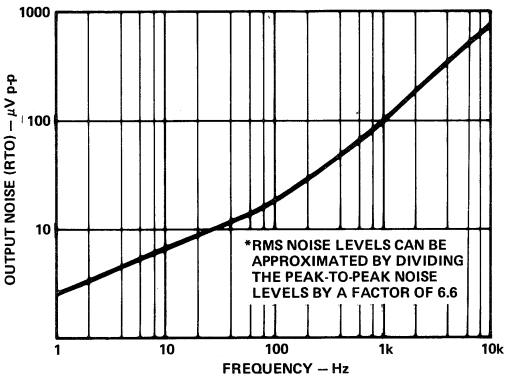


Figure 4. Output Voltage Noise vs. Bandwidth

RTI Offset Voltage, Drift and Noise: Offset voltage, referred to input (RTI) for model 277 may be computed by treating the isolator as two cascaded amplifier stages. The input stage has variable gain G_1 while the output isolation stage has a fixed gain of 1. RTI offset is given by:

$$E_{OS}\ (RTI) = E_{OS_1} + E_{OS_2}/G_1$$

where: E_{OS_1} = total input stage offset voltage
E_{OS_2} = output stage offset voltage
G_1 = input stage gain

Offset voltage drift, RTI, may be calculated in the same manner.

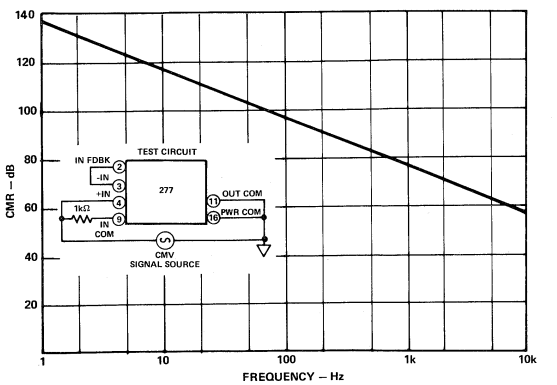


Figure 5. Input-to-Output CMR vs. Frequency with 1kΩ Source Imbalance

RTI noise, in a given bandwidth, (for Figure 8a) may be calculated as follows:

$$E_N\ (rms, RTI) = \sqrt{E_{N_1}^2 + (E_{N_2}/G_1)^2}$$

where: E_{N_1} = total rms input stage voltage noise
E_{N_2} = rms output voltage noise (RTO)

Common Mode Rejection: A 160dB rejection of potential differences between input and output common is achieved in model 277 by maintaining low coupling capacitance between the input and output stages. Input-to-output rejection is a function of frequency as shown in Figure 5 under the adverse condition of 1kΩ in series with IN COM. CMR versus frequency for the input stage is shown in Figure 2.

The section on GUARDING TECHNIQUES & INTERCONNECTION demonstrates how to calculate total CMR error for the isolator and indicates the precautions to be taken to preserve the model 277's inherently excellent CMR performance.

GUARDING TECHNIQUES & INTERCONNECTION

Model 277 CMR performance is best preserved by using shielded signal cable with the shield connected as close as possible to signal low and IN COM to reduce pickup (see Figure 6).

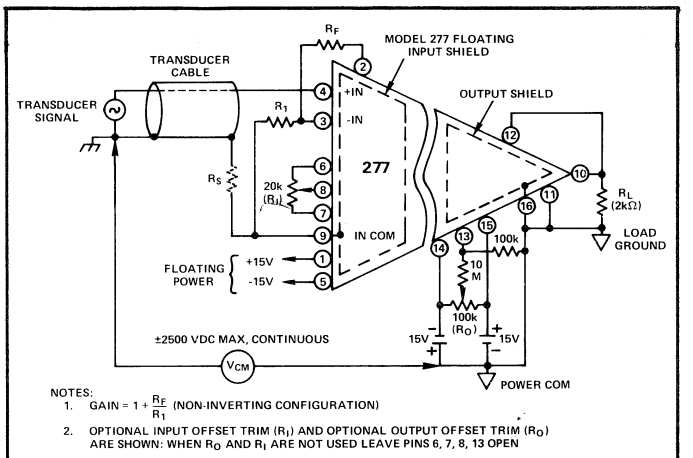


Figure 6. Transducer, Power, Gain Resistors, and Shielding Interconnection

Overall CMR error at the output (e_{err}) is due to the CMR of the input amplifier and the CMR between input and output stages and is given by:

$$e_{err} = \frac{e_{cm}}{CMR_{IN}}\ (G_1) + \frac{e_{IO}}{CMR_{IO}}$$

where: e_{cm} = input amp CMV with respect to IN COM
e_{IO} = CMV between OUT COM and signal ground
CMR_{IN} = CMR of the input op amp
CMR_{IO} = CMR from input IN COM to OUT COM
G_1 = input stage gain

To preserve CMR_{IN}, amplifier source impedances should be balanced with respect to IN COM. Components connected to the input should be enclosed by a shield tied to IN COM to reduce CMR_{IO} degradation due to unguarded capacitance to ground.

High CMR_{IO} is maintained with low capacitance between IN COM and OUT COM. For best CMR performance, printed circuit layouts should minimize stray capacitance between input and output stages. *Do not run a ground plane under the isolator since this increases input-output coupling.* CMR_{IO} also degrades

at high frequencies by resistance (R_S) between IN COM and signal ground. Voltage between OUT COM and source ground divides between this resistance (generally wire resistance) and the input-to-output capacitance resulting in an input error signal. If R_S becomes excessive, a capacitor from +IN to OUT COM will help compensate for its effect on CMR. The capacitor must withstand the isolation voltages encountered.

ADJUSTMENT PROCEDURE

The input and output offset voltage of model 277 can be trimmed as shown below with the isolator set up in the desired circuit configuration.

(1) Refer to Figure 6 for terminal and component designations.
(2) Connect IN COM to OUT COM and set input signal to zero.
(3) Place floating DVM across IN FDBK and OUTPUT terminals.
(4) Null DVM reading using output offset trim potentiometer R_O.
(5) Disconnect IN COM from OUT COM.
(6) Place DVM across IN FDBK and IN COM terminals.
(7) Adjust input offset trim potentiometer, R_I, until DVM reads zero volts.

The overall gain of the isolator may be increased over a limited range (5%) with a 5kΩ potentiometer connected between pins 10 and 12.

APPLICATIONS

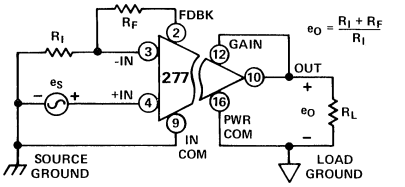
Programmable Gain Bridge Transducer Amplifier: The versatility of model 277 is shown by the programmable gain bridge transducer amplifier application of Figure 7. In this circuit the 277's uncommitted front end and floating voltage output permit both bridge excitation and signal gain conditioning to be provided by the isolation amplifier.

Control switches are driven by TTL inputs which are isolated from source ground by the opto-isolators in the control switch. Control signals operate the CMOS switch network to establish the gains shown in the table in Figure 7. The CMOS switch network is operated in a manner that causes the resistance of the switches only to be in series with the negative input of the isolator and not in series with the gain setting resistors. With this arrangement the switch resistance does not affect gain accuracy. A resistor, R_B, should be in series with -IN to reduce errors due to bias current drift.

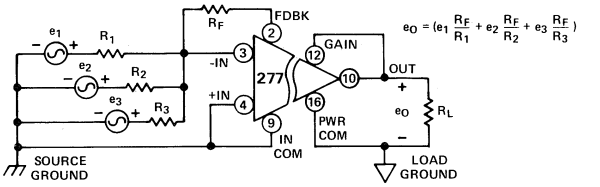
With this circuit the isolator gain can be remotely set at a value that optimizes input signal-to-noise ratio and eliminates the need for high quality post-amplifiers at the isolator output. This network is extremely useful in wide dynamic range measurements such as flow, level or pressure where auto-gain ranging would be a desirable system instrumentation feature.

INPUT CONFIGURATION

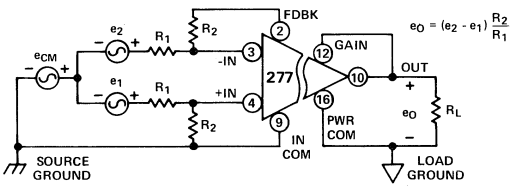
Model 277's input stage is an isolated, uncommitted operational amplifier that may be configured to suit a variety of applications. Model 277 may be used in the same way as any op amp except that the feedback is taken from the FDBK terminal rather than the OUTPUT pin. Figure 8 shows four typical input configurations for interfacing with a wide range of signal sources.



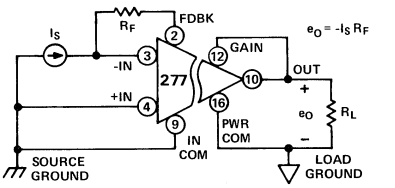
(a) Non-Inverting Configuration



(b) Summing Configuration

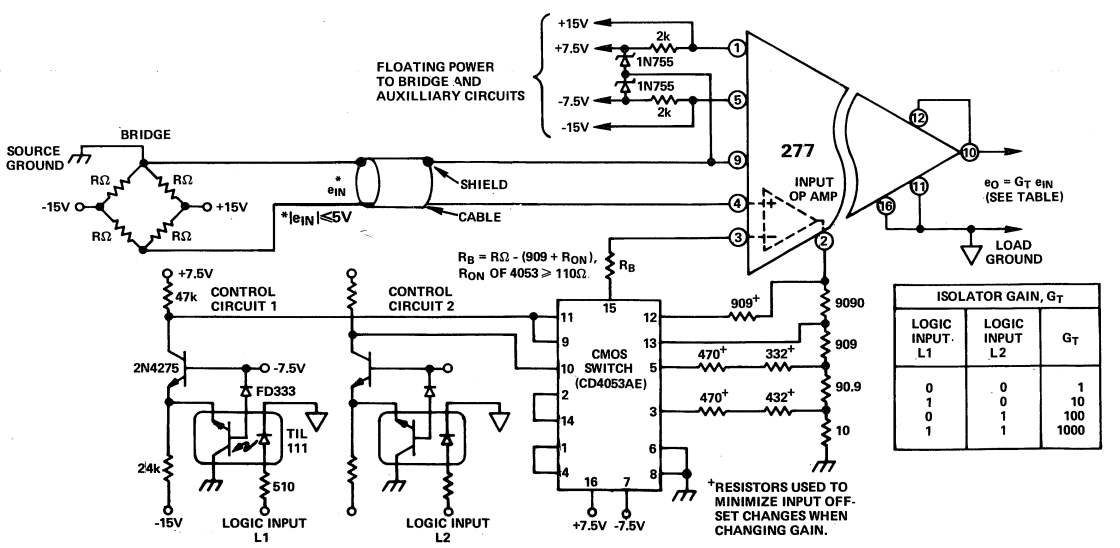


(c) Isolated Differential Configuration



(d) Current Source Amplifier Configuration

Figure 8. Model 277 Input Amplifier Configurations



ISOLATOR GAIN, G_T		
LOGIC INPUT L1	LOGIC INPUT L2	G_T
0	0	1
1	0	10
0	1	100
1	1	1000

Figure 7. Programmable Gain Bridge Transducer Amplifier

Economy, High Performance, Self Contained, Isolation Amplifier

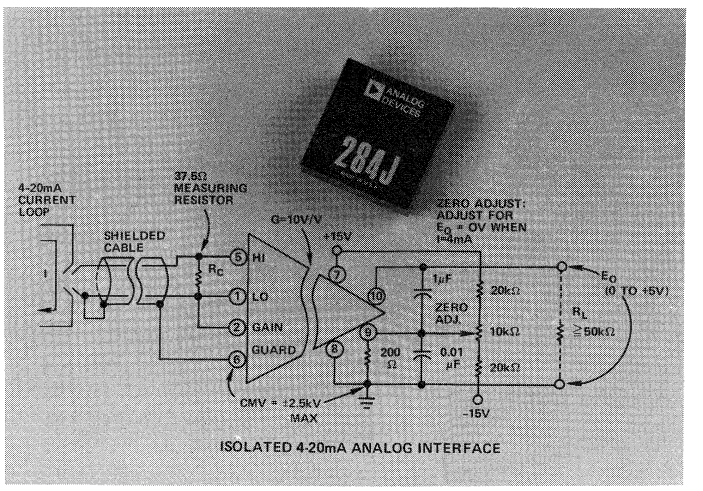
MODEL 284J

FEATURES

Low Cost
Low Nonlinearity: ±0.05% @ 10V pk-pk Output
High Gain Stability: ±0.0075%/°C, ±0.001%/1000 hours
Isolated Power Supply: ±8.5V dc @ ±5mA
High CMR: 110dB min with 5kΩ Imbalance
High CMV: ±5000V_{pk}, 10ms Pulse; ±2500V dc continuous
Small Size: 1.5″ x 1.5″ x 0.6″
Adjustable Gain: 1 to 10V/V; Single Resistor Adjust
Meets IEEE Std 472: Transient Protection (SWC)
Meets UL Std 544 Leakage: 2.0μA max @ 115V ac, 60Hz

APPLICATIONS

Biomedical and Patient Monitoring Instrumentation
Ground Loop Elimination in Industrial Control
Off-Ground Signal Measurements
4-20mA Isolated Current Loop Receiver



ISOLATED 4-20mA ANALOG INTERFACE

GENERAL DESCRIPTION

Model 284J is a low cost isolation amplifier featuring isolated power, ±8.5V dc @ ±5mA loads, ±2500V dc off-ground isolation (CMV) and 110dB minimum CMR at 60Hz, 5kΩ source imbalance, in a compact 1.5″ x 1.5″ x 0.6″ epoxy encapsulated package. This improved design achieves low nonlinearity of ±0.05% @ 10V pk-pk output, gain stability of ±0.0075%/°C and input offset drift of ±15μV/°C at G=10V/V. Using modulation techniques with reliable transformer isolation, model 284J will interrupt ground loops, leakage paths and high voltage transients to ±5kV_{pk} (10ms pulse) providing dc to 1kHz (-3dB) response over an adjustable gain range of 1V/V to 10V/V. Model 284J's fully floating guarded input stage and floating isolated power for external input circuitry, offers versatility for both medical and industrial OEM applications.

WHERE TO USE MODEL 284J

Medical Applications: In all biomedical and patient monitoring equipment such as multi-lead ECG recorders and portable diagnostic designs, model 284J offers protection from lethal ground fault currents as well as 5kV defibrillator pulse inputs. Low level bioelectric signal recording is achieved with model 284J's low input noise (8μV p-p) and high CMR (110dB, min).

Industrial Applications: In computer interface systems, process signal isolators and high CMV instrumentation, model 284J offers complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface is afforded with model 284J's 10V pk-pk input signal capability at a gain of 1V/V operation. In portable field designs, model 284J's single supply, low power drain of 85mW @ +12V operation offers long battery operation.

DESIGN FEATURES AND USER BENEFITS

Isolated Power: Dual ±8.5V dc @ ±5mA, completely isolated from the input power terminals (±2500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers and remote transducers such as thermistors or bridges.

Adjustable Gain: Model 284J's adjustable gain combined with its 10V pk-pk output signal dynamic range offers compatibility with a wide class of input signals. A single external resistor enables gain adjustment from 1V/V to 10V/V providing the flexibility of applying model 284J in both high level transducer interfacing as well as low level sensor measurements.

Floating, Guarded Front-End: The input stage of model 284J can directly accept floating differential signals, such as ECG biomedical signals, or it may be configured as a high performance instrumentation front-end to accept signals having CMV with respect to input power common.

High Reliability: Model 284J is a conservatively designed, compact module, capable of reliable operation in harsh environments. Model 284J has a calculated MTBF of over 400,000 hours and is designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). As an additional assurance of reliability, every model 284J is factory tested for CMV and input ratings by application of 5kV pk, 10ms pulses, between input terminals as well as input/output terminals.

SPECIFICATIONS (typical @ 25°C and V_S = +15V dc unless otherwise noted)

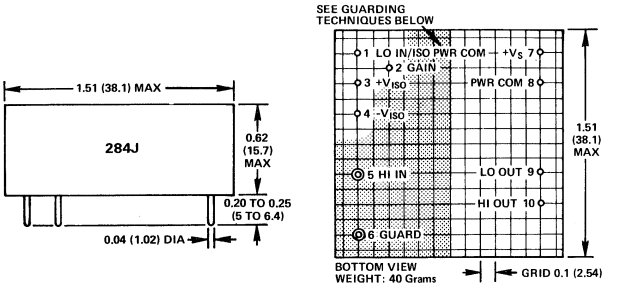
MODEL	284J
GAIN (NON-INVERTING)	
Range (50kΩ Load)	1 to 10V/V
Formula	Gain = $[1 + \frac{100k\Omega}{10.7k\Omega + R_i(k\Omega)}]$
Deviation from Formula	±3%
vs. Time	±0.001%/1000 Hours
*vs. Temperature (0 to +70°C)[1]	±0.0075%/°C
*Nonlinearity, G = 1V/V to 10V/V[2]	±0.05%
INPUT VOLTAGE RATINGS	
Linear Differential Range, G = 1V/V	±5V min
Max Safe Differential Input	
Continuous	$240V_{rms}$
Pulse, 10ms duration, 1 pulse/10 sec	$\pm 6500V_{pk}$ max
Max CMV, Inputs to Outputs	
AC, 60Hz, 1 minute duration	$2500V_{rms}$
Pulse, 10ms duration, 1 pulse/10 sec	$\pm 2500V_{pk}$ max
With 510kΩ in series with Guard	$\pm 5000V_{pk}$ max
Continuous, ac or dc	$\pm 2500V_{pk}$ max
CMR, Inputs to Outputs, 60Hz, $R_S \leq 5k\Omega$	
Balanced Source Impedance	114dB
5kΩ Source Impedance Imbalance	110dB min
CMR, Inputs to Guard, 60Hz	
1kΩ Source Impedance Imbalance	78dB
Max Leakage Current, Inputs to Power Common @ 115V ac, 60Hz	2.0μA rms max
INPUT IMPEDANCE	
Differential	$10^8\ \Omega \| 70pF$
Overload	300kΩ
Common Mode	$5x10^{10}\ \Omega \| 20pF$
INPUT DIFFERENCE CURRENT	
Initial, @ +25°C	±7nA max
vs. Temperature (0 to +70°C)	±0.1nA/°C
INPUT NOISE	
Voltage, G = 10V/V	
0.05Hz to 100Hz	8μV p-p
10Hz to 1kHz	10μV rms
Current	
0.05Hz to 100Hz	5pA p-p
FREQUENCY RESPONSE	
Small Signal, -3dB, G = 1V/V to 10V/V	1kHz
Slew Rate	25mV/μs
Full Power, 10V p-p Output	
Gain = 1V/V	700Hz
Gain = 10V/V	200Hz
Recovery Time, to ±100μV after Application of $\pm 6500V_{pk}$ Differential Input Pulse	200ms
OFFSET VOLTAGE REFERRED TO INPUT	
*Initial, @ +25°C, Adjustable to Zero	±(5 + 20/G)mV
*vs. Temperature (0 to +70°C)	±(1 + 150/G)μV/°C
vs. Supply Voltage	±1mV/%
RATED OUTPUT	
Voltage, 50kΩ Load	±5V min
Output Impedance	1kΩ
Output Ripple, 1MHz Bandwidth	5mV pk-pk
ISOLATED POWER OUTPUTS	
Voltage, ±5mA Load	±8.5V dc
Accuracy	±5%
Current	±5mA min
Regulation, No Load to Full Load	+0, -15%
Ripple, 100kHz Bandwidth	100mV p-p
POWER SUPPLY, SINGLE POLARITY[3]	
Voltage, Rated Performance	+15V dc
Voltage Operating	+(8 to 15.5)V dc
Current, Quiescent	+10mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +85°C
CASE DIMENSIONS	1.5" x 1.5" x 0.62"

*Improved performance over earlier design.
[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3] Recommended power supply, ADI model 904, ±15V @ 50mA output

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

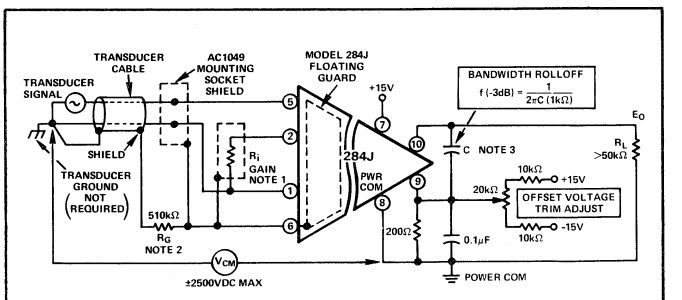


SHIELDED MOUNTING SOCKET AC1049

INTERCONNECTION AND GUARDING TECHNIQUES

Model 284J can be applied directly to achieve rated performance as shown in Figure 1 below. To preserve the high CMR performance of model 284J, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 284J as illustrated in the outline drawing above (screened area). The GUARD (Pin 6) should be connected to this shield. This guard-shield is provided with the mounting socket, model AC1049. A recommended guarding technique using model AC1049 is illustrated in Figure 1. To reduce effective cable capacitance, cable shield should be connected to the common mode signal source by connecting the shield as close as possible to the signal low.

Offset Voltage Trim Adjust: The trim adjust circuit shown in Figure 1 can be used to zero the output offset voltage over the gain range from 1 to 10V/V. The output terminals, HI OUT and LO OUT, can be floated with respect to PWR COM up to $\pm 50V_{pk}$ max, offering three-port isolation. A 0.1μF capacitor is required from LO OUT to PWR COM whenever the output terminals are floated with respect to PWR COM. LO OUT can be connected directly to PWR COM when output offset trimming is not required.



NOTE 1. GAIN RESISTOR, R_i, 1%, 50ppm/°C METAL FILM TYPE IS RECOMMENDED.
FOR GAIN = 1V/V, LEAVE TERMINAL 2 OPEN.
FOR GAIN = 10V/V, SHORT TERMINAL 2 TO TERMINAL 1

$$\text{GAIN} = 1 + \frac{100k\Omega}{10.7k\Omega + R_i(k\Omega)}$$

NOTE 2. GUARD RESISTOR, R_G, REQUIRED ONLY FOR CMV > $\pm 2500V_{PK}$ ($\pm 5kV_{PK}$ MAX).
R_G MAY BE MOUNTED ON AC1049 MOUNTING SOCKET USING STANDOFF PROVIDED.
(USE ¼ WATT, 5%, CARBON COMPOSITION TYPE; ALLEN BRADLEY RECOMMENDED).

NOTE 3. OUTPUT FILTER CAPACITOR, C, SELECT TO ROLLOFF NOISE AND OUTPUT RIPPLE: (e.g. SELECT C = 1.5μF FOR dc TO 100Hz BANDWIDTH).

Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of model 284J is derived from the carrier isolation technique which is used to transfer both signal and power between the amplifier's guarded input stage and the rest of the circuitry. The block diagram for model 284J is shown in Figure 2 below.

The 320kΩ input protection resistor limits the differential input current during periods of input amplifier saturation and also limits the differential fault current to approximately 35μA in case the preamplifier fails.

The bipolar input preamplifier operates single-ended (noninverting). Only a difference bias current flows with zero net bias current. A third wire return path for input bias current is not required. Gain can be set from 1V/V to 10V/V by changing the gain resistor, R_i. *To preserve high CMR, the gain resistor must be guarded.* Best performance is achieved by shorting terminal 2 to terminal 1 and operating model 284J at a gain of 10V/V.

For powering floating input circuitry such as buffer amplifiers, instrumentation amplifiers, calibration signals and transducers, dual isolated power is provided. High CMV isolation is achieved by the low-leakage transformer coupling between the input preamplifier, modulator section and the output circuitry. Only the 20pF leakage capacitance between the floating guarded input section and the rest of the circuitry keeps the CMR from being infinite.

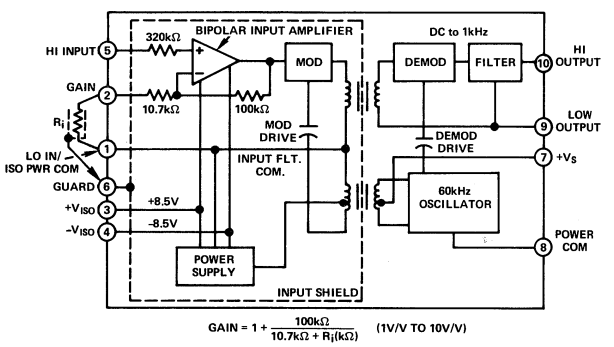


Figure 2. Block Diagram – Model 284J

INTERELECTRODE CAPACITANCE, TERMINAL RATINGS AND LEAKAGE CURRENTS LIMITS

Capacitance: Interelectrode terminal capacitance arising from stray coupling capacitance effects between the input terminals and the signal output terminals are each shunted by leakage resistance values exceeding 50kMΩ. Figure 3 illustrates the CMR ratings at 60Hz and 5kΩ source imbalance between signal input/output terminals, along with their respective capacitance.

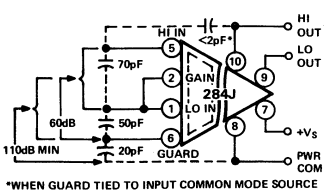


Figure 3. Model 284J Terminal Capacitance and CMR Ratings

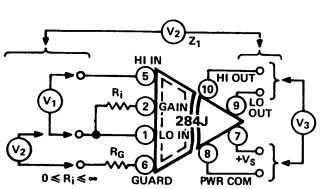


Figure 4. Model 284J Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac or dc peak ratings. Pulse ratings are intended to support defibrillator and other transient voltages. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 4 and Table 1 illustrate model 284J's ratings between terminals.

SYMBOL	RATING	REMARKS
V1 (pulse)	$\pm 6500V_{PK}$ (10ms)	Withstand Voltage, Defibrillator
V1 (cont.)	$\pm 240V_{RMS}$	Withstand Voltage, Steady State
V2 (pulse)	$\pm 2500V_{PK}$ (10ms) $R_G = 0$	Transient
V2 (pulse)	$\pm 5000V_{PK}$ (10ms) $R_G = 510k\Omega$	Isolation, Defibrillator
V2 (cont.)	$\pm 2500V_{PK}$	Isolation, Steady State
V3 (cont.)	$\pm 50V_{PK}$	Isolation, DC
Z1	50kMΩ‖20pF	Isolation Impedance

Table 1. Isolation Ratings Between Terminals

Leakage Current Limits: The low coupling capacitance between inputs and output yields a ground leakage current of less than 2.0μA rms at 115V ac, 60Hz (or 0.02μA/V ac). As shown in Figure 5, the transformer coupled modulator signal, through stray coupling, also creates an internally generated leakage current of about 5μA rms @ 60kHz. Line frequency leakage current levels are unaffected by the power on or off condition of model 284J.

For medical applications, model 284J is designed to improve on patient safety current limits proposed by F.D.A., U.L., A.A.M.I. and other regulatory agencies. (e.g. model 284J complies with leakage requirements for the Underwriters Laboratory STANDARD FOR SAFETY, MEDICAL AND DENTAL EQUIPMENT as established under UL544 for type A and B patient connected equipment – reference *Leakage Current*, paragraph 27.5).

In patient monitoring equipment, such as ECG recorders, model 284J will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. Using passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

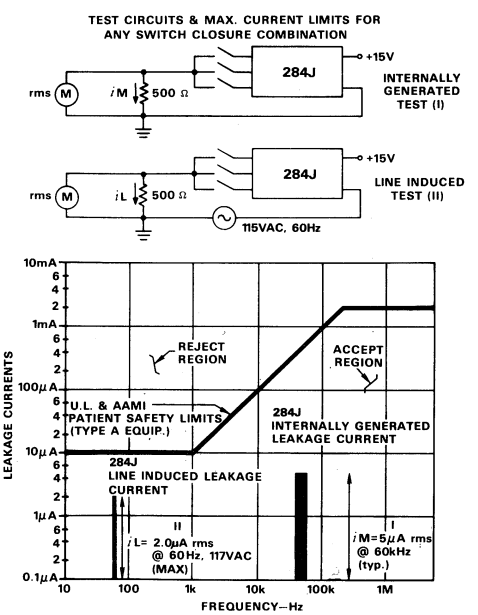


Figure 5. Model 284J Leakage Current Performance from Line Induced and Internally Generated (Modulator) Operating Conditions

PERFORMANCE CHARACTERISTICS

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 5kΩ imbalance at a gain of 10V/V. Figure 6 illustrates CMR performance as a function of signal frequency. CMR approaches 146dB at dc with source imbalances as high as 5kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V, CMR is typically 6dB lower than at a gain of 10V/V.

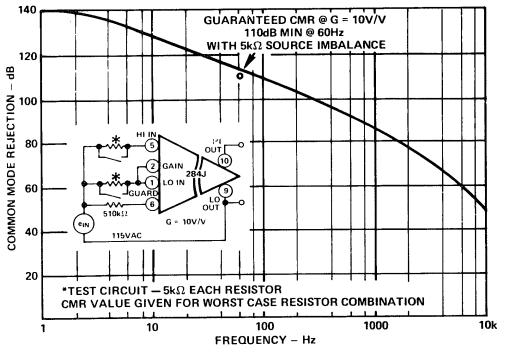


Figure 6. Common Mode Rejection vs. Frequency

Figure 7 illustrates the effect of source imbalance on CMR performance at 60Hz and Gain = 10V/V. CMR is typically 120dB at 60Hz and a balanced source. CMR is maintained greater than 80dB for source imbalances up to 100kΩ.

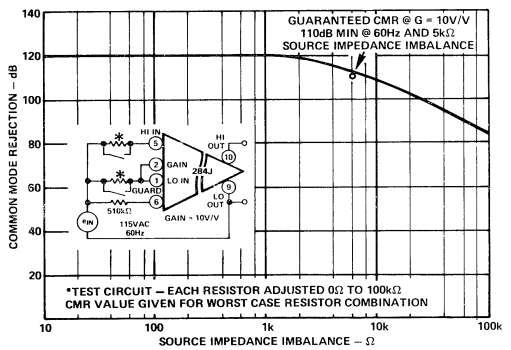


Figure 7. Common Mode Rejection vs. Source Impedance Imbalance

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 8. RMS voltage noise is shown in a bandwidth from 0.05Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is 8μV pk-pk at a gain of 10V/V. This value is derived by multiplying the rms value at f = 100Hz shown in Figure 8 (1.2μV rms) by 6.6.

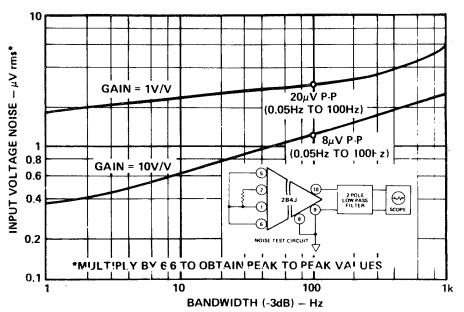


Figure 8. Input Voltage Noise vs. Bandwidth

For lowest noise performance, a low pass filter at the output should be used to selectively roll-off noise, output ripple and undesired signal frequencies beyond the bandwidth of interest (see note 3, Figure 1).

Input Offset Voltage Drift: Total input voltage drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 9 illustrates the total input voltage drift over the gain range of 1 to 10V/V.

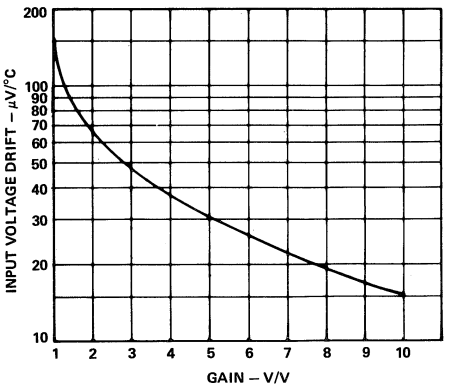
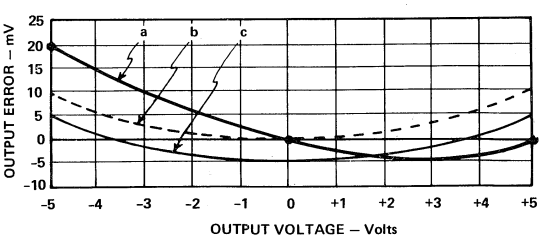


Figure 9. Input Offset Voltage Drift vs. Gain

Gain Nonlinearity: Linearity error is defined as the peak deviation of the output voltage from the best straight line and is specified as a % of peak-to-peak output voltage span; e.g. nonlinearity of model 284J operating at an output span of 10V pk-pk (±5V) is ±0.05% or ±5mV. In applying model 284J, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error over the operating output voltage span. A calibration technique illustrating how to minimize output error is shown below. In this example, model 284J is operating over an output span of +5V to -5V and a gain of 5V/V.

GAIN AND OFFSET TRIM PROCEDURE

1. Apply e_{IN} = 0 volts and adjust R_O for e_O = 0 volts.
2. Apply e_{IN} = +1.000V dc and adjust R_G for e_O = +5.000V dc.
3. Apply e_{IN} = −1.000V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one half that measured in step 3 (see curve b).
5. Apply e_{IN} = +1.000V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).



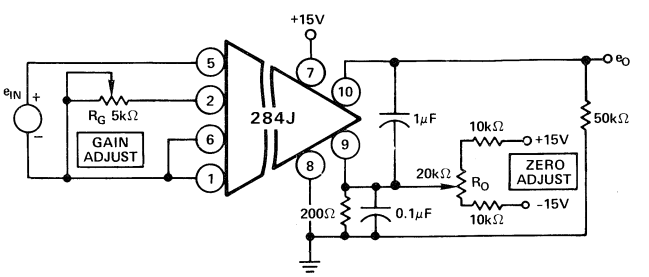


Figure 10. Gain and Offset Adjustment

GROUNDING PRACTICES

The more common sources of electrical noise arise from ground loops, electrostatic coupling and electromagnetic pickup. The guidelines listed below pertain to guarding low level, millivolt signals in hostile environments such as current shunt signals in "heavy industrial" plants.

Guidelines:

- Use twisted shielded cable to reduce inductive and capacitive pickup.
- Drive the transducer cable shield, S, with the common mode signal source, E_G, to reduce the effective cable capacitance as shown in Figure 11 below. This is accomplished by connecting the shield point S, as close as possible to the transducer signal low point B. This may not always be possible. In some cases the shield may be separated from signal low by a portion of the medium being measured (e.g. pressure transducer). This will cause a common mode signal, E_M, to be generated by the medium between the shield and the signal low. The 78dB CMR capability of model 284J between the input terminals (HI IN and LO IN) and GUARD, will work to suppress the common mode signal, E_M.
- To avoid ground loops and excessive hum, signal low, B, or the transducer cable shield, S, should never be grounded at more than one point.
- Dress unshielded leads short at the connection terminals and reduce the area formed by these leads to minimize inductive pickup.

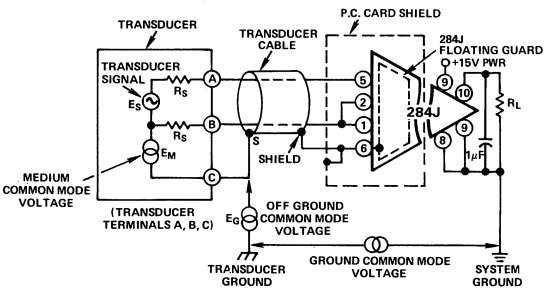


Figure 11. Transducer- Amplifier Interconnection

Isolated Power and Output Voltage Swing: Model 284J offers a floating power supply providing ±8.5V dc outputs with ±5mA output current rating. As shown in Figure 12, the minimum voltage output for $\pm V_{ISO}$, as well as the maximum load capability, is dependent on the input power supply, $+V_S$. Figure 12 also illustrates the typical output voltage range as both input supply, $+V_S$, and the isolated supply loads, $\pm I_L$, are varied. At ±5mA isolated load and V_S = +15V dc, model 284J can provide an output voltage swing of ±7.5V.

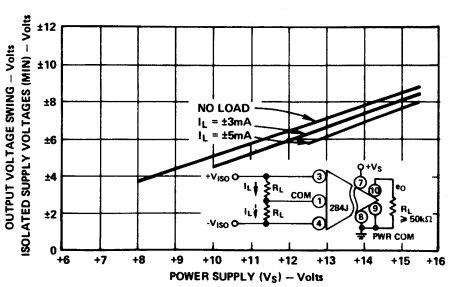


Figure 12. Isolated Power ($\pm V_{ISO}$) and Output Voltage Swing ($\pm E_O$) Versus Power Supply Input (V_S)

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Remote Sensor Interface: In chemical, nuclear and metal processing industries, model 284J can be applied to measure and control off-ground millivolt signals in the presence of ±2500V dc CMV signals. In interface applications such as pH control systems of on-line process measurement systems such as pollution monitoring, model 284J offers complete galvanic isolation to eliminate troublesome ground loop problems. Isolated power outputs and adjustable gain add to the application flexibility of this model.

Figure 13 illustrates how model 284J can be combined with a low drift, 1μV/°C max, front-end amplifier, model AD510K, to interface low level transducer signals. Model 284J's isolated ±8.5V dc power and front-end guard eliminate ground loops and preserve high CMR (114dB @ 60Hz).

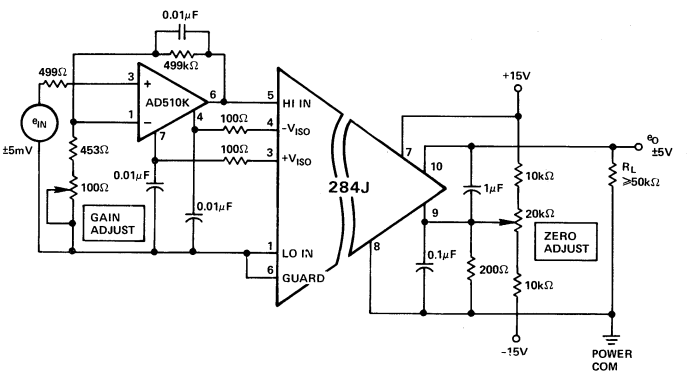


Figure 13. Input Signal Conditioning Using Isolated Power for Transducer Buffer Amplifier

Instrumentation Amplifier: Model 284J provides a floating guarded input stage capable of directly accepting isolated differential signals. The non-inverting, single-ended input stage offers simple two wire interconnection with floating input signals.

In applications where the isolated power is applied to transducers such as bridges which generate differential input signals with common mode voltages measured with respect to the isolated power common, model 284J can be connected as shown in Figure 14. To achieve high CMR with respect to the ISO PWR COM, the following trim procedure is recommended.

CMR Trim Procedure

1) Connect a 1V pk-pk oscillator between the +IN/-IN and IN COM terminals as shown in Figure 14.
2) Set the input frequency at 0.5Hz and adjust R1 for minimum e_O.
3) Set the input frequency at 60Hz and adjust R2 for minimum e_O.
4) Repeat steps 2 and 3 for best CMR performance.

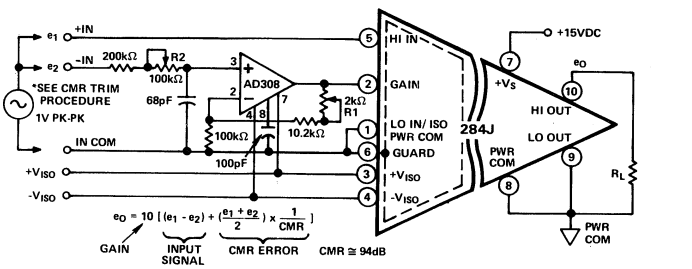


Figure 14. Application of 284J as Instrumentation Amplifier

APPLICATIONS IN BIOMEDICAL DESIGNS

Cardiac Monitoring: Heart signals can be masked by muscle noise, electrochemical noise, residual electrode voltages and 60Hz power line pickup. To achieve high performance in cardiac monitoring, model 284J's design provides high CMR in the dc to 100Hz bandwidth and substantial source impedance — to 5kΩ. An especially demanding ECG requirement is that of fetal heart monitoring as illustrated in Figure 15. The low input noise of model 284J and the dual CMR ratings are exploited in this application to extract the fetal ECG signals. The separation between the mother's and the fetal heartbeat is enhanced by the 78dB of CMR between the input electrodes and guard, while the 110dB of CMR from input to output ground screens out 60Hz pickup and other external interference.

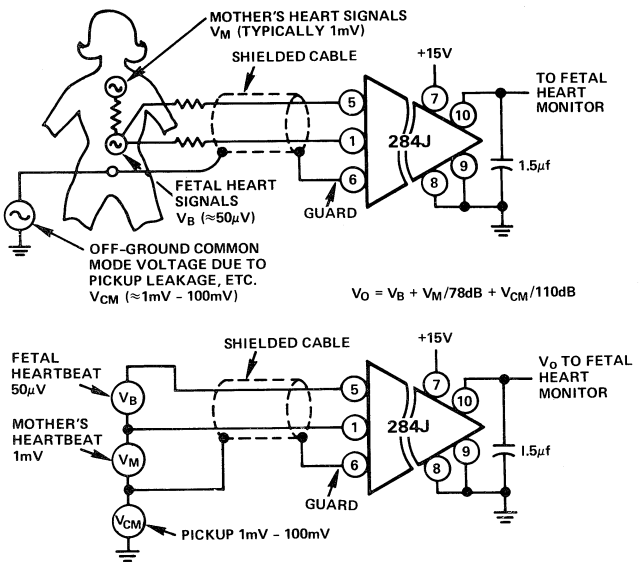


Figure 15. Fetal Heartbeat Monitoring

Single Lead ECG Recorder with Leads Off Indicator: In single lead applications model 284J offers simple two-wire hook-up to the ECG signal as illustrated in Figure 16. The floating signal can be connected directly to the HI IN and LO IN terminals using the GUARD tied to the patients' right leg for best CMR performance. Using the isolated power from model 284J an inexpensive calibration signal is easily provided. In ECG applications, model 284J provides a simple means to determine whenever a "Leads-Off" condition exists at the input. A "Leads-Off" condition ($R_S = \infty$) will cause the HI OUT terminal to be at a negative output saturation level; i.e. e_O = -8.5V to -9.5V @ V_S = +15V.

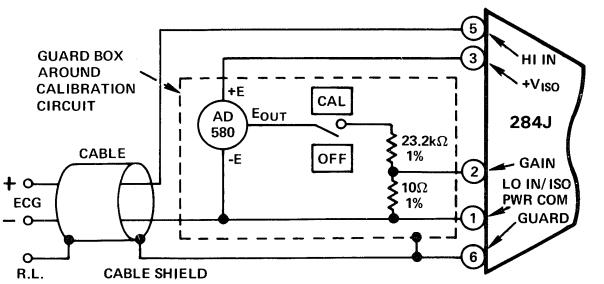


Figure 16. Single Lead ECG Recorder with 1mV Calibration Circuit and Leads Off Indicator

Multi-Lead ECG Recorder with Right Leg Drive: The small size, economy and isolated power makes model 284J an ideal isolation amplifier for application in clinical ECG recorders. Figure 17 illustrates how this new isolator can be applied in a high performance, portable multi-lead ECG recorder. In this application, model 284J's input is configured as an instrumentation amplifier with high CMR to the floating input common. The right leg drive offers improved CMR between input and isolated common by driving to zero any CMV existing between these points. The isolated power, $\pm V_{ISO}$, is used to drive the lead buffer amplifiers and the front-end, 1mV calibration signal.

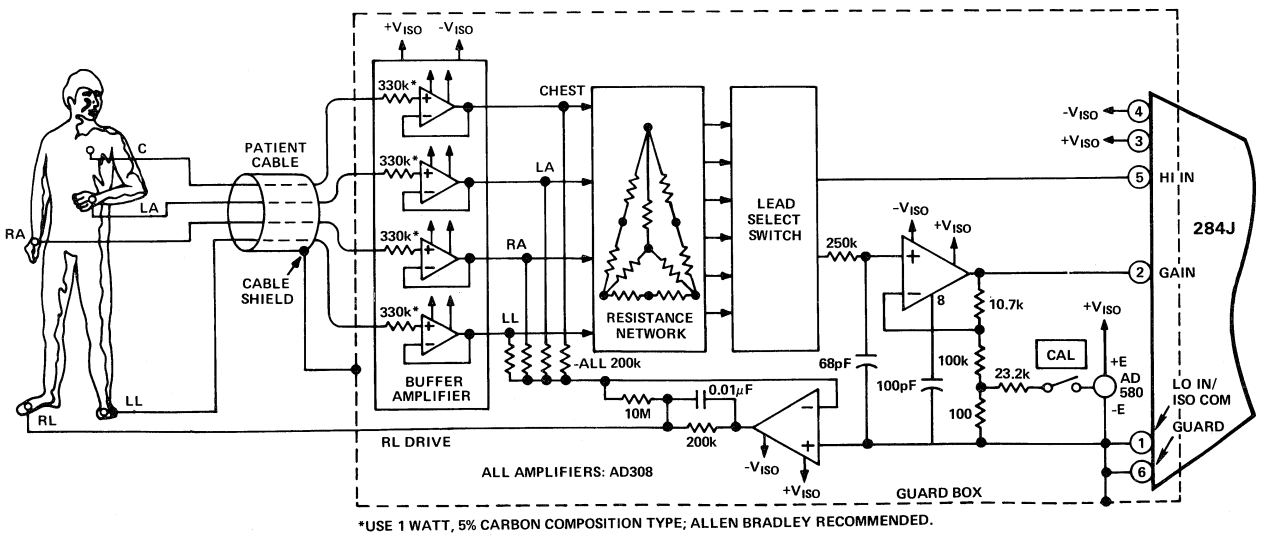


Figure 17. Multi-Lead ECG Recorder Application Using Model 284J with Right Leg Drive Output

Fully Adjustable, High CMV High Accuracy, Isolation Amplifier

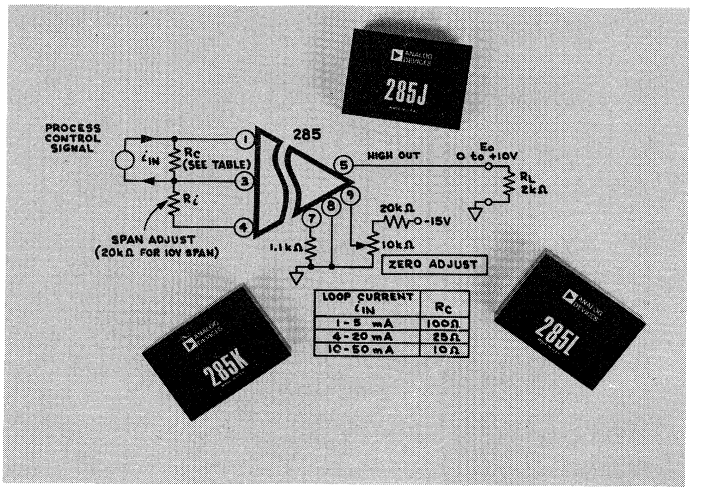
MODEL 285

FEATURES

- 3000V_{rms}, 60Hz, 1 minute Input/Output Isolation
- 115dB min CMR at 60Hz: Fully Guarded Inputs
- ±5mA Output Current (2kΩ Loads)
- ±10V Input/Output Dynamic Range
- Gain Adjustable: 1 to 1000V/V
- Low Nonlinearity Error: ±0.03% max (285L)
- Low Offset Drift: ±5μV/°C max (285L)
- Meets MIL-STD-202E Environmental Testing
- Bandwidth and Offset Voltage Adjustable

APPLICATIONS

- Process Control Isolator
- Interface Buffer
- Floating Off-Ground Signal Measurements
- High Voltage Instrumentation Amplifier
- Current Shunt Measurements



GENERAL DESCRIPTION

Models 285J, 285K and 285L are high performance isolation amplifiers featuring improved high accuracy specifications, high isolation/input protection ratings and ±5mA output current capability for instrumentation and industrial applications. This new design offers 3000V_{rms} (1 minute) total ground isolation between inputs and outputs combined with a full ±10V input/output dynamic range for output loads up to 2kΩ. Gain, bandwidth, and output offset voltage are adjustable, making model 285 the most versatile, high performance isolator available on the market.

Incorporating a fully guarded input, common mode rejection at 60Hz and 1kΩ source imbalance is guaranteed to be 115dB min with typical performance of 140dB at dc. The low coupling capacitance between inputs and output yields a ground leakage current of less than 8μA rms at 115V ac 60Hz. In addition to the high 3kV CMV rating, the differential input is protected for 125V_{rms} (±600V peak) overloads.

Three accuracy selections are available offering guaranteed low nonlinearity error; 285L: 0.1% max, 285K: 0.15% max and 285J: 0.2% max. Lower nonlinearity error is also guaranteed when output gain is set at 10V/V; 285L: 0.03% max; 285K: 0.04% max, 285J: 0.05% max.

Using modulation techniques with transformer isolation (see Figure 1, Block Diagram) for reliable operation, these new models offer adjustable gain, 1 to 1000V/V, using only one external gain resistor. Input offset voltage drift is guaranteed for each model; 285L: 5μV/°C max, 285K: 10μV/°C max and 285J: 15μV/°C max (G = 100V/V).

Adjustable gain, ±10V @ ±5mA min output capability, high CMV and CMR ratings as well as input overload protection, combine to make these new isolators an excellent choice for all critical interface applications: high voltage instrumentation, process signal isolators, current shunt measurements, pH control systems and computer interface systems.

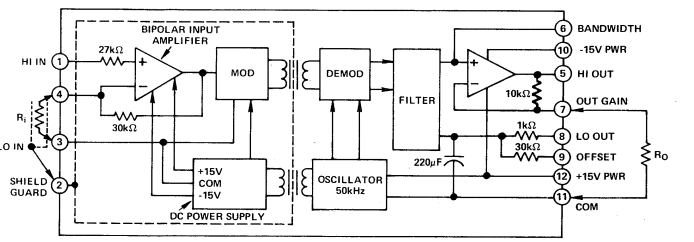


Figure 1. Block Diagram – Model 285

HIGH RELIABILITY

Model 285 isolators are conservatively designed, compact, low profile (0.88″ height), epoxy encapsulated modules capable of reliable operation in harsh environments. These models are designed to meet MIL-STD-202E environmental testing; high humidity, vibration, shock, temperature cycling, etc. (see ENVIRONMENTAL SPECIFICATIONS). Model 285 offers excellent noise immunity to EMI/RFI radiation from motors, relays and power line frequencies, thereby enabling measurements to be performed in noisy industrial environments such as electric power and electro-chemical plants. When placed between transducers and delicate monitoring equipment (computers, chart recorders, etc.), these isolators will interrupt ground loops, leakage paths and damaging high voltage transients for improved system protection.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	285J	285K	285L
GAIN (NON-INVERTING)			
Range (2kΩ Load)	1 to 1000V/V	*	*
Formula[1]	$(1 + \frac{30k\Omega}{R_i})(1 + \frac{10k\Omega}{R_o})$	*	*
Deviation from Formula	-0, +4%	*	*
vs. Temperature[2] (0 to +70°C)	±0.008%/°C	±0.004%/°C	±0.004%/°C
vs. Temperature[2] (0 to +70°C)	±0.015%/°C max	±0.01%/°C max	±0.01%/°C max
Nonlinearity[3], G_O = 10V/V	±0.05% max	±0.04% max	±0.03% max
Nonlinearity[3], G_O = 1V/V	±0.2% max	±0.15% max	±0.1% max
INPUT VOLTAGE RATINGS			
Linear Differential Range	±10V min	*	*
Max Safe Differential Input rms, Continuous	125V rms	*	*
Max CMV, Inputs to Outputs			
AC, 60Hz, 1 minute	$3000V_{rms}$ max	*	*
Nonrecurring Spike (<1 second)	±5000V max	*	*
Peak ac or dc, Continuous	±2500V max	*	*
CMR, Inputs to Outputs, 60Hz			
Balanced Source Impedance	120dB	*	*
1kΩ Source Impedance Imbalance	115dB min	*	*
CMR, Inputs to Guard, 60Hz			
1kΩ Source Impedance Imbalance	75dB	*	*
Max Leakage Current, Inputs to Common			
115V ac, 60Hz	8μA rms, max	*	*
INPUT IMPEDANCE			
Differential	$10^8\Omega \| 3pF$	*	*
Overload	27kΩ	*	*
Common Mode	$10^{11}\Omega \| 100pF$	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ +25°C	±7nA max	*	*
vs. Temperature (0 to +70°C)	±0.1nA/°C	*	*
INPUT NOISE			
Voltage, Gain = 100V/V (G_O = 10V/V)			
0.01Hz to 10Hz	4μV p-p	*	*
10Hz to 1kHz	3μV rms	*	*
Current			
0.01Hz to 10Hz	0.2pA p-p	*	*
FREQUENCY RESPONSE			
Small Signal, -3dB, G_O = 1V/V	2.5kHz	*	*
Full Power, 20V p-p Output			
G_O = 1V/V; G_i = 1 to 100V/V	300Hz	*	*
G_O = 10V/V; G_i = 1 to 100V/V	2kHz	*	*
Slew Rate, G_O = 10V/V	0.12V/μs	*	*
OFFSET VOLTAGE REFERRED TO INPUT			
Initial, @ +25°C (Adjustable to Zero)	$\pm(20 + \frac{2}{G_i} + \frac{5}{G_o})$mV	*	*
vs. Temperature (0 to +70°C)			
Gain = 1V/V	±350μV/°C max	±200μV/°C max	±100μV/°C max
Gain = 100V/V; G_O = 1V/V	±15μV/°C max	±10μV/°C max	±5μV/°C max
At Other Gains; G_O = 1 to 10V/V (μV/°C, max)	$\pm(12 + \frac{338}{G_i})$	$\pm(8 + \frac{192}{G_i})$	$\pm(4 + \frac{96}{G_i})$
vs. Supply Voltage	±100μV/V	*	*
RATED OUTPUT			
Voltage	±10V min	*	*
Current	±5mA min	*	*
Max CMV, Output Lo to Power Com.	±2V dc	*	*
POWER SUPPLY[4]			
Voltage, Rated Performance	±15V dc	*	*
Voltage, Operating	±(12 to 18)V dc	*	*
Current, Quiescent	(+15, -2)mA	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	*
Storage	-55° to +85°C	*	*
CASE DIMENSIONS	3.5" x 2.5" x 0.88"	*	*

*Specifications same as model 285J.

[1] Gain is adjustable over the range of 1 to 1000V/V by individually setting the input stage and output stage gains. Input gain ($G_i = 1 + \frac{30k\Omega}{R_i}$) is adjustable from 1 to 100V/V; output gain ($G_O = 1 + \frac{10k\Omega}{R_o}$) is adjustable from 1 to 10V/V. For a gain of 1V/V, leave gain terminals 4 and 7 open.

[2] Gain temperature drift is specified as % of output voltage.

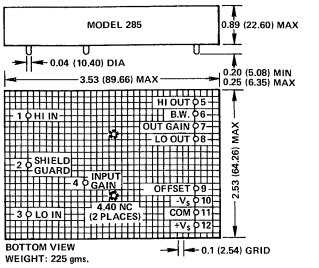
[3] Gain nonlinearity error is specified as % of peak-to-peak output voltage span (see Fig. 2).

[4] Recommended power supply, ADI model 904, ±15V @ 50mA output.

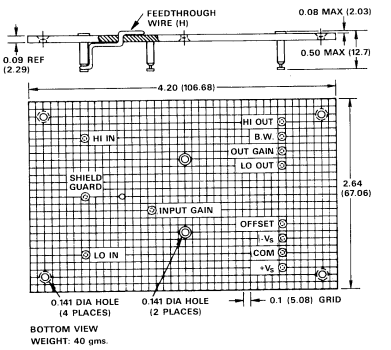
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SHIELDED MOUNTING SOCKET MODEL AC1045



GUARDING TECHNIQUES

Careful design and packaging of model 285 has yielded extremely high CMR and CMV ratings. To preserve the high CMR, care should be taken to keep the capacitance balanced about the input terminals and guard the input gain resistor, R_i, for gains less than 5V/V. A recommended shielding technique is illustrated in Figure 10, using model AC1045 mounting socket. This socket is recommended to reduce noise, pick-up, and CMR degradation from stray capacitance. Solder feedthrough wire (H) to the socket shield pin and copper foil surface. Module will cover copper shield from further exposure.

Best CMR performance will be achieved by using twisted, shielded cable to reduce inductive and capacitive pickup. To reduce effective cable capacitance, cable shield should be connected to the common mode signal source. This is accomplished by connecting the shield as close as possible to signal low and to the amplifier guard, as shown in Figure 10.

ENVIRONMENTAL SPECIFICATIONS

The reliability of instrumentation and control systems is becoming more important as the systems being controlled or measured become more complex and more expensive. To provide the reliability needed to protect plant and personnel during environmental stresses (vibration, humidity, temperature, etc.), model 285 has been designed to meet the environmental requirements of MIL-STD-202E testing, as shown in Table 1. These conditions closely simulate those seen in typical industrial applications. As an additional assurance of high performance reliability, every model 285 is factory tested for CMV rating by application of 3000V rms (±4200V peak) between input and output terminals for one minute (meets NEMA and CSA requirements for 660V rms service).

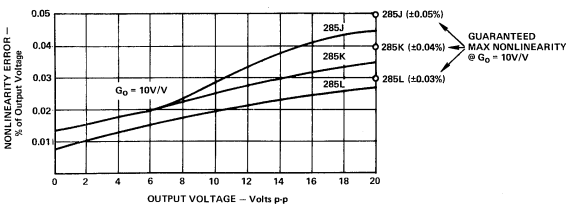
All Units Meet the Requirements of MIL-STD-202E as Outlined Below

TEST	METHOD	CONDITION
High Temperature Storage	108A	D (Non-Operating)
Moisture Resistance	106D	(10 Days)
Solderability	208C	
Thermal Shock	107D	A (5 Cycles)
Terminal Strength	211A	A (Pull Test; 10 lbs)
Temperature Cycling	102A	D (-55°C/+85°C)
Vibration	204C	B (15g Peak)
Barometric Pressure	105C	B (50,000 Feet)

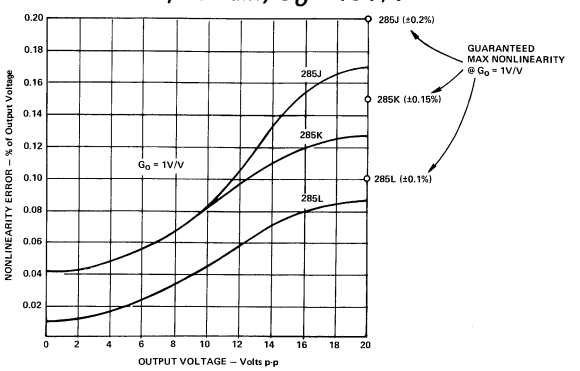
TABLE 1. Environmental Specifications

PERFORMANCE CHARACTERISTICS

Gain Nonlinearity: Nonlinearity error is presented as a % of peak-to-peak output voltage span; e.g. ±0.03% @ 20V p-p output = ±6mV max RTO nonlinearity error. Model 285 is available in three nonlinearity selections; 0.03% (285L), 0.04% (285K) and 0.05% (285J) – max, @ G_O = 10V/V. Best linearity performance is obtained when output gain, G_O, is set to 10V/V. Nonlinearity error is also specified and guaranteed when G_O = 1V/V, the curves of Figure 2 illustrate typical nonlinearity error over the entire output voltage range to 20V p-p, for G_O = 1V/V and 10V/V. At output levels less than 20V p-p nonlinearity error is typically much better than the worst case guaranteed specifications.



a. Output Gain, G_O = 10V/V



b. Output Gain, G_O = 1V/V

Figure 2. Gain Nonlinearity Error Vs. Output Voltage and Gain

Common Mode Rejection: CMR is rated at 60Hz and 1kΩ source imbalance for all gains from 1 to 1000V/V. CMR typically improves by 10dB above the specified minimum for gains greater than 2V/V. As a function of frequency, CMR response approaches 140dB at dc for all gains. (see Figure 3).

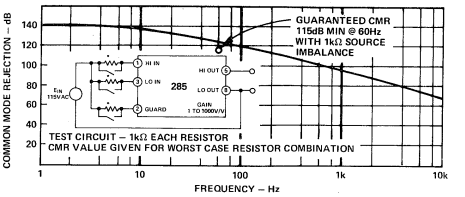


Figure 3. Common Mode Rejection vs. Frequency

Input Offset Voltage Drift: Model 285 is available in three drift selections; 5μV/°C (285L), 10μV/°C (285K) and 15μV/°C (285J) – max, RTI, G_i = 100V/V. Total input drift is composed of two sources, (input and output stage drifts) and is gain dependent. The curves of Figure 4 illustrate worst case total input drift over the gain range of 1 to 1000V/V. Best drift performance is achieved when input gain (G_i) is set to 100V/V. Output gain, G_O, can then be used to adjust overall gain from 100V/V to 1000V/V without increasing input drift.

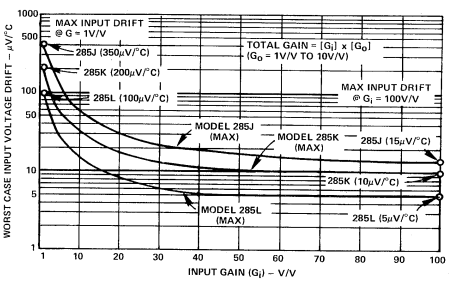


Figure 4. Input Offset Voltage Drift (Worst Case) vs. Gain

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 5. RMS voltage noise is shown in a bandwidth from 0.01Hz to the frequency shown in the horizontal axis. (e.g. noise in a bandwidth from 0.01Hz to 1kHz is 10μV p-p @ G = 100V/V). For best noise performance, input gain, G_i should be set to 100V/V; output gain, G_O, may then be used to set overall gain from 100V/V to 1000V/V with no increase in input noise. An output filter capacitor can be used to selectively roll-off noise beyond the bandwidth of interest (see Figure 10B).

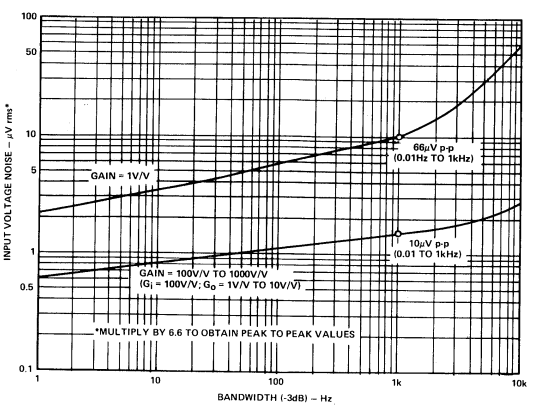
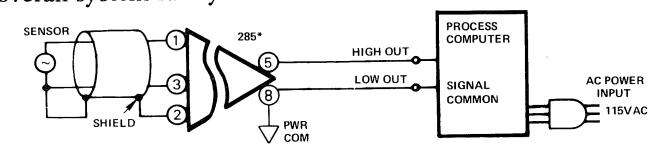


Figure 5. Input Voltage Noise vs. Bandwidth

APPLICATIONS IN INSTRUMENTATION AND PROCESS CONTROL

Interface Buffer Amplifier: Isolators are used in complex industrial systems to control, measure and interface other segments of the manufacturing/process operation and provide protection against damage caused by high voltage transients as well as continuous fault voltages. Model 285's floating, guarded input provides high rejection of common mode noise signals (115dB min) and offers input protection for both high voltage differential transients (up to ±600V peak) applied directly across the input terminals (HI IN and LO IN), as well as 3000V_{rms} input common mode signals.

In the computer interface application of Figure 6, model 285's intrinsically reliable design features offer unique application advantages wherever interface protection is required to protect vital computer process circuitry. The direct, two terminal (HI IN and LO IN) input design of model 285, simplifies the interface to remote transducers and sensors, thereby adding to the overall system safety.



*FOR OPTIONAL GAIN, OFFSET VOLTAGE ZEROING AND BANDWIDTH ROLLOFF, SEE FIGURE 10.

Figure 6. Computer Interface Buffer

Current Shunt Measurements: Model 285's high CMV (±2.5kV) and differential input protection (125V_{rms}) makes it particularly suitable for measuring SCR gate-to-cathode voltages typical in motor-control applications (see Figure 7). Wide bandwidth (dc to 2.5kHz), adjustable gain (1V/V to 1000V/V) and rugged/reliable design (meets MIL-STD-202E Environmental Testing), provide the additional performance required to accurately measure low level current signals from typical 50mV and 100mV shunts.

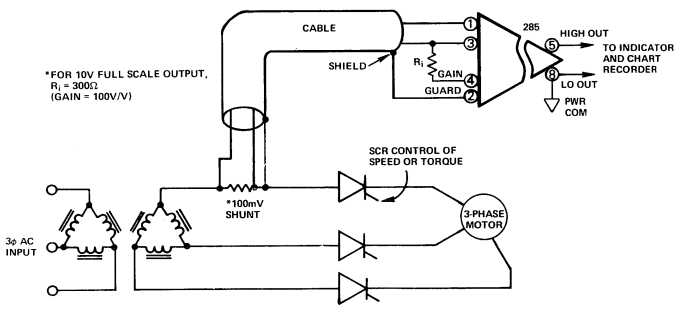
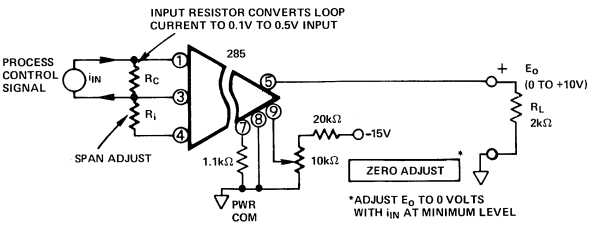


Figure 7. Motor Current Monitor Application

Process Signal Isolator: Model 285 can be easily applied in process control loops to interface standard process signals (e.g. 1mA to 5mA, 4mA to 20mA and 10mA to 50mA) and convert them to standard, zero based voltage signals (e.g. 0 to +10V). A typical hook-up of model 285 is illustrated in Figure 8, showing input current resistor (R_C), full scale span adjustment (R_i) and a zero adjust pot. (To achieve best linearity performance, model 285's output gain is set to 10V/V - R_O = 1.1kΩ). The table lists typical values for input signals, assuming a 0 to +10V output span is desired. In applications where the control loop may be located over long distances, with noise and high voltage transients frequently occurring, model 285's high 60Hz CMR (115dB) and CMV (±2.5kV) offer excellent noise rejection and protection from high voltage transients.



Loop Current i_{IN}	Input Resistor R_C	Span Resistor R_i	Output Span E_O
1 - 5mA	100Ω	20kΩ	0 to +10V
4 - 20mA	25Ω	20kΩ	0 to +10V
10 - 50mA	10Ω	20kΩ	0 to +10V

Figure 8. Process Signal Isolator, Showing Resistor Values for Typical Process Signal Levels

Bridge Transducer Amplifier: Model 285 offers total ground isolation with simplified two wire hook-up for low-level, floating signal measurements such as remote balanced bridge circuits (see Figure 9). Only differential current (±7nA) flows between the HI IN and LO IN terminals of model 285, thereby eliminating a third-wire for bias current return (required with all other types of amplifiers). The 100MΩ differential input impedance of model 285 will not load the bridge circuit. High CMV rating permits the bridge to be floated up to ±2500V dc with respect to power ground.

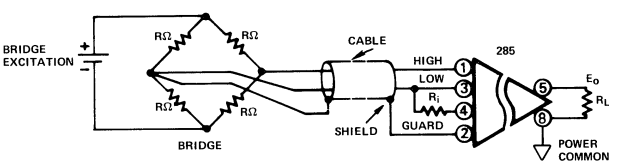
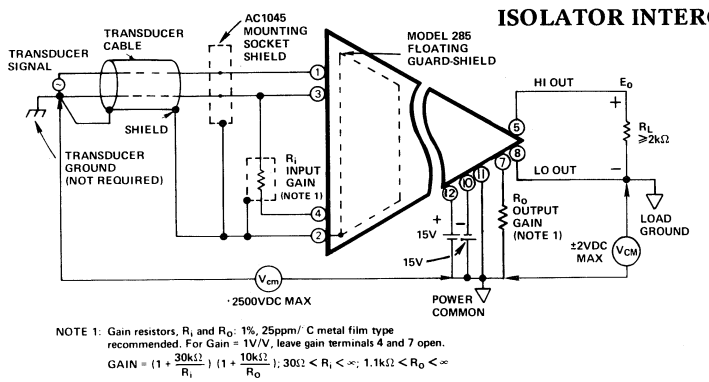


Figure 9. Bridge Transducer Amplifier

ISOLATOR INTERCONNECTION



NOTE 1: Gain resistors, R_i and R_O: 1%, 25ppm/°C metal film type recommended. For Gain = 1V/V, leave gain terminals 4 and 7 open.

$$\text{GAIN} = \left(1 + \frac{30k\Omega}{R_i}\right)\left(1 + \frac{10k\Omega}{R_O}\right);\ 30\Omega < R_i < \infty;\ 1.1k\Omega < R_O < \infty$$

Figure 10A. Transducer, Power, Gain Resistors, and Shielding Interconnection

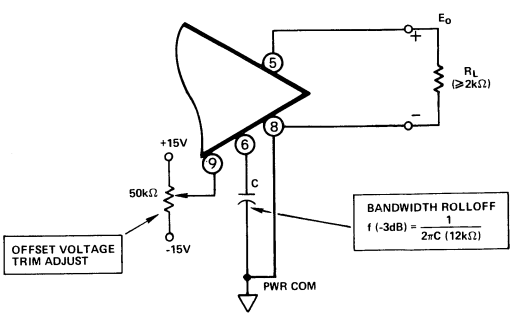


Figure 10B. Optional Connections: Offset Voltage Trim Adjust, and Bandwidth (-3dB) Rolloff

High CMV, High Performance, Synchronized Isolation Amplifier

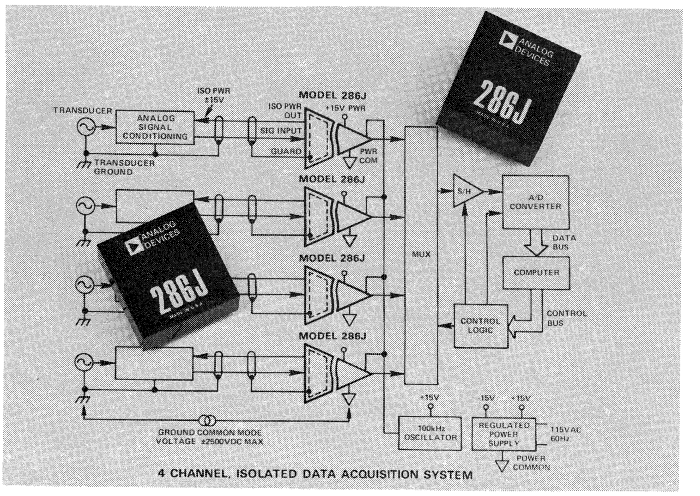
MODEL 286J, 281

FEATURES

Low Cost
Single or Multi-Channel Capability Using External Oscillator
Isolated Power Supply: ±15V dc @ ±15mA
Low Nonlinearity: 0.05% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.0075%/°C
Small Size: 1.5″ x 1.5″ x 0.62″
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 2500V dc Continuous
Wide Gain Range: 1 to 100V/V

APPLICATIONS

Ground Loop Elimination in Industrial and Process Control
High Voltage Protection in Data Acquisition Systems
Biomedical and Patient Monitoring Instrumentation
Off-Ground Signal Measurements



4 CHANNEL, ISOLATED DATA ACQUISITION SYSTEM

GENERAL DESCRIPTION

Model 286J is a low cost, compact, isolation amplifier that is optimized for single or multi-channel use in data acquisition systems for industrial and medical applications. A single external synchronizing oscillator can drive from 1 to 16 model 286J's, or a virtually limitless number of model 286's can be configured using multiple ganged oscillators. The oscillator drive circuit can be supplied by the user of specified in a compact, low cost, epoxy encapsulated module, model 281, which also includes a voltage regulator for operation over a wide single voltage range of +8V to +28V.

In addition to providing multi-channel operation, this new design features adjustable gain, 1 to 100V/V, dual isolated power, ±15V dc @ ±15mA, ±2500V dc off ground isolation (CMV) and 110dB minimum CMR at 60Hz, 5kΩ source imbalance, in a compact 1.5″ x 1.5″ x 0.6″ epoxy encapsulated package. Model 286J achieves a low input noise of 8μV pk-pk (100Hz bandwidth, G = 100V/V), nonlinearity of ±0.05% @ 10V pk-pk output, and an input/output dynamic range of 20V pk-pk.

Using modulation techniques with reliable transformer isolation, model 286J will interrupt ground loops, leakage paths, and high voltage transients to ±5kV pk (10ms pulse), providing dc to 1kHz (-3dB) response.

WHERE TO USE MODEL 286J

Industrial Applications: In multi-channel data acquisition systems, computer interface systems, process signal isolators and high CMV instrumentation, model 286J offers complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface capability is afforded with model 286J's 20V pk-pk input signal range at a gain of 1V/V operation. In portable multi-channel designs, model 286J's single supply, wide range operation (+8V to +16V) offers simple battery operation.

Medical Applications: In biomedical and patient monitoring equipment such as multi-channel VCG, ECG, and polygraph recorders, model 286J offers protection from lethal ground fault currents as well as 5kV defibrillator pulse inputs. Low level bioelectric signal recording is achieved with model 286J's low input noise (8μV pk-pk @ G = 100V/V) and high CMR (110dB, min @ 60Hz).

DESIGN FEATURES AND USER BENEFITS

High Reliability: Model 286J is a conservatively designed, compact module, capable of reliable operation in harsh environments. Model 286J has a calculated MTBF of 392,125 hours and is designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). As an additional assurance of reliability, every model 286J is factory tested for CMV and input ratings by application of 5kV pk, 10ms pulses, between input terminals as well as input/output terminals.

Isolated Power Supply: Dual ±15V dc @ ±15mA, completely isolated from the input power terminals (±2500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers as well as remote transducers such as thermistors or bridges.

Adjustable Gain: A single external resistor enables gain adjustment from 1V/V to 100V/V providing the flexibility of applying model 286J in both high-level transducer interfacing as well as low-level sensor measurements.

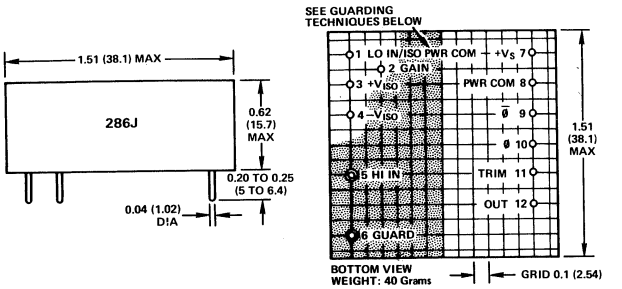
SPECIFICATIONS (typical @ +25°C and V_S = +15V dc unless otherwise noted)

MODEL	286J*
GAIN (NON-INVERTING)	
Range (50kΩ Load)	1 to 100V/V
Formula	Gain = 1 [100kΩ/(1kΩ+R_i(kΩ)]
Deviation from Formula	±4%
vs. Temperature (0 to +70°C)[1]	±0.0075%/°C
vs. Time	±0.001%/1000 hours
Nonlinearity,[2] ±5V Output (G = 1 to 100V/V)	±0.05%
Nonlinearity,[2] ±10V Output (G = 1 to 100V/V)	±0.2%
INPUT VOLTAGE RATINGS	
Linear Differential Range, G = 1V/V	±10V min
Max Safe Differntial Input	
Continuous	240V rms
Pulse, 10ms Duration, 1 Pulse/10sec	±6500V pk max
Max CMV, Inputs to Outputs	
ac, 60Hz, 1 Minute Duration	2500V rms
Pulse, 10ms Duration, 1 Pulse/10sec	±2500V pk max
With 510kΩ in series with Guard	±5000V pk max
Continuous, ac or dc	±2500V pk max
CMR, Inputs to Outputs, 60Hz, $R_S \leq$ 5kΩ	
Balanced Source Impedance	114dB
5kΩ Source Impedance Imbalance	110dB min
CMR, Inputs to Guard, 60Hz	
1kΩ Source Impedance Imbalance	78dB
Max Leakage Current, Inputs to Power Common	
@ 115V ac 60Hz	2.5μA rms max
OFFSET VOLTAGE, REFERRED TO INPUT	
Initial, @ +25°C (Adjustable to zero)	±(5 + 45/G) mV
vs. Temperature (0 to +70°C)	
At Gain = 100V/V	±10μV/°C
At Other Gains (1 to 100V/V)	±(7 + 250/G)μV/°C
vs. Supply Voltage	±1mV/%
INPUT IMPEDANCE	
Differential	10^8Ω‖150pF
Overload	300kΩ
Common Mode	5 x 10^{10}Ω‖20pF
INPUT DIFFERENCE CURRENT	
Initial, @ +25°C	±7nA max
vs. Temperature (0 to +70°C)	±0.1nA/°C
INPUT NOISE (Gain = 100V/V)	
Voltage	
0.05Hz to 100Hz	8μV pk-pk
10Hz to 1kHz	3.0μV rms
Current	
0.05Hz to 100Hz	5pA pk-pk
FREQUENCY RESPONSE (Gain: 1V/V to 100V/V)	
Small Signal Bandwidth, -3dB	1.0kHz
Slew Rate	25mV/μs
Full Power, 10V pk-pk Output	900Hz
Full Power, 20V pk-pk Output	400Hz
Recovery Time, to ±100μV	200ms
RATED OUTPUT	
Voltage, 50kΩ Load	±10V min
Output Impedance	1kΩ
Output Ripple, 1mHz Bandwidth	20mV pk-pk
OSCILLATOR DRIVE INPUT*	
Input Voltage	(8 to 16)V pk-pk
Input Frequency	100kHz ±5%, max
ISOLATED POWER SUPPLY	
Voltage	±15V dc
Accuracy	0, -6%
Current	±15mA min
Regulation, No Load to Full Load	+0, -10%
Ripple, 100kHz Bandwidth	200mV pk-pk
POWER SUPPLY, SINGLE POLARITY	
Voltage, Rated Performance	+15V dc
Voltage, Operating	+(8V dc to 16V dc)
Current, Quiescent	+13mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C
CASE DIMENSIONS	1.5" x 1.5" x 0.62"

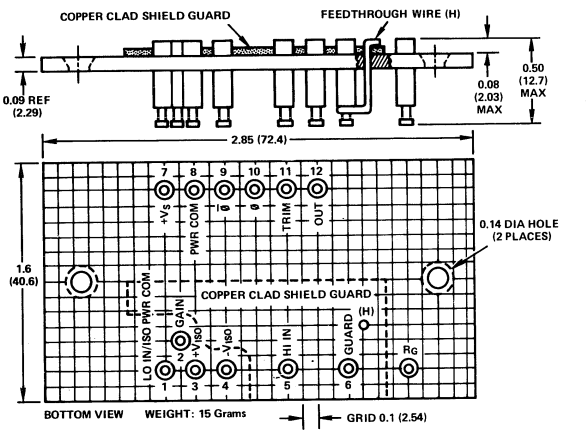
[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of output signal span.
*Specifications are for model 286J when driven by ADI model 281 oscillator circuit (see Figure 12). Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



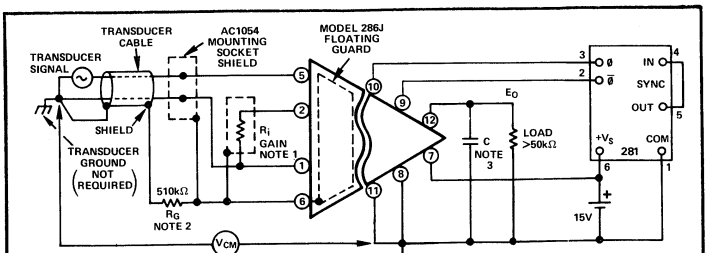
SHIELDED MOUNTING SOCKET AC1054



GUARDING TECHNIQUES

To preserve the high CMR performance of model 286, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 286 as illustrated in the outline drawing above (screened area). The GUARD (pin 6) must be connected to this shield. This shield is provided with the mounting socket, model AC1054 (solder feedthrough wire to the socket guard pin and copper foil surface.) A recommended guarding technique using model AC1054 is illustrated in Figure 1.

Best CMR performance will be achieved by using twisted, shielded cable to reduce inductive and capacitive pickup. To reduce effective cable capacitance, cable shield should be connected to the common mode signal source by connecting the shield as close as possible to signal low as shown in Figure 1.



NOTE 1. GAIN RESISTOR, R_i: USE 50ppm/°C, METAL FILM TYPE.
FOR GAIN = 1V/V, LEAVE TERMINAL 2 OPEN.
FOR GAIN = 100V/V, SHORT TERMINAL 2 TO TERMINAL 1
FOR GAINS FROM 1V/V TO 100V/V: $\text{GAIN} = 1 + \frac{100k\Omega}{1k\Omega + R_1\,(k\Omega)}$

NOTE 2. OPTIONAL GUARD RESISTOR, R_G, REQUIRED ONLY FOR CMV > ±2500V_{PK}. R_G MAY BE CONVENIENTLY MOUNTED ON AC1054 MOUNTING SOCKET USING THE STANDOFF PROVIDED (R_G). USE 1/4 WATT, 5% CARBON COMPOSITION TYPE; (ALLEN BRADLEY RECOMMENDED).

NOTE 3. OUTPUT FILTER CAPACITOR C. SELECT TO ROLL-OFF NOISE AND OUTPUT RIPPLE: (e.g. SELECT C=1.5μF FOR dc TO 100Hz BANDWIDTH)

$$F\ (-3dB) = \frac{1}{2\pi C\,(1k\Omega)}$$

Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of model 286J is derived from the carrier isolation technique which is used to transfer both signal and power between the amplifier's guarded input stage and the rest of the circuitry. The block diagram for model 286J is shown in Figure 2 below.

The 320kΩ input protection resistor limits the differential input current during periods of input amplifier saturation and also limits the differential fault current to approximately 50μA in case the preamplifier fails.

The bipolar input preamplifier operates single-ended (noninverting). Only a difference bias current flows with zero net bias current. A third wire return path for input bias current is not required. Gain can be set from 1V/V to 100V/V by changing the gain resistor, R_i. *To preserve high CMR, the gain resistor must be guarded.* Best performance is achieved by shorting terminal 2 to terminal 1 and operating model 286J at a gain of 100V/V.

For powering floating input circuitry such as buffer amplifiers, instrumentation amplifiers, calibration signals and transducers, dual isolated power is provided. High CMV isolation is achieved by the low-leakage transformer coupling between the input preamplifier, modulator section and the output circuitry.

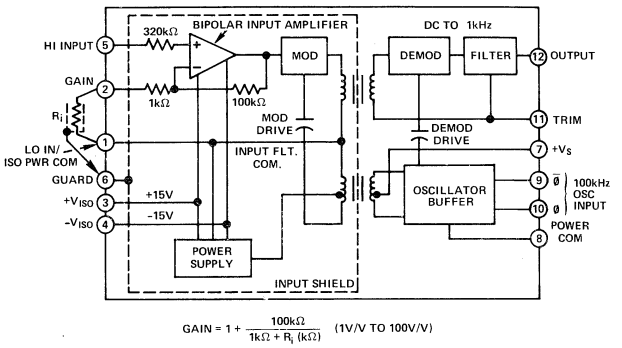


Figure 2. Block Diagram — Model 286J

OPTIONAL TRIM ADJUSTMENTS

Model 286J can be applied directly to achieve rated performance as shown in Figure 1, on page 2. Additional trim adjustment capability for bandwidth, output offset voltage and gain (for gains greater than 100V/V) is easily provided as shown in Figure 3 (below). The OUT and TRIM terminals can be floated with respect to PWR COM up to ±50V pk, max offering three-port isolation.

The TRIM terminal (pin 11) must be connected to the PWR COM terminal (pin 8) when not used to adjust the output offset voltage. A 0.1μF capacitor from pin 11 to PWR COM is recommended whenever the TRIM terminal is used.

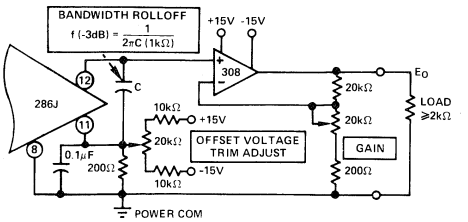


Figure 3. Optional Connections: Offset Voltage Trim Adjust, Bandwidth (-3dB) Rolloff and Gain Adjust (G>100V/V)

INTERELECTRODE CAPACITANCE, TERMINAL RATINGS AND LEAKAGE CURRENTS LIMITS

Capacitance: Interelectrode terminal capacitance arising from stray coupling capacitance effects between the input terminals and the signal output terminals are each shunted by leakage resistance values exceeding 50kMΩ. Figure 4 illustrates the CMR ratings at 60Hz and 5kΩ source imbalance between signal input/output terminals, along with their respective capacitance.

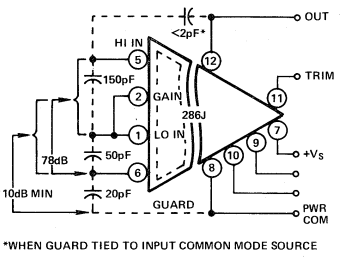


Figure 4. Model 286J Terminal Capacitance and CMR Ratings

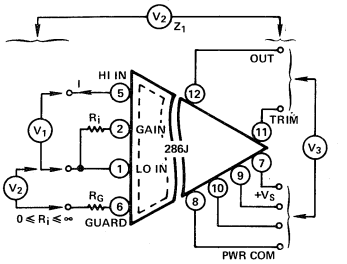


Figure 5. Model 286J Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac or dc peak ratings. Pulse ratings are intended to support defibrillator and other transient voltages. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 5 and Table 1 illustrate model 286J ratings between terminals.

SYMBOL	RATING	REMARKS
V1 (pulse)	±6500V_{PK} (10ms)	Withstand Voltage, Defibrillator
V1 (cont.)	±240V_{RMS}	Withstand Voltage, Steady State
V2 (pulse)	±2500V_{PK} (10ms) R_G = 0	Transient
V2 (pulse)	±5000V_{PK} (10ms) R_G = 510kΩ	Isolation, Defibrillator
V2 (cont.)	±2500V_{PK}	Isolation, Steady State
V3 (cont.)	±50V_{PK}	Isolation, dc
Z1	50kMΩ‖20pF	Isolation Impedance
I	50μA rms	Input Fault Limit, dc to 200kHz

Table 1. Isolation Ratings Between Terminals

Leakage Current Limits: The low coupling capacitance between inputs and output yields a ground leakage current of less than 2.5μA rms at 115V ac, 60Hz (or 0.02μA/V ac). As shown in Figure 6, the transformer coupled modulator signal, through stray coupling, also creates an internally generated leakage current of about 5μA rms @ 100kHz. Line frequency leakage current levels are unaffected by the power on or off condition of model 286J.

For medical applications, model 286J is designed to improve on patient safety current limits proposed by F.D.A., U.L., A.A.M.I. and other regulatory agencies (e.g., model 286J complies with leakage requirements for the Underwriters Laboratory STANDARD FOR SAFETY, MEDICAL AND DENTAL EQUIPMENT as established under UL544 for type A and B patient connected equipment — reference *Leakage Current*, paragraph 27.5).

In patient monitoring equipment, such as ECG recorders, model 286J will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. Using passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

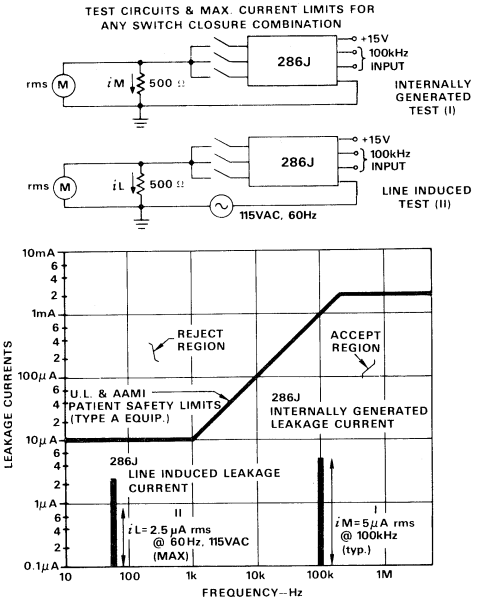


Figure 6. Model 286J Leakage Current Performance from Line Induced and Internally Generated (Modulator) Operating Conditions

PERFORMANCE CHARACTERISTICS

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 5kΩ imbalance at a gain of 100V/V. Figure 7 illustrates CMR performance as a function of signal frequency. CMR approaches 156dB at dc with source imbalances as high as 5kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V CMR is typically 6dB lower than at gain of 100V/V.

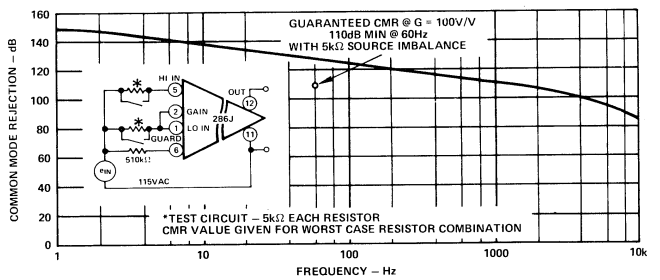


Figure 7. Common Mode Rejection vs. Frequency

Figure 8 illustrates the effect of source imbalance on CMR performance at 60Hz at gains of 1V/V, 10V/V, and 100V/V. CMR is typically 140dB at 60Hz and a balanced source. CMR is maintained greater than 80dB for source imbalances up to 100kΩ.

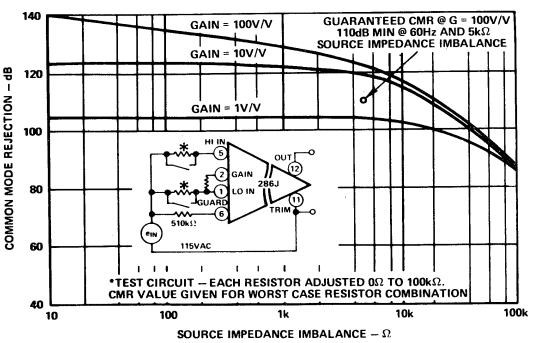


Figure 8. Common Mode Rejection vs. Source Impedance Imbalance

Gain Nonlinearity: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as a % of peak-to-peak output voltage span; e.g., nonlinearity of model 286J operating at an output span of 10V pk-pk (±5V) is ±0.05% or ±5mV. Figure 9 illustrates gain nonlinearity for any output span to 20V pk-pk (±10V).

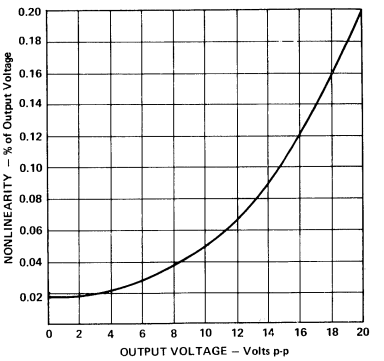


Figure 9. Gain Nonlinearity vs. Output Voltage

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 10. RMS voltage noise is shown in a bandwidth from 0.05Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is 8μV pk-pk at a gain of 100V/V. This value is derived by multiplying the rms value at f = 100Hz shown in Figure 10 (1.2μV rms) by 6.6.

For best noise performance in particular applications, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest (see note 3, Figure 1). Increasing gain will also reduce the input noise.

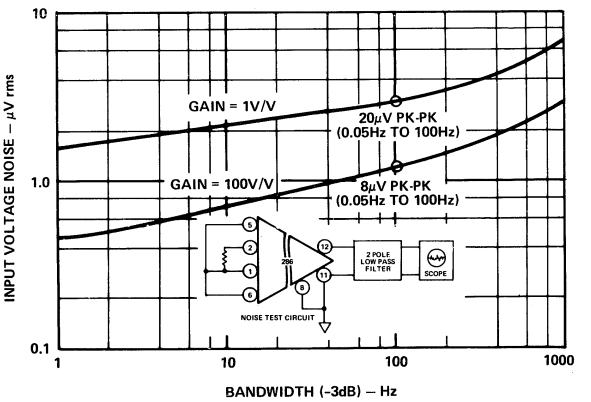


Figure 10. Input Voltage Noise vs. Bandwidth

Input Offset Voltage Drift: Total input drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 11 illustrates total input drift over the gain range of 1 to 100V/V.

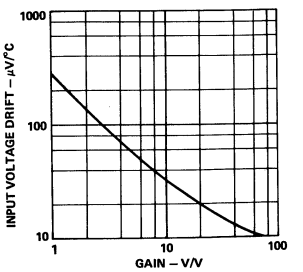
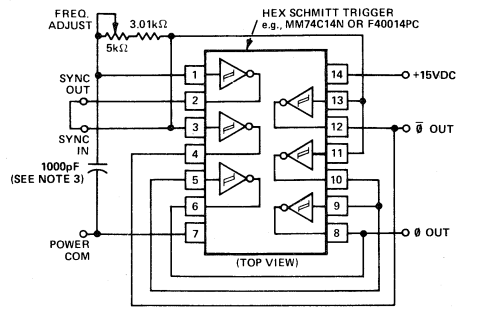


Figure 11. Input Offset Voltage Drift vs. Gain

REFERENCE EXCITATION OSCILLATOR

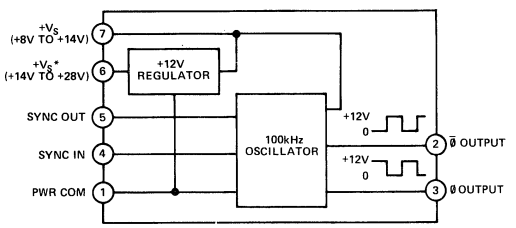
When applying model 286J, the user has the option of building a low cost 100kHz excitation oscillator, as shown in Figure 12, or purchasing a module from Analog Devices – model 281.



NOTES:
1. FREQ. ADJUST: ADJUST TRIM POT FOR OUTPUT FREQUENCY OF 100kHz ±5%.
2. FOR SLAVE OPERATION, REMOVE JUMPER FROM SYNC OUT AND SYNC IN PINS.
3. USE CERAMIC CAPACITOR, "COG" OR "NPO" CHARACTERISTIC.

Figure 12. Model 281 100kHz Oscillator – Logic and Interconnection Diagram

The block diagram of model 281 is shown in Figure 13. An internal +12V dc regulator is provided to permit the user the option of operating over two, pin selectable, power input ranges; terminal 6 offers a range of +14V dc to +28V dc; terminal 7 offers an input range of +8V dc to +14V dc.



*LEAVE TERMINAL 6 OPEN, WHEN POWER IS APPLIED TO TERMINAL 7.

Figure 13. Model 281 Block Diagram

Model 281 oscillator is capable of driving up to 16 model 286J's as shown in Figure 14. An additional model 281 may be driven in a slave-mode, as shown in Figure 15, to expand the total system channels from 16 to 32. By adding additional model 281's in this manner, systems of over 1000 channels may be easily configured.

EXTERNAL OSCILLATOR INTERCONNECTION

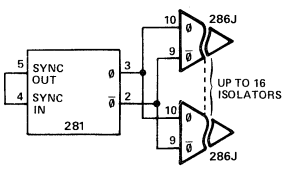


Figure 14. Model 281/286 Connection for Driving from 1 to 16 Isolators

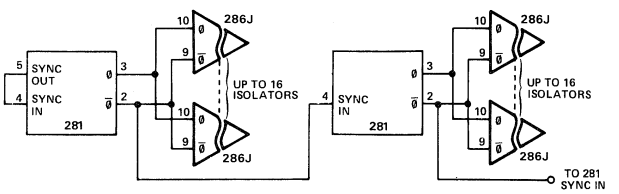


Figure 15. Model 281/286 Connection for Driving > 16 Isolators

SPECIFICATIONS

(typical @ +25°C and V_S = +15V dc unless otherwise noted)

MODEL	281
OUTPUT	
Frequency	100kHz ±5%
Waveform	Squarewave
Voltage (ϕ and $\bar{\phi}$ terminals)	0 to +12V pk
Fan-Out[1,2]	16 max
POWER SUPPLY RANGE[3]	
High Input, Pin 6	+(14 to 28)V dc
Quiescent Current, N.L.	+5mA
F.L.	+16mA
Low Input, Pin 7	+(8 to 14)V dc
Quiescent Current, N.L.	+12mA
F.L.	+33mA
TEMPERATURE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C
MECHANICAL	
Case Size	1.4" x 0.6" x 0.49"
Weight	10 grams

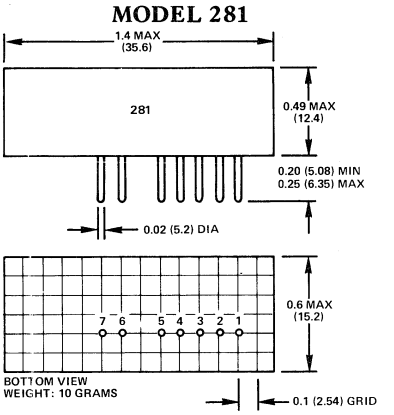
[1] Model 286J oscillator drive input represents unity oscillator load.
[2] For applications requiring more than 16 286J's, additional 281's may be used in a master/slave mode. Refer to Figure 15.
[3] Full load consists of 16 model 286J's and 281 oscillator slave.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

MODEL 281



PIN TERMINAL IDENTIFICATION

1	POWER COMMON	5	SYNC OUTPUT
2	$\bar{\phi}$ OUTPUT	6	$+V_S$: HIGH RANGE +(14 to 28)V_{dc}
3	ϕ OUTPUT	7	$+V_S$: LOW RANGE +(8 to 14)V_{dc}
4	SYNC INPUT		

MATING SOCKET:
CINCH #16 DIP OR EQUIVALENT

GUIDELINES ON EFFECTIVE SHIELDING & GROUNDING PRACTICES

- Use twisted shielded cable to reduce inductive and capacitive pickup.
- Drive the transducer cable shield, S, with the common mode signal source, E_G, to reduce the effective cable capacitance as shown in Figure 16 below. This is accomplished by connecting the shield point S, as close as possible to the transducer signal low point B. This may not always be possible. In some cases the shield may be separated from signal low by a portion of the medium being measured (e.g. pressure transducer). This will cause a common mode signal, E_M, to be generated by the medium between the shield and the signal low. The 78dB CMR capability of model 286J between the input terminals (HI IN and LO IN) and GUARD, will work to suppress the common mode signal, E_M.
- Dress unshielded leads short at the connection terminals and reduce the area formed by these leads to minimize inductive pickup.

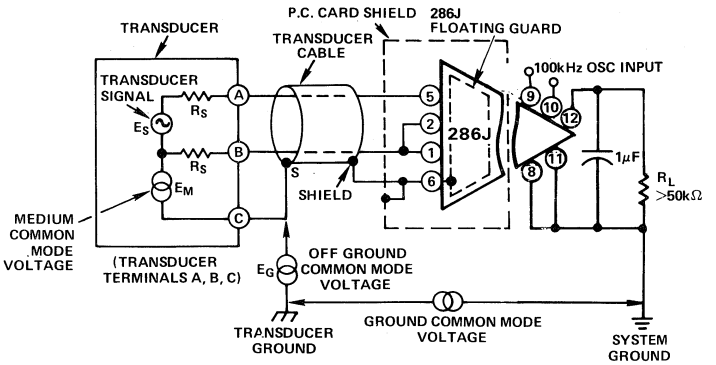
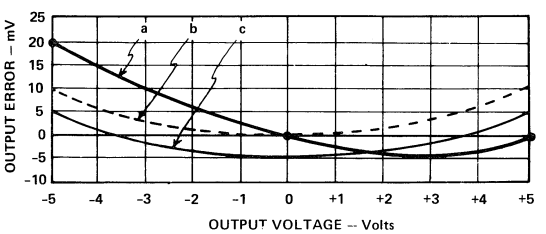


Figure 16. Transducer — Amplifier Interface

GAIN AND OFFSET TRIM PROCEDURE

In applying the isolation amplifier, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error encountered over the selected output voltage span. The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to −5V and operation at Gain = 10V/V is desired.

1. Apply e_{IN} = 0 volts and adjust R_O for e_O = 0 volts.
2. Apply e_{IN} = +0.500V dc and adjust R_G for e_O = +5.000V dc.
3. Apply e_{IN} = −0.500V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one half that measured in step 3 (see curve b).
5. Apply +0.500V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).



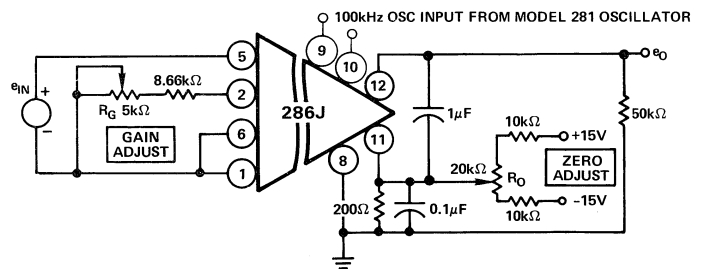


Figure 17. Gain and Offset Adjustment

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Remote Sensor Interface: In chemical, nuclear and metal processing industries, model 286J can be applied to measure and control off-ground millivolt signals in the presence of ±2500V dc CMV signals. In interface applications such as pH control systems or on-line process measurement systems such as pollution monitoring, model 286J offers complete galvanic isolation to eliminate troublesome ground loop problems. Isolated power outputs and adjustable gain add to the application flexibility of this model.

Figure 18 illustrates how model 286J can be combined with a low drift, 1μV/°C max, front-end amplifier, model AD510K, to interface low level transducer signals. Model 286J's isolated ±15V dc power and front-end guard eliminate ground loops and preserve high CMR (110dB min @ 60Hz).

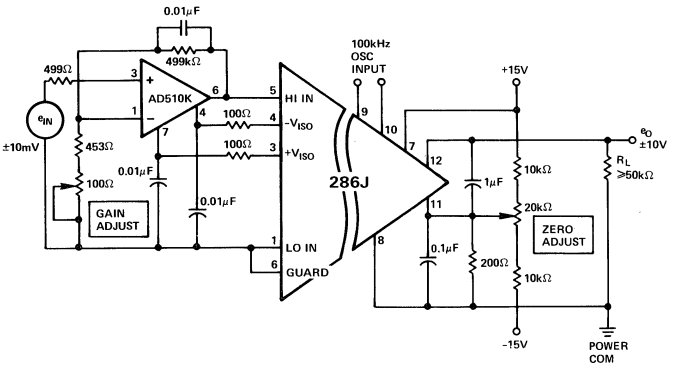


Figure 18. Input Signal Conditioning Using Isolated Power for Transducer Buffer Amplifier

Current Loop Receiver: Model 286J can be applied to measurement of analog quantities transmitted via 4-20mA current loops over substantial distances through harsh environments. Figure 19 shows an application of model 286J as a current loop receiver. A 25Ω resistor converts the 4–20mA current input from a remote loop to a 100–500mV differential voltage input, which the 286J amplifies, isolates, and translates to a 0 to +5V output level at local system ground.

Among the most-helpful characteristics of the 286J in this kind of measurement are the high common-mode rejection (110dB minimum at 60Hz with 5kΩ source unbalance) and the high common-mode rating (±2500 volts dc). The former means low noise pickup; the latter means excellent isolation and protection against large transients. The high common-mode rejection, permitting relatively low input voltage to be used (0.4V span, in this case), permits the use of a low current-metering resistance, which in turn results in low compliance-voltage loading on the current loop, and therefore permits insertion into existing loops without encountering overrange problems. The gain of 12.5 provides a substantial output span, and the floating output permits biasing to a 0 to 5V range.

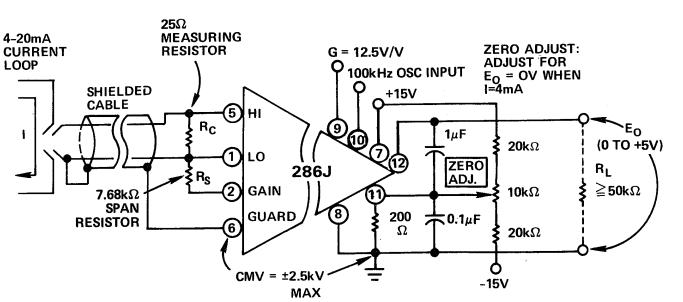


Figure 19. Isolated Analog Interface; 4 to 20mA is Converted to 0 to +5V at the Output, with Up to ±2500V of Isolation

ANALOG DEVICES

Low Cost, High Accuracy, Synchronized Isolation Amplifier

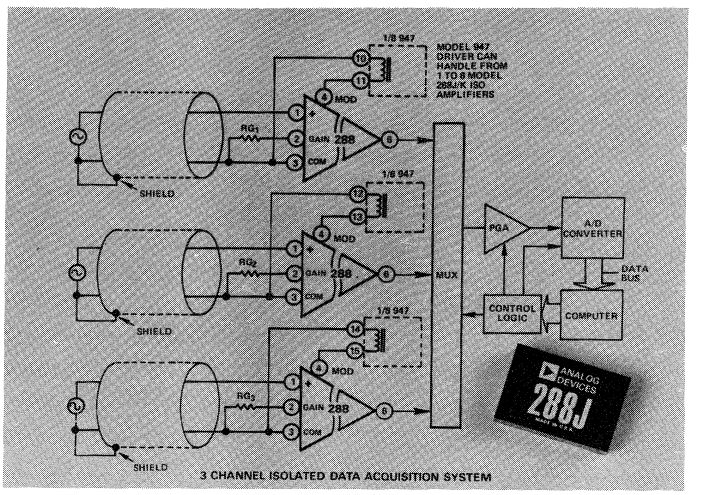
MODELS 288, 947, 948

FEATURES

Low Cost
Synchronized Design for Single and Multi-Channel Applications
Low Nonlinearity: 0.05% max, 288K
Low Gain Drift: 0.01%/°C max, 288K
Small Size: 1″ x 1″ x 0.56″ (288J/K)
Adjustable Gain, 1 to 1000V/V; Single Resistor

APPLICATIONS

Transient Voltage Protection in Data Acquisition System
Ground Loop Elimination in Industrial & Process Control
Off-Ground Signal Measurements
10 Bit Accurate Process Signal Isolator



GENERAL DESCRIPTION

Model 288 is a low cost, compact isolation amplifier offering 10 bit accuracy (model 288K) in a unique transformer isolated, synchronized design that is optimized for multi-channel industrial instrumentation and control applications. This new design features guaranteed low nonlinearity, 0.05% max, model 288K; 0.1% max, model 288J, guaranteed low gain drift, 100ppm/°C max, model 288K; 300ppm/°C max, model 288J. The input stage of model 288 is a low drift, 5μV/°C max, model 288K, bipolar op amp offering gain adjustment from 1V/V to 1000V/V with a single external resistor. Front-end protection combined with high CMV (850V dc, continuous operation) and high CMR (92dB min @ 60Hz) performance facilitate accurate low level measurements in the presence of noisy electrical equipment such as motors and power busses.

Model 288 requires external modulator and demodulator drive signals. Two compatible drive modules, models 947 and 948, are available for driving up to eight model 288J/K isolation amplifiers. Model 947, see Figure 2, offers eight isolated modular drive outputs, providing 850V dc channel-to-channel input isolation, as well as 850V dc input-to-output isolation. Model 948, see Figure 3, affords the same 850V dc input-to-output isolation for 1 to 8 model 288J/K isolation amplifiers with a common input ground reference (see Figure 4). Multiple 947 and 948 drive modules may be synchronized in system application of more than 8 channels.

WHERE TO USE MODEL 288

Using modulation techniques with reliable transformer isolation, model 288 will interrupt ground loops, leakage paths, and high voltage transients to ±850V pk, providing dc to 2.5kHz (-3dB) response. In low level multi-channel data acquisition systems, process monitoring and computer interface systems, model 288 offers complete galvanic isolation as well as protection against damage from transients and fault voltages.

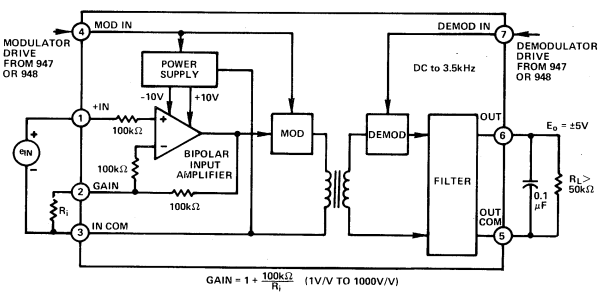


Figure 1. Block Diagram - Model 288

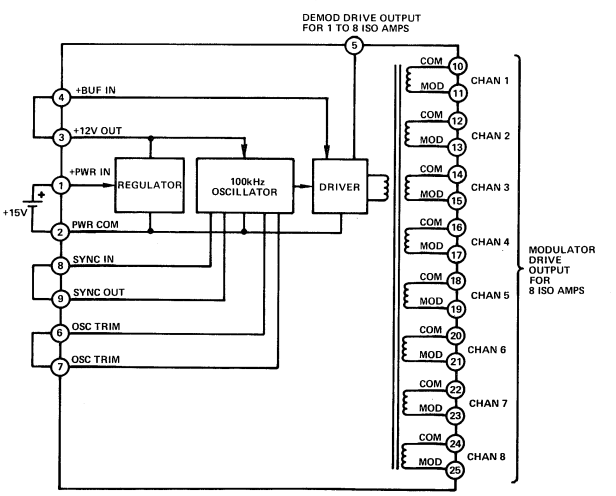


Figure 2. Block Diagram — Model 947 Driver

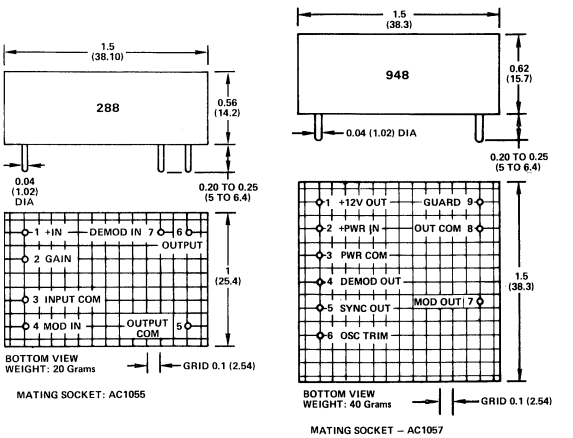
SPECIFICATIONS (typical @ +25°C and V_S = +15V dc unless otherwise noted, see note 1)

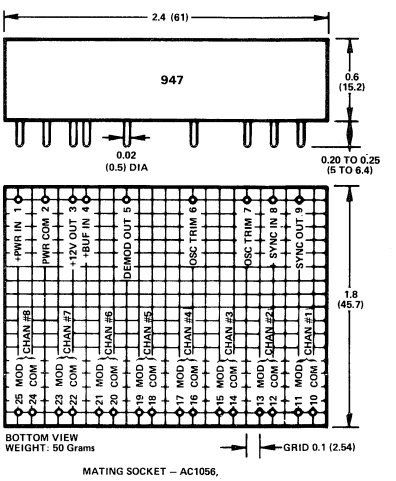
Model	288J	288K
GAIN (NON-INVERTING)		
Range (50kΩ Load)	1 to 1000V/V	
Gain Formula	Gain = 1 + 100kΩ/R_i(kΩ)	
Deviation from Formula	±4%	
vs. Temperature (0 to +70°C)[2]	±0.01%/°C typ, ±0.03%/°C max	±0.0035%/°C typ, ±0.01%/°C max
vs. Time	±0.001%/1000 hours	
Nonlinearity,[3] ±5V Output (G = 1 to 1000V/V)	±0.05% typ, ±0.1% max	±0.02% typ, ±0.05% max
INPUT VOLTAGE RATINGS		
Linear Differential Range, G = 1V/V	±5V min	
Safe Differential Input Voltage		
Continuous	240V rms max	
Pulse, 10ms Duration, 1 Pulse/sec	±400V pk max	
CMV, Inputs to Outputs		
ac, 60Hz, One Minute Duration	750V rms	
Continuous Operation	±850V pk max	
CMR, Inputs to Outputs, 60Hz, $R_S \leq 1k$		
Balanced Source Impedance	100dB	
1kΩ Source Impedance Imbalance	92dB min	
Leakage Current, Inputs to Outputs @ 115V ac, 60Hz	5.0μA rms max	
OFFSET VOLTAGE, REFERRED TO INPUT		
Initial, @ +25°C (Adjustable to zero)		
Gain = 500V/V	±0.5mV typ, ±1mV max	±0.1mV typ, ±0.5mV max
Gain = 1 to 1000V/V	±(1.0 + 50/G)mV max	±(0.5 + 30/G)mV max
vs. Temperature (0 to +70°C)		
Gain = 500V/V	±5μV/°C typ, ±10μV/°C max	±2μV/°C typ, ±5μV/°C max
Gain = 1V/V	±250μV/°C typ, ±500μV/°C max	±100μV/°C typ, ±300μV/°C max
Gain = 1 to 1000V/V	±(10 + 500/G)μV/°C max	±(5 + 300/G)μV/°C max
vs. Supply Voltage	$\pm\left(20 + \frac{500}{G}\right)$ μV/V	
INPUT BIAS CURRENT		
Initial, @ +25°C	±25nA max	
vs. Temperature (0 to +70°C)	±0.1nA/°C	
INPUT IMPEDANCE		
Differential	10^8Ω‖70pF	
Overload	200kΩ	
Common Mode	10^8Ω‖30pF	
INPUT NOISE		
Voltage, Gain = 500V/V		
0.01Hz to 10Hz	2μV pk-pk	
10Hz to 1kHz	2.5μV rms	
Current		
0.01Hz to 10Hz	5pA pk-pk	
FREQUENCY RESPONSE		
Small Signal Bandwidth, -3dB		
Gain = 500V/V	3.5kHz	
Gain = 1V/V	1.5kHz	
Full Power Response, 10V pk-pk Output		
Gain = 500V/V	2.0kHz	
Gain = 1V/V	1.5kHz	
RATED OUTPUT		
Voltage, 50kΩ Load	±5V min	
Output Impedance	1kΩ	
Output Ripple, 1MHz Bandwidth	2mV pk-pk	
POWER SUPPLY[4]		
Voltage, Rated Performance	+15V dc	
Voltage Range, Operating	+13.5V dc to +24V dc	
Current, Quiescent, Model 947	+25mA	
Current, Quiescent, Model 948	+15mA	
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	
Storage	-55°C to +85°C	
PACKAGE SIZE	1" x 1.5" x 0.56"	

NOTES:
[1] Specifications apply using either model 947 or model 948 mod/demod drive.
[2] Gain temperature drift is specified as a percentage of output signal level.
[3] Gain nonlinearity is specified as a percentage of output signal span.
[4] Power supply voltage ratings refer to models 947 or 948 mod/demod modules.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).





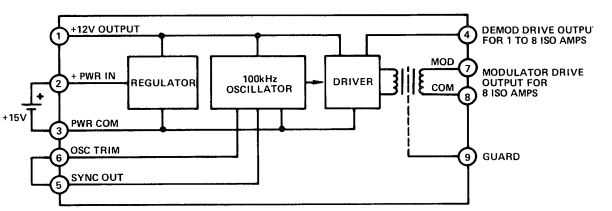


Figure 3. Block Diagram – Model 948 Driver

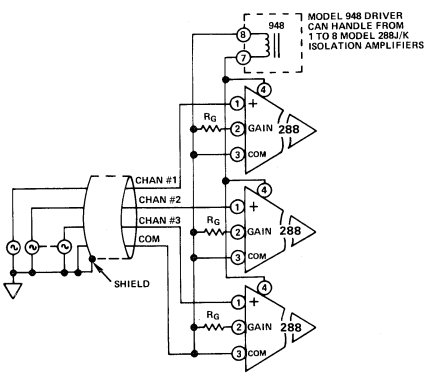


Figure 4. Application of Models 288/948 in Multi-Channel Data Isolation – (Note Common Signal Data Reference at Input)

Multipliers and Dividers

Orientation
Multipliers and Dividers

The devices catalogued in this section accept analog voltages and multiply, divide, square, and/or square-root them, depending on device properties and connections.

Multiplication For two inputs, V_x and V_y, a multiplier will provide the output, $E_{out} = V_xV_y/E_{ref}$, where E_{ref} is a dimensional constant, usually of 10V nominal value. If E_{ref} = 10V, E_{out} = 10V when V_x and V_y are 10V. Multipliers are used for modulation and demodulation, fixed and variable remote gain adjustment, power measurement, and mathematical operations in analog computing, curve fitting, and linearizing.

If the inputs may be of either positive or negative polarity, and the output polarity is in a correct relationship for multiplication, the device is called a "four-quadrant" multiplier, reflecting the 4 quadrants of the X-Y plane.

Squaring If $V_x = V_y = V_{in}$, a multiplier's output will be V_{in}^2/E_{ref}. A four-quadrant multiplier, used as a squarer, will have an output that is positive, whether V_{in} is positive or negative. Squarers are useful in frequency doubling, power measurement of constant loads, and mathematical operations.

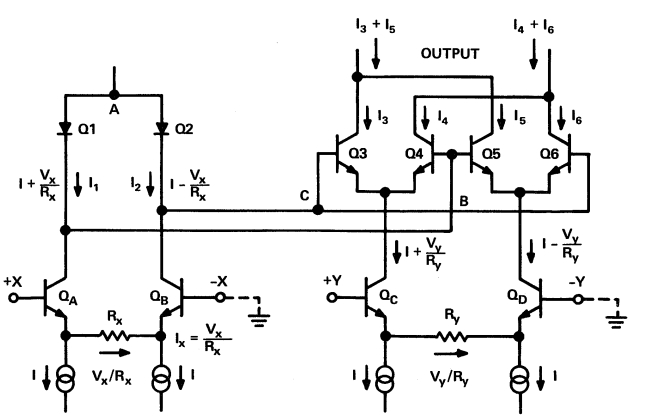
Division For a numerator input, V_z, and a denominator input, V_x, an analog divider will provide the output, $E_{out} = E_{ref}(V_z/V_x)$. If E_{ref} = 10V, E_{out} will be 10V or less for $V_z \leqslant V_x$ is of a single polarity and will not provide meaningful results if it approaches zero too closely. If V_z may be of either positive or negative polarity, the device is described as a "two-quadrant" divider, and the output will reflect the polarity of V_z. Analog dividers are used to compute ratios — such as efficiency, attenuation, or gain; they are also used for fixed and variable remote gain adjustment, ratiometric measurements, and for mathematical operations in analog computing.

Square rooting For a numerator input, V_{in}, and a denominator input, E_o (the output fed back to the denominator input), the output of a divider is $E_o = E_{ref}(V_{in}/E_o)$; hence $E_o = \sqrt{E_{ref}V_{in}}$. A square-rooter works in one quadrant; some devices require external diode circuitry to prevent latchup if the input polarity changes, even momentarily. Square roots are used in vector and rms computation, to linearize flowmeters, and for mathematical operations in analog computing.

CHOOSING A MULTIPLIER, DIVIDER, etc.
A number of devices are listed here, differing in internal architecture, external functional configuration, device technology, and performance specifications. Some have essentially fixed references; others have an actively variable or programmable reference as a third input (*multifunction devices*), and one type (model 433) performs the one-quadrant operation, $E_o = V_z(V_y/V_x)^m$, where m is an exponent adjustable from 1/5 to 5. With one exception (model 436 precision 2-quadrant divider), all of the devices listed here can be used for any of the functions defined above.

Considerable information on these functions, the nature of devices to perform them, and extensive discussions of their applications can be found in two publications available from Analog Devices.[1,2] A wealth of information is also to be found in the data sheets for the individual devices, published in this section. A brief selection guide to devices recommended for new designs may be found on page 160. In addition to the products listed here, a number of popular earlier products are still available; they are listed on page 599. Data sheets are available upon request.

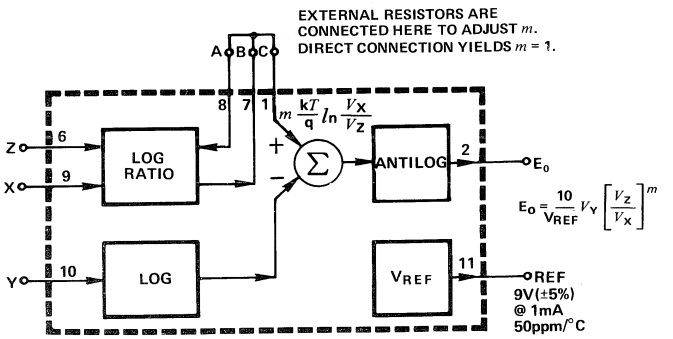
Internal Architecture All of the devices in this selection rely on the logarithmic properties of silicon P-N junctions. With the exception of models 433, 434, and 436 the circuit employed is basically like that of the "Gilbert cell" (its 4-quadrant-multiplying circuitry and performance are described in (1) and (2), with further references to original sources). The input voltages are converted to currents, the currents are multiplied together and divided by a reference, and the net output current, I_xI_y/I_{ref}, is converted to voltage by feedback around the output amplifier. The feedback terminals are available as inputs for applications involving division. In the AD531, the I_{ref} terminals are available for external programming or variation; thus, the AD531 is a 3-variable "multifunction" IC which can divide without external feedback. This versatile feature offers greater bandwidth as a divider.



Basic 4-quadrant variable-transconductance multiplier circuit

$$I_O = (I_3 + I_5) - (I_4 + I_6) = \frac{2\,V_X\,V_Y}{I\,R_X\,R_Y}$$

[1] *Multiplier Application Guide*, available upon request
[2] *Nonlinear Circuits Handbook*, D. H. Sheingold, ed., 1976, 536pp., P.O. Box 796, Norwood MA 02062



Functional Block Diagram of Model 433. Model 434 is Similar, with A, B, C Tied Together Internally.

In the multifunction Model 434, the feedback currents of the input op amps are used to develop logarithmic voltages across transistor base-emitter junctions; these voltages are summed and differenced and produce an exponential current proportional to V_yV_z/V_x via another transistor junction in the input path of the output amplifier. Thus, the output voltage is proportional to V_yV_z/V_x; an internally generated reference voltage is available as a fixed reference for the odd input in two-variable operations. In the 433, the internal emitter-voltage difference proportional to log (V_z/V_x) can be amplified or attenuated by the appropriate connection of a resistive attenuator with an attenuation ratio, m; since the antilog of m(log V_z/V_x) is $(V_z/V_x)^m$, the output of the 433 is proportional to $V_y(V_z/V_x)^m$. In the model 436 divider, the inputs are scaled and linearly combined, before the log-antilog computation takes place; the result is that the numerator (of V_z/V_x) may have positive or negative values. The 436 circuit is optimized and trimmed for performance as a dedicated divider; it has a fixed reference. Its circuit principles are discussed in some detail on the data sheet.

External functional configuration As noted earlier, with the exception of the model 436 dedicated divider, all of the devices listed here can be used for multiplication, division, squaring, and/or square-rooting (MDSSR), by the appropriate connection of external jumpers. As an example, the AD534 is shown connected for multiplication, division, and square-rooting. Performance of pretrimmed devices is optimized in one of the modes of operation, usually multiplication. The data sheets show how devices are connected for the various modes of operation; where appropriate, the trim circuits and procedures for optimizing performance are provided.

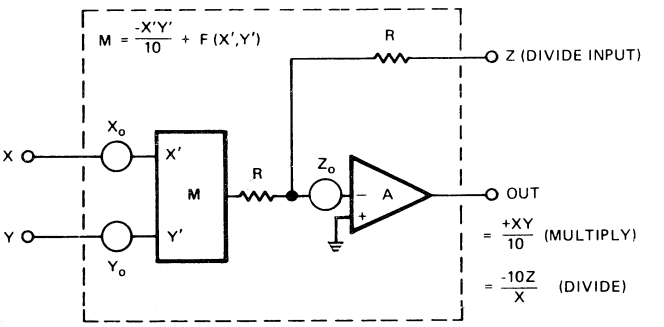
Some devices have differential inputs, which provide a great deal of flexibility. They permit polarity changes without external inversion, direct subtraction of inputs, insertion of bias voltages for additive constants, and direct multiplication of the results of differential measurements.

Technologies The devices described here are either monolithic integrated circuits of high-performance modules. For any application, the user will evaluate a device on the basis of its performance in the desired mode(s). The modules provide the highest performance: speed (model 429), accuracy as a multiplier (model 435), accuracy as a divider (436), and accuracy in multi-function applications (433 and 434). On the other hand, the IC's provide economy of cost and space, and the availability of "mil-temp" range (−55°C to +125°C) versions. The pretrimmed IC's (AD534 and AD532) use laser trimming of thin-film-on-silicon chips at the wafer stage and buried-Zener reference circuitry, as well as thermally balanced input stages and "core" circuitry, for overall maximum errors to 0.25%, and linearities as yet unmatched in the industry.

Performance Multiplier performance, specifications, and test circuitry are described in great detail in the NONLINEAR CIRCUITS HANDBOOK. Here is a brief digest of the factors relating to low-frequency performance.

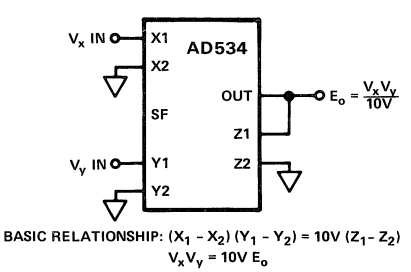
In theory, a multiplier has an output which is ideally the product of two input variables, X and Y, divided by the 10V scaling voltage. However, the practical multiplier is subject to various offset errors and nonlinearities, which must be accounted for in its application. This discussion is intended to assist the designer in understanding and interpreting multiplier and divider specifications and obtaining insight into device performance.

In practice (see the figure), the multiplier may be considered as having two parts, one (M) contains the input circuitry and the multiplying cell; the other is the gain-conditioning op amp, A.

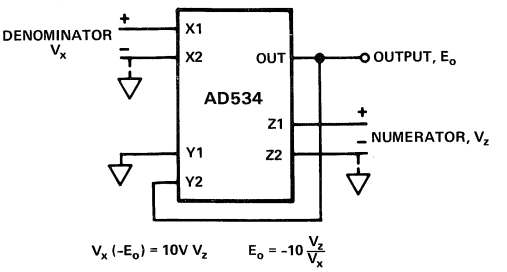


Functional Block Diagram of Model 433

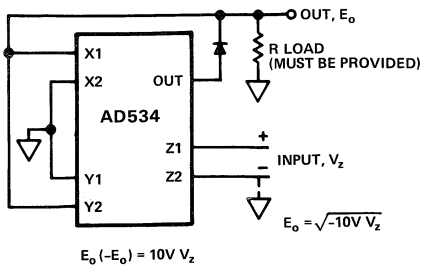
Also summed at the op-amp input is the feedback variable, Z. In multiplication, Z is connected to the output circuit. In division, Z and X are the inputs, and Y is connected to the output. The figure shows a model used for considering errors. X_o and Y_o are input offset voltages, Z_o is the offset-referred-to-the-input of the output amplifier, and $F(X', Y')$ is the nonlinearity, viewed as the departure from the ideal multiplication, $\frac{X'Y'}{10R}$. The output equation, including the errors is of the form



Multiplier



Divider



Square Rooter

$$E_o = \frac{XY}{10B} \pm \left[\frac{X_oY}{10B} \pm \frac{XY_o}{10B} \pm Z_o + f(X,Y)\right]$$

Product; X_{offset}, Y_{offset} (Linear "Y", Feedthrough "X"); Output offset; Nonlinearity and feedthrough

The errors are included in the bracketed term, except for gain error, which is the departure of "B", the gain-error term, from its nominal value of unity. The effects of input offsets (called "linear feedthrough") can be set to zero by applying external input biases, the output offset can be set to zero by biasing the output amplifier, and the gain can be externally calibrated by adjusting the reference or the feedback resistance. The remaining departure from the ideal output for any combination of input values is the irreducible *linearity error*, or *nonlinearity*, a function of X and Y that differs from device to device and, with temperature, within a given device. The component of nonlinearity for X = 0 is called "Y feedthrough" and for Y = 0, it is called "X feedthrough".

The "total error" specification includes the effects of all these errors. Although a guide to performance, it may produce an excessively conservative design in some applications. For example, output offset is not important if the output is to be capacitively coupled or the initial offset is nulled. Gain error is not important if system gain is to be adjusted elsewhere in the system or if gain is not a critical factor in system performance. If frequent calibration of offset and scale-factor errors is available (e.g., in a "smart" instrument, via software) nonlinearity becomes the limiting parameter. In such cases, improvements in predicted error can be achieved by using the approximate linearity equation:

$$f(X,Y) \cong |V_x|\epsilon_x + |V_y|\epsilon_y$$

were ϵ_x and ϵ_y are the specified fractional linearity errors (%/100) and V_x and V_y are the input signals.

When multipliers are fed back for use in division applications, it is important to recognize that maximum multiplication errors are increased approximately in proportion to the inverse of the denominator voltage ($10V/V_x$), and bandwidth is decreased in proportion to denominator voltage. Pretrimmed multipliers used in such applications, with wide dynamic range of X (e.g., 10:1), will always benefit greatly by the trimming of offsets, especially Z_o (affects offsets) and X_o (affects gain), for small values of ^{X}

DEFINITIONS OF SPECIFICATIONS*

Accuracy is defined in terms of *total error* of the multiplier at room temperature and constant nominal supply voltage. *Total error* includes the sum of the effects of input and output dc offsets, nonlinearity, and feedthrough. *Temperature dependence* and *supply-voltage effects* are specified separately.

Scale Factor The *scale-factor error* (or *gain* error) is the difference between the average scale factor and the ideal scale factor (e.g., $(10V)^{-1}$). It is expressed in percent of the output signal. *Temperature dependence* is specified.

Output Offset refers to the offset voltage at the output-amplifier stage. This offset is usually minimized at manufacture and can be trimmed where high accuracy is desired. Output *offset vs. temperature* is also specified.

Linearity Error or *Nonlinearity* is the maximum difference between actual and "best-straight-line" theoretical output, for all pairs of input values, expressed as a percentage of full scale, with all other dc errors nulled. It is the irreducible minimum error. It is usually expressed in terms of X and Y nonlinearity, with the named input swinging over its full-scale range and the other input at (±) 10V. Y nonlinearity is considerably less than X nonlinearity in "Gilbert-cell" multipliers. This specification includes nonlinear feedthrough.

X or Y Feedthrough is the signal at the output for any value of X or Y input in the rated range, when the other input is zero. It has two components, a linear one, corresponding to an *input offset* at the zero input, which can be trimmed out (but can drift and has a *temperature specification*), and a nonlinear one, which is irreducible. *Feedthrough* is usually specified at one frequency (50Hz) for a 20V p-p sine wave input. It increases with frequency, and plots of typical feedthrough vs. frequency are provided on multiplier data sheets.

Noise is specified and measured with both inputs at zero signal and zero impedance (i.e., shorted). For low-frequency applications, filtering the output of the multiplier may improve small-signal resolution significantly.

Dynamic Parameters include: *small-signal bandwidth, full-power response, slew(ing) rate, small-signal amplitude error,* and *settling time.*

Small-signal bandwidth is the frequency at which the output is down 3dB from its low-frequency value (i.e., by about 30%) for a nominal output amplitude of 10% of full scale.

Full-power response is the maximum frequency at which the multiplier can produce full-scale voltage into its rated load without noticeable distortion.

Slew(ing) rate is the maximum rate of change of output voltage for the product of a full-scale dc voltage and a full-scale step input.

Small-signal amplitude error is defined in relation to the frequency at which the amplitude response, or scale factor, is in error by 1%, measured with a small (10% of full-scale) signal.

Settling time, for the product of a ±10V step and 10Vdc, is the total length of time the output takes to respond to an input change and stay within some specified error band of its final value. Settling time cannot be accurately predicted from any other dynamic specifications; it is specified in terms of a prescribed measurement.

Vector error is the most-sensitive measure of dynamic error. It is usually specified in terms of the frequency at which a phase error of 0.01 radians (0.57°) occurs.

*These are general definitions. Further definitions are provided as footnotes to the specification tables; they should be read carefully.

Selection Guide
Multipliers and Dividers

Type	Characteristics	Page
AD534J/K/L/S/T†	General-purpose high-performance 4-quadrant IC, differential inputs and feedback, pretrimmed to 0.25% max total error (L), 0.01%/°C max (T)	179
AD532J/K/S	General-purpose 4-quadrant IC, differential inputs, standard pinouts, pretrimmed to 1.0% max total error (K), 0.04%/°C max (S)	169
AD533J/K/L/S	Lowest cost general-purpose 4-quadrant IC, external trim to 0.5% max total error (L)	175
Model 435J/K	Highest-accuracy 4-quadrant, module, pretrimmed to 0.1% max total error (K), 0.01%/°C max (K)	199
Model 429A/B†	Widest-bandwidth 4-quadrant, module, full-power response to 2MHz min, slewing rate 120V/μs min, -3dB bandwidth 10MHz, small-signal, 1% settling-time 500ns; pretrimmed to 0.5% max error (B)	187
DIVIDER ONLY		
Model 436A/B	High-accuracy 2-quadrant module, pretrimmed to 0.25% max error (B, denominator [V_X] range from +0.1V to +10V [$\|V_Z\| \leqslant \|V_X\|$]), 2% max error over temperature (B), 1% max error 0 to +70°C	203
MULTIFUNCTION DEVICES		
Model 433J/B	Programmable multifunction module, $Y(Z/X)^m$ ($10V/E_{REF}$), one-quadrant, m adjustable from 0.2 to 5, max division error 25mV (B, V_Z from 0.01V to 10V, V_X from 0.1V to 10V, $V_Z \leqslant V_X$), 1% max over temperature	191
Model 434A/B	High-accuracy multifunction module, YZ/X, one-quadrant, max division error pretrimmed to 0.25% max (B, V_Z from 0.01V to 10V, V_X from 0.1V to 10V, $V_Z \leqslant V_X$, m = 1), 1% max over temperature (B), current or voltage input	195
AD531J/K/L/S	4-quadrant XY/IR IC multiplier with variable or programmable denominator (scale factor), can be externally trimmed to 0.5% max total error (L)	161

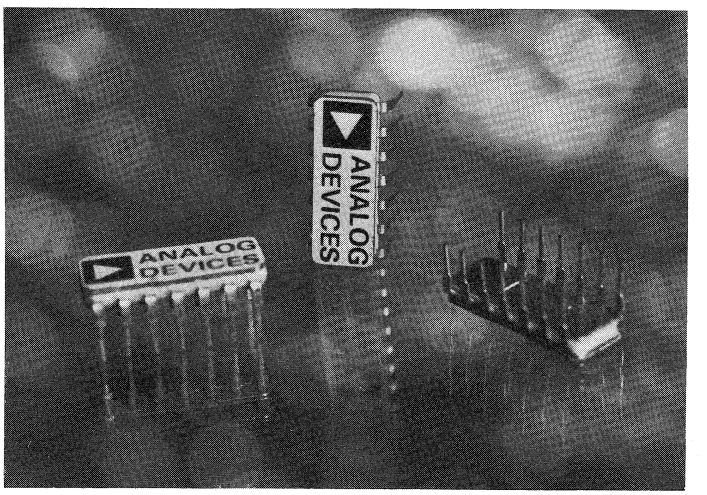
†Rated operating temperature ranges: J/K/L, 0°C to 70°C; A/B, -25°C to +85°C; S/T, -55°C to +125°C

IC Programmable Multiplier Divider Computation Circuit

AD531

FEATURES
Transfer Function: XY/Z
Guaranteed ±0.5% max
4-Quadrant Error (AD531L)
Guaranteed Accuracy over
Temperature (AD531L and AD531S)
High Speed: 45V/μs
Fully Protected Inputs and Output
Monolithic Construction

APPLICATIONS
Multiplication & Division
True rms-to-dc Conversion
Vector Computation
Absolute Value



GENERAL DESCRIPTION

The AD531 is the first monolithic programmable multiplier/divider to provide the true transfer function $V_X \cdot V_Y / kI_Z$ without the need for an external level shifting op amp at the output. Not just a multiplier, the AD531 is truly a computation circuit that is ideally suited to such applications as automatic gain control (AGC), true rms-to-dc conversion, ratio determination and vector operations; in addition, it provides the normal mathematical functions of four-quadrant multiplication, two-quadrant division and squaring, and square rooting. Flexibility of operation is achieved by means of the variable scale factor kI_Z, which can be set by an external resistor or varied dynamically by an externally derived reference current to obtain the overall transfer function $V_X \cdot V_Y / V_Z$. This provision for the direct computation of three variables greatly simplifies the design of such complex circuits as the true rms-to-dc converter and Flow Rate Computers. Further, multipliers less flexible than the AD531 must put the multiplying element in the feedback of an op amp to obtain division, often with significant sacrifice in accuracy and bandwidth.

The unique features of the AD531 include a differential V_X input with 75dB of common mode rejection, an internally derived stable reference for use in fixed scale applications, and a sense feedback terminal for simple load sensing or special applications. Further, the AD531's guaranteed accuracy, overall high performance and ease of use compare favorably with modular multipliers, while its IC construction provides significant advantages in size, reliability and economy.

The AD531 consists of a differential input transconductance multiplying element, a stable reference and an output amplifier on a single monolithic chip. The circuit's complement of required external components is limited to feedthrough and output zero adjusting trim pots and passive or active adjustment of the scaling current, I_Z.

The AD531J, AD531K and AD531L feature maximum multiplying errors of ±2%, ±1% and ±0.5% (I_Z = full scale) respectively at +25°C, and are rated for operation from 0 to +70°C. The AD531S has a maximum multiplying error of ±1% (I_Z = full scale) at +25°C and is rated for operation over the full military temperature range, −55°C to +125°C. All types are provided in the hermetically sealed TO-116 ceramic DIL package.

GUARANTEED TEMPERATURE PERFORMANCE

In addition to verification of accuracy at +25°C, the AD531L and AD531S are 100% tested for maximum error limits of ±1.5% and ±3.0% respectively at their extreme operating temperature limits (0 and +70°C for the L version; −55°C and +125°C for the S version).

SPECIFICATIONS

(typical @ +25°C, externally trimmed, $R_L \geq 2k\Omega$, sense terminal connected to output, and $V_S = \pm 15V$ dc unless otherwise specified

PARAMETER	CONDITIONS	AD531J	AD531K	AD531L	AD531S
ABSOLUTE MAX RATINGS					
Supply Voltage		±18V	*	*	±22V
Internal Power Dissipation		500mW	*	*	*
Input Voltage (Note 1)					
V_X, V_Y, Sense, C, Y_O, V_{OS}		$\pm V_S$	*	*	*
X_O		0V to $+V_S$	*	*	*
B input		$-V_S$ to ($-V_S$ +6V dc)	*	*	*
Input Current					
C input		+750μA	*	*	*
Rated Operating Temp Range		0 to +70°C	*	*	−55°C to +125°C
Storage Temp Range		−65°C to +150°C	*	*	*
Lead Temperature	60 sec. soldering	+300°C	*	*	*
Output Short Circuit	To ground	Indefinite	*	*	*
PERFORMANCE SPECIFICATIONS					
Transfer Function		V_XV_Y/kI_Z	*	*	*
Total Error (% of full scale)	kI_Z = +10V	±2.0% max [±1.5% typ]	±1.0% max [±0.7% typ]	±0.5% max [±0.3% typ]	±1.0% max [±0.5% typ]
	T_{min} to T_{max}, kI_Z = +10V	±2.5%	±1.5%	±1.5% max	±3.0% max
vs. Temperature	T_{min} to T_{max}, kI_Z = +10V	±0.04%/°C	±0.03%/°C	±0.01%/°C	±0.02%/°C max [±0.01%/°C typ]
Total Error	kI_Z = +1V dc, V_X = ±1V dc	±2.0%	±1.0%	±0.5%	±1.0%
Nonlinearity					
X input (Note 2)	$V_X = V_O$ = 20V(p-p)	±0.8%	±0.5%	±0.3%	±0.5%
Y input (Note 2)	$V_Y = V_O$ = 20V(p-p)	±0.3%	±0.2%	**	**
I_Z input	kI_Z = +1.0 to +10.0V	±0.5%	*	*	*
Feedthrough					
X input	kI_Z = +10V, V_X = 20V(p-p), V_Y = 0, f = 50Hz	150mV(p-p) max [50mV(p-p) typ]	80mV(p-p) max [30mV(p-p) typ]	40mV(p-p) max [20mV(p-p) typ]	80mV(p-p) max [30mV(p-p) typ]
Y input	kI_Z = +10V, V_Y = 20V(p-p), V_X = 0, f = 50Hz	100mV(p-p) max [30mV(p-p) typ]	60mV(p-p) max [25mV(p-p) typ]	30mV(p-p) max [15mV(p-p) typ]	60mV(p-p) max [25mV(p-p) typ]
X or Y vs. Temperature	T_{min} to T_{max}	2.0mV(p-p)/°C	1.0mV(p-p)/°C	0.5mV(p-p)/°C	1.0mV(p-p)/°C
INPUT SPECIFICATIONS					
Input Resistance					
X input, common mode	V_{cm} = ±10V	80MΩ‖8pF	*	*	*
X input, differential	V_{diff} = ±10V	10MΩ‖4pF	*	*	*
Y input	V_Y = ±10V	6MΩ‖4pF	*	*	*
Sense input		36kΩ	*	*	*
Input Bias Current					
X, Y inputs	kI_Z = +10V dc	3μA	4μA max [1.5μA typ]	2μA max [1μA typ]	4μA max [1.5μA typ]
	T_{min} to T_{max}	10μA	8μA	4μA	8μA
Sense input		±10μA	±15μA max [±5μA typ]	**	**
	T_{min} to T_{max}	±30μA	±25μA	**	**
Input Offset Current					
X inputs	kI_Z = +1.0 to +10.0V	±0.3μA	±0.1μA	**	**
Common Mode Rejection					
X inputs	V_{cm} = ±10V dc	40dB min	40dB min [60dB typ]	60dB min [75dB typ]	40dB min [60dB typ]
Scaler Current I_Z					
C input	kI_Z = +10V dc	300μA min [500μA max]	*	*	*
Input Voltage					
V_X, V_Y, V_{sense}	T_{min} to T_{max} for rated accuracy	±10V	*	*	*
V_X/kI_Z	T_{min} to T_{max} for rated accuracy	±1.0V	*	*	*
Null Input Voltage	max required to trim				
Y_O, V_{OS}		±15V max [±5V typ]	±10V max [±3V typ]	**	**
X_O		+15V max [+12.5V min]	*	*	*
DYNAMIC SPECIFICATIONS					
Small Signal, Unity Gain		1.0MHz	*	*	*
Full Power Bandwidth		750kHz	*	*	*
Slew Rate		45V/μs	*	*	*
Small Signal Amplitude Error		1% at 75kHz	*	*	*
Small Signal 1% Vector					
Error	0.5° phase shift	5kHz	*	*	*
Settling Time	±10V step	1μs to 2%	*	*	*
Overload Recovery		2μs to 2%	*	*	*
OUTPUT AMPLIFIER SPECIFICATIONS					
Output Impedance	Open Loop	100Ω	*	*	*
Output Voltage Swing	T_{min} to T_{max}, $R_L \geq 2k\Omega$, $C_L \leq 1000pF$	±10V min [±13V typ]	*	*	*
Output Noise	f = 5Hz to 10kHz	0.6mV(rms)	*	*	*
	f = 5Hz to 5MHz	3.0mV(rms)	*	*	*
Output Offset Voltage		trimmable to zero	*	*	*
vs. Temperature	T_{min} to T_{max}	0.7mV/°C	*	1.0mV/°C max	2.0mV/°C max
POWER SUPPLY SPECIFICATIONS					
Supply Voltage	rated performance	±15V	*	*	*
	operating	±15V to ±18V	±10V to ±18V	**	±10V to ±22V
Supply Current	quiescent	6.5mA max [5mA typ]	*	*	*
Power Supply Rejection	*includes* effects of recommended null pots				
Accuracy		±0.5%/%	*	*	*
Output Offset		±10mV/%	*	*	*
Scale Factor	internal reference	±0.1%/%	*	*	*
Feedthrough		±10mV/%	*	*	*

NOTES: 1. Max input voltage is zero when supplies are turned off.
2. See also Figure 6.

*Specifications same as AD531J.
**Specifications same as AD531K.

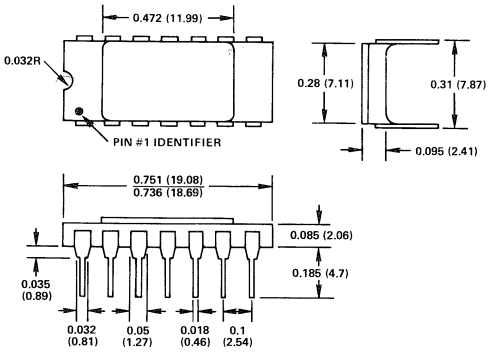
Specifications subject to change without notice. Ordering Guide on next page.

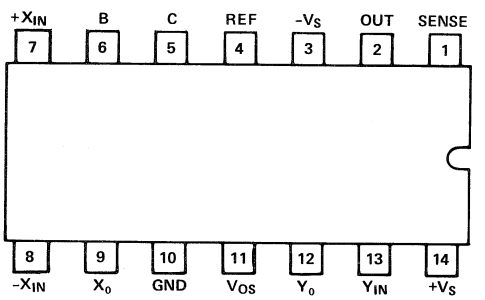
PIN CONFIGURATION & DIMENSIONS

Dimensions shown in inches and (mm).

AD531D

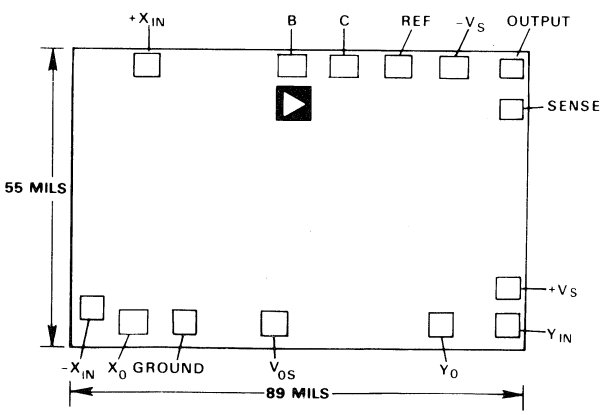
TO-116





BONDING DIAGRAM

The AD531 is available in chip or wafer form, fully tested at +25°C. Because of the critical nature of using unpackaged devices, it is suggested that the factory be contacted for specific information regarding price, delivery and testing.



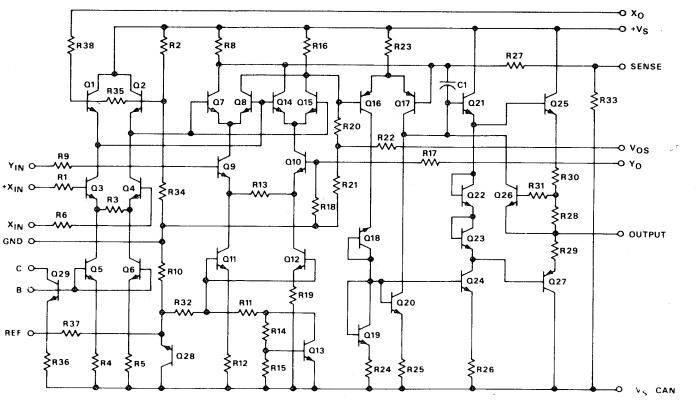


Figure 1a. AD531 Schematic Diagram

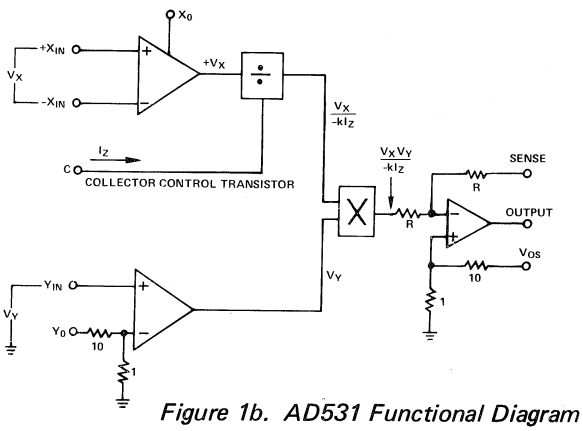


Figure 1b. AD531 Functional Diagram

FUNCTIONAL DESCRIPTION

The basic operation and terminal limits of the AD531 can be derived from the block diagram and complete circuit schematic shown in Figure 1.

The V_X input is fed to a high impedance differential amplifier featuring low distortion and good common mode rejection. The gain of the X channel is set by the externally programmed current source I_Z giving the transfer function V_X/kI_Z within the terminal limits $0 \leqslant V_X/kI_Z < \pm 2.5$ (where k is dimensioned in ohms). Voltage offset is adjusted out at X_O. The V_Y input is fed to one input of a high impedance differential amplifier; the other input being used to null its voltage offset.

The product of the V_X/kI_Z and V_Y terms is resolved in the multiplying cell using Gilbert's linearized transconductance technique. The built-in op amp converts the output of the multiplier cell to the more useful low impedance, single-ended voltage output format. The feedback sense pin provides for load sensing or special applications.

ORDERING GUIDE

ORDER NUMBER	MAX. ERROR	TEMP. RANGE
AD531JD	±2.0%	0 to +70°C
AD531KD	±1.0%	0 to +70°C
AD531LD	±0.5%	0 to +70°C
AD531SD	±1.0%	−55°C to +125°C
AD531S/883	±1.0%	−55°C to +125°C

TRIM PROCEDURE

The standard circuit configuration for computing the function $V_X \cdot V_Y / V_Z$ is shown in Figure 2. The scale factor circuitry has been refined over that shown in Figure 5(a) by adding a Z_O adjust to optimize the dynamic range in V_Z. [For fixed scale applications, the I_Z input can be derived with the circuit shown in Figure 5(b).]

The trim procedure outlined here is designed to provide an optimum set of adjustments with full scale input-output signals of ±10V and a 30dB dynamic range in V_Z (= kI_Z). For different ranges in inputs and/or scale factor (fixed or dynamically variable), the procedure should be modified to reflect the real application (e.g.; for fixed gain applications, trim the AD531 with kI_Z equal to the desired scale factor). Remember too that for best accuracy, V_X is restricted to $V_X/kI_Z \leq 1.0$.

The simplified circuit in Figure 3 offers one approach for trimming the AD531. The test equipment requirements are quite simple, a precision +10.0V dc reference, a signal generator for 20V(p-p) at 10Hz, a CRO, and 10kΩ and 15kΩ resistors to offset the output for the Gain and Z_O adjustments.

Three switches set the conditions for the inputs as noted in the Trim Table, while a fourth switch is used to connect the output to the CRO. Note that the CRO display is a cross-plot between the input 20V(p-p) sine wave generator and the resultant error signals at the output.

While the offset errors will be around zero, the Gain and Z_O adjustments must be made with V_{out} at full scale (±10V). The 10kΩ and 15kΩ resistor divider to the −15V supply is provided to bias the AD531 output to the CRO so that these adjustments can be accurately made around zero volts on the CRO.

Referring to the Trim Table in Figure 4, the output voltage offset V_{OS} is first adjusted to bring the output within normal range on the CRO. Note that the response to $kI_Z < 0V$ (negative half of sine wave) should be ignored as the scale input (I_Z) is bounded by the diode resistor clamp circuit at the output of the op amp. In the next steps, the voltage offset of the Y_{in} and X_{in} amplifiers are zeroed to minimize X_{in} and Y_{in} feedthrough respectively. In both cases, adjust for minimum average (p-p) ac response, ignoring the dc error. The output voltage offset V_{OS} is then readjusted to obtain the best average about dc over the range in kI_Z of interest. Again, ignore

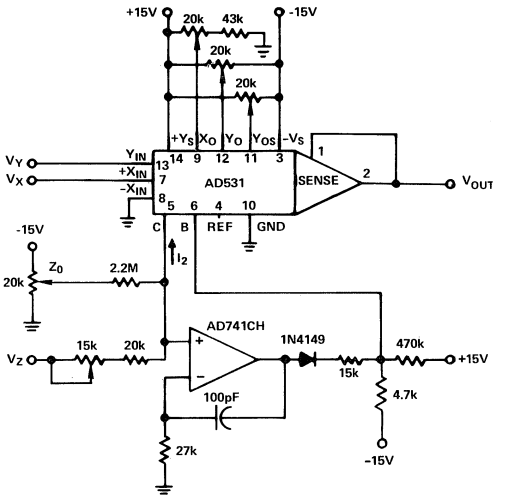


Figure 2. Trim Pot Connections

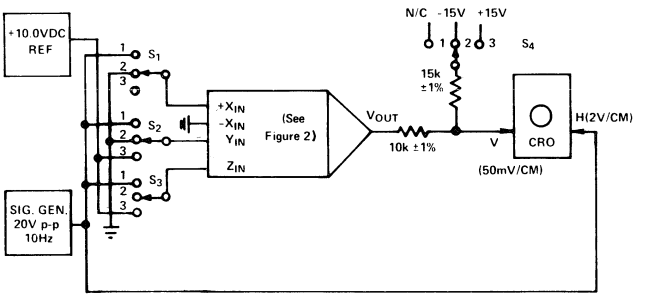


Figure 3. Test Setup

response for $kI_Z < 0V$. The Gain and Z_O pots are now adjusted to obtain the best average performance about 10V (zero volts on the offset CRO display) for the desired range in V_Z. For critical applications, recheck the feedthrough and offset adjustments.

Finally, full scale gain can be fine adjusted to obtain the best average performance in the quadrants of interest. This is done by equalizing the full scale errors between the lowest and highest gain quadrants.

Step	$S_1/(V_X)$	$S_2/(V_Y)$	$S_3/(kI_Z = V_Z)$	S_4/(CRO)	Adjust	CRO Pattern
1	2/(0V)	2/(0V)	1/(20V p-p)	1/(Direct)	V_{OS}: Adjust for best avg dc error for $kI_Z > 0$.	$kI_Z > 0$
2	1/(20V p-p)	2/(0V)	3/(+10V)	1/(Direct)	Y_O: Min (p-p) ac response	min
3	2/(0V)	1/(20V p-p)	3/(+10V)	1/(Direct)	X_O: Min (p-p) ac response	min
4	2/(0V)	2/(0V)	1/(20V p-p)	1/(Direct)	V_{OS}: Adjust for best avg dc error for $kI_Z > 0$.	$kI_Z > 0$
5[1]	1/(20V p-p)	3/(+10V)	1/(20V p-p)	2/(Offset)	Gain: Min error at +10V (scope result about zero)	$kI_Z > 0$
6[2]	1/(20V p-p)	3/(+10V)	1/(20V p-p)	2/(Offset)	Z_O: Best accuracy for low value of kI_Z over range of interest	$kI_Z > 0$

Figure 4. Trim Table

NOTES:
[1] The small error introduced by the divider network to -15V (or +15V for four quadrant scaling) can be removed by fine trimming the divider or the supply to obtain 0V out with +10V (or -10V) in, or by calibrating the device separately at full scale. To optimize gain in two or more quadrants split the errors equally between the highest and lowest gain quadrants of interest.
[2] Step 6 may be omitted for Fixed Gain applications.

GAIN OR SCALE FACTOR ADJUST ($V_Z = kI_Z$)

The principle advantage the AD531 offers over standard transconductance multipliers is its dynamically adjustable gain or scale factor without significant degradation in overall bandwidth throughout its dynamic range. This feature allows for the implicit solution of many complex functions, such as true rms-to-dc conversion and Absolute Value, which will be discussed later under Applications. While standard multipliers can be configured as dividers or AGC loops by connecting the multiplying element in the feedback of an op amp, they are still restricted to the computation of two variables. Further, accuracy and bandwidth are adversely affected with decreasing denominator.

In the AD531 the gain through the X_{in} amplifier is inversely proportional to its "common mode" current, I_r. Thus, to achieve a variable scale factor, a control transistor Q_{29} has been provided to force this current to be equal to an externally derived scaler current I_Z, as shown in Figure 5(c).

FIXED SCALE FACTOR

For fixed scale applications the current I_Z can be set by shorting the Base-Collector (B and C) terminals of the control transistor Q_{29} together and connecting them to the built-in voltage reference V_{ref} through an external gain setting resistor as shown in Figure 5(b). The nominal resistor value is given by $R = [(V_{ref} - V_{BE})/I_Z] - 15k\Omega$, and its required adjustment range by variations in I_Z (= 300 to 500μA, full scale).

Alternatively, the scaling current can be derived by connecting the B and C terminals to ground through an adjustable resistor. This approach improves the overall T.C. in I_Z, but requires a well-regulated $-V_S$ supply.

VARIABLE SCALE FACTOR

For variable gain applications, the control transistor's collector current I_Z can be derived from a programmable current source, such as the voltage-to-current op amp circuit shown in Figure 5(a). The current I_Z is determined by V_Z/R, with the value for R set by both variations in I_Z (= 300 to 500μA, full scale) and the desired full scale response to V_Z. Note that V_Z must be unipolar and positive valued as shown. As the control transistor Q_{29} is inside the amplifier loop, the base of the transistor is servoed by the op amp to support the programmed collector current I_Z.

The non-inverting input of the op amp is used as the summing point because of the inherent inversion from base to collector in the reference transistor. A stabilizing capacitor (100pF) is recommended because there is active gain with Q_{29} inside the loop. Resistors R_1, R_2, R_3 and diode CR_1 are used to both level shift the op amp output to the nominal −13V level at the base of the reference transistor and to prevent op amp latchup.

USER'S GUIDE TO PERFORMANCE SPECIFICATIONS

A clear understanding of the various error sources of the AD531 will assist the user in obtaining optimum performance under his particular operating conditions. The principle sources of error are feedthrough, nonlinearity, output offset, and scale factor (or gain) when using the internally derived reference. In addition, their variations attributable to changes in power supply voltage, operating frequency, and ambient temperature must be considered.

ACCURACY

Accuracy is defined in terms of total error at +25°C with the rated power supply. The value specified is in percent of full scale and includes X_{in} and Y_{in} nonlinearities, feedthrough, and quadrant-to-quadrant scale factor error with I_Z adjusted to full scale (kI_Z = 10V). To this must be added such application dependent error terms as power supply rejection, common mode rejection and temperature coefficients. (Worst-case error over temperature is specified for the AD531L and AD531S however). Total expected error is the rms sum of the individual components, since they are uncorrelated. As the denominator is decreased ($kI_Z < 10V$), an additional error is introduced due to I_Z nonlinearity and feedthrough effects. The former is trimmed at Z_O; the latter at X_O (optional). Finally, additional nonlinearity is introduced as the ratio V_X/kI_Z is made greater than unity. The limiting value is about ±2.5 where the X-input amplifier saturates.

NONLINEARITY

While errors due to output offset, feedthrough and gain can be substantially reduced by external adjustments, nonlinearity remains a basic irreducible limitation to achievable accuracy. Nonlinearity is measured by setting two of the three inputs V_X, V_Y, kI_Z (actually V_X/kI_Z) to full scale and applying a low frequency sine wave of full scale amplitude to the third. The ac output is nulled against the ac input, the gain fine adjusted, and the reduced peak-to-peak error voltage is then a measure of nonlinearity referred to a best straight line.

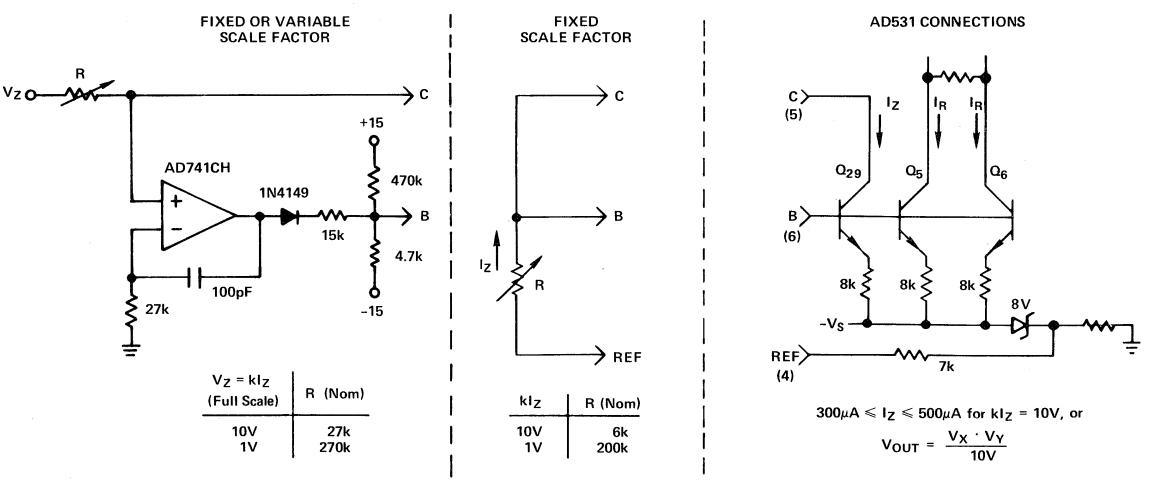


Figure 5. Scale Factor Adjustments

Typical curves for V_X and V_Y nonlinearity are shown in Figure 6. However, the actual wave shapes for each can vary significantly from that shown. The V_X/kI_Z nonlinearity is shown in Steps 5 and 6 of the trim procedure section.

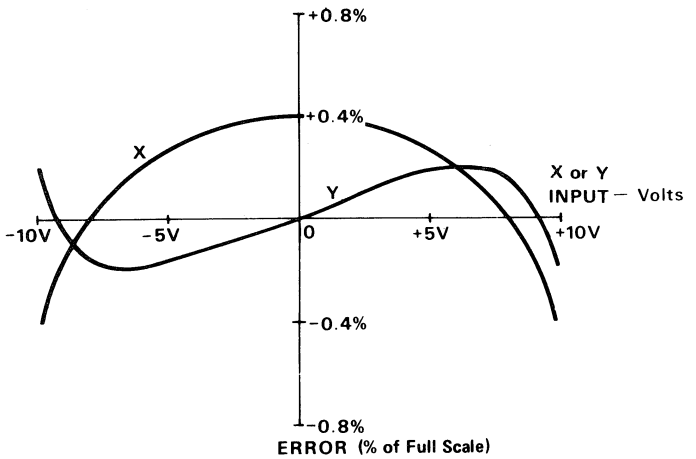


Figure 6. Typical X and Y Nonlinearity for kI_Z = 10V

FEEDTHROUGH

Ideally, the output of a multiplier should be zero when either of the inputs in the numerator is zero, regardless of the signals applied to any of the remaining inputs. Actually there is usually a small residual output that is proportional to the varying inputs and this error is defined as feedthrough.

Low frequency feedthrough is composed of two components, one of which can be trimmed to zero with two external null pots. The trimmable feedthrough error is attributable to the dc voltage offsets of the input differential amplifiers, and can be nulled at X_O and Y_O. (However, as X_O is used to adjust both V_Y and kI_Z feedthrough, the user may have to accept a compromise null point for best performance.)

The untrimmable component is due to the nonlinearity of the multiplier cell, and is the value shown in the electrical specifications. Figure 7 shows typical low frequency feedthrough performance before and after nulling.

At high frequencies, the circuit acts as if there were capacitive coupling between each input and the output. Therefore, at some corner frequency, feedthrough will rise with increasing frequency at 6dB/octave as illustrated in Figure 8, until other shunt capacitance begins to attenuate this effect. This high frequency feedthrough will primarily consist of the fundamental component and will vary in proportion to the non-zero input signal(s).

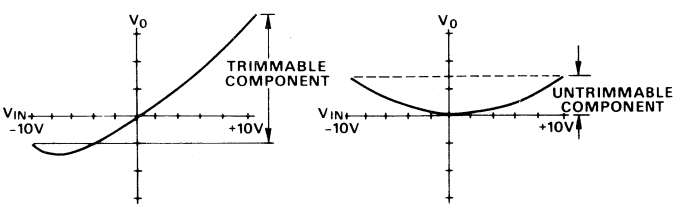


Figure 7. Typical X or Y Feedthrough Before and After Nulling

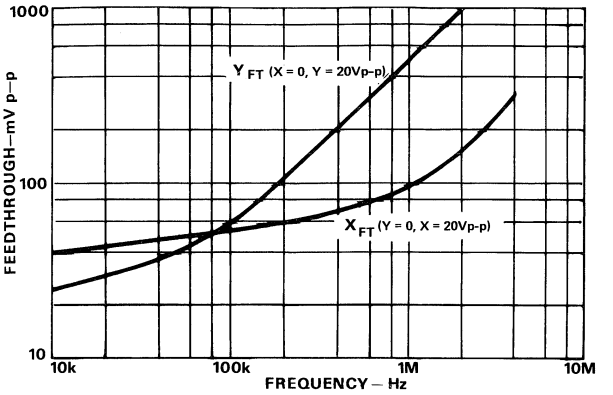


Figure 8. Typical Feedthrough vs. Frequency, kI_Z = 10V

OUTPUT OFFSET

This error obviously has the greatest percentage effect on accuracy for low level output signals. An external trimming pot is used with the AD531 to adjust the initial offset to zero. Output offset drift with temperature and supply voltage variation becomes the limit in accuracy for low level dc output signals.

SCALE FACTOR

The scale factor sets the gain of the multiplier and is represented by $1/kI_Z$. The magnitude and stability of the scaler are determined by the external circuitry or the internal temperature compensated reference source (drift 0.02% typ), if used. Specified overall performance assumes zero error contribution from this source.

DYNAMIC CHARACTERISTICS

The closed loop frequency response of the AD531 in the multiplier mode typically exhibits a 3dB bandwidth of 1MHz and rolls at 6dB/octave thereafter, governed by the output op amp internal compensation. Response through all inputs is essentially identical and is shown in Figure 9 below.

Stable operation is maintained with capacitive loads up to 1000pF in all modes. Higher capacitive loads can be driven if a 100Ω resistor is used in series with the output for isolation.

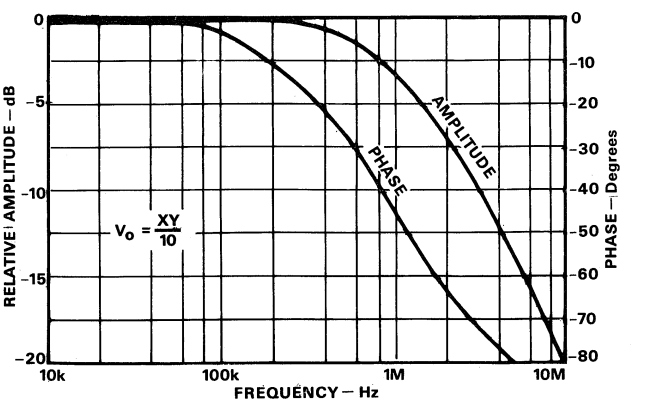


Figure 9. Typical Closed Loop Frequency and Phase Response

For some applications, the instantaneous (sometimes called the absolute) error between the output and input signals may be of primary concern. In this case, vector errors due to phase shift accumulate much more rapidly as a function of frequency than do amplitude or scaler errors. This follows since a phase shift of only 0.57° will cause a vector error of 1%, whereas the amplitude error is only 0.005% at this phase shift. The relationship between these errors is illustrated in the vector diagram of Figure 11.

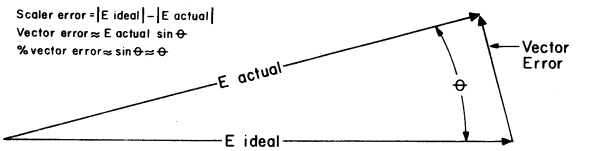


Figure 11. Relationship of Dynamic Errors

POWER SUPPLY CONSIDERATIONS

Although the AD531 is tested and specified with ±15 volt supplies, the K and L versions may be operated at any supply voltage from ±10V to ±18V and the S version from ±10V to ±22V with little affect on overall performance. The input and output signals must be reduced proportionately to prevent saturation at supply voltages below ±15V (see Figure 10).

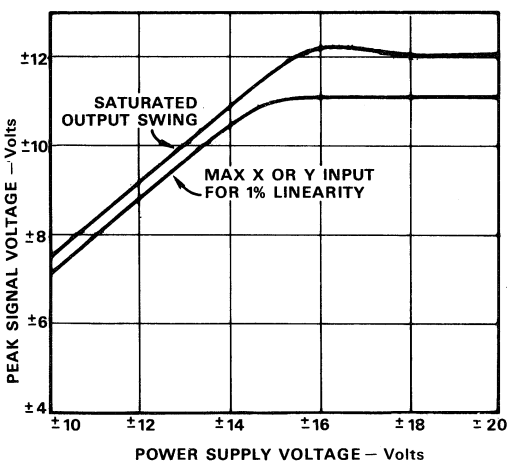


Figure 10. Typical Allowable Signal Swing vs. Supply Voltage, kI_Z = 10V

Power supply rejection figures are specified for accuracy, feedthrough, output offset and scale factor to enable the user to determine supply regulation requirements commensurate with his operating conditions. All the specifications include effects of the recommended null pots.

NOISE CHARACTERISTICS

All AD531's are screened on a sampling basis, both at the wafer stage and at final test, to assure that output noise will have no appreciable effect on accuracy. Typical spot noise vs. frequency characteristics are shown in Figure 12.

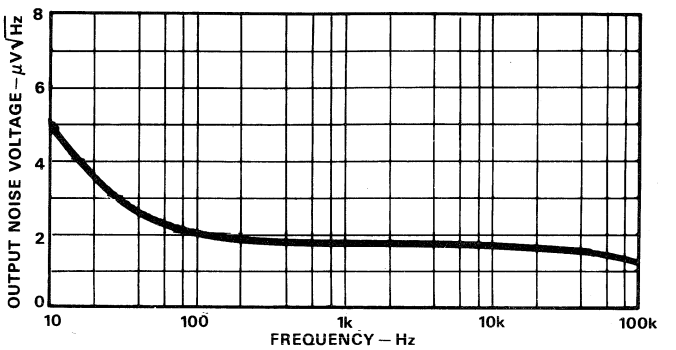


Figure 12. Typical Spot Noise vs. Frequency

APPLYING THE AD531

The differential input and variable gain or scale factor features of the AD531 bring new capability and flexibility to the design of multiplier-divider related circuits. The AD531 is especially well-suited to applications such as the AGC, True rms-to-dc Converter and Vector Computation circuits where the programmable gain feature allows for the implicit solution of these functions over a wide dynamic range of inputs.

The simple multiplier shown in Figure 13 demonstrates how the scale factor kI_Z can be set with a resistor. For squaring applications, simply short Y_{in} to either $+X_{in}$ or $-X_{in}$ (grounding the other) according to the desired polarity at the output. The I_Z linearity adjustments Z_O can be omitted for both cases. The Y_O feedthrough can also be eliminated for the squaring application as a single input offset adjustment is sufficient.

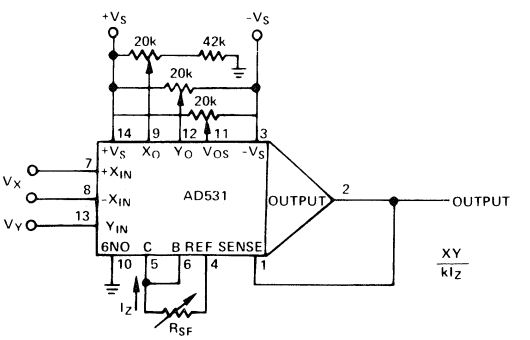


Figure 13. Multiplier/Squarer Connection

In Figure 14 the AD531 is combined with a simple filter to obtain the true rms value of an ac input signal. Unlike averaging circuits that are calibrated to read rms with sine wave inputs, accuracy is not degraded here by wave shape provided that the rms value is scaled to keep $V_x/kI_z \leqslant 2.5$ and $V_A \leqslant 10V$ peak. The circuit is accurate for dc signals and ac inputs within the bandwidth $(100/2\pi RC) \leqslant f \leqslant 100kHz$. By scaling V_{out} = 10V dc for a ±10V dc input, this circuit will give a direct rms reading for 100Hz to 100kHz sine wave inputs from 0.2V to 7.0V peak. Larger input values can saturate the output of the multiplier.

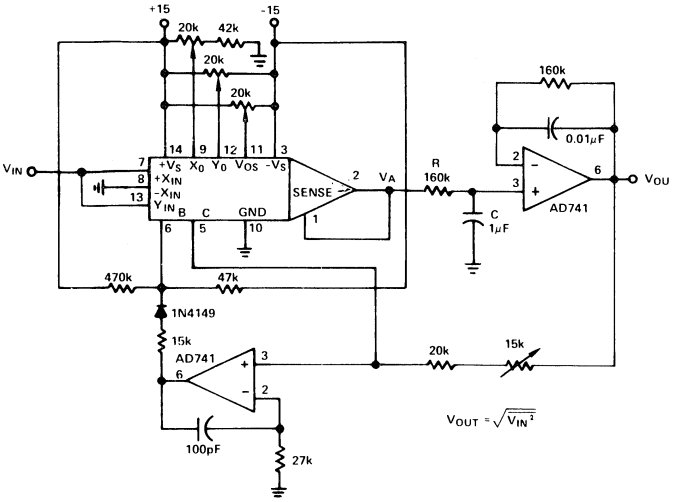


Figure 14. True rms Circuit

The amplitude stabilizing circuit of Figure 15 operates by rectifying the supposedly constant output signal, and comparing it with the voltage at the set level pot. The comparator output is then applied as the control signal (V_Z) to the AD531. The Y-input is biased at near full scale and the input is connected at $+X_{in}$. The X and Y feedthrough adjustments can be eliminated and all of the offset adjusted out at V_{OS}. Unlike standard multipliers connected as AGC loops, the bandwidth of the AD531 is not appreciably reduced with low level denominators. Thus, this circuit can regulate V_{out} to 3V(p-p) ±2% for inputs from 0.4V(p-p) to 6.0V(p-p) from 30Hz to 400kHz.

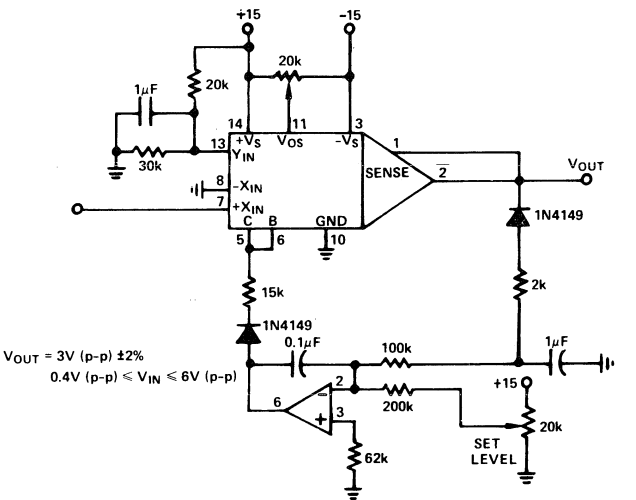


Figure 15. Precision AGC

The Vector Computation Circuit in Figure 16 uses two inexpensive op amps with the AD531 to derive the square root of the sum of the squares. The output of the AD531 is V_A^2/V_Z, which is summed with V_B in the output amplifier. As $V_Z = V_{out} + V_B$, the output will be servoed to achieve the identity . . . .

$$V_{out} = \sqrt{V_A^2 + V_B^2}$$

Operation is restricted to two quadrants, as V_B must be positive. Calibration is simplified by adjusting R_1 with V_A = 10V and V_B = 0V, and then adjusting R_2 with some mid value of V_A and V_B. The Z_O pot is adjusted for accuracy with low level inputs.

Of interest, connecting V_A to $-X_{in}$ and grounding $+X_{in}$ will result in the identity.....

$$V_{out} = \sqrt{V_B^2 - V_A^2}$$

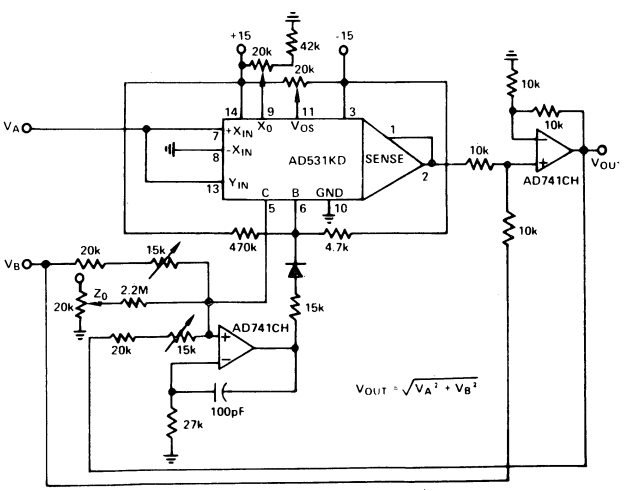


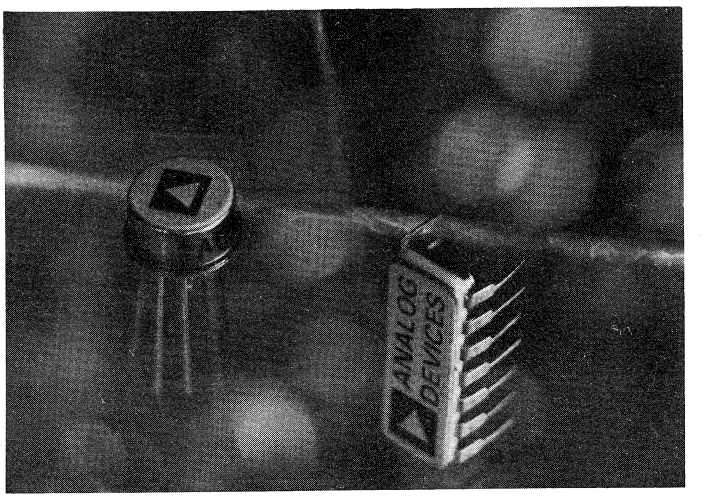
Figure 16. Vector Computer

Internally Trimmed Integrated Circuit Multiplier

AD532

FEATURES
- Pretrimmed To ±1.0% (AD532K)
- No External Components Required
- Guaranteed ±1.0% max 4-Quadrant Error (AD532K)
- Diff Inputs For $(X_1-X_2)(Y_1-Y_2)/10$ Transfer Function
- Monolithic Construction, Low Cost

APPLICATIONS
- Multiplication, Division, Squaring, Square Rooting
- Algebraic Computation
- Power Measurements
- Instrumentation Applications



PRODUCT DESCRIPTION

The AD532 is the first pretrimmed single chip monolithic multiplier/divider. It guarantees a maximum multiplying error of ±1.0% and a ±10V output voltage without the need for any external trimming resistors or output op amp. Because the AD532 is internally trimmed, its simplicity of use provides design engineers with an attractive alternative to modular multipliers, and its monolithic construction provides significant advantages in size, reliability and economy. Further, the AD532 can be used as a direct replacement for other IC multipliers that require external trim networks (such as the AD530).

FLEXIBILITY OF OPERATION

The AD532 multiplies in four quadrants with a transfer function of $(X_1-X_2)(Y_1-Y_2)/10$, divides in two quadrants with a $10Z/(X_1-X_2)$ transfer function, and square roots in one quadrant with a transfer function of $\pm\sqrt{10Z}$. In addition to these basic functions, the differential X and Y inputs provide significant operating flexibility both for algebraic computation and transducer instrumentation applications. Transfer functions, such as XY/10, $(X^2-Y^2)/10$, $\pm X^2/10$, and $10Z/(X_1-X_2)$ are easily attained, and are extremely useful in many modulation and function generation applications, as well as in trigonometric calculations for airborne navigation and guidance applications, where the monolithic construction and small size of the AD532 offer considerable system advantages. In addition, the high CMRR (75dB) of the differential inputs makes the AD532 especially well qualified for instrumentation applications, as it can provide an output signal that is the product of two transducer-generated input signals.

GUARANTEED PERFORMANCE OVER TEMPERATURE

The AD532J and AD532K are specified for maximum multiplying errors of ±2% and ±1% of full scale, respectively at +25°C, and are rated for operation from 0 to +70°C. The AD532S has a maximum multiplying error of ±1% of full scale at +25°C; it is also 100% tested to guarantee a maximum error of ±4% at the extended operating temperature limits of -55°C and +125°C. All devices are available in either the hermetically-sealed TO-100 metal can or TO-116 ceramic DIL packages.

ADVANTAGES OF ON-THE-CHIP TRIMMING OF THE MONOLITHIC AD532

1. True ratiometric trim for improved power supply rejection.
2. Reduced power requirements since no networks across supplies are required.
3. More reliable since standard monolithic assembly techniques can be used rather than more complex hybrid approaches.
4. High impedance X and Y inputs with negligible circuit loading.
5. Differential X and Y inputs for noise rejection and additional computational flexibility.

SPECIFICATIONS (typical @ +25°C with V_S = ±15V dc, V_{OS} grounded, unless otherwise specified)

PARAMETER	CONDITIONS	AD532J	AD532K	AD532S
ABSOLUTE MAX RATINGS				
Supply Voltage		±18V	*	±22V
Internal Power Dissipation		500mW	*	*
Input Voltage (Note 1)				
X, Y, V_{OS}, Z		$\pm V_S$	*	*
Rated Operating Temp Range		0 to +70°C	*	−55°C to +125°C
Storage Temp Range		−65°C to +150°C	*	*
Lead Temperature	60 Sec Soldering	+300°C	*	*
Output Short Circuit	To Ground	Indefinite	*	*
MULTIPLIER SPECIFICATIONS				
Transfer Function		$(X_1-X_2)(Y_1-Y_2)/10$	*	*
Total Error (% F.S.)	V_X = 0/±10V, V_Y = 0/±10V	±2.0% max [±1.5% typ]	±1.0% max [±0.7% typ]	±1.0% max [±0.5% typ]
	T_A = min to max	±2.5%	±1.5%	±4.0% max
vs. Temperature	T_A = min to max	±0.04%/°C	±0.03%/°C	±0.04%/°C max [±0.01%/°C typ]
Nonlinearity				
X Input	V_X = 20V(p-p), V_Y = ±10V	±0.8%	±0.5%	**
Y Input	V_Y = 20V(p-p), V_X = ±10V	±0.3%	±0.2%	**
Feedthrough				
X Input	V_X = 20V(p-p), V_Y = 0, f = 50Hz	200mV(p-p) max [50mV(p-p) typ]	100mV(p-p) max [30mV(p-p) typ]	**
Y Input	V_Y = 20V(p-p), V_X = 0, f = 50Hz	150mV(p-p) max [30mV(p-p) typ]	80mV(p-p) max [25mV(p-p) typ]	**
vs. Temperature	T_A = min to max	2.0mV(p-p)/°C	1.0mV(p-p)/°C	**
DIVIDER SPECIFICATIONS				
Transfer Function		$10Z/(X_1-X_2)$	*	*
Total Error (Note 2)	V_X = −10V, V_Z = ±10V	±2%	±1%	**
	V_X = −1V, V_Z = ±10V	±4%	±3%	**
SQUARER SPECIFICATIONS				
Transfer Function		$(X_1-X_2)^2/10$	*	*
Total Error		±0.8%	±0.4%	**
SQUARE ROOTER SPECIFICATIONS				
Transfer Function		$-\sqrt{10Z}$	*	*
Total Error (Note 2)	V_Z = 0/+10V	±1.5%	±1.0%	**
INPUT SPECIFICATIONS				
Input Resistance				
X, Y Inputs		10MΩ	*	*
Z Input		36kΩ	*	*
Input Bias Current				
X, Y Inputs		3μA	4μA max [1.5μA typ]	**
Z Input		±10μA	±15μA max [±5μA typ]	**
X, Y Inputs	T_A = min to max	10μA	8μA	**
Z Input	T_A = min to max	±30μA	±25μA	**
Input Offset Current				
X, Y Inputs		±0.3μA	±0.1μA	**
Input Voltage Diff/CM	T_A = min to max			
X, Y, Z Inputs	For Rated Accuracy	±10V	*	*
CMRR (X or Y Inputs)	X or Y = ±10V	40dB min	50dB min	**
DYNAMIC SPECIFICATIONS				
Small Signal, Unity Gain		1.0MHz	*	*
Full Power Bandwidth		750kHz	*	*
Slew Rate		45V/μs	*	*
Small Signal Amplitude Error		1% at 75kHz	*	*
Small Signal 1% Vector Error	0.5° phase shift	5kHz	*	*
Settling Time	±10V step	1μs to 2%	*	*
Overload Recovery		2μs to 2%	*	*
OUTPUT AMPLIFIER SPECIFICATIONS				
Output Impedance	Closed Loop	1Ω	*	*
Output Voltage Swing	T_A = min to max			
	$R_L \geq 2k\Omega$, $C_L \leq 1000pF$	±10V min [±13V typ]	*	*
Output Noise	f = 5Hz to 10kHz	0.6mV(rms)	*	*
	f = 5Hz to 5MHz	3.0mV(rms)	*	*
Output Offset Voltage				
Initial Offset	Trimmable To Zero	±40mV	±30mV max	**
vs. Temperature	T_A = min to max	0.7mV/°C	*	2.0mV/°C max
POWER SUPPLY SPECIFICATIONS				
Supply Voltage	Rated Performance	±15V	*	*
	Operating	±10V to ±18V	*	±10V to ±22V
Supply Current	Quiescent	±6mA max [±4mA typ]	*	*
Power Supply Variation				
Multiplier Accuracy		±0.05%/%	*	*
Output Offset		±2.5mV/%	*	*
Scale Factor		−0.03%/%	*	*
Feedthrough		±0.25mV/%	*	*

NOTE: 1. Max input voltage is zero when supplies are turned off. 2. With recommended external trim (see Applications).

*Specifications same as AD532J.

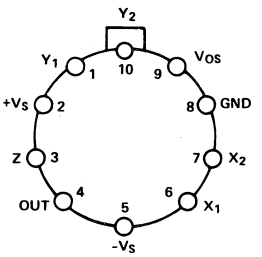
**Specifications same as AD532K.

Specifications subject to change without notice.

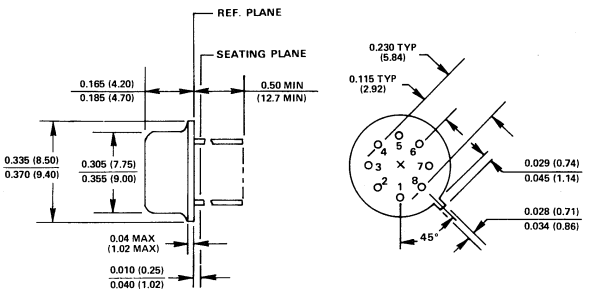
PIN CONFIGURATION & DIMENSIONS

Dimensions shown in inches and (mm).

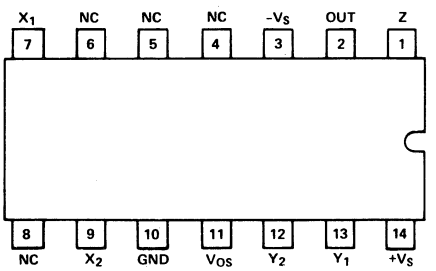
AD532H



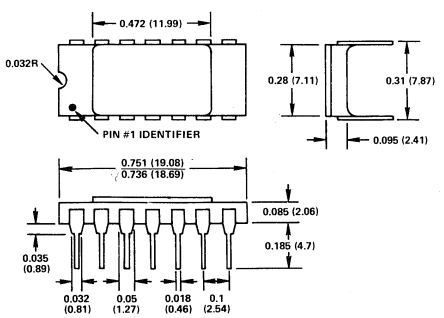
TO-100



AD532D



TO-116



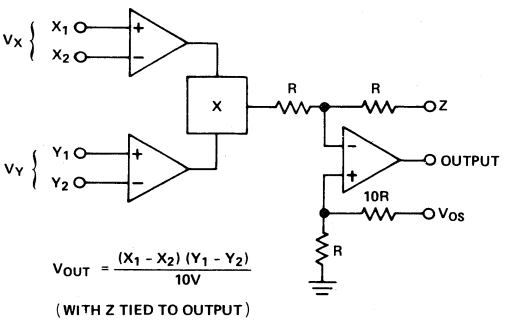


Figure 1. Functional Block Diagram

FUNCTIONAL DESCRIPTION

The functional block diagram for the AD532 is shown in Figure 1, and the complete schematic in Figure 2. In the multiplying and squaring modes, Z is connected to the output to close the feedback around the output op amp. (In the divide mode, it is used as an input terminal.)

The X and Y inputs are fed to high impedance differential amplifiers featuring low distortion and good common mode rejection. The amplifier voltage offsets are actively laser trimmed to zero during production. The product of the two inputs is resolved in the multiplier cell using Gilbert's linearized transconductance technique. The cell is laser trimmed to obtain $V_{out} = (X_1 - X_2)(Y_1 - Y_2)/10$ volts. The built-in op amp is used to obtain low output impedance and make possible self-contained operation. The residual output voltage offset can be zeroed at V_{OS} in critical applications....otherwise it is grounded.

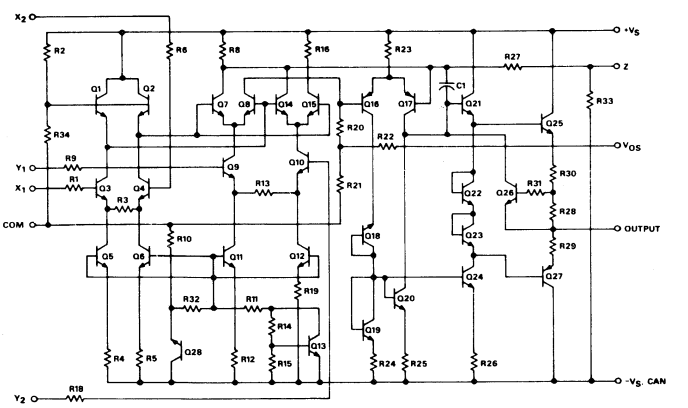


Figure 2. AD532 Schematic Diagram

ORDERING GUIDE

MODEL*	MAX MULT ERROR	TEMPERATURE RANGE
AD532J	±2.0%	0 to +70°C
AD532K	±1.0%	0 to +70°C
AD532S	±1.0%	-55°C to +125°C
AD532S/883	±1.0%	-55°C to +125°C

*Add suffix.....H for TO-100 package; D for TO-116 package.

AD532 PERFORMANCE CHARACTERISTICS

Multiplication accuracy is defined in terms of total error at +25°C with the rated power supply. The value specified is in percent of full scale and includes X_{in} and Y_{in} nonlinearities, feedback and scale factor error. To this must be added such application-dependent error terms as power supply rejection, common mode rejection and temperature coefficients (although worst case error over temperature is specified for the AD532S). Total expected error is the rms sum of the individual components, since they are uncorrelated.

Accuracy in the divide mode is only a little more complex. To achieve division, the multiplier cell must be connected in the feedback of the output op amp as shown in Figure 13. In this configuration, the multiplier cell varies the closed loop gain of the op amp in an inverse relationship to the denominator voltage. Thus, as the denominator is reduced, output offset, bandwidth and other multiplier cell errors are adversely effected. The divide error and drift are then $\epsilon_m \cdot 10/(X_1 - X_2)$ where ϵ_m represents multiplier full scale error and drift, and $(X_1 - X_2)$ is the absolute value of the denominator.

NONLINEARITY

Nonlinearity is easily measured in percent harmonic distortion. The curves of Figures 3 and 4 characterize output distortion as a function of input signal level and frequency respectively, with one input held at plus or minus 10V dc. In Figure 4 the sine wave amplitude is 20V(p-p).

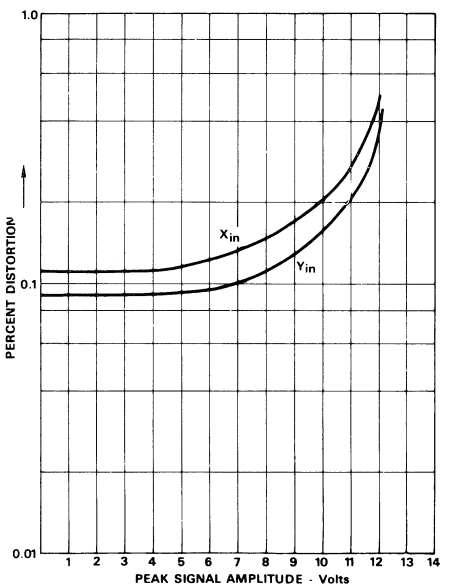


Figure 3. Percent Distortion vs. Input Signal

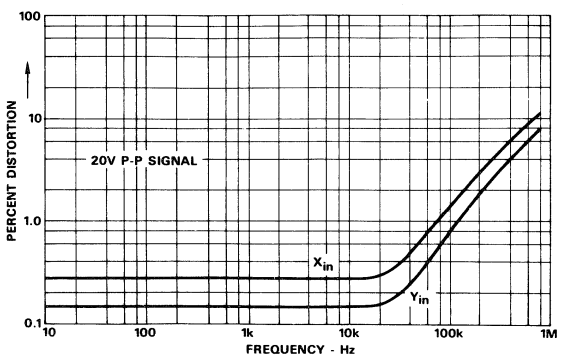


Figure 4. Percent Distortion vs. Frequency

AC FEEDTHROUGH

AC Feedthrough is a measure of the multiplier's zero suppression. With one input at zero, the multiplier output should be zero regardless of the signal applied to the other input. Feedthrough as a function of frequency for the AD532 is shown in Figure 5. It is measured for the condition $V_X = 0$, $V_Y = 20V(p\text{-}p)$ and $V_Y = 0$, $V_X = 20V(p\text{-}p)$ over the given frequency range. It consists primarily of the second harmonic and is measured in millivolts peak-to-peak.

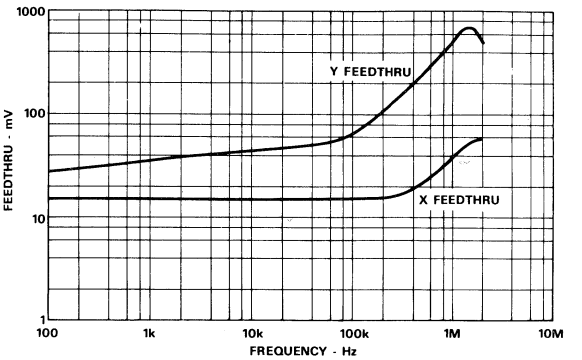


Figure 5. Feedthrough vs. Frequency

COMMON MODE REJECTION

The AD532 features differential X and Y inputs to enhance its flexibility as a computational multiplier/divider. Common mode rejection for both inputs as a function of frequency is shown in Figure 6. It is measured with $X_1 = X_2 = 20V(p\text{-}p)$, $(Y_1 - Y_2) = \pm 10V$ dc and $Y_1 = Y_2 = 20V(p\text{-}p)$, $(X_1 - X_2) = \pm 10V$ dc.

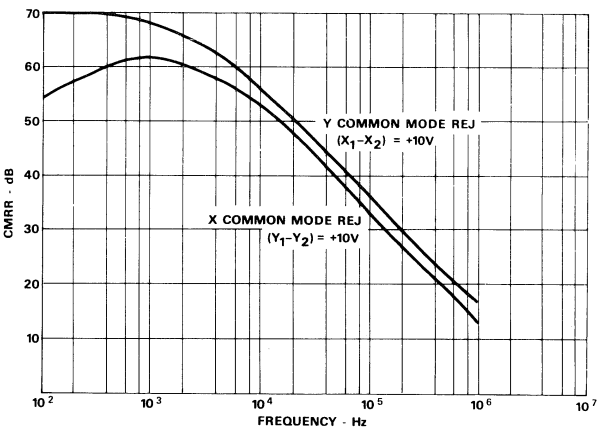


Figure 6. CMRR vs. Frequency

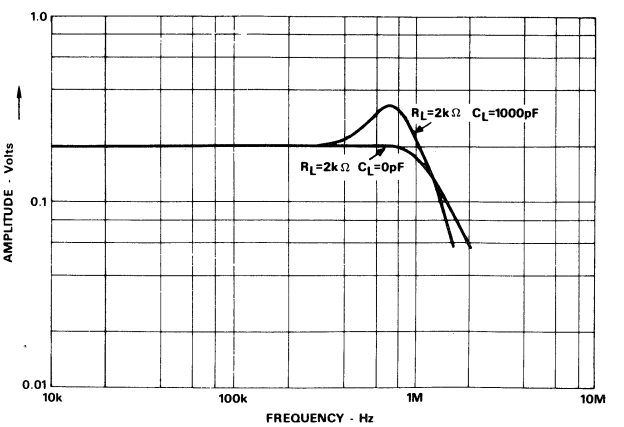


Figure 7. Frequency Response, Multiplying

DYNAMIC CHARACTERISTICS

The closed loop frequency response of the AD532 in the multiplier mode typically exhibits a 3dB bandwidth of 1MHz and rolls off at 6dB/octave thereafter. Response through all inputs is essentially the same as shown in Figure 7. In the divide mode, the closed loop frequency response is a function of the absolute value of the denominator voltage as shown in Figure 8.

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the output for isolation.

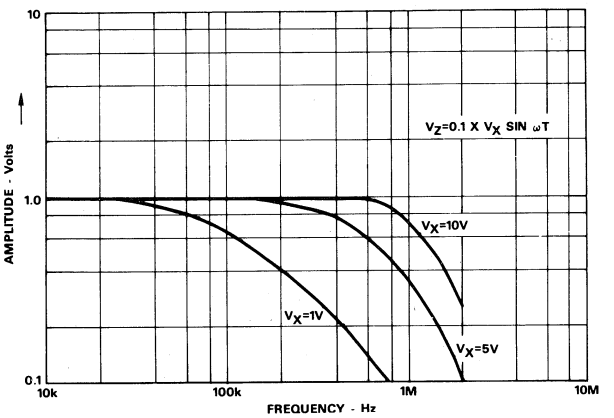


Figure 8. Frequency Response, Dividing

POWER SUPPLY CONSIDERATIONS

Although the AD532 is tested and specified with ±15V dc supplies, it may be operated at any supply voltage from ±10V to ±18V for the J and K versions and ±10V to ±22V for the S version. The input and output signals must be reduced proportionately to prevent saturation, however, with supply voltages below ±15V, as shown in Figure 9. Since power supply sensitivity is not dependent on external null networks as in the AD530 and other conventionally nulled multipliers, the power supply rejection ratios are improved from 3 to 40 times in the AD532.

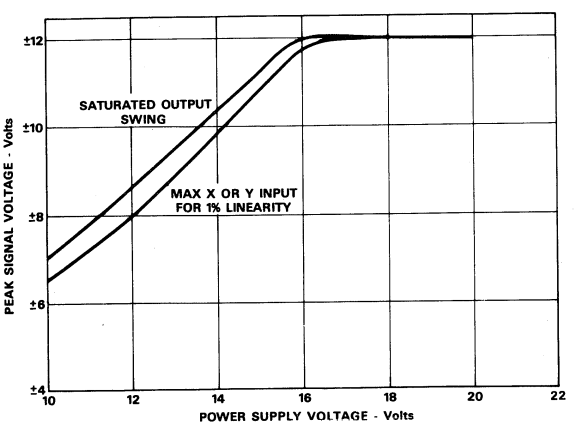


Figure 9. Signal Swing vs. Supply

NOISE CHARACTERISTICS

All AD532's are screened on a sampling basis to assure that output noise will have no appreciable effect on accuracy. Typical spot noise vs. frequency is shown in Figure 10.

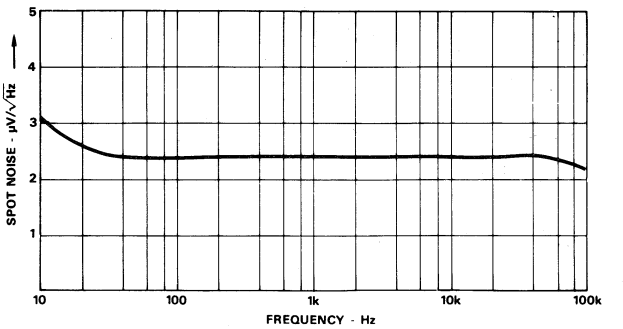


Figure 10. Spot Noise vs. Frequency

APPLICATIONS CONSIDERATIONS

The performance and ease of use of the AD532 is achieved through the laser trimming of thin film resistors deposited directly on the monolithic chip. This trimming-on-the-chip technique provides a number of significant advantages in terms of cost, reliability and flexibility over conventional in-package trimming of off-the-chip resistors mounted or deposited on a hybrid substrate.

First and foremost, trimming on the chip eliminates the need for a hybrid substrate and the additional bonding wires that are required between the resistors and the multiplier chip. By trimming more appropriate resistors on the AD532 chip itself, the second input terminals that were once committed to external trimming networks (e.g., AD530) have been freed to allow fully differential operation at both the X and Y inputs. Further, the requirement for an input attenuator to adjust the gain at the Y input has been eliminated, letting the user take full advantage of the high input impedance properties of the input differential amplifiers. Thus, the AD532 offers greater flexibility for both algebraic computation and transducer instrumentation applications.

Finally, provision for fine trimming the output voltage offset has been included. This connection is optional however, as the AD532 has been factory-trimmed for total performance as described in the listed specifications.

REPLACING OTHER IC MULTIPLIERS

Existing designs using IC multipliers that require external trimming networks (such as the AD530) can be simplified using the pin-for-pin replaceability of the AD532 by merely grounding the X_2, Y_2 and V_{OS} terminals. (The V_{OS} terminal should always be grounded when unused.)

APPLICATIONS

MULTIPLICATION

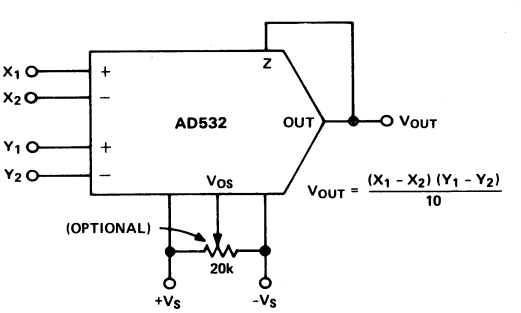


Figure 11. Multiplier Connection

For operation as a multiplier, the AD532 should be connected as shown in Figure 11. The inputs can be fed differentially to the X and Y inputs, or single-ended by simply grounding the unused input. Connect the inputs according to the desired polarity in the output. The Z terminal is tied to the output to close the feedback loop around the op amp (see Figure 1). The offset adjust V_{OS} is optional and is adjusted when both inputs are zero volts to obtain zero out, or to buck out other system offsets.

SQUARE

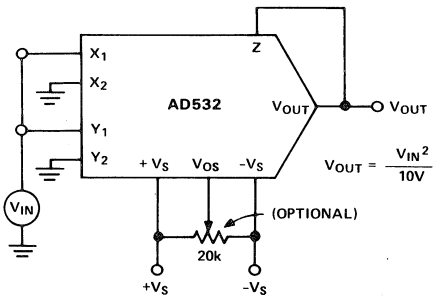


Figure 12. Squarer Connection

The squaring circuit in Figure 12 is a simple variation of the multiplier. The differential input capability of the AD532 can be used, however, to obtain a positive or negative output response to the input....a useful feature for control applications, as it might eliminate the need for an additional inverter somewhere else.

DIVISION

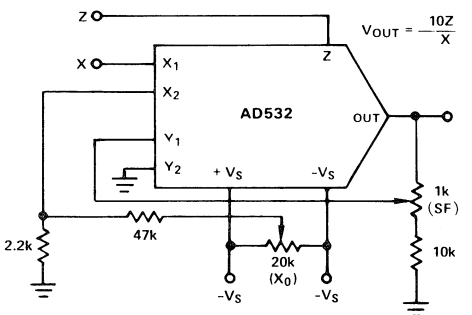


Figure 13. Divider Connection

The AD532 can be configured as a two-quadrant divider by connecting the multiplier cell in the feedback loop of the op amp and using the Z terminal as a signal input, as shown in Figure 13. It should be noted, however, that the output error is given approximately by $10\epsilon_m/(X_1 - X_2)$, where ϵ_m is the total error specification for the multiply mode; and bandwidth by $f_m \cdot (X_1 - X_2)/10$, where f_m is the bandwidth of the multiplier. Further, to avoid positive feedback, the X input is restricted to negative values. Thus for single-ended negative inputs (0V to −10V), connect the input to X_1 and the offset null to X_2; for single-ended positive inputs (0V to +10V), connect the input to X_2 and the offset null to X_1. For optimum performance, gain (S.F.) and offset (X_O) adjustments are recommended as shown and explained in Table I.

For practical reasons, the useful range in denominator input is approximately $-500mV \leqslant (X_1 - X_2) \leqslant -10V$. The voltage offset adjust (V_{OS}), if used, is trimmed with Z at zero and $(X_1 - X_2)$ at full scale.

SQUARE ROOT

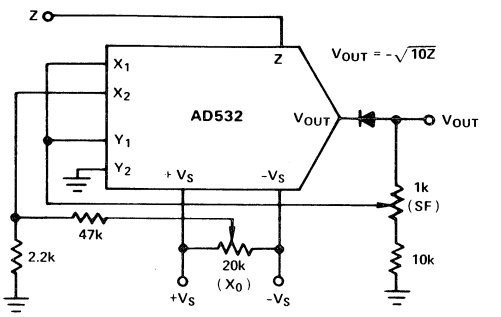


Figure 14. Square Rooter Connection

The connections for square root mode are shown in Figure 14. Similar to the divide mode, the multiplier cell is connected in the feedback of the op amp by connecting the output back to both the X and Y inputs. The diode D_1 is connected as shown to prevent latch-up as Z_{in} approaches 0 volts. In this case, the V_{OS} adjustment is made with Z_{in} = +0.1V dc, adjusting V_{os} to obtain -1.0V dc in the output, $V_{out} = -\sqrt{10Z}$. For optimum performance, gain (S.F.) and offset (X_O) adjustments are recommended as shown and explained in Table I.

DIFFERENCE OF SQUARES

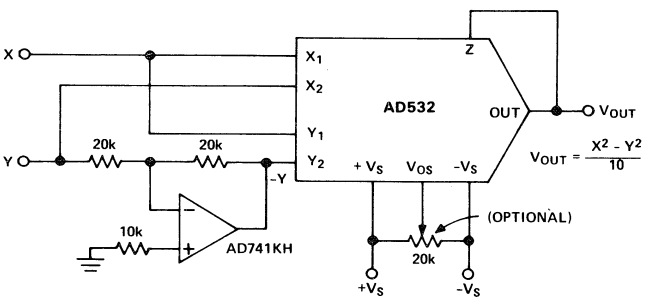


Figure 15. Difference of Squares Connection

The differential input capability of the AD532 allows for the algebraic solution of several interesting functions, such as the difference of squares, $X^2 - Y^2/10$. As shown in Figure 15, the AD532 is configured in the square mode, with a simple unity gain inverter connected between one of the signal inputs (Y) and one of the inverting input terminals ($-Y_{in}$) of the multiplier. The inverter should use precision (0.1%) resistors or be otherwise trimmed for unity gain for best accuracy.

TABLE I

ADJUST PROCEDURE (Divider or Square Rooter)

	DIVIDER			SQUARE ROOTER	
	With:		Adjust for:	With:	Adjust for:
Adjust	X	Z	Vout	Z	Vout
Scale Factor	−10V	±10V	±10V	±10V	−10V
X_o (Offset)	−1V	±1V	±10V	±0.1V	−1V

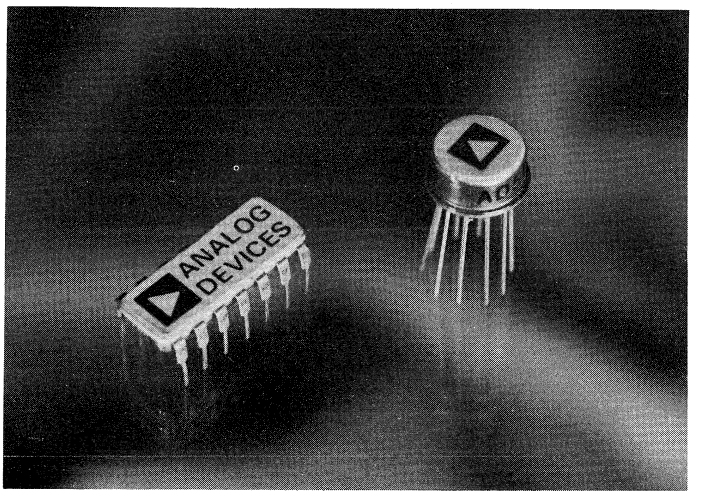
Repeat if required.

ANALOG DEVICES

Low Cost IC Multiplier,Divider,Squarer,Square Rooter

AD533

FEATURES
Low Cost
Simplicity of Operation: Only Four External Adjustments
Max 4-Quadrant Error Below 0.5% (AD533L)
Low Temperature Drift: 0.01%/°C (AD533L)
Multiplies, Divides, Squares, Square Roots



PRODUCT DESCRIPTION

The Analog Devices AD533 is a low cost integrated circuit multiplier comprised of a transconductance multiplying element, stable reference, and output amplifier on a monolithic silicon chip. Specified accuracy is easily achieved by the straight-forward adjustment of feedthrough, output zero, and gain trim pots. The AD533 multiplies in four quadrants with a transfer function of XY/10, divides in two quadrants with a 10Z/X transfer function, and square roots in one quadrant with a transfer function of $-\sqrt{10Z}$. Several levels of accuracy are provided: the AD533J, AD533K, and AD533L, for 0 to +70°C operation, are specified for maximum multiplying errors of 2%, 1%, and 0.5% respectively at +25°C. The AD533S, for operation from -55°C to +125°C, is guaranteed for a maximum 1% multiplying error at +25°C. The maximum error specification is a true measure of overall accuracy since it includes the effects of offset voltage, feedthrough, scale factor, and nonlinearity in all four quadrants.

The low drift design of the AD533 insures that high accuracy is maintained with variations in temperature. The op amp output provides ±10 volts at 5mA, and is fully protected against short circuits to ground or either supply voltage: all inputs are fully protected against over-voltage transients with internal series resistors. The devices provide excellent ac performance, with typical small signal bandwidth of 1.0MHz, full power bandwidth of 750kHz, and slew rate of 45V/μs.

The low cost and simplicity of operation of the AD533 make it especially well suited for use in such widespread applications as modulation and demodulation, automatic gain control and phase detection. Other applications include frequency discrimination, rms computation, peak detection, voltage controlled oscillators and filters, function generation, and power measurements.

All models are available in the hermetically-sealed TO-100 metal can and TO-116 ceramic DIL packages.

SPECIFICATIONS (typical @ +25°C, externally trimmed and V_S = ±15V dc unless otherwise specified)

PARAMETER	CONDITIONS	AD533J	AD533K	AD533L	AD533S
ABSOLUTE MAX RATINGS					
Internal Power Dissipation		500mW	*	*	*
Input Voltage (Note 1)					
X_{in}, Y_{in}, Z_{in}, X_O, Y_O, Z_O		$\pm V_S$	*	*	*
Rated Operating Temp Range		0 to +70°C	*	*	-55°C to +125°C
Storage Temp Range		-65°C to +150°C	*	*	*
Output Short Circuit	To Ground	Indefinite	*	*	*
MULTIPLIER SPECIFICATIONS					
Transfer Function		XY/10	*	*	*
	Untrimmed	XY/6 max [XY/10 min]	*	*	*
Total Error (of full scale)		±2.0% max	±1.0% max	±0.5% max	±1.0% max
	T_A = min to max	±3.0%	±2.0%	±1.0%	±1.5%
vs. Temperature	T_A = min to max	±0.04%/°C	±0.03%/°C	±0.01%/°C	±0.01%/°C
Nonlinearity					
X Input	$V_X = V_O$ = 20V(p-p)	±0.8%	±0.5%	**	**
Y Input	$V_Y = V_O$ = 20V(p-p)	±0.3%	±0.2%	**	**
Feedthrough					
X Input	V_X = 20V(p-p), V_y = 0, f = 50Hz	150mV(p-p) max	200mV(p-p) max	50mV(p-p) max	100mV (p-p) max
Y Input	V_y = 20V(p-p), V_X = 0, f = 50Hz	200mV(p-p) max	150mV(p-p) max	50mV(p-p) max	100mV (p-p) max
DIVIDER SPECIFICATIONS					
Transfer Function		10Z/X	*	*	*
	Untrimmed	10Z/X max [6Z/X min]	*	*	*
Total Error (of full scale)	V_x=-10V dc, V_z=±10V dc	±1.0%	±0.5%	±0.2%	±0.5%
	V_x=-1V dc, V_z=±10V dc	±3.0%	±2.0%	±1.5%	±2.0%
SQUARER SPECIFICATIONS					
Transfer Function		$X^2/10$	*	*	*
	Untrimmed	$X^2/6$ max [$X^2/10$ min]	*	*	*
Total Error (of full scale)		±0.8%	±0.4%	±0.2%	±0.4%
SQUARE ROOTER SPECIFICATIONS					
Transfer Function		$-\sqrt{10Z}$	*	*	*
	Untrimmed	$-\sqrt{10Z}$ max [$-\sqrt{6Z}$ min]	*	*	*
Total Error (of full scale)		±0.8%	±0.4%	±0.2%	±0.4%
INPUT SPECIFICATIONS					
Input Resistance					
X Input		10MΩ	*	*	*
Y Input		6MΩ	*	*	*
Z Input		36kΩ	*	*	*
Input Bias Current					
X, Y Inputs		3μA	7.5μA max	5μA max	7.5μA max
Z Input		±25μA	*	*	*
X, Y Inputs	T_A = min to max	12μA	10μA	7μA	7μA
Z Input	T_A = min to max	±35μA	*	*	*
Input Voltage	T_A = min to max				
V_X, V_y, V_z	For Rated Accuracy	±10V	*	*	*
DYNAMIC SPECIFICATIONS					
Small Signal, Unity Gain		1.0MHz	*	*	*
Full Power Bandwidth		750kHz	*	*	*
Slew Rate		45V/μs	*	*	*
Small Signal Amplitude Error		1% at 75kHz	*	*	*
Sm Sig 1% Vector Error	0.5° phase shift	5kHz	*	*	*
Settling Time	±10V step	1μs to 2%	*	*	*
Overload Recovery		2μs to 2%	*	*	*
OUTPUT AMPLIFIER SPECIFICATIONS					
Output Impedance		100Ω	*	*	*
Output Voltage Swing	T_A = min to max				
	$R_L \geq 2k\Omega$, $C_L \leq 1000pF$	±10V min	*	*	*
Output Noise	f = 5Hz to 10kHz	0.6mV(rms)	*	*	*
	f = 5Hz to 5MHz	3.0mV(rms)	*	*	*
Output Offset Voltage		Trimmable To Zero	*	*	*
vs. Temperature	T_A = min to max	0.7mV/°C	*	*	*
POWER SUPPLY SPECIFICATIONS					
Supply Voltage	Rated Performance	±15V	*	*	*
	Operating	±15V to ±18V	±10V to ±18V	±10V to ±18V	±10V to ±22V
Supply Current	Quiescent	±6mA max	*	*	*
Power Supply Variation	*Includes* Effects of Recommended Null Pots				
Multiplier Accuracy		±0.5%/%	*	*	*
Output Offset		±10mV/%	*	*	*
Scale Factor		±0.1%/%	*	*	*
Feedthrough		±10mV/%	*	*	*

Note 1: Max input voltage is zero when supplies are turned off.

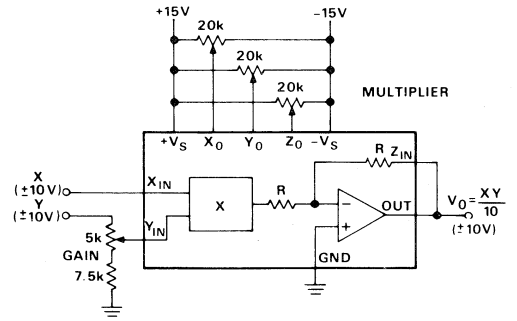
*Specifications same as AD533J

**Specifications same as AD533K

Specifications subject to change without notice.

MULTIPLIER

Multiplier operation is accomplished by closing the loop around the internal op amp with the Z input connected to the output. The X_O null pot balances the X input channel to minimize Y feedthrough and similarly the Y_O pot minimizes the X feedthrough. The Z_O pot nulls the output op amp offset voltage and the gain pot sets the full scale output level.



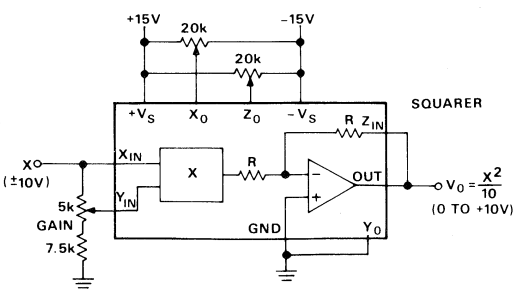
TRIM PROCEDURES

1. With X = Y = 0 volts, adjust Z_O for 0V dc output.
2. With Y = 20 volts p-p (at f = 50Hz) and X = 0V, adjust X_O for minimum ac output.
3. With X = 20 volts p-p (at f = 50Hz) and Y = 0V, adjust Y_O for minimum ac output.
4. Readjust Z_O for 0V dc output.
5. With X = +10V dc and Y = 20 volts p-p (at f = 50Hz), adjust gain for output = Y_{in}.

NOTE: For best accuracy over limited voltage ranges (e.g., ±5V), gain and feedthrough adjustments should be optimized with the inputs in the desired range, as linearity is considerably better over smaller ranges of input.

SQUARER

Squarer operation is a special case of multiplier operation where the X and Y inputs are connected together and two quadrant operation results since the output is always positive. When the X and Y inputs are connected together, a composite offset results which is the algebraic sum of the individual offsets which can be nulled using the X_O pot alone.

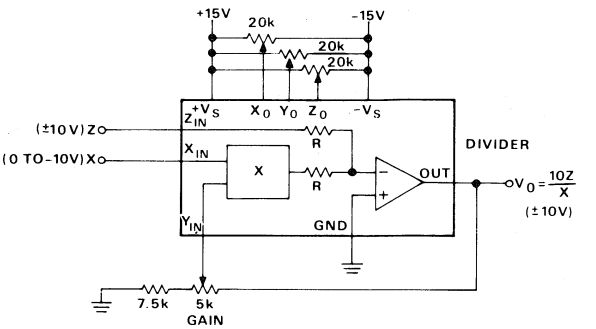


TRIM PROCEDURES

1. With X = 0 volts, adjust Z_O for 0V dc output.
2. With X = +10V dc, adjust gain for +10V dc output.
3. Reverse polarity of X input and adjust X_O to reduce the output error to ½ its original value, readjust the gain to take out the remaining error.
4. Check the output offset with input grounded. If nonzero, repeat the above procedure until no errors remain.

DIVIDER

The divide mode utilizes the multiplier in a fed-back configuration where the Y input now controls the feedback factor. With X = full scale, the gain (V_O/Z) becomes unity after trimming. Reducing the X input reduces the feedback around the op amp by a like amount, thereby increasing the gain. This reciprocal relationship forms the basis of the divide mode. Accuracy and bandwidth decrease as the denominator decreases.

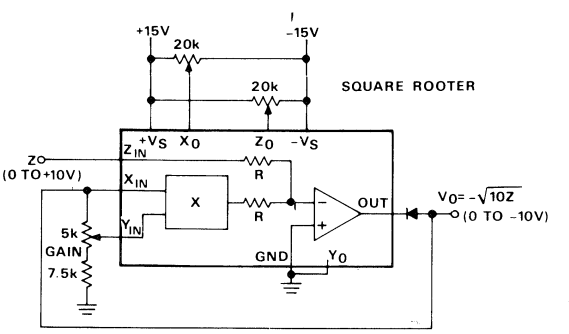


TRIM PROCEDURES

1. Set all pots at mid-scale.
2. With Z = 0V, trim Z_O to hold the output constant, as X is varied from -10V dc through -1V dc.
3. With Z = 0V.X = -10V dc, trim Y_O for 0V dc.
4. With Z = X or -X, trim X_O for the minimum worst-case variations as X is varied from -10V dc to -1V dc.
5. Repeat steps 2 and 3 if step 4 required a large initial adjustment.
6. With Z = X or -X, trim the gain for the closest average approach to ±10V dc output as X is varied from -10V dc to -3V dc.

SQUARE ROOTER

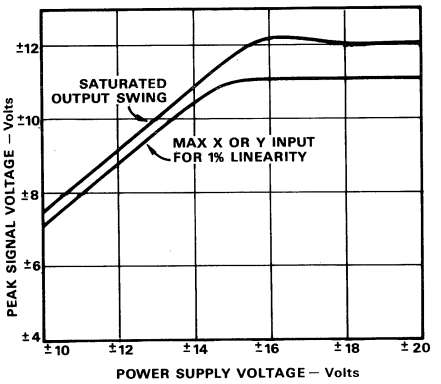
This mode is also a fed-back configuration with both the X and Y inputs tied to the op amp output through an external diode to prevent latchup. Accuracy, noise and frequency response are proportional to $\sqrt{Z}$, which implies a wider usable dynamic range than the divide mode.



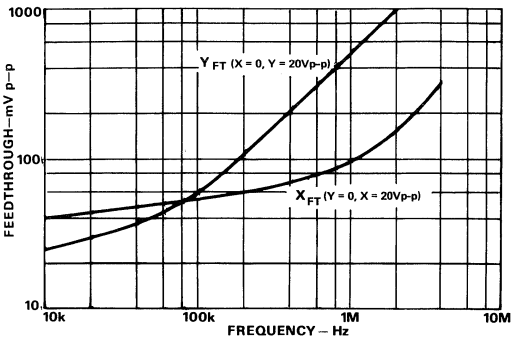
TRIM PROCEDURES

1. With Z = +0.1V dc, adjust Z_O for Output = -1.0V dc.
2. With Z = +10.0V dc, adjust gain for Output = -10.0V dc.
3. With Z = +2.0V dc, adjust X_O for Output = -4.47 ±0.1V dc.
4. Repeat steps 2 and 3, if necessary. Repeat step 1.

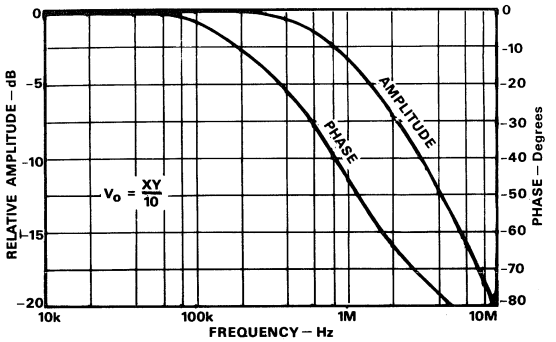
TYPICAL PERFORMANCE CHARACTERISTICS



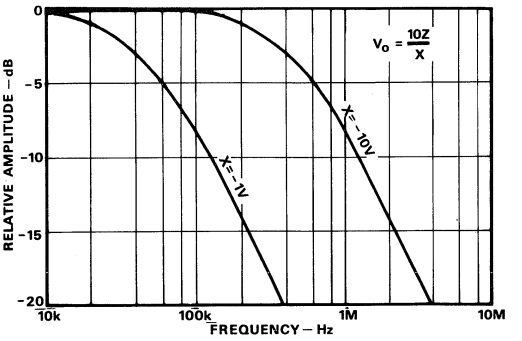
Allowable Signal Swing vs. Supply Voltage



Feedthrough vs. Frequency



Closed Loop Frequency and Phase Response

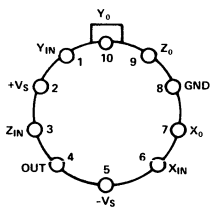


Divide Mode Frequency Response

PIN CONFIGURATION & DIMENSIONS

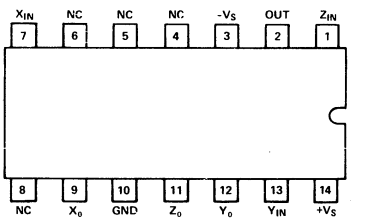
Dimensions shown in inches and (mm).

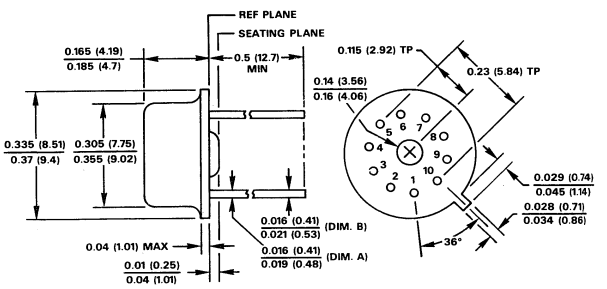
AD533H
TO-100

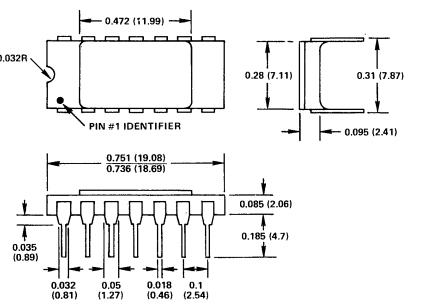


TOP VIEW

AD533D
TO-116







ORDERING GUIDE

MODEL	MULT. ERROR (Max @ +25°C)	TEMP. RANGE	ORDER NUMBER
AD533J	±2.0%	0 to +70°C	AD533JH*
			AD533JD†
AD533K	±1.0%	0 to +70°C	AD533KH
			AD533KD
AD533L	±0.5%	0 to +70°C	AD533LH
			AD533LD
AD533S	±1.0%	–55°C to +125°C	AD533SH
			AD533SD

*TO-100 metal can package †TO-116 ceramic DIL package

ANALOG DEVICES

Internally Trimmed Precision I.C. Multiplier

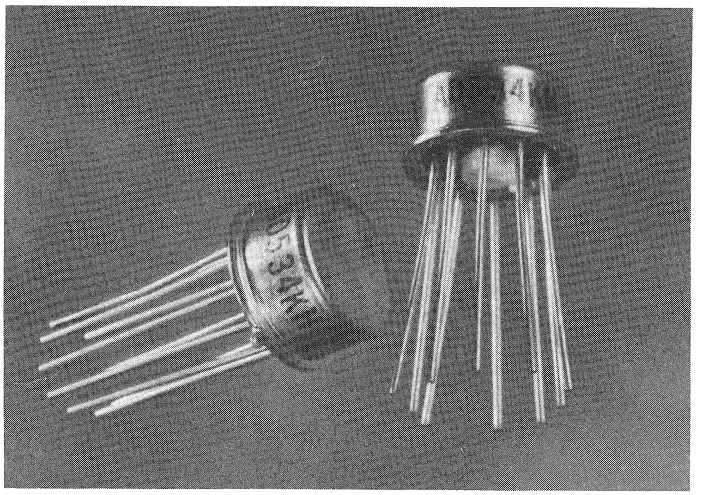
AD534

FEATURES

Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X100 Gain
Low Noise Design: 90μV rms, 10Hz–10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

APPLICATIONS

High Quality Analog Signal Processing
Differential Ratio and Percentage Computations
Algebraic and Trigonometric Function Synthesis
Wideband, High-Crest rms-to-dc Conversion
Accurate Voltage Controlled Oscillators and Filters



PRODUCT DESCRIPTION

The AD534 is a monolithic laser trimmed four-quadrant multiplier-divider having accuracy specifications previously found only in expensive hybrid or modular products. A maximum multiplication error of ±0.25% is guaranteed for the AD534L without any external trimming. Excellent supply-rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions of use. It is the first multiplier to offer fully differential, high impedance operation on all inputs, including the Z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00; by means of an external resistor, this can be reduced by any amount down to 3, with corresponding reductions in bias current and noise level.

The wide spectrum of applications and the availability of several grades commend this multiplier as the first choice for all new designs. The AD534J (±1% max error), AD534K (±0.5% max) and AD534L (±0.25% max) are specified for operation over the 0 to +70°C temperature range. The AD534S (±1% max) and AD534T (±0.5% max) are specified over the extended temperature range, −55°C to +125°C. All devices are available in the hermetically-sealed TO-100 metal can.

PROVIDES GAIN WITH LOW NOISE

The AD534 is the first general purpose multiplier capable of providing gains up to X100, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. In effect, the AD534 can be very effectively employed as a variable gain differential input amplifier with high common mode rejection. The gain option is available in all modes, and will be found to simplify the implementation of many function-fitting algorithms such as those used to generate sine and tangent. The utility of this feature is enhanced by the inherent low noise of the AD534: 90μV, rms (depending on the gain), a factor of 10 lower than previous monolithic multipliers. Drift and feedthrough are also substantially reduced over earlier designs.

UNPRECEDENTED FLEXIBILITY

The precise calibration and differential Z-input provide a degree of flexibility found in no other currently available multiplier. Standard MDSSR functions (multiplication, division, squaring, square-rooting) are easily implemented while the restriction to particular input/output polarities imposed by earlier designs has been eliminated. Signals may be summed into the output, with or without gain and with either a positive or negative sense. Many new modes based on implicit-function synthesis have been made possible, usually requiring only external passive components. The output can be in the form of a current, if desired, facilitating such operations as integration.

SPECIFICATIONS (typical at +25°C, with $\pm V_S$ = 15V, $R_L \geq 2k$, unless otherwise stated)

PARAMETER	CONDITIONS	AD534J	AD534K	AD534L	AD534S	AD534T
MULTIPLIER PERFORMANCE						
Transfer Function		$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$	*	*	*	*
Total Error[1]	-10V ≤ X, Y ≤ +10V	±1.0% max	±0.5% max	±0.25% max	*	**
	T_A = min to max					
	V_S = ±14 to ±16V	±1.5%	±1.0%	±0.5%	±2.0% max	±1.0% max
vs. Temperature		±0.022%/°C	±0.015%/°C	±0.008%/°C	±0.02%/°C max	±0.01%/°C max
Scaling Voltage Error	SF = 10.00 nominal[2]	±0.25%	±0.1%	**	*	**
Temperature-Coefficient of						
Scaling-Voltage	T_A = min to max	±0.02%/°C	±0.01%/°C	±0.005%/°C	*	±0.005%/°C max
Supply-Related Error	$\pm V_S$ = (15V) ±1V	±0.01%	*	*	*	*
Nonlinearity, X	X = 20V pk-pk					
	Y = ±10V	±0.4%	±0.2% (0.3% max)	±0.1% (0.12% max)	*	**
Nonlinearity, Y	Y = 20V pk-pk					
	X = ±10V	±0.01%	±0.01% (±0.1% max)	±0.005% (±0.1% max)	*	**
Feedthrough[3], X	Y nulled					
	X = 20V pk-pk 50Hz	±0.3%	±0.15% (0.3% max)	±0.05% (0.12% max)	*	**
Feedthrough[3], Y	X nulled					
	Y = 20V pk-pk 50Hz	±0.01%	±0.01% (±0.1% max)	±0.003% (±0.1% max)	*	**
Output Offset Voltage		±5mV (±30mV max)	±2mV (±15mV max)	±2mV (±10mV max)	*	**
DIVIDER PERFORMANCE						
Transfer Function	$X_1 > X_2$	$10\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$	*	*	*	*
Total Error[1]	X = 10V					
	-10V ≤ Z ≤ +10V	±0.75%	±0.35%	±0.2%	*	**
	X = 1V					
	-1V ≤ Z ≤ +1V	±2.0%	±1.0%	±0.8%	*	**
	0.1V ≤ X ≤ 10V					
(Note 4)	-10V ≤ Z ≤ +10V	±2.5%	±1.0%	±0.8%	*	**
SQUARER PERFORMANCE						
Transfer Function		$\frac{(X_1 - X_2)^2}{10} + Z_2$	*	*	*	*
Total Error[1]	-10V ≤ X ≤ +10V	±0.6%	±0.3%	±0.2%	*	**
SQUARE-ROOTER PERFORMANCE						
Transfer Function	$Z_1 < Z_2$	$\sqrt{10(Z_2 - Z_1)} + X_2$	*	*	*	*
Total Error[1]	1V ≤ Z ≤ 10V	±1.0%	±0.5%	±0.25%	*	**
INPUT AMPLIFIERS (X, Y and Z)[5]						
Signal Voltage Range	Rated Accuracy					
	(Diff. or CMR)	±10V	*	*	*	*
	Operating (Diff.)	±12V	*	*	*	*
Offset Voltage, X, Y		±5mV (±20mV max)	±2mV (±10mV max)	**	*	**
Drift	T_A = min to max	100μV/°C	50μV/°C	**	*	150μV/°C
Offset Voltage, Z		±5mV (±30mV max)	±2mV (±15mV max)	±2mV (±10mV max)	*	**
Drift	T_A = min to max	200μV/°C	100μV/°C	**	500μV/°C max	300μV/°C max
CMRR (X, Y, Z)	50Hz, 20V pk-pk	80dB (60dB min)	90dB (70dB min)	**	*	**
Bias Current	Diff. Input = 0	0.8μA (2μA max)	*	*	*	*
Offset Current	Diff. Input = 0	0.1μA	*	0.05μA (0.2μA max)	*	*
Differential Resistance		10MΩ	*	*	*	*
OUTPUT AMPLIFIER[5]						
Open-Loop Gain	f = 50Hz	70dB	*	*	*	*
Small-Signal BW	V_{OUT} = 0.1V rms	1MHz	*	*	*	*
1% Amplitude Error	C_{LOAD} = 1000pF	50kHz	*	*	*	*
Output Voltage Swing	T_A = min to max	±11V min	*	*	*	*
Slew Rate	V_{OUT} 20V pk-pk	20V/μs	*	*	*	*
Settling Time to ±1%	ΔV_{OUT} = 20V	2μs	*	*	*	*
Output Impedance	Unity-Gain, f ≤1kHz	0.1Ω	*	*	*	*
Noise Spectral-Density	SF = 10	$0.8\mu V/\sqrt{Hz}$	*	*	*	*
	SF = 3 (Note 6)	$0.4\mu V/\sqrt{Hz}$	*	*	*	*
Wideband Noise	f = 10Hz to 5MHz	1mV rms	*	*	*	*
	f = 10Hz to 10kHz	90μV rms	*	*	*	*
	f = 10Hz to 10kHz,					
	SF = 3 (Note 6)	60μV rms	*	*	*	*
Maximum Output Current	R_L = 0, T_A = min to max	30mA	*	*	*	*
POWER SUPPLY SPECIFICATIONS						
Supply Voltage	Rated Performance	±15V	*	*	*	*
	Operating	±8V to ±18V	*	*	±8V to ±22V	±8V to ±22V
Supply Current	Quiescent	4mA (6mA max)	*	*	*	*

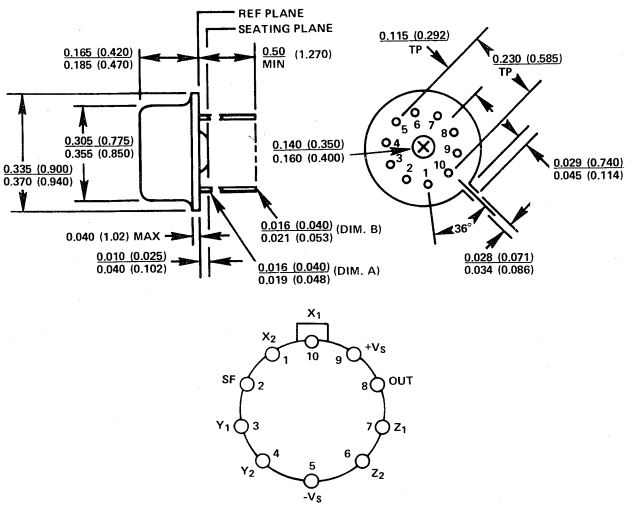
NOTES
*Same as AD534J specs. **Same as AD534K specs.
Specifications subject to change without notice.

[1] Figures given are percent of full-scale, ±10V (i.e., 0.01% = 1mV).
[2] May be adjusted to values between 3V and 10V using external resistor between $-V_S$ and SF.
[3] Irreducible component due to nonlinearity: excludes effect of offsets.
[4] With external Z-offset adjustment, Z ≤ ±X.
[5] See Functional Block Diagram, Figure 1, for definition of sections.
[6] Using external resistor adjusted to give SF = 3.

PIN CONFIGURATION & DIMENSIONS

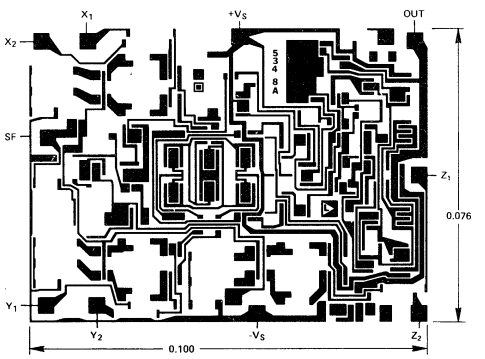
Dimensions shown in dimensions and (mm).

TO-100

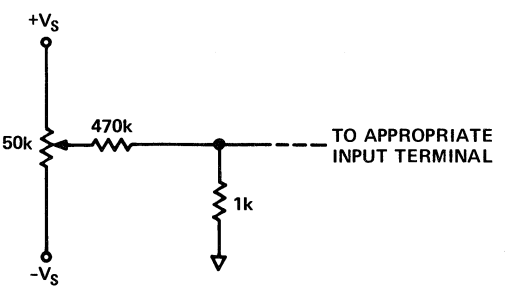


TOP VIEW

CHIP DIMENSIONS & PAD LAYOUT



OPTIONAL TRIMMING CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

	AD534J, K, L	AD534S, T
Supply Voltage	±18V	±22V
Internal Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages, X_1 X_2 Y_1 Y_2 Z_1 Z_2	$\pm V_S$	*
Rated Operating Temperature Range	0 to +70°C	-55 to +125°C
Storage Temperature Range	-65 to +150°C	*
Lead Temperature, 60s soldering	+300°C	*

*Same as AD534J specs.

FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD534. Inputs are converted to differential currents by three identical voltage-to-current converters, each trimmed for zero offset. The product of the X- and Y-currents is generated by a multiplier cell using Gilbert's translinear technique with an internal scaling voltage equivalent to 13.33V at the inputs, providing over-range capacity. The Z signal is multiplied by a fixed factor of 0.75, which restores the overall scaling voltage, SF, to 10.00, also laser trimmed to value. The difference between XY/SF and Z is then applied to the high gain output amplifier. This permits various closed loop configurations and dramatically reduces nonlinearities due to the input amplifiers, a dominant source of distortion in earlier designs. The effectiveness of the new scheme can be judged from the fact that under typical conditions as a multiplier the nonlinearity on the Y-input, with X at full scale (±10V), is ±0.005% of F.S.; even at its worst point, which occurs when X = ±6.4V, it is typically only ±0.025% of F.S. Nonlinearity for signals applied to the X-input, on the other hand, is determined almost entirely by the multiplier element and is parabolic in form. This error is a major factor in determining the overall accuracy of the unit, and hence, is closely related to the device grade.

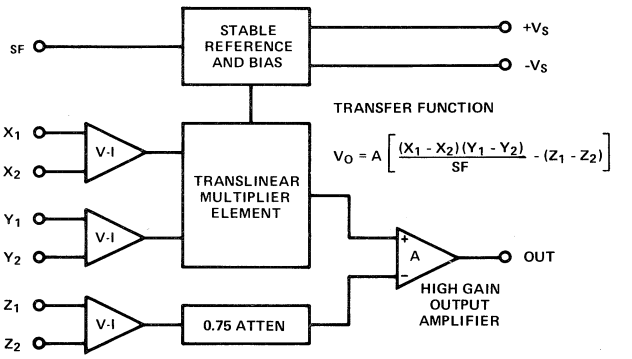


Figure 1. AD534 Functional Block Diagram

The generalized transfer function for the AD534 is given by:

$$V_{OUT} = A\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages (full scale = ±SF, peak= ±1.25SF)

SF = scale factor, pretrimmed to 10.00 but adjustable by the user down to 3.

In most cases the open loop gain can be regarded as infinite, and SF will be 10. The operation performed by the AD534, can then be described in terms of equation:

$$(X_1 - X_2)(Y_1 - Y_2) = 10(Z_1 - Z_2)$$

The user may adjust SF for values between 10.00 and 3 by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K\frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF} by ±25% using the potentiometer. Considerable reduction in bias currents, noise and drift can be achieved by decreasing SF. This has the overall effect of increasing signal gain without the customary increase in noise and offsets. Note that the peak input signal is always limited to 1.25SF (i.e., ±5V for SF = 4) so the overall transfer function will show a maximum gain of 1.25. The performance with small input signals, however, is improved by using a lower SF since the dynamic range of the inputs is now fully utilized. Bandwidth is unaffected by the use of this option.

Supply voltages of ±15V are generally assumed. However, satisfactory operation is possible down to ±8V (see curve 1). Since all inputs maintain a constant peak input capability of ±1.25SF some feedback attenuation will be necessary to achieve output voltage swings in excess of ±12V when using higher supply voltages.

OPERATION AS A MULTIPLIER

Figure 2 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

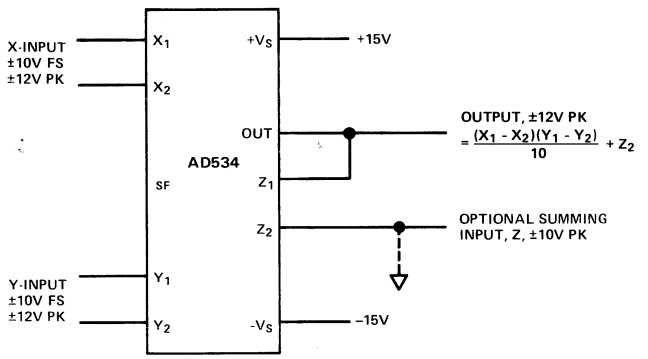


Figure 2. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage of about ±30mV to the X or Y input (see Optional Trimming Configuration, previous page). Curve 4 shows the typical ac feedthrough with this adjustment mode. Note that the Y input is a factor of 10 lower than the X input and should be used in applications where null suppression is critical.

The high impedance Z_2 terminal of the AD534 may be used to sum a further signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1MHz small signal bandwidth and a 20V/μs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective ground potentials to realize the full accuracy of the AD534.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 3. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80kHz without the peaking capacitor C_F = 200pF. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications. Adjustment is made by connecting a 4.7MΩ resistor between Z_1 and the slider of a pot connected across the supplies to provide ±300mV of range at the output.

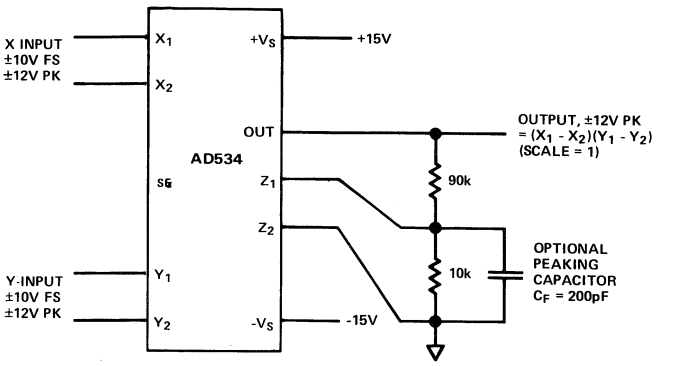


Figure 3. Connections for Scale-Factor of Unity

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the high impedance Z_2 terminal where they are amplified by +10 or to the common ground connection where they are amplified by +1. Input signals may also be applied to the lower end of the 10kΩ resistor, giving a gain of -9. Other values of feedback ratio, up to X100, can be used to combine multiplication with gain.

Occasionally it may be desirable to convert the output to a current, into a load of unspecified impedance or dc level. For example, the function of multiplication is sometimes followed by integration; if the output is in the form of a current, a simple capacitor will provide the integration function. Figure 4 shows how this can be achieved. This method can also be applied in squaring, dividing and square rooting modes by appropriate choice of terminals. This technique is used in the voltage-controlled low-pass filter and the differential-input voltage-to-frequency converter shown in the Applications Section.

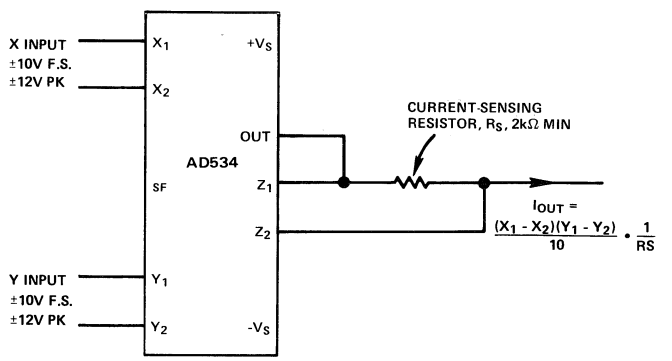


Figure 4. Conversion of Output to Current

OPERATION AS A SQUARER

Operation as a squarer is achieved in the same fashion as the multiplier except that the X and Y inputs are used in parallel. The differential inputs can be used to determine the output polarity (positive for $X_1 = Y_1$ and $X_2 = Y_2$, negative if either one of the inputs is reversed). Accuracy in the squaring mode is typically a factor of 2 better than in the multiplying mode, the largest errors occurring with small values of output for input below 1V.

If the application depends on accurate operation for inputs that are always less than ±3V, the use of a reduced value of SF is recommended as described in the FUNCTIONAL DESCRIPTION section (previous page). Alternatively, a feedback attenuator may be used to raise the output level. This is put to use in the difference-of-squares application to compensate for the factor of 2 loss involved in generating the sum term (see Figure 10).

The difference-of-squares function is also used as the basis for a novel rms-to-dc converter shown in Figure 14. The averaging filter is a true integrator and the loop seeks to zero its input. For this to occur, $(V_{IN})^2 - (V_{OUT})^2 = 0$ (for signals whose period is well above the averaging time-constant). Hence V_{OUT} is forced to equal the rms value of V_{IN}. The absolute accuracy of this technique is very high; at medium frequencies, and for signals near full scale, it is determined almost entirely by the ratio of the resistors in the inverting amplifier. The multiplier scaling voltage affects only open loop gain. The data shown is typical of performance that can be achieved with an AD534K, but even using an AD534J, this technique can readily provide better than 1% accuracy over a wide frequency range, even for crest-factors in excess of 10.

OPERATION AS A DIVIDER

Figure 5 shows the connection required for division. Unlike earlier products, the AD534 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in curve 8.

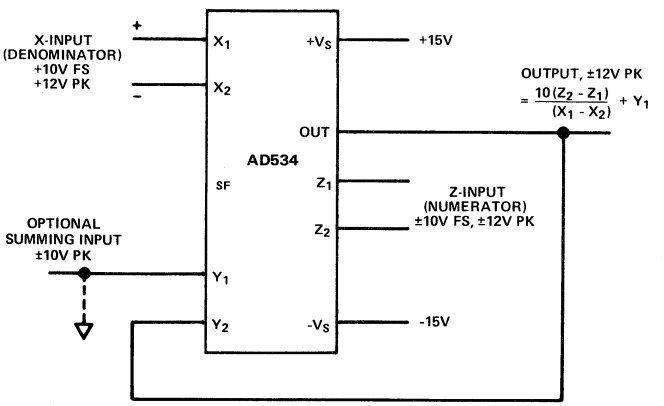


Figure 5. Basic Divider Connection

Without additional trimming the accuracy of the AD534K and L is sufficient to maintain a 1% error over a 10V to 1V denominator range. This range may be extended to 100:1 by simply reducing the X-offset with an externally generated trim voltage of ±3.5mV max applied to the unused X-input (see Optional Trimming Configuration). To trim, apply a ramp of +100mV to +1V at 100Hz to both X_1 and Z_1 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.

Since the output will be near +10V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100.

As with the multiplier connection, overall gain can be introduced by inserting a simple attenuator between the output and Y_2 terminal. This option, and the differential-ratio capability of the AD534 are utilized in the percentage-computer application shown in Figure 11. This configuration generates an output proportional to the percentage deviation of one variable (A) with respect to a reference variable (B), with a scale of one volt per percent.

OPERATION AS A SQUARE ROOTER

The operation of the AD534 in the square root mode is shown in Figure 6. The diode prevents a latching condition which could occur if the input momentarily changed polarity. As shown, the output is always positive; it may be changed to a negative output by reversing the diode direction and interchanging the X-inputs. Since the signal input is differential, all combinations of input and output polarities can be realized, but operation is restricted to the one quadrant associated with each combination of inputs.

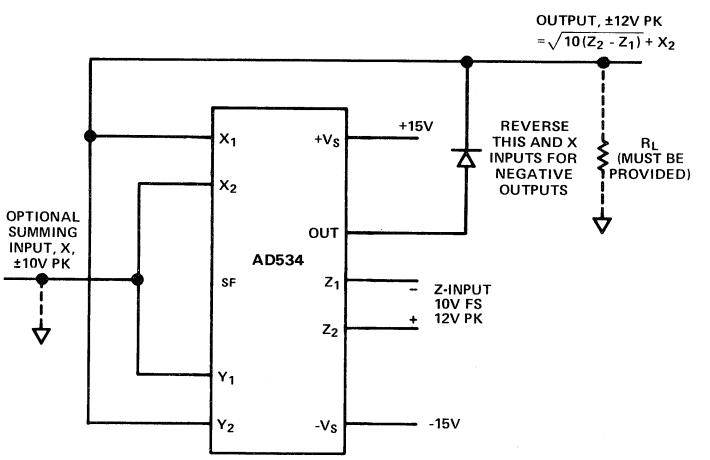
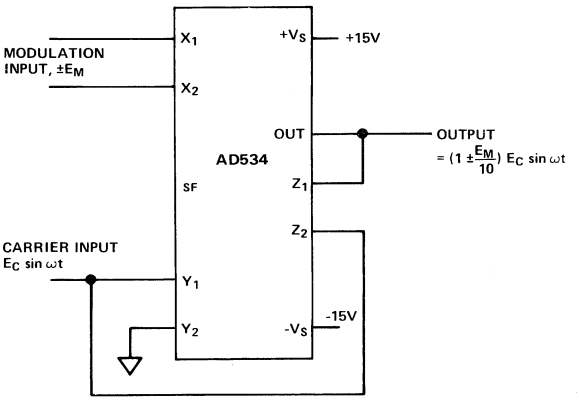


Figure 6. Square-Rooter Connection

In contrast to earlier devices, which were intolerant of capacitive loads in the square root modes, the AD534 is stable with all loads up to at least 1000pF. For critical applications, a small adjustment to the Z-input offset (see Optional Trimming Configuration) will improve accuracy for inputs below 1V.



THE SF PIN OR A Z-ATTENUATOR CAN BE USED TO PROVIDE OVERALL SIGNAL AMPLIFICATION. OPERATION FROM A SINGLE SUPPLY IS POSSIBLE; BIAS Y_2 TO $V_S/2$.

Figure 7. Linear AM Modulator

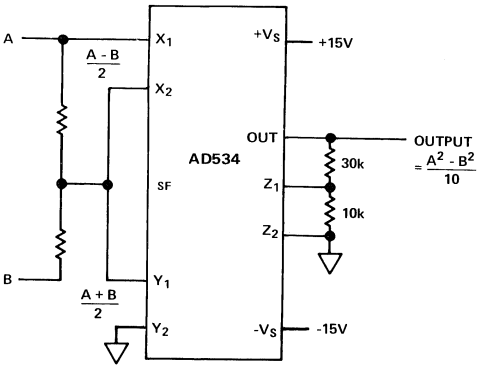
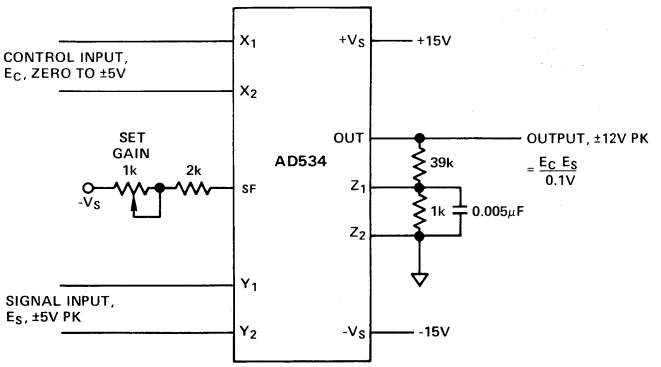
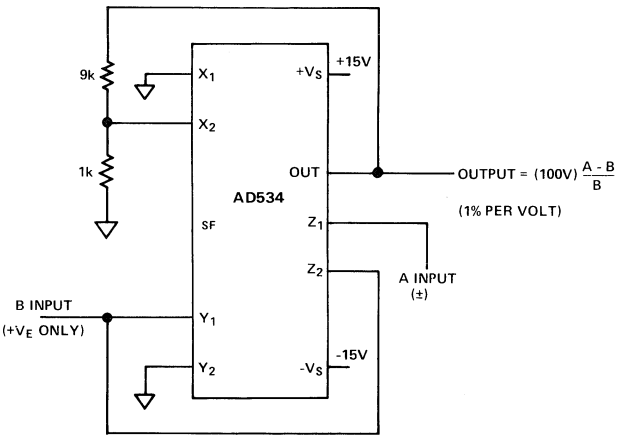


Figure 10. Difference-of-Squares



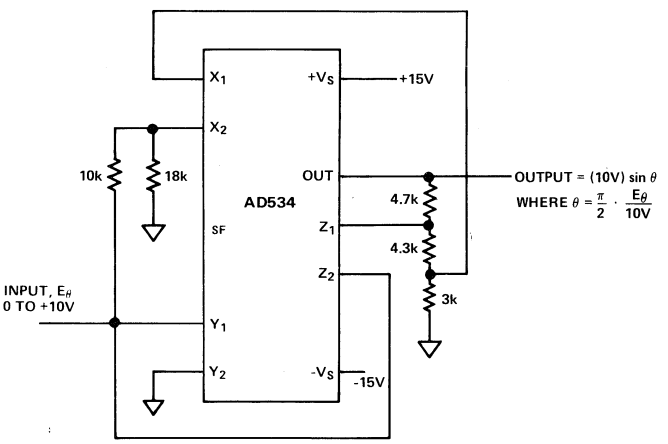
NOTES:
1) GAIN IS X10 PER VOLT OF E_C, ZERO TO X50
2) WIDEBAND (10Hz – 30kHz) OUTPUT NOISE IS 3mV RMS, TYP CORRESPONDING TO A F.S. S/N RATIO OF 70dB
3) NOISE REFERRED TO SIGNAL INPUT, WITH E_C = ±5V, IS 60μV RMS, TYP
4) BANDWIDTH IS DC TO 20kHz, -3dB, INDEPENDENT OF GAIN

Figure 8. Voltage-Controlled Amplifier



OTHER SCALES, FROM 10% PER VOLT TO 0.1% PER VOLT CAN BE OBTAINED BY ALTERING THE FEEDBACK RATIO.

Figure 11. Percentage Computer



USING CLOSE TOLERANCE RESISTORS AND AD534L, ACCURACY OF FIT IS WITHIN ±0.5% AT ALL POINTS. θ IS IN RADIANS.

Figure 9. Sine-Function Generator

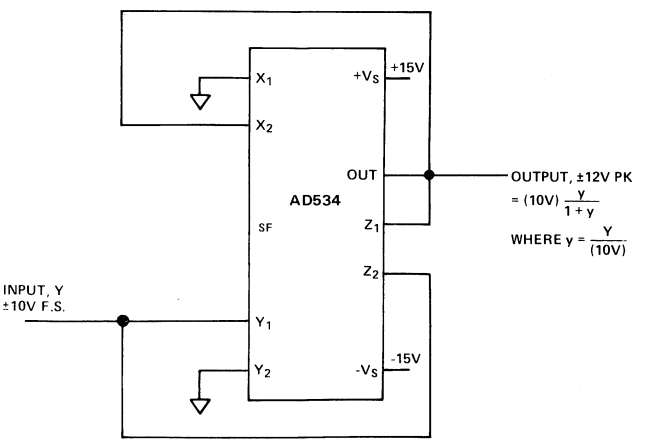
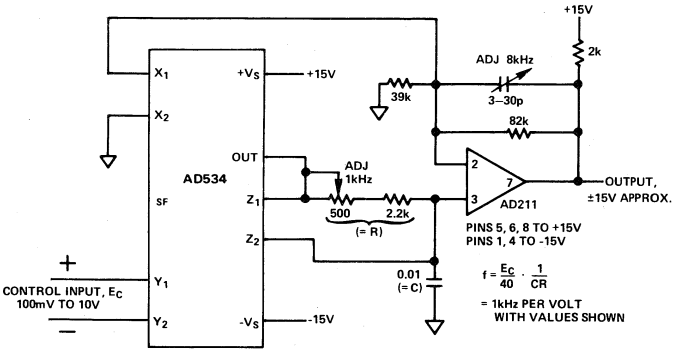


Figure 12. Bridge-Linearization Function



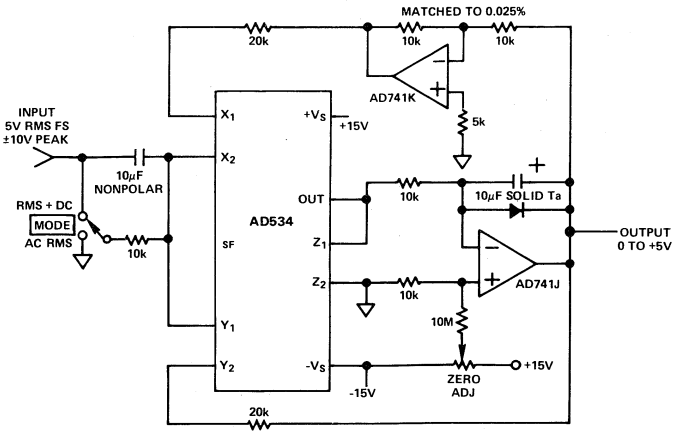
CALIBRATION PROCEDURE:

WITH E_C = 1.0V, ADJUST POT TO SET f = 1.000kHz. WITH E_C = 8.0V, ADJUST TRIMMER CAPACITOR TO SET f = 8.000kHz. LINEARITY WILL TYPICALLY BE WITHIN ±0.1% OF F.S. FOR ANY OTHER INPUT.

DUE TO DELAYS IN THE COMPARATOR, THIS TECHNIQUE IS NOT SUITABLE FOR MAXIMUM FREQUENCIES ABOVE 10kHz, BUT SCALING TO OTHER F.S. VALUES IS STRAIGHTFORWARD.

A TRIANGLE-WAVE OF ±5V PK APPEARS ACROSS THE 0.01μF CAPACITOR; IF USED AS AN OUTPUT A VOLTAGE-FOLLOWER SHOULD BE INTERPOSED.

Figure 13. Differential-Input Voltage-to-Frequency Converter



CALIBRATION PROCEDURE:

WITH 'MODE' SWITCH IN 'RMS + DC' POSITION, APPLY AN INPUT OF +1.00VDC. ADJUST ZERO UNTIL OUTPUT READS SAME AS INPUT. CHECK FOR INPUTS OF ±10V; OUTPUT SHOULD BE WITHIN ±0.05% (5mV).

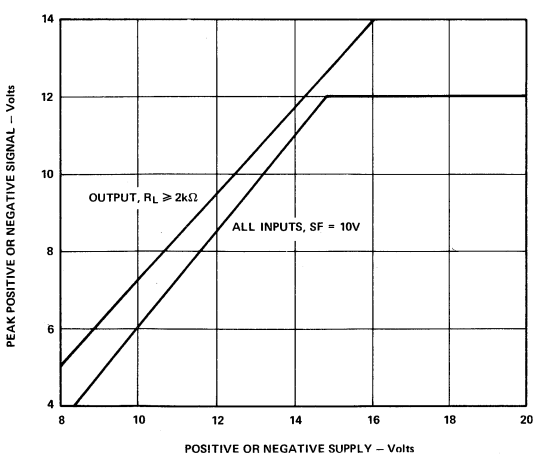
ACCURACY IS MAINTAINED UP TO 100kHz, AND IS TYPICALLY HIGH BY 0.5% AT 1MHz FOR V_{IN} = 4V RMS (SINE, SQUARE OR TRIANGULAR WAVE).

PROVIDED THAT THE PEAK INPUT IS NOT EXCEEDED, CREST-FACTORS UP TO AT LEAST TEN HAVE NO APPRECIABLE EFFECT ON ACCURACY.

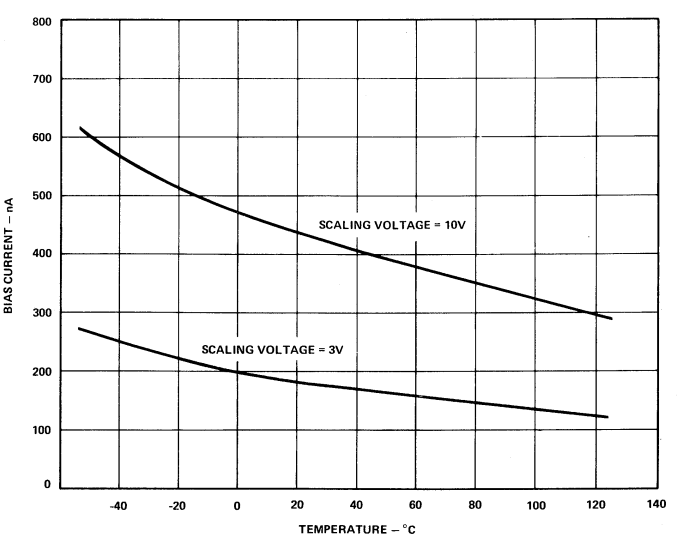
INPUT IMPEDANCE IS ABOUT 10kΩ; FOR HIGH (10MΩ) IMPEDANCE, REMOVE MODE SWITCH AND INPUT COUPLING COMPONENTS.

Figure 14. Wideband, High-Crest Factor rms-to-dc Converter

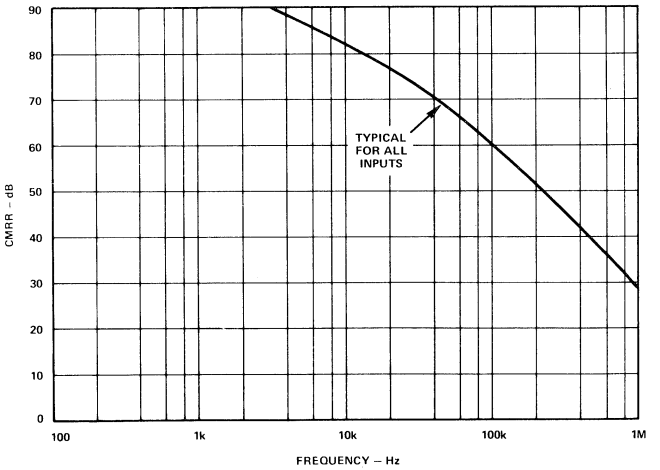
Typical Performance Curves (typical at +25°C, with $\pm V_S$ = +15V, unless otherwise stated)



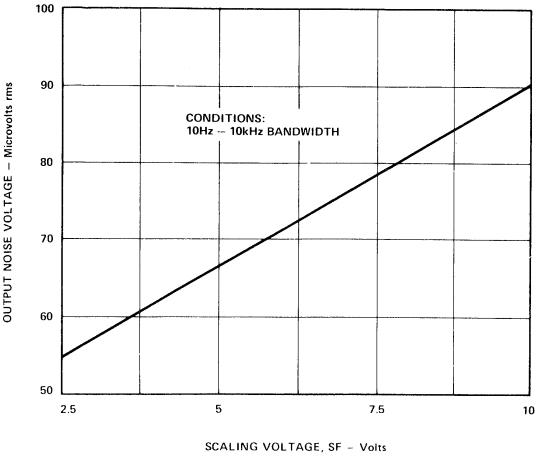
Curve 1. Input/Output Signal Range Vs. Supply Voltages



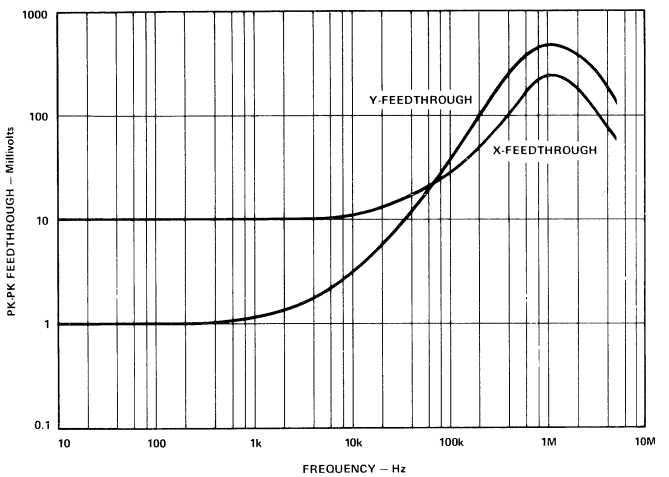
Curve 2. Bias Currents Vs. Temperature (X, Y or Z inputs)



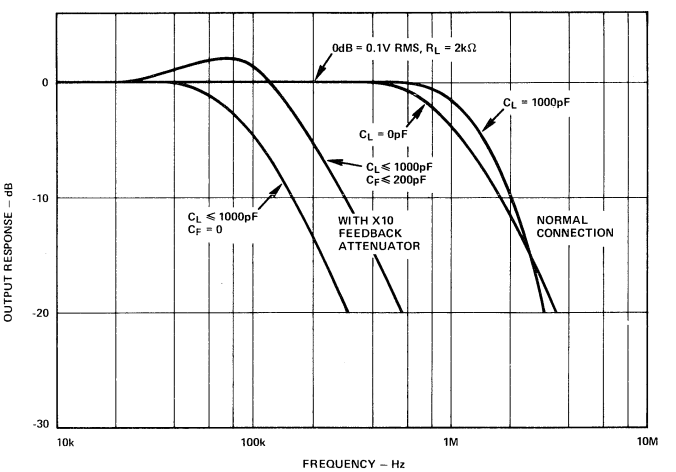
Curve 3. Common-Mode-Rejection-Ratio Vs. Frequency



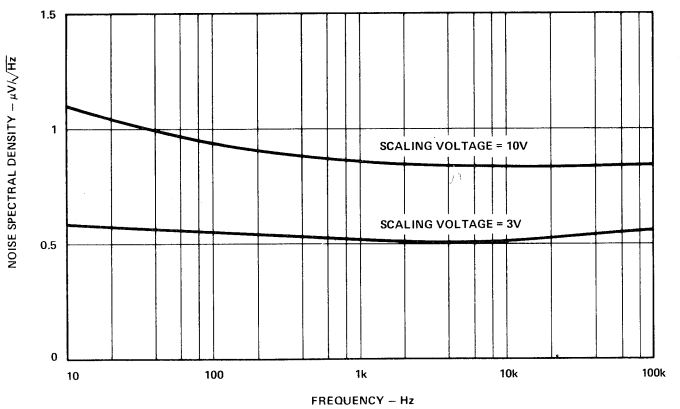
Curve 6. Wideband Noise Vs. Scaling Voltage



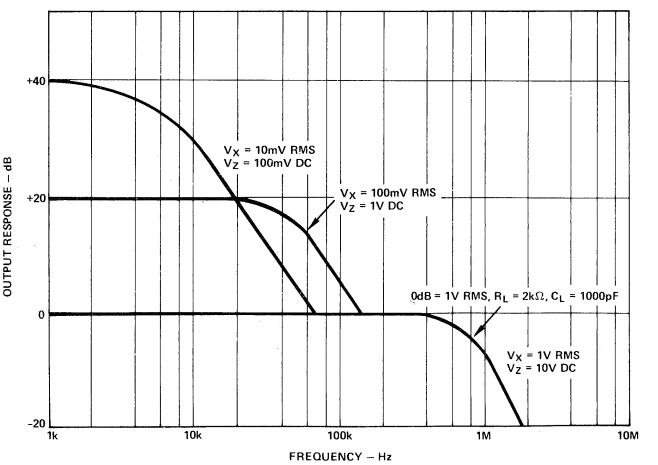
Curve 4. AC Feedthrough Vs. Frequency



Curve 7. Frequency Response as a Multiplier



Curve 5. Noise Spectral Density Vs. Frequency



Curve 8. Frequency Response as a Divider

Accurate, Wideband, Multiplier, Divider, Square Rooter

MODEL 429

FEATURES:
- 1.0%/0.5% Accuracy without Trimming (429A/B)
- Low Drift to 1.0mV/°C max
- Wideband – 10MHz
- 0.2% Nonlinearity max (429B)
- External Amplifiers not Required

APPLICATIONS:
- Fast Divider
- Modulation and Demodulation
- Phase Detection
- Instrumentation Calculations
- Analog Computer Functions
- Adaptive Process Control
- Trigonometric Computations

GENERAL DESCRIPTION

The model 429, an extremely fast multiplier/divider, should be considered if bandwidth, temperature coefficient, or accuracy are critical parameters. Based on the transconductance principle to achieve high speed, the model 429 offers a unique combination of features, those being ½% max error (429B) and 10MHz small signal bandwidth.

Both models 429A and 429B are internally trimmed achieving max errors of 1.0% and 0.5% respectively. By fine trimming the offset and feedthrough with external trim potentiometers typical performance may be improved to 0.5% for the 429A and 0.2% for the 429B.

In addition to high accuracy and high bandwidth, the model 429 offers exceptionally good stability for changes in ambient temperature. Model 429B is 100% temperature tested in order to guarantee an overall accuracy temperature coefficient of only 0.04%/°C max. Additionally, offset drift is held to only 1mV/°C max. To satisfy OEM requirements of low cost, the 429 uses transconductance principles with the latest design techniques and components to achieve guaranteed performance at competitive prices.

MULTIPLICATION ACCURACY

Multiplication accuracy is generally specified as a percentage of full scale output. This implies that error is independent of signal level. However, for signal levels less than 2/3 of full scale, error tends to decrease roughly in proportion to the input signal. A good approximation of error behavior is:

$f(X, Y) \cong |X| \epsilon_x + |Y| \epsilon_y$, where ϵ_x and ϵ_y are the fractional nonlinearities specified for the X and Y inputs

EXAMPLE: For Model 429A, $\epsilon_x = 0.5\%$, $\epsilon_y = 0.3\%$. What maximum error can one expect for x = 5V, y = 1V, providing the offset is zeroed out? Can one get less by interchanging inputs?

1. Nominal output is XY/10 = (5)(1)/10 = 500mV
2. Expected error is (5) (0.5%) + (1) (0.3%) = 28mV, 5.6% of output (0.28% of F.S.)
3. Interchanging inputs (1) (0.5%) + (5) (0.3%) = 20mV, 4.0% of output (0.20% of F.S.)

Compare this with the overly conservative error predicted by the overall 1% of full scale specification: 100mV, or 20% of output.

FREQUENCY RELATED SPECIFICATIONS

Accuracy, and its components, feedthrough, linearity, gain, (and phase shift) are frequency dependent. Feedthrough is constant up to 100kHz for the Y input, and up to 400kHz for the X input. Beyond these frequencies it rises at approximately a 6dB/octave rate due to distributed capacitive coupling. A plot of typical feedthrough vs. frequency is shown in Figure 1. For this measurement one input is driven with a 20V p-p sine wave while the other input is grounded and the feedthrough is measured at the output. This error will decrease roughly in proportion to the input signal, and will also vary with temperature (about 0.01%/°C of the nonzero input). Low frequency feedthrough error can be further reduced from the internally trimmed limits by the use of optional external potentiometers.

Non-linearity likewise increases with frequency at a 6dB/octave rate above the break frequency. With the Y input driven

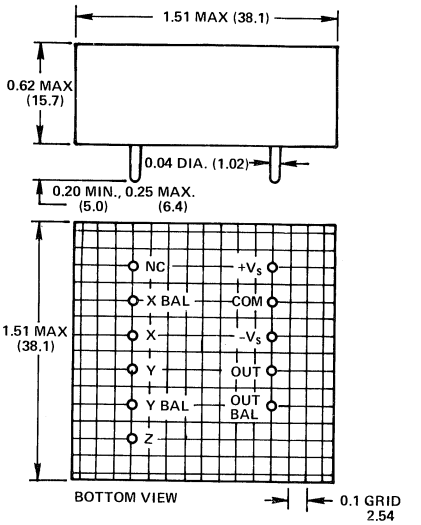
SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	429A	429B
MULTIPLICATION CHARACTERISTICS		
Output Function	XY/10	*
Error, with Internal Trim, at +25°C	±1% max	±0.5% max
Error, with External Trim, at +25°C	±0.7%	±0.3%
Avg vs. Temp (-25°C to +85°C)	±0.05%/°C	±0.04%/°C max
Avg vs. Supply	±0.05%/%	*
SCALE FACTOR		
Initial Error at +25°C	0.5%	0.25%
Avg vs. Temp (-25°C to +85°C)	0.03%/°C	0.02%/°C
Avg vs. Supply	0.03%/%	*
OUTPUT OFFSET		
Initial at +25°C (Adjustable to Zero)	±20mV max	±10mV max
Avg vs. Temp (-25°C to +85°C)	±2mV/°C	±1mV/°C max
Avg vs. Supply	±1mV/%	*
NONLINEARITY		
X Input (X = 20V p-p 50Hz, Y = ±10V)	0.5% max	0.2% max
Y Input (Y = 20V p-p 50Hz, X = ±10V)	0.3% max	0.2% max
FEEDTHROUGH		
X = 0, Y = 20V p-p, 50Hz	50mV p-p, max	20mV p-p, max
With External Trim	16mV p-p	10mV p-p
Y = 0, X = 20V p-p, 50Hz	100mV p-p, max	30mV p-p, max
With External Trim	50mV p-p	20mV p-p
BANDWIDTH		
-3dB	10MHz	*
Full Power Response	2MHz min	*
Slew Rate	120V/μs min	*
1% Amplitude Error	300kHz min	*
1% Vector Error (0.57°)	50kHz min	*
Differential Phase Shift ($\theta_x - \theta_y$)	1° @ 1MHz	*
Small Signal Rise Time 10-90%	40ns	*
Settling to ±1% (±10V step)	500ns	*
Overload Recovery	0.2μs	*
OUTPUT NOISE		
5Hz to 10kHz	0.6mV rms	*
5Hz to 10MHz	3.0mV rms	*
OUTPUT CHARACTERISTICS		
Voltage, 1kΩ load	±11V min	*
Current	±11mA min	*
Load Capacitance	0.01μF max	*
INPUT RESISTANCE		
X Input	10kΩ±5%	*
Y Input	11kΩ±2%	*
Z Input	27kΩ±10%	*
INPUT BIAS CURRENT		
Input X, Y, Z	±100nA	*
Z	±20μA	*
MAXIMUM INPUT VOLTAGE		
For Rated Accuracy	±10.5V	*
Maximum Safe	±16V	*
WARM UP		
To Rated Specifications	1 second	*
POWER SUPPLY[1]		
Rated Performance	±(14.8 to 15.3)V dc	*
Operating	±(14 to 16)V dc	*
Quiescent Current	±12mA	*
TEMPERATURE RANGE		
Rated Performance	-25°C to +85°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Weight	2 oz.	*
Socket	AC1023	*
Case Dimensions	1.5" x 1.5" x 0.62"	*

*Specifications same as Model 429A.
[1] Recommend Model 904 available from Analog Devices
Specifications subject to change without notice.

OUTLINE DIMENSIONS

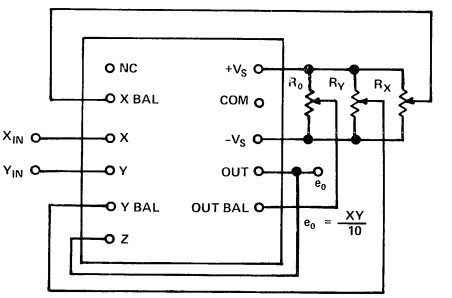
Dimensions shown in inches and (mm).



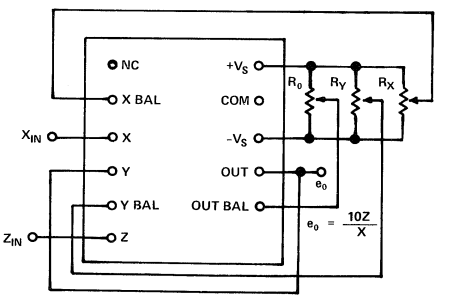
PIN CONNECTIONS

Bottom View Shown in all Cases.
Optional Trim Pots
Shown are not Required
for Rated Accuracy.

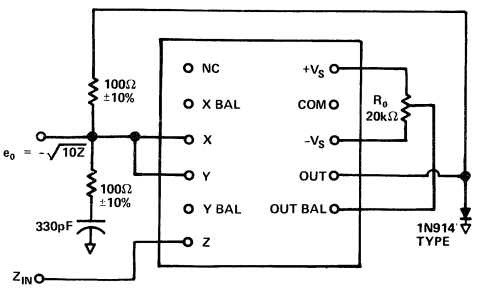
MULTIPLY MODE



DIVIDE MODE



SQUARE ROOT MODE



All trim pots 20kΩ; PN79PR20k

at 10V p-p, and the X input anywhere between ±10V dc, the break frequency is 25kHz. For corresponding X input conditions, the break occurs at 60kHz. Figure 2 is a plot of the typical nonlinearity vs. frequency for the model 429..

Gain and input to output phase shift for the model 429 are shown in Figure 2. Naturally, no multiplier will maintain accuracy at frequencies approaching the small signal bandwidth. For the model 429, the 1% amplitude error will occur at 500kHz. If input to output phase shift is a criterion, then the 1% "vector" error occurs at 50kHz.

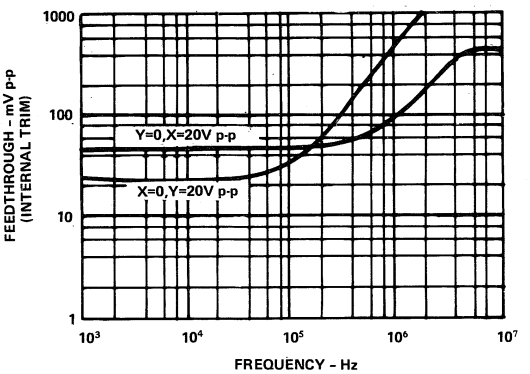


Figure 1. Feedthrough vs Frequency

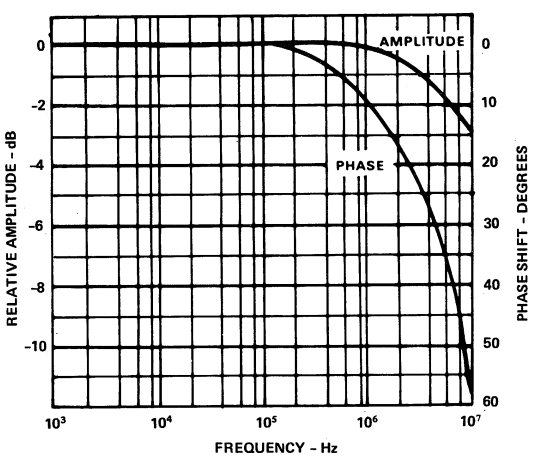


Figure 2. Typical Amplitude and Phase vs Frequency

OPTIONAL TRIM — MULTIPLY MODE

As shipped, the multiplier meets its listed specifications without use of any external trim potentiometers. Terminals are provided for optional feedthrough and offset adjustments. Using these adjustments overall static multiplication error may be reduced to only 0.2%. The 20kΩ trim potentiometers should be connected across the ± supply voltage terminals with the arm of each potentiometer connected to the desired balance terminal (see previous page).

ADJUSTMENT PROCEDURE FOR OFFSET

1. Jumper X input and Y input to ground.
2. Adjust R_0 for an output of zero volts.
3. Remove jumper from X and Y inputs.

ADJUSTMENT PROCEDURE FOR FEEDTHROUGH

1. Jumper Y input to ground and apply 20 VPP at 1kHz to X input.
2. Adjust R_Y for minimum output voltage.
3. Remove jumper from Y input.
4. Jumper X input to ground and apply 20 VPP at 1kHz to Y input.
5. Adjust R_X for minimum output voltage.
6. Remove jumper from X terminal.

DIVISION

The high bandwidth and excellent linearity of model 429 allows it to be used in divider applications achieving high performance in the dc to 8MHz region. Restrictions imposed on divide operation, and the contribution of error terms are illustrated in the error analysis below.

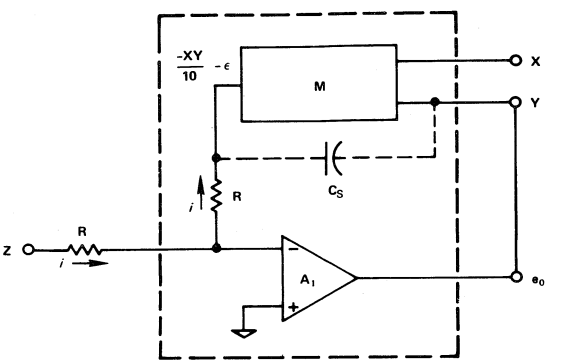


Figure 3. Divider Circuit

Shown in Figure 3 is a typical multiplier/divider which has been connected for divide operation by inserting the multiplier cell, M, in the op amp's feedback loop. Errors associated with the op amp, A_1, are incorporated in ϵ, which represents all errors. In order to insure negative feedback, the X input range is restricted to negative values.

Summing currents at the op amp's summing junction:

$$\frac{Z}{R} = \frac{\frac{XY}{10} + \epsilon}{R}$$

Solving for Y, which is also ϵ_0:

$$Y = \frac{10\,(Z - \epsilon)}{X}$$

or,

$$\epsilon_0 = \frac{10Z}{X} - \frac{10\epsilon}{X}$$

And now breaking ϵ into its constituents

$$\epsilon_0 = \underbrace{\frac{10Z}{X}}_{\text{ideal divider}} - \underbrace{\frac{10E_{NV}}{X}}_{\text{noise error}} - \underbrace{\frac{10E_{OS}}{X}}_{\text{offset error}} - \underbrace{\frac{10E_{OS}/^{\circ}C}{X}}_{\text{offset drift error}} - \underbrace{\frac{10E_{NLX}}{X}}_{\text{X nonlinearity error}} - \underbrace{\frac{10E_{NLY}}{X}}_{\text{Y nonlinearity error}}$$

These errors can be broken down into two categories, static errors and signal dependent errors. All of the static errors associated with the divide mode are inversely proportional to the denominator signal level. The signal dependent errors are the X and Y nonlinearities. For model 429B nonlinearity errors are 0.2% for both the X and Y inputs. Substituting these values in the error terms yields:

$$-\frac{10\,(0.2\%)\,X}{X} - \frac{10\,(0.2\%)\,Y}{X}$$

The importance of using the terminal with largest nonlinearity for the denominator is revealed by the above expression. Effects of X nonlinearity are virtually independent of signal level and may be trimmed out. Nonlinearities of Y typically contribute 200mV for X = Z = 1V i.e., (10 [0.2%] 10V) = 200mV. This error can be reduced if external trims are used to optimize divider performance.

Bandwidth is also degraded with a decrease in denominator level, due to the increase in system gain;

i.e.) for X = Z = 1V, ϵ_0 = 10V

$$\text{and} \quad \frac{\epsilon_0}{Z} = \frac{10}{1} = 10$$

Since the gain bandwidth product is constant, a bandwidth of 1/10 of that obtained for full scale denominator levels will be obtained for division at 1V levels.

For other denominator levels, bandwidth is determined by:

$$\text{B. W.} = \frac{\text{Denominator Level}}{\text{Full Scale Denominator}} \text{ x (Multiplier B.W.) x K}$$

where K is a constant having a value less than unity. It is introduced due to a combination of stray capacitance paralleling the multiplier cell and effects of feedthrough. For model 429

$$\text{B.W.} = \left(\frac{X}{10}\right) 8\text{MHz}$$

Before selecting a multiplier/divider for divide applications, errors resulting from the lowest anticipated denominator signal should be considered. After such considerations have been made, one can further appreciate the importance of starting with an accurate, high speed multiplier such as model 429. It is also highly recommended that the optional trim procedure for division be performed.

OPTIONAL TRIMMING – DIVIDE MODE

Connections are made as shown previously.

The suggested trim procedure is (starting with centered adjust adjustments):

*1. With Z = 0, trim R_0 to hold output constant, as X is varied from -10V toward -1.0V.
2. With Z = 0, trim R_Y for zero at X = -10V.
3. With Z = X and/or Z = -X, trim R_X for minimum worst-case variation as X is varied from -10V to -1.0V.
4. Repeat 1 and 2 if step 3 required large initial adjustment.

*For best accuracy X should be allowed to vary from -10V to lowest expected denominator.

SQUARE ROOTING

When connected as shown previously, the model 429 will provide the square root of Z_{IN}.

By summing currents at the op amp's summing junction:

$$\frac{Z}{R} = \frac{XY}{10R} + \frac{\epsilon}{R} = \frac{Y^2}{10R} + \frac{\epsilon}{R}$$

where ϵ represents all errors associated with the multiplier. Solving for the output voltage, Y.

$$\epsilon_0 = \pm \sqrt{10\,(Z - \epsilon)}$$

There are two values of ϵ_0 for every value of Z. However, only negative values of ϵ_0 will provide the negative feedback necessary for circuit stability. To restrict the output from going positive, a diode is connected as shown previously. The output is then:

$$\epsilon_0 = -\sqrt{10\,(Z - \epsilon)}$$

Errors, ϵ, associated with the multiplier, are inside the square root and consequently their effect, for large values of Z, is reduced. The reason for the improved performance can be seen by inspecting the circuit. The output is fed back to both the X and Z terminals, resulting in twice the feedback as would be obtained for the divide mode. An alternative method of considering error performance is to consider errors as being at the Z terminal. By differentiating the ideal transfer function with respect to Z, errors for various values of Z may be determined:

$$\frac{de_0}{dZ} = \frac{d}{dZ}\sqrt{10Z} = \tfrac{1}{2}\sqrt{\frac{10}{Z}}$$

The factor of ½ has the advantage of reducing errors by a factor of 2 for Z = 10, but also introduces the potential problem of instability. Since the feedback gain is the reciprocal of the forward gain, the slope of the forward gain is 2. Additional phase margin is required to support the increased gain in the feedback path. Model 429 is optimized for phase margin in the multiply and divide modes producing minimum vector errors at high frequencies. To avoid the potential problem of instability, the RC network shown previously is recommended. This network restricts the bandwidth and guarantees stability for all positive values of Z.

OPTIONAL ADJUSTMENT PROCEDURE – SQUARE ROOT

1. Apply a voltage to the Z terminal equal to the lowest anticipated input voltage.
2. Adjust R_0 such that $e_0 = -\sqrt{10Z}$, where Z is the voltage applied in step 1.

DIVISION SPECIFICATIONS (TYPICAL)

OUTPUT FUNCTION	10(Z)/X
Numerator Range	±10V
Denominator Range, 1% Accuracy	-1 to -10V
Denominator Range, 5% Accuracy	-0.2V to -10V
Bandwidth Formula, (Hz, -3dB)	(8MHz)(X)/10

SQUARE ROOTING SPECIFICATIONS (TYPICAL)

OUTPUT FUNCTION	$-\sqrt{10(Z)}$
Dynamic Range	1000 to 1 (+0.010V ≤Z≤+10V)
Accuracy (% of Full Scale)	0.5%
Bandwidth Formula, (Hz, -3dB)	(5MHz) $\sqrt{\lvert X\rvert/10}$

Table 1. Division & Square Rooting Specifications

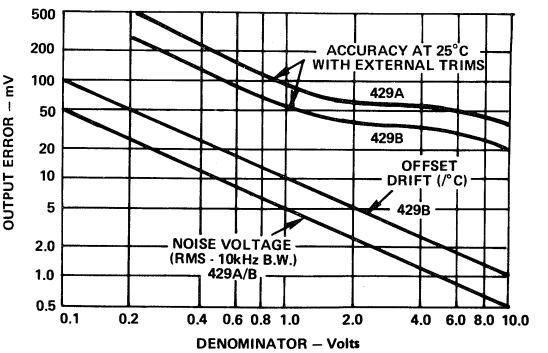


Figure 3. Typical Error Performance of Model 429 in Divide Mode for Worst Case of $|e_0| = 10V$

ANALOG DEVICES

Programmable Multifunction Module

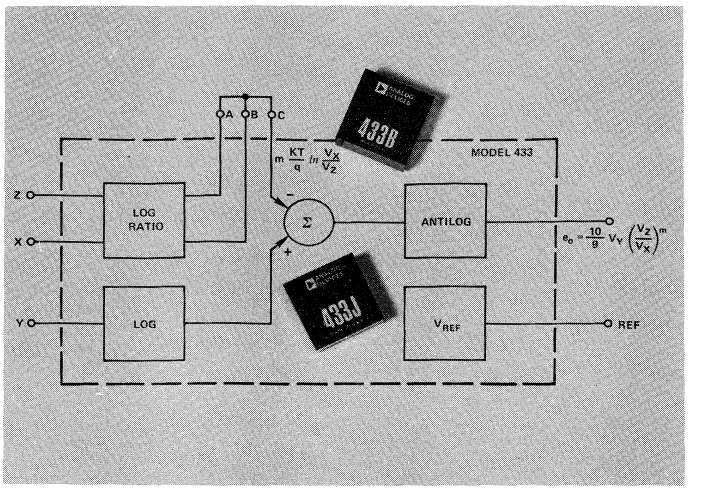
MODEL 433

FEATURES

- **Versatility: Provides Transfer Characteristics of Several Function Modules**
- **Divides Over a 100:1 Range With a Max Error of 0.25% (433B)**
- **Internal Voltage Reference**
- **Hermetically Sealed Semiconductors**
- **No External Trims Required**
- **Low Noise**

APPLICATIONS

- **Transducer Linearization**
- **Signal Processing**
- **Raising to Arbitrary Powers**
- **Vector Functions**
- **Trigonometric Functions (Sine, Cosine, Arctangent)**



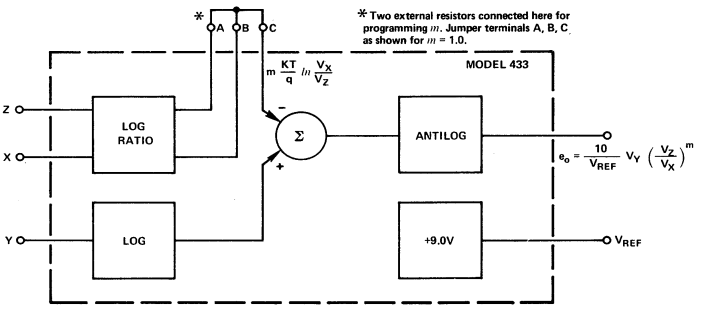


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The model 433 is an extremely versatile function module which implements the transfer function:

$$e_o = \frac{10}{V_{REF}} V_y \left(\frac{V_z}{V_x}\right)^m, \quad 0.2 \leq m \leq 5.0$$

$V_{REF} = +9.0$ Volts

By either jumper connections on the pins, or selection of two external resistors the user can program the 433 to: multiply, divide, square, square root, root of a ratio, square of a ratio, or raise voltage ratios to an arbitrary power, *m*.

When used with a low cost op amp, such as AD741, the model 433 may be used to compute the true rms value of a varying signal. With two such op amps, the 433 can be used to perform accurate vector computations over wide ranges of the vector sum.

Due to its log/antilog circuit approach, signal levels of 100mV to 10V may be processed with a maximum output error of 0.25% F.S. (433B). The allowable input range for the three input variables is 0.01 to +10V, for which there is a typical error of ±5mV ±0.3% of the theoretical output voltage for model 433J, and ±1mV ±0.15% for 433B.

Because of its small size, accuracy, versatility, and speed (and all at low cost), the model 433 will prove to be an essential component in equipment requring on-the-spot computations in real time, or for linearizing a wide range of transducer characteristics in medical, industrial, and process control equipment. Designed with the OEM's needs in mind, the model 433 is attractively priced for new equipment designs.

PRINCIPLE OF OPERATION

The model 433 is comprised of log and antilog circuits interconnected as shown in Figure 1. The log ratio circuit provides the log of V_X/V_Z to terminals A, B, C where, for exponents other than unity, it is scaled by two external programming resistors (see hook-up diagrams for connection and values of these two resistors). The scaled log ratio from terminal C is subtracted from a signal proportional to the log of V_Y. The resulting expression is operated on by the antilog circuit, yielding an output of

$$e_o = \frac{10}{V_{REF}} V_y \left(\frac{V_z}{V_x}\right)^m, \quad V_{REF} = +9.0 \text{ Volts}$$

The voltage reference circuit is a high stability (0.005%/°C) voltage source which is generated internally. It is provided as an output terminal for user convenience, and may be used as a constant at any of the input terminals.

ONE-QUADRANT DIVIDER

When connected as a divider, the model 433B has less than ¼% output error over an input signal range of 100:1. This performance is obtained with no external trims, and is nearly twenty times better than that attainable with a 0.1% multiplier/divider connected in a feedback loop.

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

Model	433J	433B
Transfer Function	$e_o = +\frac{10}{V_{REF}} V_y \left(\frac{V_z}{V_x}\right)^m$	*
Reference Terminal Voltage[1]		
V_{ref} (Internal Source)	+9.0V ±5% @ 1mA	*
vs Temp (−25°C to +85°C)	±0.005%/°C	*
Rated Output[1]	+10.5V @ 5mA, min	*
Input		
Signal Range	$0 \leqslant V_x, V_y, V_z \leqslant +10V$,	*
Max Safe Input	$V_x, V_y, V_z \leqslant \pm 18V$	*
Resistance		
X Terminal	100kΩ ±1%	*
Y Terminal	90kΩ ±10%	*
Z Terminal	100kΩ ±1%	*
External Adjustment of the Exponent, m		
Range for m <1 (Root)	$1/5 \leqslant m < 1$, $m = \frac{R_2}{R_1 + R_2}$	*
Range for m >1 (Power)	$1 \leqslant m < 5$, $m = \frac{R_1 + R_2}{R_2}$	*
	$(R_1 + R_2) \leqslant 200\Omega$	*
Accuracy (Divide Mode, m = 1, $V_y = V_{REF}$)[2,3]		
Total Output Error @ +25°C (for specified input range)		
Typical (RTO)	±5mV ±0.3% of output	±1mV ±0.15% of output
Max Error (RTO)	±50mV	±25mV
Input Range ($V_z \leqslant V_x$)	0.01V to 10V, V_z	*
	0.1V to 10V, V_x	*
Over Specified Temp. Range	±1%	±1% max
Output Offset Voltage (Not Adjustable)		
Initial @ +25°C	±5mV	±2mV max
Offset vs Temp.	±1mV/°C	±1mV/°C max
Noise, 10Hz to 1kHz		
V_x = +10V	100μV rms	*
V_x = +0.1V	500μV rms	*
Bandwidth, V_y, V_z Small Signal (-3dB), 10% of dc Level	V_y or V_z	*
$V_y = V_z = V_x$ = 10V	100kHz	*
$V_y = V_z = V_x$ = 1V	20kHz	*
$V_y = V_z = V_x$ = 0.1V	1kHz	*
$V_y = V_z = V_x$ = 0.01V	400Hz	*
Full Output (V_y or V_z = 5V dc ±5V ac)	(V_x) x (5kHz)	*
Power Supply Range		
Rated Performance	±15V dc @ 10mA	*
Operating	±(12 to 18)V dc	*
Temperature Range		
Rated Performance	0 to +70°C	−25°C to +85°C
Storage	−55°C to +125°C	−55°C to +125°C
Mechanical		
Case Size	1.5" x 1.5" x 0.62"	*
Mating Socket	AC1038	*

*Same specifications as 433J.

[1] Terminals short circuit protected to ground.

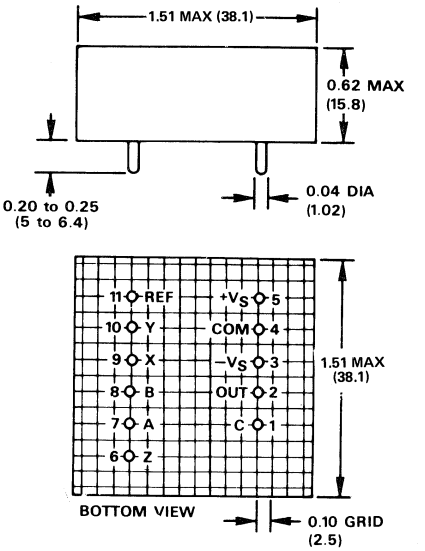
[2] Accuracy is specified in divide mode. Input range is 10mV to 10V for specified accuracy when connected as a multiplier.

[3] Error is defined as the difference between the measured output and the theoretical output for any given pair of specified input voltages.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

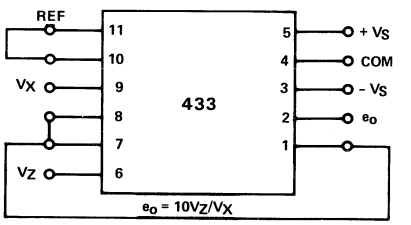


Mating Socket AC1038

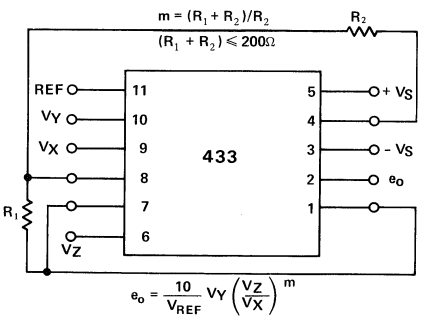
WIRING CONNECTIONS

Bottom View Shown in All Cases

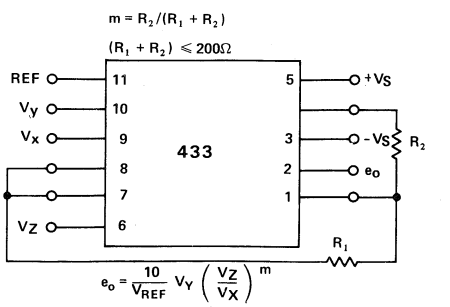
DIVIDE MODE (m = 1, $V_y = V_{REF}$)



POWERS m ⩾ 1



ROOTS m ⩽ 1



MODEL 433B – 0.25% DIVIDER, WIDE DYNAMIC RANGE

Probably the most impressive performance improvement owing to model 433's log/antilog circuit approach, is its ability to hold high divider accuracies over a wide 100:1 input signal range.

When using a conventional multiplier/divider as a divider, accuracy, offset drift, and noise performance are all degraded as the denominator is decreased.

For model 433, accuracy, offset drift, and noise performance are all virtually independent of denominator level as illustrated in Figure 2 and this performance is obtained with no external trims.

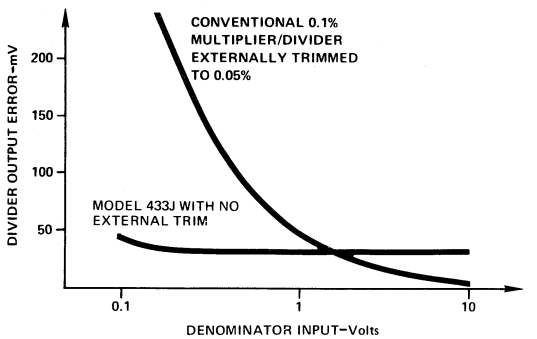


Figure 2. Comparison of Divider Error vs. Denominator Level for Model 433J and a Conventional Mult./Div.

FREQUENCY RESPONSE

A curve of amplitude vs. bandwidth for model 433 is shown in Figure 3. For all input terminals, the small signal frequency response (-3dB point) is signal level dependent, decreasing from 100kHz for a 10V input to 400Hz for a 10mV input. These small signal measurements are made by superimposing a 10% small signal amplitude on the dc level being characterized.

Full output for a ±5 volt signal superimposed on a 5V dc level is 50kHz for the multiplier, and V_X x 5kHz for the divider.

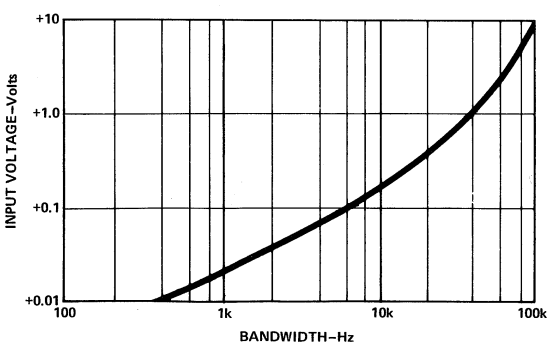


Figure 3. 433 Small Signal Bandwidth vs. Input Voltage

VARYING THE EXPONENT, m

Presented in Figure 4 is a family of curves which illustrates the effect of varying the exponent, m. All curves have been scaled for the full scale output of 10V by reducing the 433's transfer equation to $e_O = 10\ (V_Z/V_X)^m$. For applications where a continuous variation in m is desired, connections should be made as shown in Figure 5C. Model 433 features very small accuracy changes (≈0.1%) as m is adjusted over the entire range from 0.2 to 5.

Various values of m are programmed by two external resistors, R_1 and R_2. For values of $m < 1$ resistor connections are made

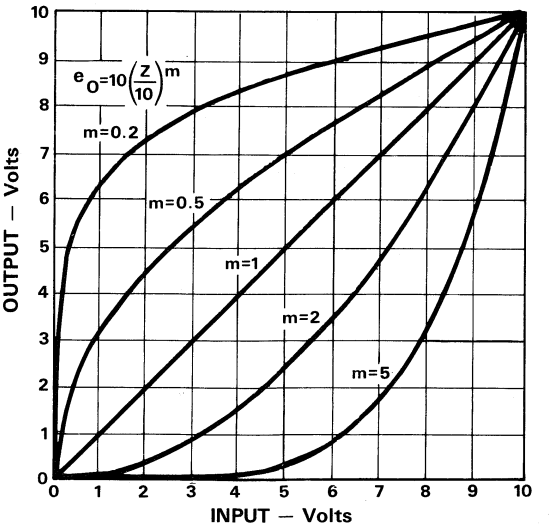


Figure 4. Varying the Exponent, m

to terminals, 1, 7, 8 as shown in Figure 5A. For values of $m > 1$, see Figure 5B. For $m = 1$, connect terminals 1, 7 and 8 together.

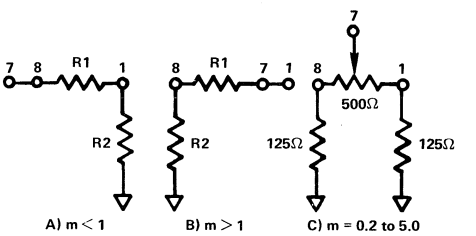


Figure 5. Resistor Programming for the Exponent, m

NOISE PERFORMANCE

The curves shown in Figure 6 are for output noise vs. signal level in a 1kHz BW for worst case conditions. These conditions exist when V_X is equal to V_Z and is varied over the specified range. It should be noted that for 0.1V inputs the effective gain is 100. To retain the full performance capability of model 433, all external noise sources should be isolated from the input terminals.

An exceptional advantage of the 433 over other means of dividing is revealed by these curves. That feature being that noise is virtually independent of signal level. For a 100:1 signal level change of the denominator, the output noise is changed only 3:1. Division by using a multiplier in the feedback loop exhibits a 100:1 increase in output noise for a denominator signal level change of 100:1.

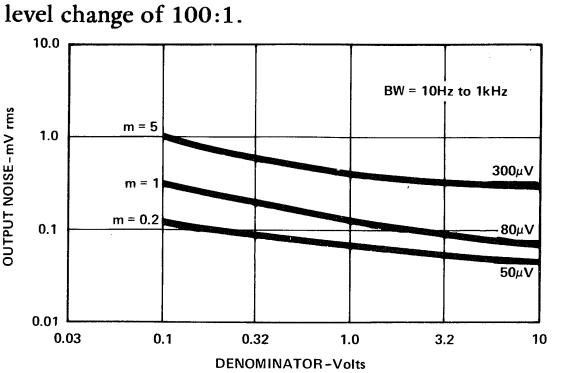


Figure 6. Model 433 Noise vs. Denominator for Various Exponents, m

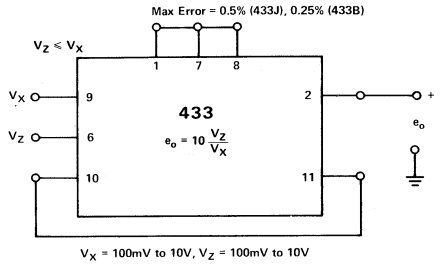


Figure 7. Divider

When connected as a divider as shown above, the 433 has less than ½% error (50mV) for input signals from 100mV to 10V. Output noise, offset drift and accuracy are all virtually independent of signal level and no trims are required.

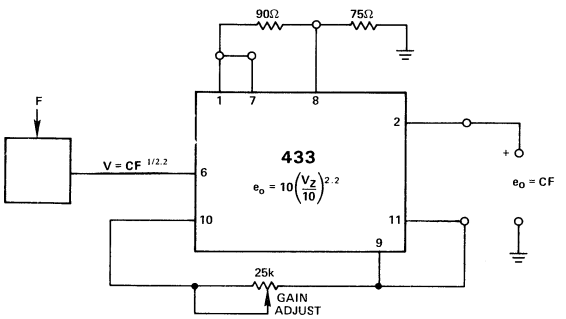


Figure 8. Transducer Linearization

A transducer's output may be linearized by utilizing the 433 as an exponentiator. In the example above, a transducer is used to convert a force, F, to a voltage, V. The desired relationship being V directly proportional to F; i.e., V = CF where C is constant.

The actual output for this example is proportional to F, but is a nonlinear relation which can be approximated by $CF^{1/2.2}$ Connecting the 433 as shown with m = 2.2 provides the desired relation of e_O = CF.

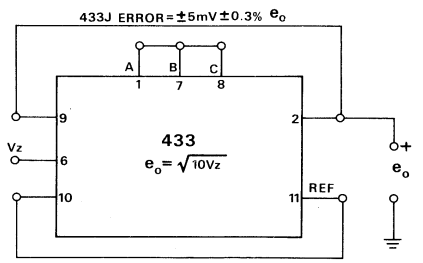


Figure 9. Square Root

The square root of a single variable may be obtained with no external components when connected as shown above. Noise performance is even better than that for the multiply or divide mode.

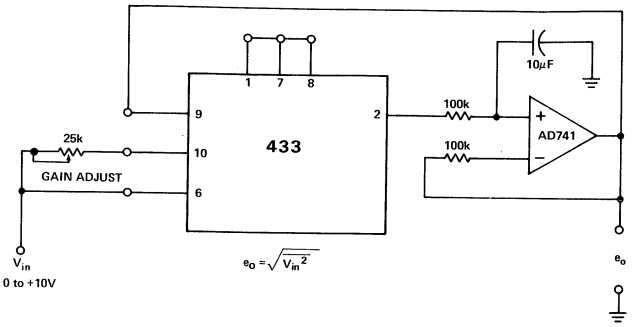
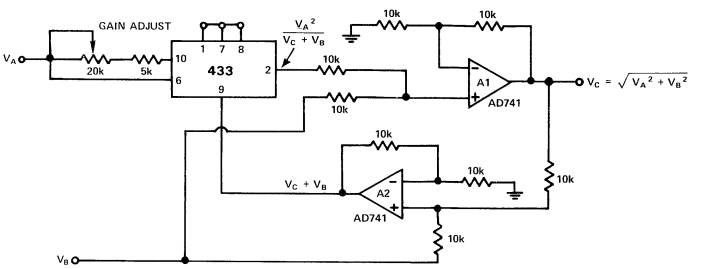


Figure 10. True rms

By combining the 433 with a simple filter, using an external op amp as shown above, the true rms value of a one quadrant input signal may be computed. Accuracy is not degraded by crest factor, provided the maximum input is 10V or less.

The 433 output is applied to an integrator to average the signal and is then fed back to the X input to obtain the square root of the mean square of the input.

Accuracy of 5mV + 0.1% of reading may be achieved over an input range of 500:1.



$$V_C = \sqrt{V_A^2 + V_B^2}$$

$$V_C^2 = V_A^2 + V_B^2$$

$$V_A^2 = V_C^2 - V_B^2$$

$$V_A^2 = (V_C - V_B)(V_C + V_B)$$

$$\frac{V_A^2}{V_C + V_B} = (V_C - V_B)$$

$$V_C = \frac{V_A^2}{V_C + V_B} + V_B$$

Figure 11. Vector Computation $V_C = \sqrt{V_A^2 + V_B^2}$

The vector computation circuit shown in Figure 11 illustrates the extreme versatility of model 433. Used with two inexpensive op amps the 433 is used as a basic building block, which in this case, provides the square root of the sum of the squares.

This application is based on the identity for the difference of squares. The derivation is shown by the equations above and the final equation for V_C is implemented.

Due to the excellent inherent accuracy of the above circuit (error = 0.1% of reading), matched resistors with a low T.C. should be used. Errors of only 0.1% of the theoretical output may be achieved over signal levels of +100mV to +10V.

The usefulness of model 433 extends beyond the illustrative examples shown above. Model 433 may also be used to generate basic trigonometric functions (sine, cosine, arctangent). Further detailed applications information on model 433 is provided in the Nonlinear Circuits Handbook, published by Analog Devices

Versatile, High Accuracy, Analog Divider

MODEL 434

FEATURES
- Optimized One Quadrant Divider
- 100:1 Range with Max Error ¼% (434B)
- Current or Voltage Inputs
- Programmable Gain
- Wide Operating Temperature Range, -25°C to +85°C
- Hermetically Sealed Semiconductor

APPLICATIONS
- Transducer Linearization
- Signal Processing
- Vector Computation
- One-Quadrant Multiplier
- Wide Range, ¼% Square Rooter

GENERAL DESCRIPTION

The model 434 is a one quadrant divider that maintains accuracy to within ¼% (434B) over a 100:1 range of denominators without the use of any external trims. Optional trimming may be used to eliminate all dc offset errors and further improve accuracy and dynamic range. This module is designed to accept either current or voltage inputs and has the following operating transfer functions:

$$e_o = \frac{10}{V_{REF}} V_Y \frac{V_Z}{V_X} \quad \text{or} \quad e_o = \frac{10}{V_{REF}} V_Y \frac{I_Z}{I_X}$$

By appropriate pin interconnections these functions can be simplified to the following: (See REFERENCE VOLTAGE).

$$e_o = 10\frac{V_Z}{V_X} \quad \text{or} \quad e_o = 10\frac{I_Z}{I_X}$$

As seen from the transfer equations, model 434 can be used in simple circuits to synthesize a variety of computational functions and allows overall signal gain to be programmed through the selection of voltage V_Y. In addition, all hermetically sealed semiconductors are used in the manufacture of the model 434 in order to insure reliable performance over a wide range of temperatures (-25°C to +85°C).

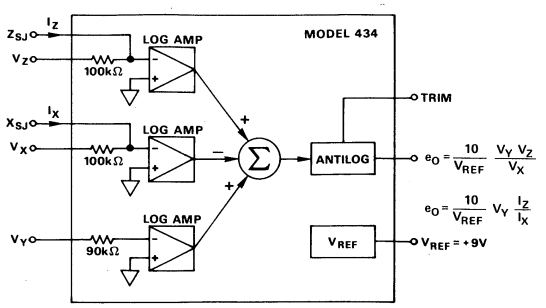


Figure 1. Block Diagram

The combination of small size, accuracy, versatility and reliability make the model 434 an ideal component for use in real time computations (divide, square root, vector sums), and for linearization of transducers in medical, industrial and process control equipment. This level of performance is available at a low cost (434A) that is attractive when considering 434's for new OEM equipment designs.

REFERENCE VOLTAGE

A +9.0 volt reference voltage is provided at an output terminal for user convenience and can be used to facilitate setting signal gain at 10. The reference source has excellent stability (0.005%°C) and may be utilized as a constant at any of the input terminals. When the reference is connected to the scale factor input (V_Y), the transfer functions will be:

$$e_o = 10\frac{V_Z}{V_X} \quad \text{or} \quad e_o = 10\frac{I_Z}{I_X}$$

SCALE FACTOR ADJUSTMENT

One of the many advantages of the model 434 is that the scale factor can be readily adjusted by controlling the voltage on the V_Y terminal. This is most useful when the 434 is used to compute the ratio of V_Z/V_X when $V_Z > V_X$. V_Y, and therefore the overall scale factor (K), can be selected so that computations can be made without saturating the output of the divider. For instance, if V_Z = 10V and V_X = 1V, K can be adjusted to 1V and the ratio of 10V/1V can be computed without saturation since:

$$e_o = (1V) \times 10V/1V = 10V$$

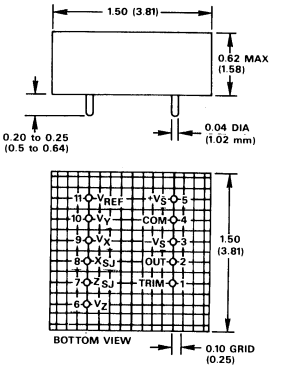
SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	434A	434B
TRANSFER FUNCTION	$e_o = \frac{10}{V_{REF}} V_y \frac{V_z}{V_x}$ $\left(e_o = \frac{10}{V_{REF}} V_y \frac{I_z}{I_x}\right)$	*
REFERENCE TERMINAL (V_{REF})		
Voltage (Internal Source)	+9.0V ±5%	*
vs. Temperature (-25°C to +85°C)	±0.005%/°C	*
Current	1.0mA, max	*
RATED OUTPUT[1]		
Voltage	+10.5V, min	*
Current	+5.0mA, min	*
Impedance	0.1Ω, max	*
INPUT SPECIFICATIONS		
Voltage Signal Range	$0 \leqslant V_x, V_y, V_z \leqslant 10V$	*
Current Signal Range	$0 \leqslant I_x, I_z, \leqslant 100\mu A$	*
Max Safe Voltage (V_x, V_y, V_z)	18V	*
Max Safe Current (I_x, I_z)	1mA	*
Offset Voltage (V_x, V_z)	100μV	*
Offset Voltage (V_y)	5mV	*
vs. Temperature (V_x, V_y, V_z)	±15μV/°C	*
Bias Current (Z_{sj}, X_{sj})	+10nA	*
vs. Temperature (-25°C to +85°C)	-0.1nA/°C	*
NONLINEARITY ($+0.1 \leqslant V_X \leqslant +10V$)	0.1%	*
INPUT IMPEDANCE		
V_x, V_z Terminal	100k ±1%	*
V_y Terminal	90k ±10%	*
OUTPUT SPECIFICATIONS		
Offset Voltage, Initial[2]	±2mV	±2mV, max
vs. Temperature (-25°C to +85°C)	±1mV/°C	±1mV/°C, max
Noise, 10Hz to 1kHz		
$V_z = V_x = +10V$ ($I_z = I_x = 100\mu A$)	100μV, rms	*
$V_z = V_x = +0.1mV$ ($I_z = I_x = 1\mu A$)	300μV, rms	*
FREQUENCY RESPONSE		
Small Signal (-3dB)		
$V_x = V_y = V_z = 10V$	100kHz	*
$V_x = V_y = V_z = 0.1V$	1kHz	*
Full Power Bandwidth		
V_y or V_z = 5V dc ±5V ac	(V_x) (5kHz)	*
ACCURACY (DIVIDE MODE, $V_y = V_{REF}$)[3]		
Total Output Error[4]		
(Over Specified Input Ranges)	±0.5%, max	±0.25%, max
Input Ranges	$0.01 \leqslant V_z \leqslant +10V$	*
($V_z \leqslant V_x$; $I_z \leqslant I_x$; $V_y = V_{ref}$)	$0.1 \leqslant V_x \leqslant +10V$	*
	$0.1 \leqslant I_z \leqslant +100\mu A$	*
	$1 \leqslant I_x \leqslant +100\mu A$	*
Over Temperature Range (-25°C to +85°C)	±1%	±1%, max
ACCURACY (SQUARE ROOT MODE, $V_y = V_{REF}$)		
Total Output Error[4]		
(Over Specified Input Range)	±0.5%, max	±0.25%, max
Input Range	$0.01 \leqslant V_z \leqslant +10V$	*
POWER SUPPLY[5]		
Voltage, Rated Performance	±15V	*
Voltage, Operating	±(12 to 18)V	*
Current, Quiescent	±8mA	*
TEMPERATURE RANGE		
Rated Specifications	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Case Size	1.5" x 1.5" x 0.62"	*
Mating Socket	AC1038	*
Weight	50 gm.	*

[1] Short circuit protected to ground.
[2] With TRIM terminal open. Adjustable to zero with external 20k potentiometer.
[3] Accuracy is specified in divide mode. Input range is 10mV to 10V for specified accuracy when connected as a multiplier.
[4] Error is guaranteed with no external trimming.
[5] Recommended power supply: Analog Devices model 904, ±15V @ 50mA
*Specifications same as model 434A. Specifications subject to change without notice.

OUTLINE DIMENSIONS

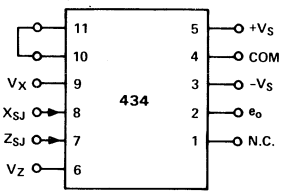
Dimensions shown in inches and (mm).



Mating Socket AC 1038

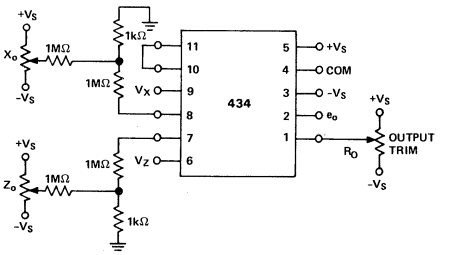
WIRING CONNECTIONS
Bottom View Shown in All Cases

DIVIDE MODE[1]



$e_o = 10 \frac{V_Z}{V_X}$ or $e_o = 10 \frac{I_Z}{I_X}$

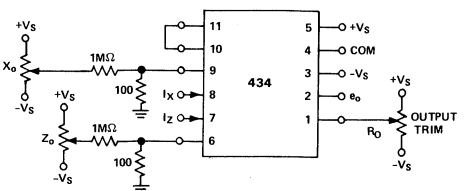
OPTIONAL TRIM, VOLTAGE INPUT[2]



TRIM PROCEDURE

1. Set V_X = +10V; V_Z = 0. Adjust R_O for e_O = 0.
2. Set $V_X = V_Z$ = +10V. Record e_O.
3. Set $V_X = V_Z$ = +0.1V. Adjust X_O for same reading as recorded in step 2.
4. Set V_X = +0.1V, V_Z = +0.01V. Adjust Z_O for +1.00V.

OPTIONAL TRIM, CURRENT INPUT[2]



[1] For current operation apply input currents directly to X_{sj} and Z_{sj} instead of to the V_X and V_Z terminals.
[2] All trim pots 20K, 20 turn. ADI No. 79PR20K

The accuracy of the model 434 is not degraded for scale factors between 1V and 10V.

The voltage level for V_Y can be applied by using a potentiometer connected between V_{REF} and common as shown in Figure 2. An external signal source can be applied to V_Y if it is desired to have a dynamic gain control.

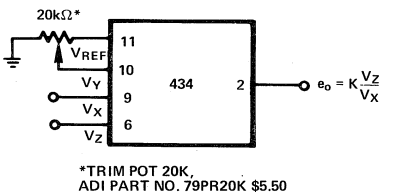


Figure 2. Scale Factor Adjustment Circuit

FREQUENCY RESPONSE

A curve of amplitude vs. bandwidth for model 434 is shown in Figure 3. For all input terminals, the small signal frequency response (-3dB point) is signal level dependent, decreasing from 100kHz for a 10V input to 400Hz for a 10mV input. These small signal measurements are made by superimposing a 10% small signal amplitude on the dc level being characterized.

Full output for a ±5 volt signal superimposed on a 5V dc level is 50kHz for the multiplier, and V_X x 5kHz for the divider.

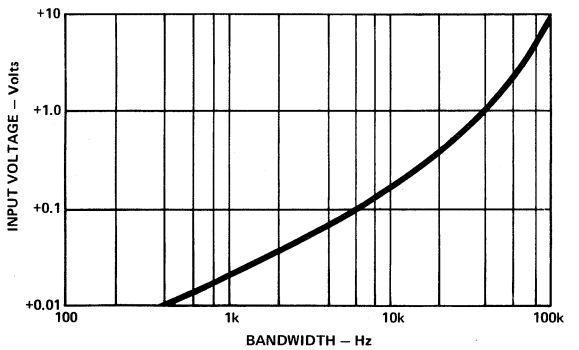


Figure 3. 434 Small Signal Bandwidth vs. Input Voltage

NOISE PERFORMANCE

The curve in Figure 4 shows output noise vs. signal level in a 1kHz BW for worst case conditions. These conditions exist when V_X is equal to V_Z and is varied over the specified operating range. It should be noted that for 0.1V inputs the effective gain is 100. To retain the full performance capability of model 434, all external noise sources should be isolated from the input terminals.

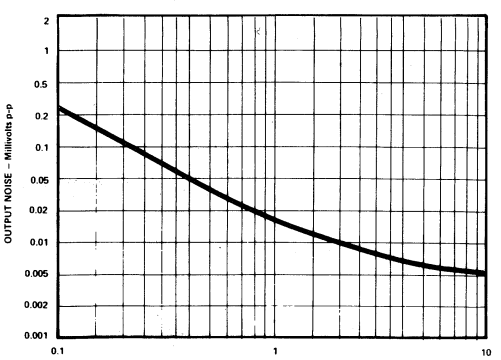


Figure 4. Output Noise vs. Denominator f = 0.01Hz to 10Hz

Figure 5 shows the relationship between output noise vs. denominator level for a 10Hz to 10kHz bandwidth.

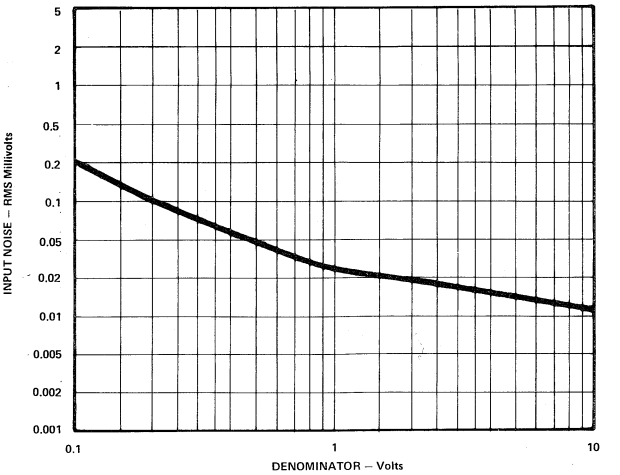


Figure 5. Output Noise vs. Denominator in 10Hz to 10kHz Bandwidth

As shown in these two figures, the noise for model 434 does not vary in direct relation to the denominator signal level. A typical multiplier/divider would demonstrate a 100:1 increase in noise as the denominator is varied from 10V to 0.01V. The model 434 displays a significantly lower change in noise over this range of inputs.

NONLINEARITY

The model 434, by virtue of its log-antilog circuitry, is capable of providing low distortion that is virtually independent of denominator level. Figure 6 shows dc nonlinearity as a function of input signal level for both trimmed and untrimmed units. Less than 0.05% nonlinearity over a range of denominators between +0.01V and +10V is possible through the use of external trims.

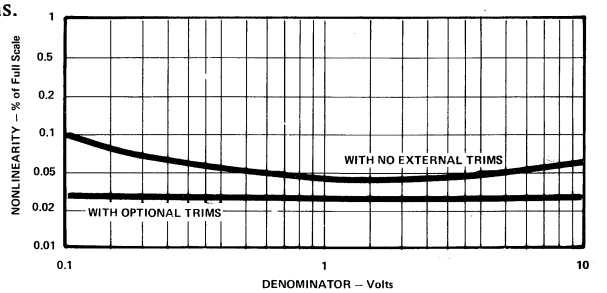


Figure 6. Nonlinearity vs. Signal Level for Constant Output = 10V dc

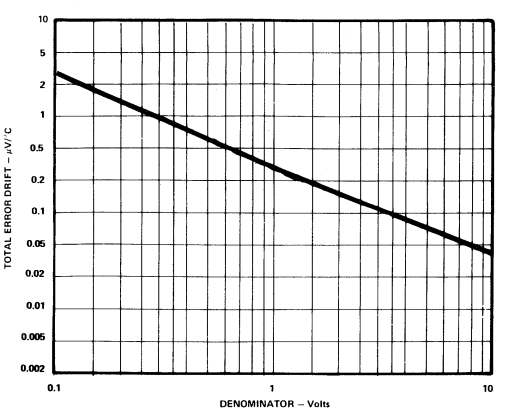


Figure 7. Total Output Error Drift vs. Denominator

OUTPUT ERROR DRIFT

Model 434 provides very low total output error drift over temperature. By virtue of its low drift, the 434 is capable of maintaining exceptional accuracy over a wide temperature and input signal range. Figure 7 shows total output error as a function of temperature for model 434.

APPLICATIONS

The model 434 is an extremely versatile module that allows the designer to synthesize a great variety of functions. Because of its extensive abilities, the 434 is an ideal component to select for such applications as ratiometric measurements, real-time computations and transducer linearization. A few of the possible uses of the model 434 are given below. The examples shown utilize the voltage inputs of the divider, but the same networks can also be applied using the 434's current input terminals.

MODEL 434B – 0.25% DIVIDER, WIDE DYNAMIC RANGE

Probably the most impressive performance of model 434's log/antilog circuit approach, is its ability to hold high divider accuracies over a wide 100:1 input signal range.

When using a conventional multiplier/divider, accuracy, offset drift, and noise performance are all degraded as the denominator is decreased.

For model 434, overall divider accuracy is virtually independent of denominator level as illustrated in Figure 8 and this performance is obtained with no external trims.

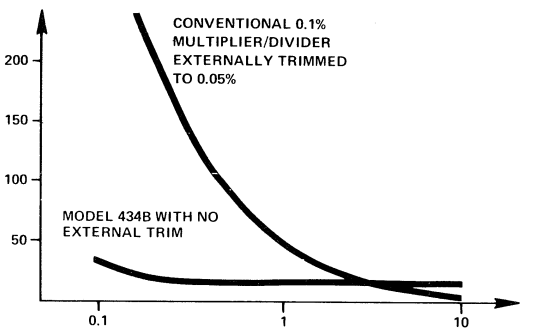


Figure 8. Comparison of Divider Error vs. Denominator Level for Model 434B and a Conventional Mult./Div.

SQUARE ROOT CALCULATIONS

The square root of a single variable may be obtained with no external components when connected as shown above. Noise performance is even better than that for the multiply or divide mode. The overall gain of the computation may be varied by selecting the voltage level applied to the V_Y terminal.

As shown in Table I, model 434 provides outstanding performance when operating in the square root mode.

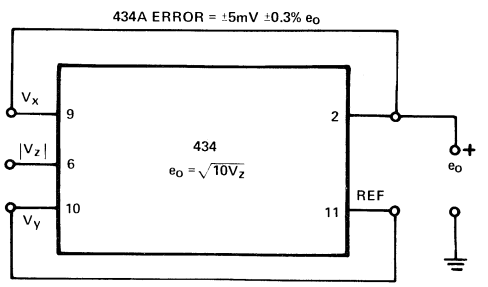


Figure 9. Square Root Connections

SQUARE ROOTING SPECIFICATIONS (TYPICAL, TRIMMED)

OUTPUT FUNCTION	$-\sqrt{10\|Z\|}$
Dynamic Range	1000 to 1 (+0.01V ≤ Z ≤ +10V)
Accuracy (% of Full Scale)	0.25%

Table I. Square Rooting Specifications

VECTOR COMPUTATIONS

The vector computation circuit shown in Figure 10 demonstrates the versatility of model 434. Used with two inexpensive op amps the 434 is used as a basic building block, which in this case, provides the square root of the sum of the squares.

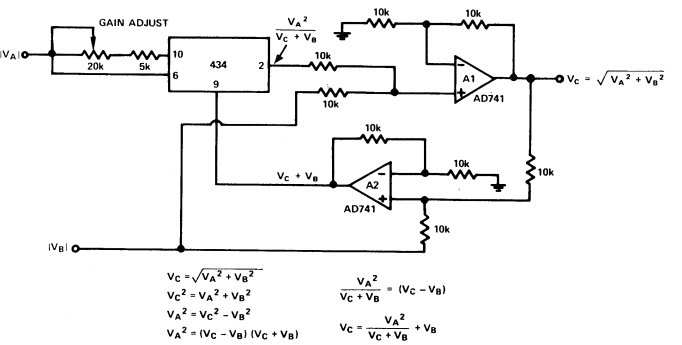


Figure 10. Vector Computation $V_C = \sqrt{V_A^2 + V_B^2}$

This application is based on the identity for the difference of squares. The derivation is shown by the equations above and the final equation for V_C is implemented.

Due to the excellent inherent accuracy of the above circuit (error = 0.1% of reading), matched resistors with a low T.C. should be used. Errors of only 0.1% of the theoretical output may be achieved over signal levels of +100mV to +10V.

When using this circuit, the designer must take care that the input levels, V_A and V_B, and the output, V_C, are all less than 10V for any computation.

Figure 11 shows a vector computation network for n variables. Again the designer must take care that input levels do not cause the output to saturate.

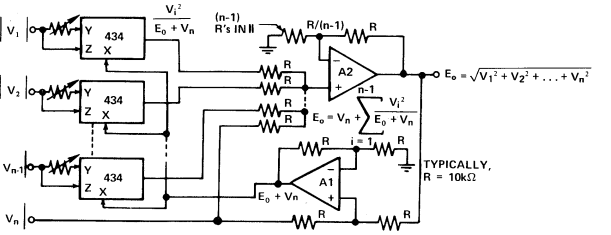


Figure 11. Extension of the Vector Computation Technique to n Input Signals

Precision, 1/4%, 1/10% Multiplier, Divider, Square Rooter

MODEL 435

FEATURES

- High Accuracy Without Trimming: 0.1% max (435K); 0.25% max (435J)
- Low Accuracy Drift: 0.01%/°C max (435K)
- Low Output Offset Drift: 0.2mV/°C max (435K)
- Scale Factor Adjustment: Single Trim Pot
- Low Nonlinearity: 0.05% max (435K)
- Low Noise: 1mV rms (10Hz to 1MHz)

APPLICATIONS

- Phase Detection
- Power Measurement
- Automatic Gain Control
- Modulation and Demodulation

GENERAL DESCRIPTION

Model 435K is a precision transconductance multiplier that combines factory trimmed accuracy to within 0.1% max with output offset drift of only 0.002%/°C max, and nonlinearity of 0.05% max. Corresponding specifications for model 435J are 0.25% max accuracy, 0.003%/°C max offset drift and nonlinearity of 0.1% max. All specifications apply for any X or Y input signal within ±10 volts over all four quadrants. Optional trimming may be used to further improve accuracy, typically by a factor of two. In addition, the model 435 features excellent noise performance of 1mV, rms in a bandwidth of 10Hz to 1MHz. Bandwidth is 250kHz (-3dB) and feedthrough for model 435J is 20mV p-p, max and 10mV p-p, max for model 435K. Model 435 may also be used as a precision divider, squarer or square rooter.

ACCURACY

Multiplication accuracy is specified as a percentage of full scale output and is guaranteed without external trimming. Full scale output for model 435 is ±10 volts; the maximum error for model 435K is ±0.1%, or ±10mV. This error includes all room temperature error terms (scale factor, output offset, feedthrough and nonlinearity) for any input (X or Y) combination of ±10 volts. For improved accuracy, the output offset, scale factor and feedthrough may be trimmed using external trim potentiometers connected to the power supply. When external trimming is used to improve accuracy, nonlinearity becomes the limiting error term. Model 435 features very low nonlinearity (±0.05% max, 435K) to enable the user to perform very accurate operations using model 435. Output noise, typically 250μV, rms (10Hz to 10kHz) is significantly reduced over previous multiplier designs to permit improved signal resolution.

SCALE FACTOR ADJUSTMENT

Model 435 features a unique scale factor (gain) adjustment control which permits the user to easily compensate for system errors. The external scale factor (gain) pot will provide an adjustment range of at least ±1% and may be located away from the 435 module for operator convenience.

FREQUENCY RELATED SPECIFICATIONS

Feedthrough, linearity, gain and phase shift, which are components of overall multiplier accuracy, are frequency dependent parameters. On model 435, feedthrough is constant for both X and Y inputs up to 1kHz. Between 1kHz and 9kHz, it rises at about 6dB/octave. Above 9kHz, the X input feedthrough remains constant. Y input feedthrough continues to rise at 6dB/octave up to 60kHz and then levels off above that frequency. A plot of feedthrough vs. frequency is shown in Figure 1.

Nonlinearity for both the X and Y inputs also increases with frequency at a 6dB/octave rate above the break frequency of 1.5kHz. Figure 1 shows a typical plot of nonlinearity vs. frequency for the 435. Gain and input to output phase shift for the model 435 are shown in Figure 2; the data was recorded with Y input = +10V and X input = 2V p-p. All multipliers have a reduced gain at frequencies approaching the small signal bandwidth. For model 435 a 1% amplitude error occurs at 30kHz and a 1% "vector" error in output phase shift occurs at 2kHz.

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	435J	435K
TRANSFER FUNCTIONS		
Multiply Mode	$e_O = XY/10$	*
Divide Mode	$e_O = 10Z/X$	*
Square Root Mode	$e_O = -\sqrt{10Z}$	*
Squaring Mode	$e_O = X^2/10$	*
ACCURACY (MULTIPLICATION MODE)[1]		
Total Output Error at +25°C		
Internal Trim	±0.25% max	±0.1% max
External Trim	±0.08%	±0.05%
vs. Temperature 0 to +70°C	±0.01%/°C	±0.01%/°C max
vs. Supply Voltage	±0.02%/%	*
Warm Up Time, to Rated Performance	5 minutes	*
NONLINEARITY		
X Input (Y = ±10V; X = 20V p-p, 10Hz)	±0.1% max	±0.05% max
Y Input (X = ±10V; Y = 20V p-p, 10Hz)	±0.1% max	±0.05% max
OUTPUT OFFSET		
Initial, @ +25°C	±10mV max	±5mV max
vs. Temperature, 0 to +70°C	±0.3mV/°C max	±0.2mV/°C max
vs. Supply Voltage	±1mV/%	*
SCALE FACTOR		
Initial Error, @ +25°C	±0.1%	±0.05%
vs. Temperature, 0 to +70°C	±0.01%/°C	*
FEEDTHROUGH		
X = 0, Y = 20V p-p, 10Hz	20mV p-p max	10mV p-p max
With External Trim	5mV p-p	*
Y = 0, X = 20V p-p, 10Hz	20mV p-p max	10mV p-p max
With External Trim	5mV p-p	*
FREQUENCY RESPONSE		
-3dB, Small Signal	250kHz	*
Full Power Response	25kHz	*
Slew Rate	2V/μs	*
1% Amplitude Error	30kHz	*
1% Vector Error (0.57°)	2kHz	*
Overload Recovery Time	5μs	*
Settling Time, ±1%, 20V Step	10μs	*
Settling Time, ±0.1%, 20V Step	20μs	*
RATED OUTPUT[2]		
Voltage, 2kΩ Load	±10V min	*
Current	±5mA min	*
Impedance	0.1Ω	*
Load Capacitance	0.01μF min	*
OUTPUT NOISE		
Voltage, 10Hz to 10kHz	250μV rms	*
Voltage, 10Hz to 1MHz	1mV rms	*
INPUT RESISTANCE		
X Input Terminal	100kΩ	*
Y Input Terminal	100kΩ	*
Z Input Terminal	70kΩ	*
INPUT BIAS CURRENT		
X Input Terminal	50nA	*
vs. Temperature, 0 to +70°C	50pA/°C	*
Y Input Terminal	100nA	*
vs. Temperature, 0 to +70°C	100pA/°C	*
Z Input Terminal	70μA	*
vs. Temperature, 0 to +70°C	5nA/°C	*
MAXIMUM INPUT VOLTAGE		
For Rated Accuracy, X, Y, Z Terminals	±10V	*
Safe Input Level	$\pm V_S$	*
POWER SUPPLY[3]		
Voltage, Rated Performance	±15V	*
Voltage, Operating	±(12 to 18)V	*
Current, Quiescent	±8mA	*
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage	-55°C to +125°C	*
MECHANICAL		
Case Size	1.65" x 3.07" x 0.65"	*
Weight, grams	85	*
Mating Socket	AC1023	*

*Specifications same as model 435J.

[1] Accuracy is guaranteed with no external trim adjustments when connected in the multiplication mode. All accuracy is % of full scale output where full scale output is ±10V (±0.1% = ±10mV error).

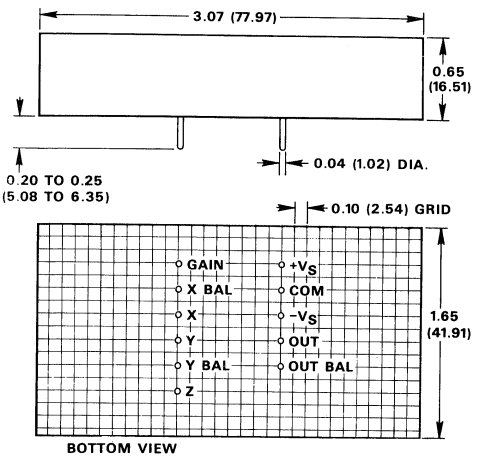
[2] Short circuit protected to ground.

[3] Recommended power supply; ADI model 904, ±15V @ 50mA output

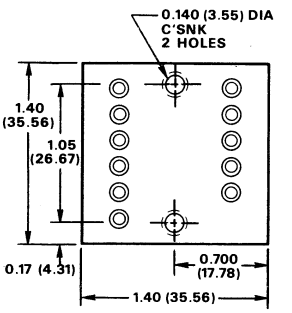
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

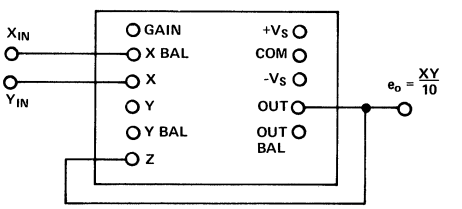


MATING SOCKET AC1023



MULTIPLIER CONNECTIONS

Bottom View



ADDITIONAL MULTIPLIERS/DIVIDERS

Analog Devices manufactures a wide array of modules to fill almost any multiplier/divider design need. A list of some of these models with their salient operating features is given below. One of these devices will surely provide the optimum solution to your engineering problem.

429 - High Speed, fp = 2MHz — 1%, ½% Accuracy
426 - Best Buy — 1% — Low Nonlinearity and Feedthrough
436 - High Accuracy 2-Quadrant Divider
434 - High Accuracy 1-Quadrant Divider, Square Rooter

NONLINEAR CIRCUITS HANDBOOK

The Nonlinear Circuits Handbook, available from Analog Devices, is an invaluable source of information on principles, circuitry, performance specifications, testing and application of the class of devices designed for use in nonlinear applications. This text provides you with all the fundamentals and guidelines necessary for the proper selection and use of function modules.

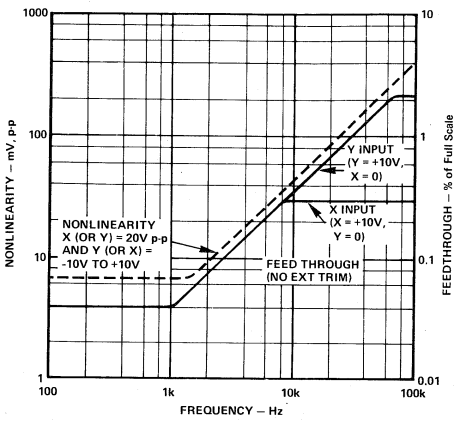


Figure 1. Feedthrough and Nonlinearity vs. Frequency.

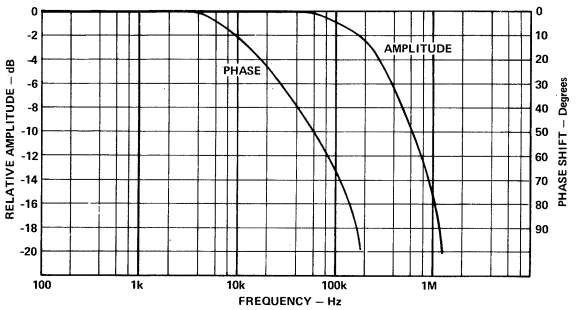


Figure 2. Amplitude and Phase vs. Frequency

OPTIONAL TRIM – MULTIPLY MODE

As shipped, the multiplier meets its listed specifications without the use of any external trim potentiometers. Terminals are provided for optional feedthrough and offset adjustments. Using these adjustments overall static multiplication error may be reduced to only 0.08% (435J). The 20kΩ trim potentiometers should be connected as shown in Figure 3.

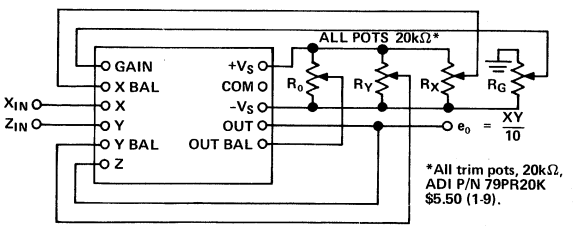


Figure 3. Multiplier Connections

NOTE: Allow unit to warm up for 5 minutes before making adjustments.

ADJUSTMENT PROCEDURE FOR OFFSET

1. Jumper X input and Y input to ground.
2. Adjust R_0 for an output of zero volts.
3. Remove jumper from X and Y inputs.

ADJUSTMENT PROCEDURE FOR FEEDTHROUGH

1. Jumper Y input to ground and apply 20 VPP at 1kHz to X input.
2. Adjust R_Y for minimum output voltage.
3. Remove jumper from Y input.
4. Jumper X input to ground and apply 20 VPP at 1kHz to Y input.
5. Adjust R_X for minimum output voltage.
6. Remove jumper from X terminal.

ADJUSTMENT PROCEDURE FOR GAIN

1. Set X and Y inputs to +10.000V dc (tie X and Y inputs together).
2. Adjust gain pot for desired output level (10.00V dc ±1%).

DIVISION

Model 435 has a wide bandwidth and excellent linearity which allows it to achieve very high performance in divider applications in the dc to 250kHz region. Restrictions and limitations imposed on divider operation and the contribution of error terms are illustrated in the discussion below.

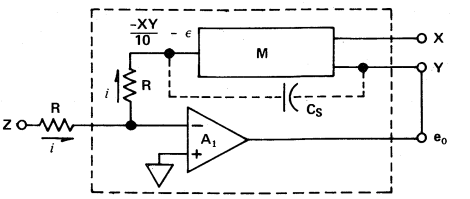


Figure 4. Divider Model

The expression for divider operation can be written:

$$e_o = \underbrace{\frac{10Z}{X}}_{\text{Ideal Division}} - \underbrace{\frac{10E}{X}}_{\text{Error Term}}$$

where E represents the errors associated with the divider.

Breaking E into its component parts, e_o can be expressed as follows:

$$e_o = \underbrace{\frac{10Z}{X}}_{\text{ideal divider}} - \underbrace{\frac{10E_{NV}}{X}}_{\text{noise error}} - \underbrace{\frac{10E_{OS}}{X}}_{\text{offset error}} - \underbrace{\frac{10E_{OS}/^{\circ}C}{X}}_{\text{offset drift error}} - \underbrace{\frac{10E_{NLX}}{X}}_{\text{X nonlinearity error}} - \underbrace{\frac{10E_{NLY}}{X}}_{\text{Y nonlinearity error}}$$

All of these errors, both static errors and signal dependent errors, are inversely proportional to the denominator signal level. Figure 5 shows the inverse relationship of output voltage noise vs. denominators for the 435 in the divider mode.

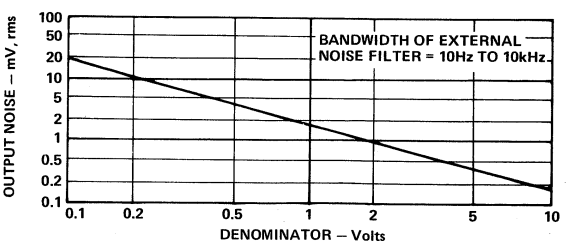


Figure 5. Output Voltage Noise vs. Denominator-Divide Mode

Signal dependent errors are the X and Y nonlinearities. It is important to use the terminal with the largest nonlinearity for the denominator. Since E_{NLX} and E_{NLY} can be expressed as a percentage of the input signal, it can be seen, in the error terms

$$\frac{-10E_{NLX}}{X} \text{ and } \frac{-10E_{NLY}}{X}$$

that the effect of X nonlinearities are practically independent of signal and may be trimmed out.

Bandwidth is also degraded with a decrease in denominator level, due to the increase in system gain;

i.e.) for X = Z = 1V, e_0 = 10V

$$\text{and } \frac{e_0}{Z} = \frac{10}{1} = 10$$

Since the gain bandwidth product is constant, a bandwidth 1/10 of that obtained for full scale denominator levels will be obtained for division at 1V levels.

For other denominator levels, bandwidth is determined by:

$$\text{B.W.} = \frac{\text{Denominator Level}}{\text{Full Scale Denominator}} \times (\text{Multiplier B.W.})$$

Before selecting a multiplier/divider for divide applications, errors resulting from the lowest anticipated denominator signal should be considered. After such considerations have been made one can further appreciate the importance of starting with an accurate, high speed multiplier such as model 435K. It is also highly recommended that the optional trim procedure for division be performed.

OPTIONAL TRIMMING – DIVIDE MODE

Connections are made as shown in Figure 6.

NOTE: Allow unit to warm up for 5 minutes before making adjustments.

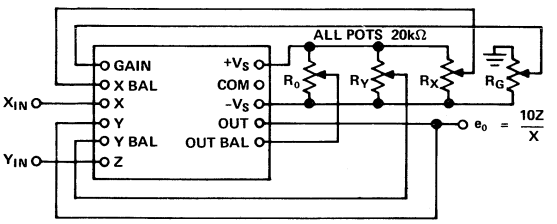


Figure 6. Divider Connections

The suggested trim procedure is (starting with centered adjustments):

*1. With Z = 0, trim R_0 to hold output constant, as X is varied from -10V toward -1.0V.
2. With Z = 0, trim R_Y for zero at X = -10V.
3. With Z = X and/or Z = -X, trim R_X for minimum worst-case variation as X is varied from -10V to -1.0V.
4. Repeat 1 and 2 if step 3 required large initial adjustment.
5. With Z = X = 1.00V (tie Z and X inputs together) adjust R_g for desired output (10.0V ±1%).

*For best accuracy X should be allowed to vary from -10V to lowest expected denominator.

SQUARE ROOTING

When connected as shown in Figure 7, the model 435 will provide the square root of Z_{IN}.

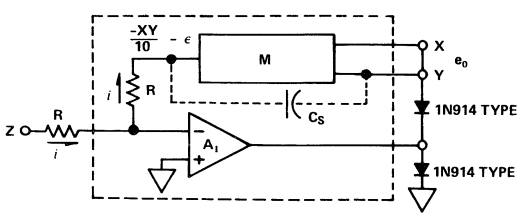


Figure 7. Square Root Model

By summing currents at the op amp's summing junction

$$\frac{Z}{R} = \frac{XY}{10R} + \frac{\epsilon}{R} = \frac{Y^2}{10R} + \frac{\epsilon}{R}$$

where ϵ represents all errors associated with the multiplier. Solving for the output voltage, Y,

$$e_0 = \pm\sqrt{10\,(Z - \epsilon)}$$

There are two values of e_0 for every value of Z. However, only negative values of e_0 will provide the negative feedback necessary for circuit stability. To restrict the output from going positive, diodes are connected as shown in Figure 7. The output is then:

$$e_0 = -\sqrt{10\,(Z - \epsilon)}$$

Errors, ϵ, associated with the multiplier, are inside the square root and consequently their effect, for large values of Z, is reduced. The reason for the improved performance can be seen by inspecting the circuit. The output is fed back to both the X and Y terminals, resulting in twice the feedback.

OPTIONAL ADJUSTMENT PROCEDURE – SQUARE ROOT

1. Apply a voltage to the Z terminal equal to the lowest anticipated input voltage.
2. Adjust R_0 such that $e_0 = -\sqrt{10Z_{IN}}$ where Z_{IN} is the voltage applied in step 1.

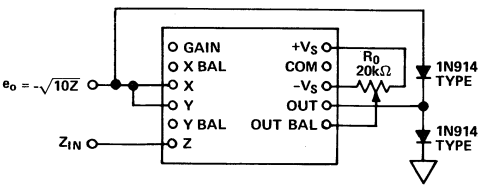


Figure 8. Square Root Connections

DIVISION SPECIFICATIONS (TYPICAL, TRIMMED)

OUTPUT FUNCTION	10(Z)/X
Numerator Range	±10V
Denominator Range, 0.1% Accuracy	-1V to -10V
Denominator Range, 1% Accuracy	-0.1V to -10V
Bandwidth Formula, (-3dB)	(X/10) 300kHz

SQUARE ROOTING SPECIFICATIONS (TYPICAL, TRIMMED)

OUTPUT FUNCTION	$-\sqrt{10(Z)}$
Dynamic Range	1000 to 1 (+0.010V ≤Z≤+10V)
Accuracy (% of Full Scale)	0.1%
Bandwidth Formula, (-3dB)	(300kHz) $\sqrt{\lvert X\rvert/10}$

Table 1. Division & Square Rooting Specifications

ANALOG DEVICES

High Accuracy, Two Quadrant Analog Divider

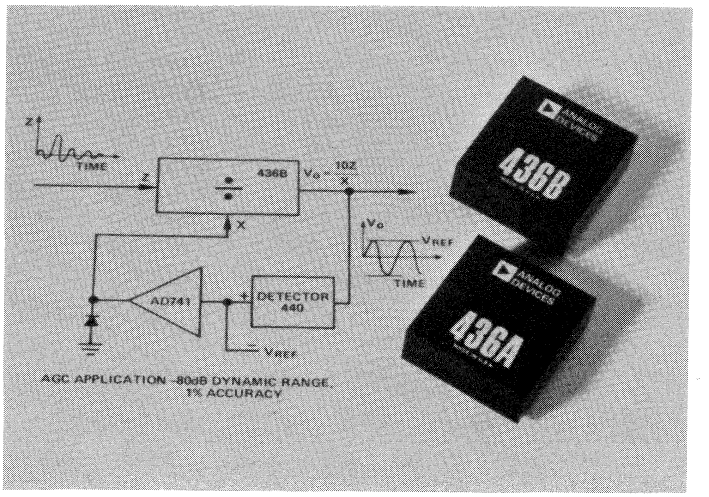
MODEL 436

FEATURES

- Two Quadrant: Numerator Range: ±10V
- High Accuracy: 0.5% max (436A), 0.25% max (436B) over 100:1 Dynamic Range
- No Trimming Required to Achieve Rated Accuracy
- 1000:1 Denominator Range: With External Trim
- Low Nonlinearity: 0.05% (436B)
- Low Harmonic Distortion: -66dB (436B)
- All Hermetically-Sealed Semiconductors
- Wide Operating Temperature Range, -25°C to +85°C

APPLICATIONS

- Linear Gain Control (80dB Range)
- Transducer Linearization
- Instrumentation Calculation
- Adaptive Process Control



GENERAL DESCRIPTION

Model 436 is a precision, two-quadrant variable transconductance analog divider featuring guaranteed accuracy of ±0.5% (model 436A) and ±0.25% (model 436B) over a 100:1 denominator signal range (100mV to 10V) with no external adjustments. With the use of optional external trimming, accuracy may be improved to ±0.05% (436B) over a 1000:1 denominator signal range (10mV to 10V). In addition to this excellent accuracy, model 436 offers a small signal bandwidth (-3dB) of 300kHz and typical numerator nonlinearity of less than ±0.05% (5Hz to 30kHz).

Through the use of hermetically-sealed semiconductors, the model 436 affords exceptional reliability over a wide operating temperature range (-25°C to +85°C). This compact (1.5″ x 1.5″ x 0.6″) epoxy module provides further reliability by protecting the output against damage due to short circuits to ground. The model 436 is pin compatible with most modular multipliers. This allows the model 436 to replace inverted multiplier type dividers in existing sockets to give improved accuracy and increased dynamic range.

TWO QUADRANT OPERATION

Dividers are generally available as single and two-quadrant devices. Dividers that are formed by closing the loop around a four-quadrant transconductance multiplier are capable of operating in two quadrants. Unfortunately, because of the feedback around the multiplier, these dividers suffer from errors which increase directly as the denominator decreases. Even using 0.1% multipliers, these errors become large as the denominator becomes small and high performance is possible only over a limited range of input levels. This denominator dependency of divider errors can be greatly reduced by application of log-antilog techniques, as in the model 434 that has a 0.25% accuracy for denominators within 0.1 to 10V. However, while dividers that use log-antilog circuits are inherently more accurate than inverted multiplier devices, they are limited to single-quadrant operation by the nature of the log function.

The model 436 employs a unique log-antilog circuit to provide two-quadrant operation with high accuracy over a very wide range of denominators.

THEORY OF OPERATION

Model 436 is comprised of summing networks, log circuits and a transconductance differential amplifier as shown in Figure 1.

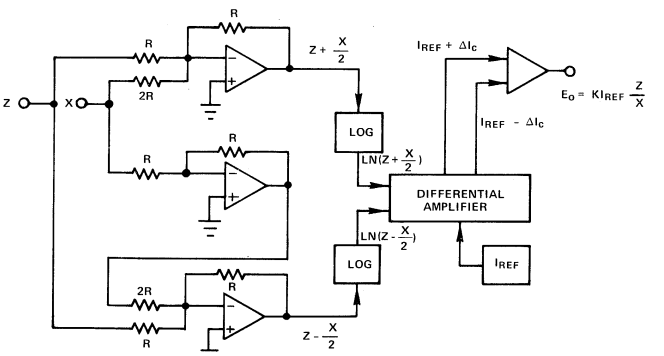


Figure 1. Functional Block Diagram

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL		436A	436B
TRANSFER FUNCTION	$\|V_Z\| \leq V_X$; $V_X > 0$	$e_O = 10V_Z/V_X$	*
ACCURACY[1]			
Total Output Error, @ +25°C	$\|V_Z\| \leq 10V$		
No External Trim	$+0.1 \leq V_X \leq +10V$	±0.5%, max	±0.25%, max
External Trim	$+0.1 \leq V_X \leq +10V$	±0.3%, max	±0.1%, max
Over Temperature	$+0.1 \leq V_X \leq +10V$		
No External Trim	0 to +70°C	±2.0%, max	±1.0%, max
No External Trim	-25°C to +85°C	±4.0%, max	±2.0%, max
Vs. Supply Voltage		±0.02%/%	*
Warm Up Time to Rated Performance		5 Minutes	*
NONLINEARITY	$\|V_Z\|/V_X$, $+0.1 \leq V_X \leq +10V$	±0.15% max (0.1% typ)	±0.1% max (0.05% typ)
RATED OUTPUT[2]			
Voltage		±10V, min	*
Current		±5mA, min	*
Resistance		0.1Ω	*
Capacitance Load		0 to 1000pF, min	*
INPUT SPECIFICATIONS			
Voltage, Numerator Signal (V_Z)	$\|V_Z\| \leq V_X$	±10V	*
Voltage, Denominator (V_X)	$V_X > 0$	+10V	*
Safe Input Voltage, V_Z and V_X		$\pm V_S$, max	*
Offset Voltage, @ +25°C, V_Z and V_X		±100μV	*
vs. Temperature	-25°C to +85°C, V_Z, V_X	±20μV/°C	*
vs. Supply Voltage, V_Z and V_X		±30μV/%	*
External Trim Adjustment Range, V_Z		±4.5mV	*
External Trim Adjustment Range, V_X		±1.5mV	*
Voltage Noise, 10Hz to 10kHz, V_X and V_Z		15μV, rms	*
INPUT IMPEDANCE			
Numerator, V_Z		9kΩ, ±2%	*
Denominator, V_X		25kΩ, ±1%	*
OUTPUT SPECIFICATIONS[3]			
Offset Voltage, @ +25°C, V_X = +10V		±10mV	*
vs. Temperature -25°C to +85°C, V_X = +10V		±500μV/°C	*
vs. Supply Voltage		±50μV/%	*
External Trim Adjustment Range		±20mV	*
Voltage Noise, 10Hz to 10kHz, V_X = +10V		200μV, rms	*
10Hz to 300kHz, V_X = +10V		750μV, rms	*
FREQUENCY RESPONSE			
Small Signal, -3dB,	$+0.1 \leq V_X \leq +10V$	300kHz	*
Full Power	$+0.1 \leq V_X \leq +10V$	30kHz	*
Slew Rate	$+0.1 \leq V_X \leq +10V$	2V/μs	*
Settling Time, to ±0.5%, ±10 Volt Step, V_X = +10V		10μs	*
Settling Time, to ±0.5%, ±10 Volt Step, V_X = +0.1V		10μs	*
Overload Recovery, $+0.1 \leq V_X \leq +10V$		5μs	*
POWER SUPPLY[4]			
Voltage, Rated Performance		±15V dc	*
Voltage, Operating		±(12 to 18)V dc	*
Current, Quiescent		±9mA	*
TEMPERATURE RANGE			
Rated Performance		-25°C to +85°C	*
Storage		-55°C to +125°C	*
MECHANICAL			
Case Size		1.5" x 1.5" x 0.62"	*
Mating Socket		AC-1041	*
Weight, grams		36	*

*Specifications same as model 436A.

[1] Error is specified as a percentage of full scale output where full scale output is 10 volts.

[2] Output is protected for short circuits to ground, indefinite.

[3] Output offset is specified with no external trimming; optional 50kΩ potentiometer may be connected to zero the output offset voltage.

[4] Recommended power supply; model 904, ±15V @ 50mA output

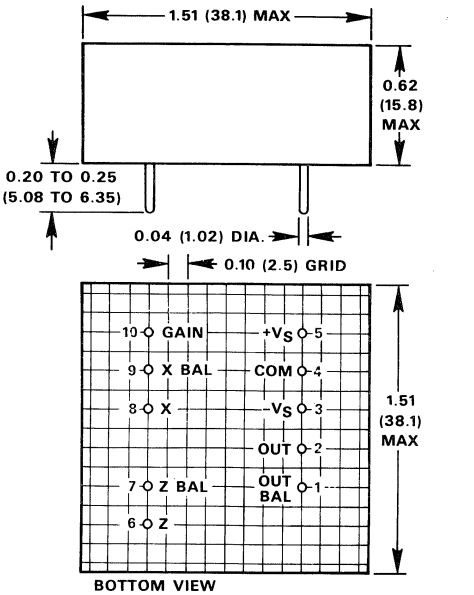
Specifications subject to change without notice.

NONLINEAR CIRCUITS HANDBOOK

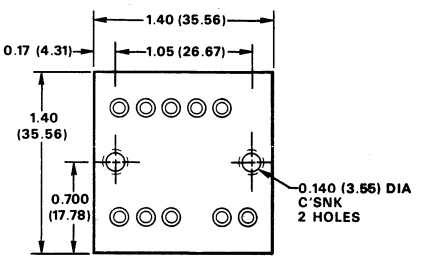
The Nonlinear Circuits Handbook, available from Analog Devices, is an invaluable source of information on principles, circuitry, performance specifications, testing and application of the class of devices designed for use in nonlinear applications. This text provides you with all the fundamentals and guidelines necessary for the proper selection and use of function modules.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET AC-1041



WIRING CONNECTIONS

Bottom View Shown in all Cases

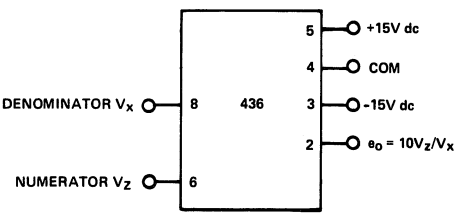


Figure 2. Divide Mode Connections

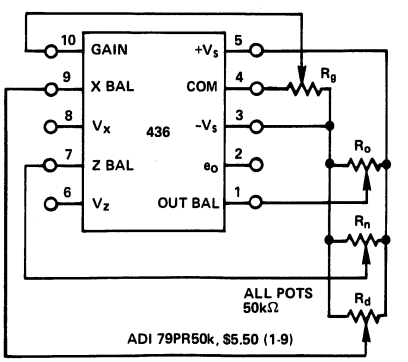


Figure 3. Optional Trim Connections

The summing and log circuits provide signals to the input of the differential amplifier that are proportional to the sum and difference of the X and Z inputs. The difference between these two signals causes an imbalance current, ΔI_C, in the differential amplifier. The resultant output currents of the differential amplifier are equal to $I_{REF}/2 + \Delta I_C$ and $I_{REF}/2 - \Delta I_C$, where I_{REF} is a stable reference current supply. These two output currents bear a relationship to the input signals that is expressed by:

$$\frac{X + Z/2}{X - Z/2} = \frac{I_{REF}/2 + \Delta I_C}{I_{REF}/2 - \Delta I_C}$$

The final amplifier stage of the model 436 processes these currents and yields an output voltage whose expression is,

$$E_O = KI_{REF}\frac{Z}{X} = \frac{10Z}{X}$$

This ratio relationship between X and Z is very accurate even for small value of X. Also by virtue of the log-antilog nature of this technique, output errors remain reasonably constant over the specified range of denominator inputs. Beyond the specified denominator range, second order effects, due to input offsets, cause the output error to increase with decreasing denominator. In the model 436, these second order effects are minimized. Input offsets can be further reduced by means of external trims. Trimming allows the 436 to maintain rated accuracy over a 1000:1 range of denominator inputs. Therefore, model 436 provides excellent performance and stability over a wide range of input signals and operating conditions. For a detailed explanation of the design used in the 436, refer to Analog Devices' Nonlinear Circuits Handbook ($5.95).

ACCURACY VS. DENOMINATOR

By virtue of the nature of the log function, the errors associated with log-antilog type dividers can be expressed as a constant plus a constant fraction of the output over the specified input range. Therefore, unlike inverted multiplier type dividers which demonstrate an inverse relationship between accuracy and denominator, the model 436 has outstanding accuracy which is reasonably denominator independent over a 100:1 range. Model 436A and 436B are guaranteed to have maximum output error of 0.5% and 0.25% respectively for denominator values from 100mV to 10 volts. A plot of typical output error vs. denominator for the 436 is shown in Figure 4.

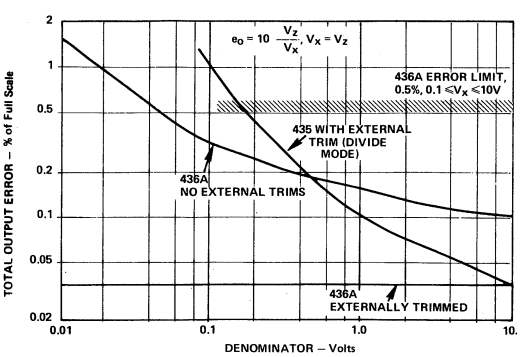


Figure 4. Total Output Error vs. Denominator at Constant Ratio $V_Z/V_X = 1$. Comparison of Model 436 with Model 435, 0.1% Multiplier-Divider.

The accuracy of the 436 can be further improved by use of external trims (see Optional Adjustment Procedure). Figure 4 shows accuracy vs. denominator for a 436 with external trim. Optional trimming allows the 436B to maintain better than 0.1% accuracy over a 1000:1 range of the denominator signal.

ACCURACY VS. TEMPERATURE

The output offset drift vs. temperature of the model 436 remains fairly constant over a 100:1 range of denominators. Total error drift is typically 1mV/°C at V_X = 10V and 2mV/°C at V_X = 100mV. Model 436 is therefore capable of maintaining outstanding accuracy over a wide range of temperature and denominator signal level. Figure 5 shows total error drift vs. denominator for the 436.

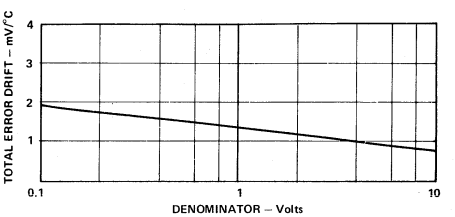


Figure 5. Total Error Drift vs. Denominator

NON-LINEARITY

The symmetry of the type of circuit used in model 436 provides low numerator distortion independent of denominator level. Figure 6 shows nonlinearity vs. denominator.

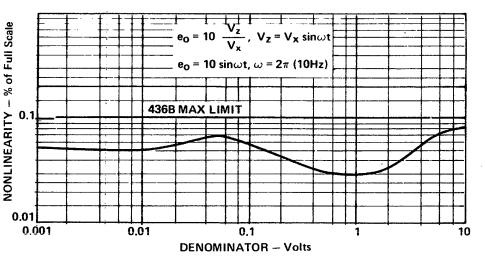


Figure 6. Nonlinearity vs. Signal Level for Constant Output = 10 sinωt (10Hz)

FREQUENCY RESPONSE

The bandwidth of any divider decreases with a decrease in denominator due to the increase in system gain. Figure 7 shows a typical plot of the small signal and full power bandwidth vs. denominator for the model 436.

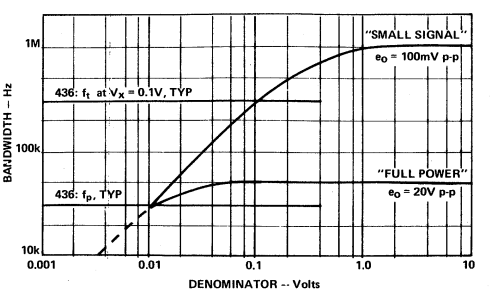


Figure 7. Small Signal Bandwidth (-3dB) and Full Power Bandwidth vs. Denominator

NOISE PERFORMANCE

Model 436 offers very good output noise performance in addition to its other excellent operating characteristics. Output noise can be an important parameter in dynamic computing. The model 436 typically has a 200μV rms output noise level in the 10 to 10kHz band for V_X = +10V.

Figure 8 shows output noise vs. denominator for model 436.

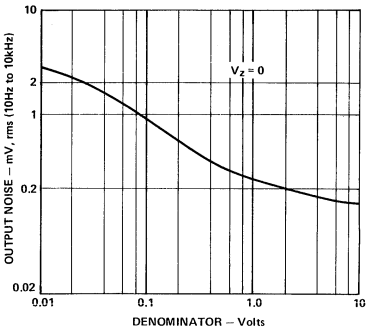


Figure 8. Output Noise vs. Denominator – 5Hz to 10kHz

OPTIONAL ADJUSTMENT PROCEDURE

One of model 436's features is high untrimmed accuracy. As shown in Figure 4, significant improvement in performance can be achieved with external trimming. Model 436 can be typically trimmed to less than ±0.1% of full scale accuracy (±10mV error) for a denominator signal range from +10mV to +10V (1000:1). To achieve this performance, the following adjustment procedure is recommended: (see Figure 3)

1) Allow unit to warm up for approximately 5 minutes. Let denominator (V_X) = +10V and numerator (V_Z) = 0V (connect to common pin). Adjust OUTPUT OFFSET potentiometer (R_O) for 0mV output.

2) Let denominator = +10mV and numerator = 0V (connect to common pin). Adjust NUMERATOR OFFSET potentiometer (R_n) for 0mV output.

3) a. Let denominator = numerator = +10.000V and adjust GAIN potentiometer (R_g) for +10.000V output.
b. Reverse the polarity of numerator (to - 10.000V), and note the output voltage error (error = 10.000 - $|e_o|$). The GAIN potentiometer R_g should be readjusted to achieve the lowest error for both step a. and step b.

4) Connect both numerator/denominator together and apply a +10mV input. Adjust DENOMINATOR OFFSET potentiometer (R_d) for +10.000V output.

REPLACEMENT OF 0.1% MULTIPLIERS

In divider applications requiring high accuracy over a wide range of denominators, the model 436 provides significant advantages over 0.1% multipliers used in the inverted multiplier divide mode. As shown in Figure 4, an untrimmed 436 yields better overall accuracy than the most accurate available multiplier (435K) for a 100:1 change in denominator. With external trimming, model 436 delivers vastly superior performance over an even wider spread of denominator levels. The inverted multiplier type dividers suffer from the magnification of errors by $10/V_X$ whereas the errors of the variable transconductance circuit of model 436 are nearly independent of denominator. This advantage of the 436 design also is reflected in the reduced dependency of total error drift and bandwidth on the value of V_X. Figure 9 shows small signal bandwidth vs. denominator for the 436 and for 0.1% multiplier-dividers.

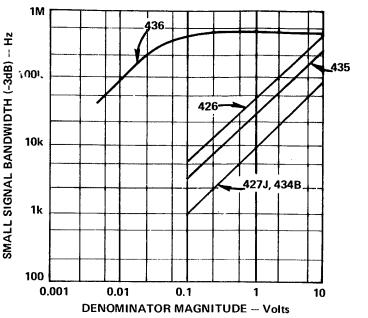


Figure 9. Bandwidth (-3dB) vs. Denominator

APPLICATIONS

Ratiometric Measurements

Dividers are useful for direct readout of such ratios as efficiencies, losses or gains, % distortion, impedance magnitudes, elasticity (stress/strain). Ratios may be taken of instantaneous, average, RMS or peak quantities. Furthermore, in conjunction with sample/hold devices, ratios may be taken of any of these measurements at different instants of time.

Ratiometric measurements are not new, but the low cost of precision analog dividers, like the model 436, should serve as an encouragement to designers to consider employment of the technique as a realistic alternative to expensive, tightly regulated reference sources for measurement. The divider output can profitably provide constant direct readout information on a DPM, such as the AD2026. In addition to eliminating the need for precise sources, the cost of calibration time required in systems currently depending on these sources can be reduced by ratiometric techniques employing the 436 divider.

A simple example involving the use of dividers in eliminating the effects of a common parameter is found in bridge measurements, where variations of the power supply directly affect the scale factor. But, if the output is divided by the bridge supply voltage, the scale factor depends only on the stability of the divider. The model 436 has the initial accuracy and stability which makes it useful in many ratio applications.

Compensation for reference-voltage variations is an example of reducing the effects of a common electrical parameter. However, ratios can also be used to eliminate the effects of a common physical parameter. For example, in light transmission measurements, it is common to compensate for variations in light intensity by transmitting two beams, one through a reference medium, the other through the medium being measured, and to take the ratio of the two measurements.

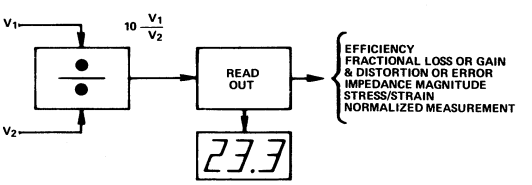


Figure 10. Ratio Measurements

The resultant output of ratiometric measurements may also be used as a feedback signal in adaptive process control networks. This technique facilitates accurate on-line monitoring and control of vital system parameters.

Logarithmic Amplifiers

Orientation
Logarithmic Amplifiers

The devices catalogued in this section are complete, self-contained modules that provide output voltage proportional to the logarithm or the antilogarithm (exponential) of an input quantity. These modules operate on the instantaneous values of inputs from dc to an upper cutoff frequency below 1MHz.

LOGS AND LOG RATIOS

In the *logarithmic* mode, the ideal output equation is

$$E_o = -K \log_{10} \left(\frac{I_{in}}{I_{ref}}\right)$$

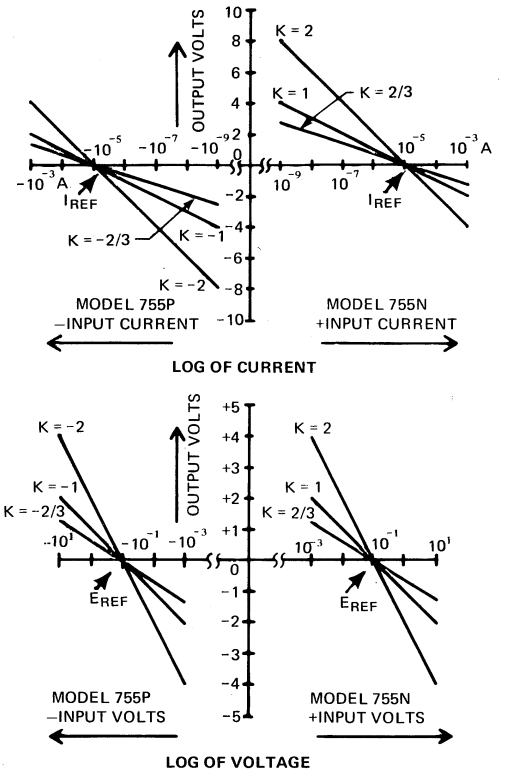
E_o can be positive or negative; it is zero when the ratio is unity, i.e., $I_{in} = I_{ref}$. K is the output scale constant; it is equal to the number of output volts corresponding to a decade* change of the ratio. In the 755 and 759 log amplifiers, K is pin-programmable to be either 1V, 2V, or 2/3V, or externally adjustable to any value $\geqslant$ 2/3V; in the model 757 log-ratio amplifier, K may be either a preset value of 1V, or an arbitrary value adjustable by an external resistance ratio.

I_{in} is a unipolar input current within a 6-decade range (1nA to 1mA); it may be applied directly, as a current, or derived from an input voltage via an input resistor (in which case, the ratio becomes $E_{in}/(R_{in}I_{ref}) = E_{in}/E_{ref}$. In models 755 and 759, the magnitude of I_{ref} is internally fixed at 10μA (E_{ref} = 0.1V) or externally adjusted; but model 757 is a *log-ratio* amplifier, in which both I_{in} and I_{ref} (or E_{in} and E_{ref}, using external scaling resistors) are input variables.

Each of the log amplifiers is available as a "P" or "N" option, depending on the polarity of the input voltage. Logarithms may be computed only for positive arguments, therefore the reference current must be of appropriate polarity to make the ratio positive. "N" indicates that the input current (or voltage) for the log mode is *positive;* "P" indicates that only *negative* voltage or current may be applied in the log mode. The polarity of K also differs: K is positive for "N" versions and negative for "P" versions. Thus, +10V applied to model 759N, with K = +1V, would produce an output voltage, $E_o = -1V \log (100) = -2V$; on the other hand, -10V applied to model 759P, with K = 1V, would produce an output voltage, $E_o = -(-1V) \log (100) = +2V$. The figure shows, in condensed form, the outputs of P and N log-amps, with differing K values, for voltage and current inputs.

Log amplifiers in the log mode are useful for applications requiring *compression* of wide-range analog input data, *linearization* of transducers having exponential outputs, and *analog computing*, ranging from simple translation of natural relationships in log form (e.g., computing absorbance as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

*A *decade* is a 10:1 ratio, two decades is 100:1, etc. For example, if K = 2, and the ratio is 10, the magnitude of the output would be 2V, and its polarity would depend on whether the ratio were greater or less than unity. If the input signal then changed by a factor of 1000 (3 decades), the output would change by 6V.



Output vs. Input of Model 755N & 755P in Log Connection (Log Input Scales), Showing Voltages, and Polarity Relationships

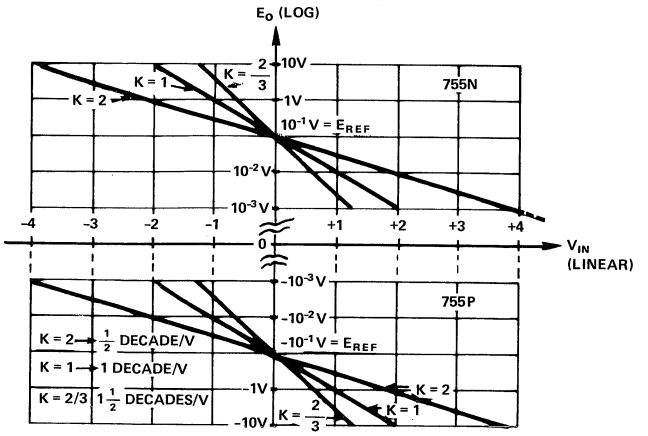
ANTILOGS

In the *antilogarithmic* (exponential) mode, the ideal output equation is

$$E_o = E_{ref} \exp_{10} (-E_{in}/K)$$

E_{in} can be positive or negative; when it is zero, $E_o = E_{ref}$. However, E_o is always of single polarity, positive for "N" versions, negative for "P" versions. Thus, for 759P, connected for K = -2V, if E_{in} = +4V, and E_{ref} = -0.1V, then $E_o = -0.1V \cdot 10^{-4/-2}$, or -10V; if $E_{in} = -4V$, then $E_o = -0.1V \cdot 10^{-(-4)/-2} = -1mV$. The figure on the next page shows, in condensed form, the outputs of P and N log amps, connected for antilogarithmic operation, with different K values.

Antilog amplifiers are useful for applications requiring *expansion* of compressed data, *linearization* of transducers having logarithmic outputs, *analog function fitting* or function generation, to obtain relationships or generate curves having volt-



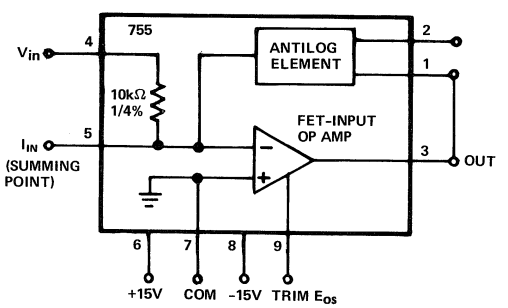
Antilog Operator Response Curves, Semilog Scale
$E_O = E_{REF}\ 10^{V_{IN}/-K}$

age-programmable rates of growth or decay, and in *analog computing*, for such functions as compound multiplication and division of terms having differing exponents.

LOG-ANTILOG AMPLIFIER PERFORMANCE

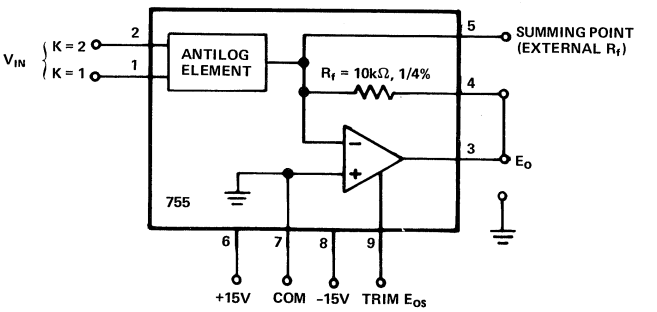
Considerable information regarding log- and antilog-amplifier circuit design, performance, selection, and applications is to be found in the NONLINEAR CIRCUITS HANDBOOK[1]. Several salient points will be covered here, and specifications will be defined. A brief Selection Guide will be found on page 212.

A log/antilog amplifier consists of an operational amplifier and an element with antilogarithmic transconductance (i.e., the voltage into the element produces a current that is an exponential function of the voltage). As the figure shows, for logarithmic operations, the input current is applied at the op-amp summing point, and the feedback circuit causes the amplifier output to produce whatever voltage is required to provide a feedback current that will exactly balance the input current.



a) Log/Antilog Amplifier Connected in the Log Mode (K = 1)

[1] Analog Devices, Inc., 1974, 1976, 536pp, edited by D.H. Sheingold, $5.95; send check or complete Master-Charge data to P.O. Box 796, Norwood MA 02062



b) Log/Antilog Amplifier Connected in the Exponential Mode
Log/Antilog Amplifier Connections

In antilog operation, the input voltage is applied directly to the input of the antilog element, producing an exponential input current to the op-amp circuit. The feedback resistance transduces it to an output voltage.

The wide range of log/exponential behavior is made possible by the exponential current-voltage relationship of transistor base-emitter junctions,

$$I = I_0(e^{qV/kT} - 1) \cong I_0 e^{qV/kT}$$

and $V = (kT/q) \ln (I/I_0)$

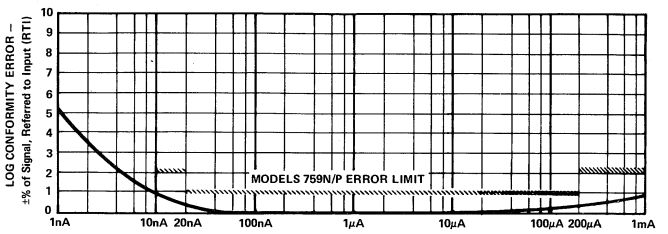
where I is the collector current, I_0 is the extrapolated current for V = 0, V is the base-emitter voltage, q/k (11605° K/V) is the ratio of charge of an electron to Boltzmann's constant, and T is junction temperature kelvin. In log/antilog devices, two matched transistors are connected so as to subtract the junction voltages associated with the input and reference currents, making the ratio independent of I_0's variation with temperature.

$$\begin{aligned}\Delta V &= (kT/q) \ln (I_{in}/I_o) - (kT/q) \ln (I_{ref}/I_o) \\ &= (kT/q) (\ln I_{in} - \ln I_{ref}) + (kT/q) (\ln I_o - \ln I_o) \\ &= (kT/q) \ln (I_{in}/I_{ref})\end{aligned}$$

The temperature-dependence of gain is compensated for by a resistive attenuator that uses a temperature-sensitive resistor for compensation. The attenuator also produces amplification of K to the specified nominal values, e.g., from the basic 59mV/decade (kT/q) ln10 at room temperature) to 1V/decade.

Errors are introduced by the offset current of the amplifier, and the offset voltage, for voltage inputs; by inaccuracy of the reference current (or the effective reference voltage, for voltage inputs) in fixed-reference devices; and by inaccuracy of setting K. Additional errors are introduced by drift of these parameters with temperature. At any temperature, if these parameters are nulled out, there remains a final irreducible difference between the actual output and the theoretical output, called *log-conformity error*, which is manifested as a "nonlinearity" of the input-output plot on semilog paper. Best log conformity is realized away from the extremities of the rated signal

range. For example, log-conformity error of model 755 is ±1% maximum, referred to the input, over the entire 6-decade range from 1nA to 1mA; but it is only ±0.5% maximum over the 4-decade range from 10nA to 100μA. A plot of log conformity error for model 759 is shown here.



Log Conformity Error for Models 759N and 759P

Errors occurring at the input, and log-conformity errors, can only be observed at the output, but it is useful to refer them to the input (RTI). Equal percentage errors at the input, at whatever input level, produce equal incremental errors at the output, for a given value of K. For example, if K = 1, and the RTI log-conformity error is +1%, the magnitude of the output error will be

$$\begin{aligned}\text{Error} &= \text{Actual output} - \text{ideal output}\\ &= 1V\cdot\log(1.01\, I/I_{ref}) - 1V\cdot\log(I/I_{ref})\\ &= 1V\cdot\log 1.01 = 0.0043V = 4.3mV\end{aligned}$$

If, in this example, the input range happens to be 5 decades, the corresponding output range will be 5 volts, and the 4.3mV log-conformity error, as a percentage of total *output* range, will be less than 0.1%. Because this ambiguity can prove confusing to the user, it is important that a manufacturer specify whether the error is referred to the input or the output. The table below indicates the conversion between RTI percentage and output error-magnitudes, for various percent errors, and various values of K.

LOG OUTPUT ERROR (mV)

% ERROR RTI	K = 1V	K = 2V	K = (2/3)V
0.1	0.43	0.86	0.28
0.5	2.2	4.3	1.4
1.0	4.3	8.6	2.9
2.0	8.6	17.	5.7
3.0	13.	26.	8.6
4.0	17.	34.	11.
5.0	21.	42.	14.
10.0	41.	83.	28.

For antilog operations, input and output errors are interchanged.

To arrive at the total error, an error budget should be made up, taking into account each of the error sources, and its contribution to the total error, over the temperature range of interest.

Dynamic response of log amps is a function of the input level. Small-signal bandwidths of ac input signals biased at currents above 1μA tend to be roughly comparable. However, below 1μA, bandwidth tends to be in rough proportion to current level. Similarly, rise time depends on step magnitude and direction – step changes in the direction of increasing current are responded to more quickly than step decreases of current.

DEFINITIONS OF SPECIFICATIONS

Log-Conformity Error When the parameters have been adjusted to compensate for offset, scale-factor, and reference errors, the *log-conformity error* is the deviation of the resulting function from a straight line on a semilog plot over the range of interest.

Offset Current (I_{os}) is the bias current of the amplifier, plus any stray leakage currents. This parameter can be a significant source of error when processing signals in the nanoampere region. Its contribution in antilog operation is negligible.

Offset Voltage (E_{os}) depends on the operational amplifier used for the log operation. Its effect is that of a small voltage in series with the input resistor. For current-logging operations, with high-impedance sources, its error contribution is negligible. However, for voltage logging, it modifies the value of V_{in}. Though it can be adjusted to zero at room temperature, its drift over the temperature range should be considered. In antilog operation, E_{os} appears at the output as an essentially constant voltage; its percentage effect on error is greatest for small outputs.

Reference Current (I_{ref}) is the effective internally-generated current-source output to which all values of input current are compared. I_{ref} tolerance appears as a dc offset at the output; it can be adjusted towards zero by adjusting the reference current, adding a voltage to the output by injecting a current into the scale-factor attenuator, or simply by adding a constant bias at the output's destination.

Reference Voltage (E_{ref}) is the effective internally generated voltage to which all input voltages are compared. It is related to I_{ref} by the equation: $E_{ref} = I_{ref}R_{in}$, where R_{in} is the value of input resistance. Typically, I_{ref} is less stable than R_{in}; therefore, practically all the tolerance is due to I_{ref}.

Scale Factor (K) is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope (on a semilog plot), and is specified in percent of the nominal value.

Selection Guide
Logarithmic Amplifiers

MODEL	CHARACTERISTICS	PAGE
Model 755N/P Log-antilog amplifier	High performance: ±1% max log-conformity error for 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V), and 0.5% max conformity error for 4 decades of current (10nA to 100μA) and 3 decades of voltage (1mV to 1V), 1.5″ x 1.5″ x 0.4″ module. Antilog output range: 4 decades, 1mV to 10V, K = 1, 2, 2/3 V/decade, I_{ref} = 10μA (externally adjustable).	213
Model 759N/P Log-antilog amplifier	Small size and low cost: 1.13″ x 1.13″ x 0.4″ module, wide bandwidth 200kHz @ 1μA, ±2% max log-conformity error for 5 decades of current (10nA to 1mA) or 4 decades of voltage (1.0mV to 10V), and ±1% max conformity error for 4 decades of current (20nA to 200μA). Log operating range: 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V). Antilog output range: 4 decades (1mV to 10V), K = 1, 2, 2/3 V/decade, I_{ref} = 10μA (externally adjustable).	221
Model 757N/P Log-ratio module	Input dynamic range, 6 decades of current (1nA to 1mA), either channel, log conformity error ±1.0% max; for 4 decades (10nA to 100μA), log conformity error ±0.5% max. Log of voltage by using external resistors. K = 1 V/decade, ±1%, max, or externally programmable. Can be used for antilog operations.	217

NOTE:
The Complete log devices listed above and catalogued in this section are recommended for new designs. Model 752 log transconductor and model 751 basic log element, popular early devices for assembly in log circuits by the user, are still available. Data sheets will be provided upon request.

6-Decade, High Accuracy Log, Antilog Amplifiers

MODELS 755N, 755P

FEATURES

Complete Log/Antilog Amplifier
- **External Components Not Required; Internal Reference; Temperature Compensated**

6 Decades Current Operation — 1nA to 1mA
- **1/2% max Error — 10nA to 100μA**
- **1% max Error — 1nA to 1mA**

4 Decades Voltage Operation — 1mV to 10V
- **1/2% max Error — 1mV to 1V**
- **1% max Error — 1mV to 10V**

APPLICATIONS

Log Current or Voltage
Antilog Voltage
Data Compression or Expansion
Absorbence Measurements
Computing Powers and Log Ratios

GENERAL DESCRIPTION

Model 755 is a complete dc logarithmic amplifier consisting of an accurate temperature compensated antilog element, and a low bias current FET amplifier. In addition to offering 120dB of current logging (1nA to 1mA) and 80dB of voltage logging (1mV to 10V), the 755 features exceptionally low bias currents of 10pA and 15μV/°C voltage drift to satisfy most wide range applications. Conformance to ideal log operation is held to ±1% over its total 120dB current range (1nA to 1mA), with ±0.5% conformity guaranteed over an 80dB range (10nA to 100μA). Two models are available, model 755N and model 755P. The N version computes the log of positive input signals and the P version computes the log of negative input signals.

Advanced design techniques and improved component selection are used to obtain exceptionally good performance. For example, the use of monolithic devices greatly reduces the influence of temperature variations. Offering both log and antilog operation, model 755's price and performance are especially attractive as an alternative to in-house designs of OEM applications. This log design also improves significantly over competitive designs in price, performance, and package size.

MAJOR IMPROVEMENTS IN I_{OS}

For most low level applications, the input bias current I_{OS}, is especially critical, since it is the major source of error when processing low level currents. At 1nA of input current there is an error contribution of 1% for every 10pA of I_{OS}. Recognizing the importance of this parameter, bias current of model 755 is maintained below 10pA.

APPLICATIONS

When connected in the current or voltage logging configuration, as shown in Figure 1, the model 755 may be used in several key applications. A plot of input current versus output voltage is also presented to illustrate the log amplifier's transfer characteristics.

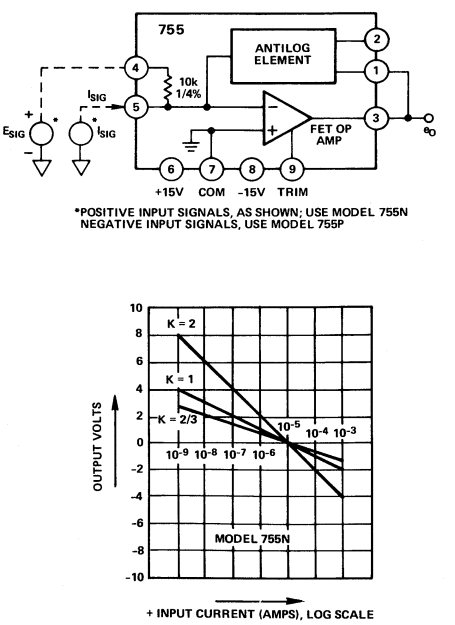


Figure 1. Functional Block Diagram and Transfer Function

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	755N/P
TRANSFER FUNCTIONS	
Current Mode	$e_O = -K\log_{10}\frac{I_{SIG}}{I_{REF}}$
Voltage Mode	$e_O = -K\log_{10}\frac{E_{SIG}}{E_{REF}}$
Antilog Mode	$e_O = E_{REF}\ 10^{-\left(\frac{E_{SIG}}{K}\right)}$
TRANSFER FUNCTION PARAMETERS	
Scale Factor (K) Selections[1, 2]	2, 1, 2/3 Volt/Decade
Error @ +25°C	±1% max
vs. Temperature (0 to +70°C)	±0.04%/°C max
Reference Voltage (E_{REF})[2]	0.1V
Error @ +25°C	±3% max
vs. Temperature (0 to +70°C)	±0.1%/°C max
Reference Current (I_{REF})[2]	10μA
Error @ +25°C	±3% max
vs. Temperature (0 to +70°C)	±0.1%/°C max

LOG CONFORMITY ERROR

I_{SIG} Range	E_{SIG} Range	R.T.I.	R.T.O. (K = 1)
1nA to 10nA	–	±1% max	±4.3mV max
10nA to 100μA	1mV to 1V	±0.5% max	±2.17mV max
100μA to 1mA	1V to 10V	±1% max	±4.3mV max
1nA to 1mA	–	±1% max	±4.3mV max

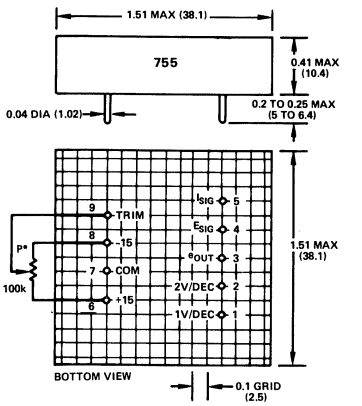
INPUT SPECIFICATIONS	
Current Signal Range	
Model 755N	+1nA to +1mA min
Model 755P	−1nA to −1mA min
Max Safe Input Current	±10mA max
Bias Current @ +25°C	(0, +) 10pA max
vs. Temperature (0 to +70°C)	x2/+10°C
Voltage Signal Range (Log Mode)	
Model 755N	+1mV to +10V min
Model 755P	−1mV to −10V min
Voltage Signal Range, Antilog Mode Model 755N, 755P	$-2 \leqslant \frac{E_{SIG}}{K} \leqslant 2$
Offset Voltage @ +25°C (Adjustable to 0)	±400μV max
vs. Temperature (0 to +70°C)	±15μV/°C max
vs. Supply Voltage	±15μV/%
FREQUENCY RESPONSE, Sinewave	
Small Signal Bandwidth, −3dB	
I_{SIG} = 1nA	80Hz
I_{SIG} = 1μA	10kHz
I_{SIG} = 10μA	40kHz
I_{SIG} = 1mA	100kHz
RISE TIME	
Increasing Input Current	
10nA to 100nA	100μs
100nA to 1μA	7μs
1μA to 1mA	4μs
Decreasing Input Current	
1mA to 1μA	7μs
1μA to 100nA	30μs
100nA to 10nA	400μs
INPUT NOISE	
Voltage, 10Hz to 10kHz	2μV rms
Current, 10Hz to 10kHz	2pA rms
OUTPUT SPECIFICATIONS[3]	
Rated Output	
Voltage	±10V min
Current	
Log Mode	±5mA
Antilog Mode	±4mA
Resistance	0.5Ω
POWER SUPPLY	
Rated Performance	±15V dc
Operating	±(12 to 18)V dc
Current, Quiescent	±7mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	−25°C to +85°C
Storage	−55°C to +125°C
CASE SIZE	1.5" x 1.5" x 0.4"

[1] Use terminal 1 for K = 1V/decade; terminal 2 for K = 2V/decade; terminals 1 or 2 (shorted together) for K = 2/3V/decade.
[2] Specification is + for model 755N; - for model 755P.
[3] No damage due to any pin being shorted to ground.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



*Optional 100kΩ external trim pot – ADI PN79PR100k. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim terminal 9 left open, input offset voltage will be ±0.4mV maximum.

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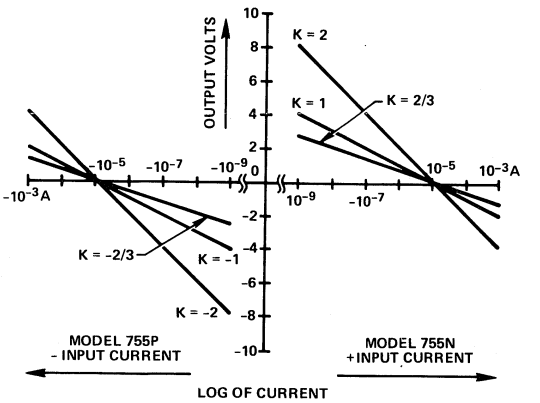
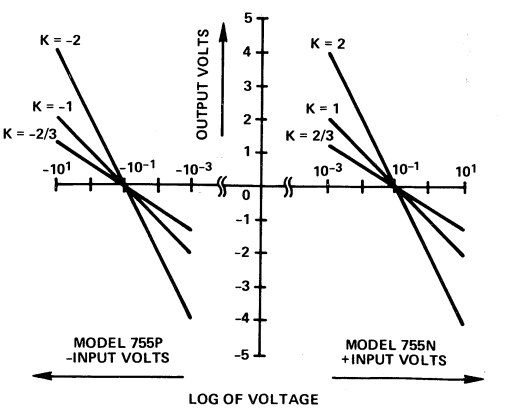
TRANSFER CURVES



Plot of Output Voltage vs Input Current for Model 755 Connected in the Log Mode



Plot of Output Voltage vs Input Voltage for Model 755 Connected in the Log Mode

PRINCIPLE OF OPERATION

Log operation is obtained by placing the antilog element in the feedback loop of the op amp as shown in Figure 1. At the summing junction, terminal 5, the input signal current to be processed is summed with the output current of the antilog element. To attain a balance of these two currents, the op amp provides the required output voltage to the antilog feedback element. Under these conditions the ideal transfer equation (K = 1) is:

$$e_{OUT} = 1V \log_{10} I_{SIG}/I_{REF}$$

The log is a mathematical operator which is defined only for numbers, which are dimensionless quantities. Since an input current would have the dimensions of amperes it must be referenced to another current, I_{REF}, the ratio being dimensionless. For this purpose a temperature compensated reference of 10μA is generated internally.

The scale factor, K, is a multiplying constant. For a change in input current of one decade (decade = ratio of 10:1), the output changes by K volts. K may be selected as 1V or 2V by connecting the output to pin 1 or 2, respectively. If the output is connected to both pins 1 and 2, K will be 2/3V.

A graph of the ideal transfer function for model 755N is presented in Figure 2, for one decade of operation. Although specific values of i_{in} and e_{out} are presented for n = 1, other values may be plotted by varying n.

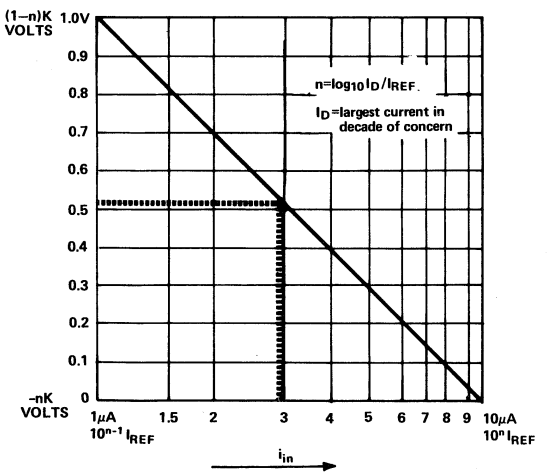


Figure 2. Input vs. Output for Any One Decade of Operation

REFERRING ERRORS TO INPUT

A unique property of log amplifiers is that a dc error of any given amount at the output corresponds to a constant percent of the input, regardless of input level. To illustrate this, consider the output effects due to changing the input by 1%.

The output would be:

$$e_{out} = 1V \log_{10} (I_{SIG}/I_{REF})(1.01) \text{ which is equivalent to:}$$

$$e_{out} = \underbrace{1V \log_{10} I_{SIG}/I_{REF}}_{\text{Initial Value}} \quad \underbrace{\pm 1V \log_{10} 1.01}_{\text{Change}}$$

The change in output, due to a 1% input change is a constant value of ±4.3mV. Conversely, a dc error at the output of ±4.3mV is equivalent to a change at the input of 1%. An abbreviated table is presented below for converting between errors referred to output (R.T.O.), and errors referred to input (R.T.I.).

TABLE 1

Error R.T.I. (N)	Error R.T.O. K = 1	K = 2	K = 2/3
0.1%	0.43mV	0.86mV	0.28mV
0.5	2.17	4.34	1.45
1.0	4.32	8.64	2.88
3.0	12.84	25.68	8.56
4.0	17.03	34.06	11.35
5.0	21.19	42.38	14.13
10.0	41.39	82.78	27.59

Table 1. Converting Output Error in mV to Input Error in %

NOTE:
Data may be interpolated with reasonable accuracy, for small errors by adding various values of N and their corresponding R.T.O. terms. That is, for N = 2.5% and K = 1, combine 2% and 0.5% terms to obtain 10.77mV.

SOURCES OF ERROR

When applying the model 755, a firm understanding of error sources associated with log amplifiers is beneficial for achieving maximum performance. The definitions, limitations and compensation techniques for errors specified on log amplifiers will be discussed here.

Log Conformity Error – Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the value of the transfer equation and the actual value which occurs at the output of the log module, after scale factor, reference and offset errors are eliminated or taken into account. For model 755, the best linearity performance is obtained in the middle 4 decades (10nA to 100μA). For this range, log conformity error is ±0.5% R.T.I. or 2.17mV R.T.O. To obtain optimum performance, the input data should be scaled to this range.

Offset Voltage (E_{OS}) – The offset voltage, E_{OS}, of model 755 is the offset voltage of the internal FET amplifier. This voltage appears as a small dc offset voltage in series with the input terminals. For current logging applications, its error contribution is negligible. However, for log voltage applications, best performance is obtained by an offset trim adjustment.

Offset Current (I_{OS}) – The offset current, I_{OS}, of model 755 is the bias current of the internal FET amplifier. This parameter can be a significant source of error when processing signals in the nanoamp region. For this reason, I_{OS}, for model 755, is held within a conservative 10pA max.

Reference Current (I_{REF}) – I_{REF} is the internally generated current source to which all input currents are compared. I_{REF} tolerance errors appear as a dc offset at the output. The specified value of I_{REF} is ±3%, referred to the input, and, from Table 1, corresponds to a dc offset of ±12.84mV, for K = 1. This offset is independent of input signal and may be removed by injecting a current into terminal 1 or 2.

Reference Voltage (E_{REF}) – E_{REF} is the effective internally generated voltage to which all input voltages are compared. It is related to I_{REF} through the equation: $E_{REF} = I_{REF} \times R_{in}$, where R_{in} is an internal 10kΩ, precision resistor. Virtually all tolerance in E_{REF} is due to I_{REF}. Consequently, variations in I_{REF} cause a shift in E_{REF}.

Scale Factor (K) – Scale factor is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope, and is specified in per cent of the nominal value. An external adjustment may be performed if fine trimming is desired for improved accuracy.

EXTERNAL ADJUSTMENTS FOR LOG OPERATION (OPTIONAL)

Trimming E_{OS} – The amplifier's offset voltage, E_{OS}, may be trimmed for improved accuracy with the model 755 connected in its log circuit. To accomplish this, a 100kΩ, 10 turn pot is connected as shown in Figure 3, and the input terminal, pin 4, is connected to ground. Under these conditions the output voltage is:

$$e_{out} = -K \log_{10} E_{os}/E_{REF}$$

To obtain an offset voltage of 100μV or less, for K = 1, the trim pot should be adjusted until the output voltage is between +3 and +4 volts for model 755N, and −3 to −4V for model 755P.

For other values of K, the trim pot should be adjusted for an output of e_{out} = 3 x K to 4 x K where K is the scale factor.

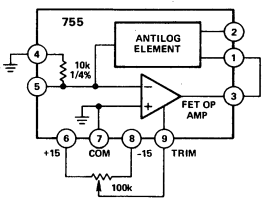


Figure 3. Trimming E_{OS} in Log Mode

REFERENCE CURRENT OR REFERENCE VOLTAGE

The reference current or voltage of model 755 may be shifted by injecting a constant current into the unused scale factor terminal (pin 1 or pin 2). Each 66μA of current injected will shift the reference one decade, in accordance with the expression: $I_I = 66\mu A \log 10\mu A/I_{REF}$, where I_I = current to be injected and I_{REF} = the desired reference current.

By changing I_{REF}, there is a corresponding change in E_{REF} since, $E_{REF} = I_{REF} \times R_{in}$. An alternate method for rescaling E_{REF} is to connect an external R_{in}, at the I_{in} terminal (pin 5) to supplant the 10kΩ supplied internally (leaving it unconnected). The expression for E_{REF} is then, $E_{REF} = R_{in} I_{REF}$. Care must be taken to choose R_{in} such that $(e_{in}\ max)/R_{in} \leqslant 1mA$.

Scale Factor (K) Adjustment – Scale factor may be increased from its nominal value by inserting a series resistor between the output terminal, pin 3, and either terminal 1 or 2. The table below should be consulted when making these scale factor changes.

TABLE 2

Range of K	Connect Series R to Pin	Value of R	Note
2/3V to 1.01V	1	15kΩ x (K − 2/3)	use pins 1, 2
1.01V to 2.02V	1	15kΩ x (K − 1)	use pin 1
>2.02V	2	15kΩ x (K − 2)	use pin 2

Table 2. Resistor Selection Chart for Shifting Scale Factor

ANTILOG OPERATION

The model 755 may be used to develop the antilog of the input voltage when connected as shown in Figure 4. The antilog transfer function (an exponential), is:

$$e_{out} = E_{REF}\ 10^{-e_{in}/K}$$

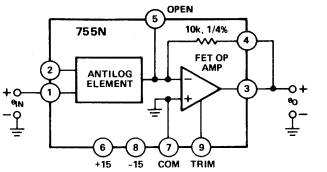


Figure 4. Functional Block Diagram

Principle of Operation – The antilog element converts the voltage input, appearing at terminal 1 or 2, to a current which is proportional to the antilog of the applied voltage. The current-to-voltage conversion is then completed by the feedback resistor in a closed-loop op amp circuit.

A more complete expression for the antilog function is:

$$e_{out} = E_{REF}\ 10^{-e_{in}/K} + E_{OS}$$

The terms K, E_{OS}, and E_{REF} are those described previously in the LOG section.

Offset Voltage (E_{OS}) Adjustment – Although offset voltage of the antilog circuit may be balanced by connecting it in the log mode, and using the technique described previously, it may be more advantageous to use the circuit of Figure 5. In this configuration, offset voltage is equal to $e_{out}/100$. Adjust for the desired null, using the 100k trim pot. After adjusting, turn power off, remove the external 100Ω resistor, and the jumper from pin 1 to +15V. For 755P, use the same procedure but connect pin 1 to −15V.

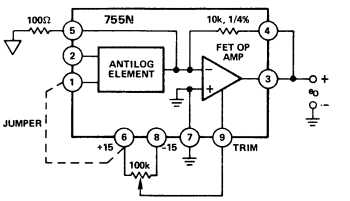


Figure 5. Trimming E_{OS} in Antilog Mode

Reference Voltage (E_{REF}) Adjustment – In antilog operation, the voltage reference appears as a multiplying constant. E_{REF} adjustment may be accomplished by connecting a resistor, R, from pin 5 to pin 3, in place of the internal 10kΩ. The value of R is determined by:

$$R = E_{REF}\ \text{desired}/10^{-5}\ A$$

Scale Factor (K) Adjustment – The scale factor may be adjusted for all values of K greater than 2/3V by the techniques described in the log section. If a value of K, less than 2/3V is desired for a given application, an external op amp would be required as shown in Figure 6. The ratio of the two resistors is approximately:

$$R1/R_G = (1/K - 1) \text{ where K = desired scale factor}$$

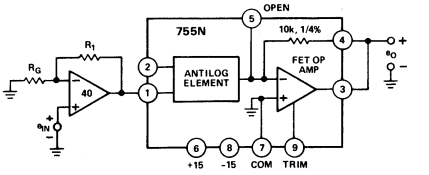


Figure 6. Method for Adjusting K<2/3V

6-Decade, High Accuracy Log Ratio Module

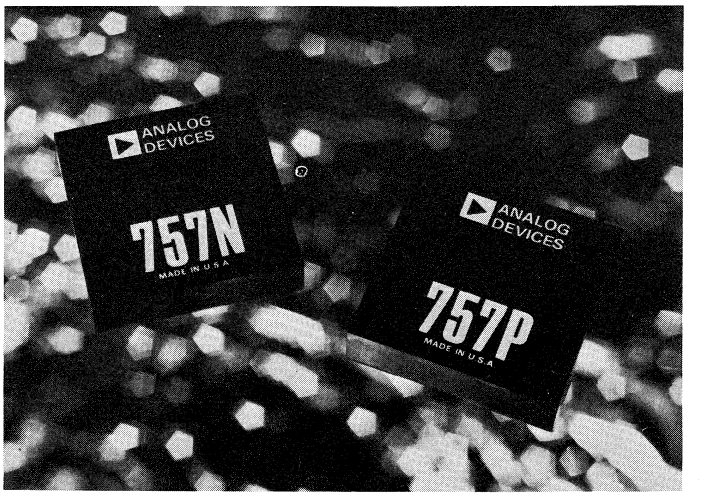
MODELS 757N, 757P

FEATURES

- 6 Decade Operation – 1nA to 1mA
- ½% Log Conformity – 10nA to 100μA
- Symmetrical FET Inputs
- Voltage or Current Operation
- Temperature Compensated
- Antilog Operation

APPLICATIONS

- Absorbance Measurements
- Log/Antilog Ratios of Voltages or Currents
- Data Compression
- Transducer Linearization



GENERAL DESCRIPTION

Model 757 is a complete, temperature compensated, dc-coupled log ratio module. It is comprised of two input channels for processing signals spanning up to 6 decades in dynamic range (1nA to 1mA). By virtue of its symmetrical FET input stages, the 757 can accommodate this 6 decade signal range at either channel. Log conformity is maintained to within ½% over 4 decades of input (10nA to 100μA) and to within 1% over the full input range. Unlike other log ratio designs, model 757 does not restrict the relative magnitude of the two signal inputs to achieve rated performance. Either input can be operated within the specified range regardless of the signal level at the other channel.

The model 757 log-ratio module design makes available both input amplifier summing junctions. As a result, it can directly interface with photo diodes operating in the short-circuit current mode without the need of additional input circuitry.

The excellent performance of model 757 can be further improved by means of external scale factor and output offset adjustments. A significant feature of model 757 not found on competing devices is that, when the offset adjustment is used to establish a fixed bias at the output, the output offset level does not vary as a function of input signal magnitude. On other designs, the sensitivity of output offset to input levels results in output effects resembling log conformity errors.

Model 757 can operate with either current or voltage inputs. Its excellent performance makes it ideally suited for log ratio applications such as blood analysis, chromatography, chemical analysis of liquids and absorbance measurements.

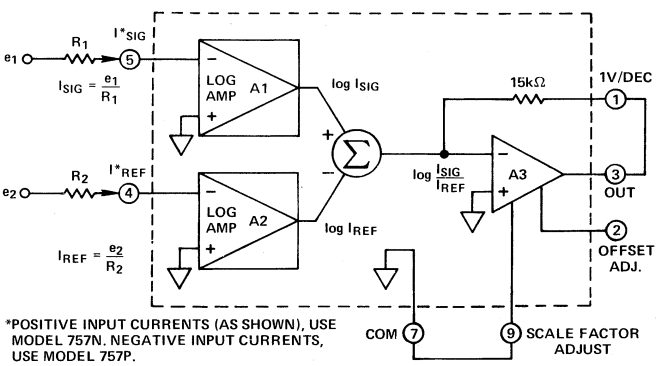


Figure 1. Functional Block Diagram of Model 757

CURRENT LOG RATIO

Current log ratio is accomplished by model 757 when two currents, I_{SIG} and I_{REF}, are applied directly to the input terminals (see Figure 1). The two log amps process these signals providing voltages which are proportional to the log of their respective inputs. These voltages are then subtracted and applied to an output amplifier. The scale factor, when connected as shown, is 1V/dec. However, higher scale factors may be achieved by connecting external scale factor adjusting resistors. (See section on optional adjustments and trims.)

VOLTAGE LOG RATIO

The principle of operation for voltage log ratio is identical to that of current log ratio after the voltage signal has been converted to a current. To accomplish this conversion, an external

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	757N/P
TRANSFER FUNCTION [1]	
Current Mode	$e_O = -K \log_{10} \frac{I_{SIG}}{I_{REF}}$
Voltage Mode	$e_O = -K \log_{10} \left[\frac{e_1}{e_2} \times \frac{R_2}{R_1}\right]$
ACCURACY	
Log Conformity [2]	
I_{SIG}, I_{REF} = 10nA to 100μA	±0.5%, max
I_{SIG}, I_{REF} = 1nA to 1mA	±1%, max
Scale Factor (1V/Dec)	(+0, -2%) max
vs. Temperature (0 to +70°C)	±0.04%/°C max
INPUT SPECIFICATIONS — Both Input Channels	
Current	
Signal Range, Rated Performance	
Model 757N	+1nA to +1mA
Model 757P	-1nA to -1mA
Max Safe	±10mA
Bias Current, @ +25°C	-10pA
vs. Temperature (0 to +70°C)	x2/+10°C
Offset Voltage, @ +25°C	±1mV max
vs. Temperature (0 to +70°C)	
I_{SIG} Channel	±25μV/°C max
I_{REF} Channel	±85μV/°C max
vs. Supply Voltage	±5μV/%
FREQUENCY RESPONSE, Sinewave	
Small Signal Response (-3dB)	
Signal Channel	
I_{SIG} = 1nA	300Hz
I_{SIG} = 1μA	25kHz
I_{SIG} = 100μA	50kHz
Reference Channel	
I_{REF} = 1nA	3kHz
I_{REF} = 1μA	25kHz
I_{REF} = 100μA	50kHz

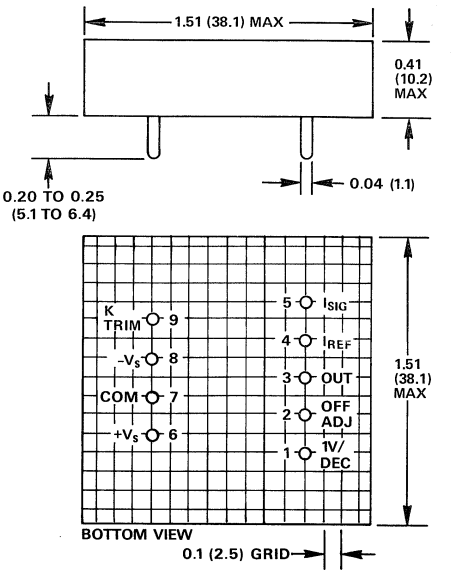
RISE TIME	Signal Channel (I_{REF} = 10μA)	Reference Channel (I_{SIG} = 10μA)
Increasing Input Current		
1nA to 10nA	250μs	80μs
10nA to 100nA	50μs	40μs
100nA to 1μA	30μs	30μs
1μA to 100μA	25μs	25μs
Decreasing Input Current		
100μA to 1μA	25μs	25μs
1μA to 100nA	30μs	30μs
100nA to 10nA	100μs	40μs
10nA to 1nA	600μs	70μs

INPUT NOISE	
Voltage (10Hz to 10kHz)	3μV rms
Current (10Hz to 10kHz)	0.1pA rms
OUTPUT SPECIFICATIONS	
Rated Output	
Voltage	±10V min
Current	
Log Mode	±5mA, min
Antilog Mode	±4mA, min
Resistance	0.1Ω
Offset Voltage [3] (K = 1V/Decade)	±10mV max
vs. Temperature (0 to +70°C)	±0.3mV/°C
vs. Supply	±5μV/V
POWER SUPPLY [4]	
Rated Performance	±15V dc
Operating	±(12 to 18)V dc
Current, Quiescent	±8mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C
MECHANICAL	
Case Size	1.5" x 1.5" x 0.4"
Mating Socket	AC1048
Weight	21 grams

[1] For model 757N, K = +1V/Decade and input currents must be positive. For model 757P, K = -1V/Decade and input currents must be negative. (Input currents are defined as positive when flowing into the input terminals, 4 and 5. Refer to TRANSFER CURVES.)
[2] The log conformity error is referred to input (RTI). 1% error RTI is equivalent to 4.3mV of error at the output for K = 1V/Dec.
[3] Externally adjustable to zero.
[4] Recommended power supply: Analog Devices model 904, ±15V @ 50mA.
Specifications subject to change without notice.

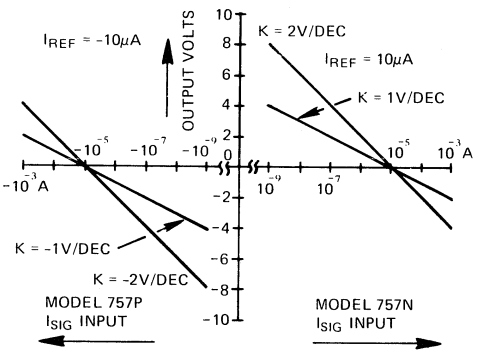
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Mating Socket AC1048

TRANSFER CURVES



Log mode output voltage vs. input current for I_{REF} = 10μA. For voltage input calculate I_{SIG} as e_1/R_1 (see Figure 1).

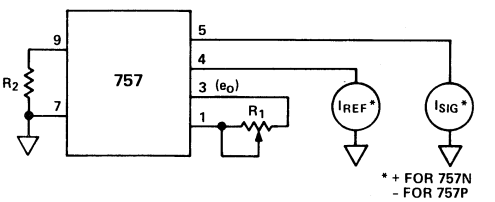


Figure 2. Scale Factor Adjustment

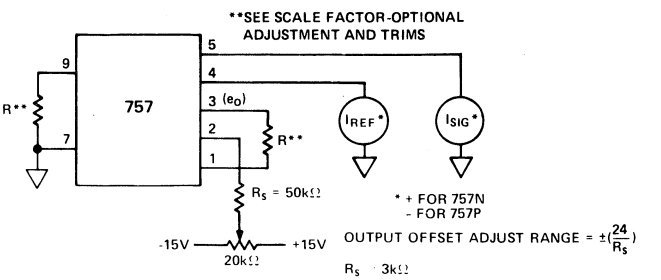


Figure 3. Output Voltage Offset Adjustments

resistor is attached from the voltage signal to the appropriate input current terminal of the 757. Input currents are then determined by:

$$I_{SIG} = \frac{e_1}{R_1}, I_{REF} = \frac{e_2}{R_2}$$

OPTIONAL ADJUSTMENTS AND TRIMS

Scale Factor – A one volt per decade scale factor is available when pin 1 is tied to 3 and pin 7 is connected to 9. Higher scale factors are possible by using a potentiometer, R_1, between pins 1 and 3 and a resistor, R_2, between pins 7 to 9 as shown in Figure 2. The value of the required resistor is (15kΩ) (K-1) where K is the desired scale factor. The approximate potentiometer value is also (15kΩ) (K-1). The scale factor adjustment procedure is as follows:

1. Connect the appropriate value of resistor between pins 7 and 9.
2. Set I_{REF} = 1μA, I_{SIG} = 10μA. Measure e_o.
3. Set I_{REF} = 1μA, I_{SIG} = 100μA. Adjust R_1 until the difference in e_o corresponding to steps 2 and 3 is K volts.
4. Repeat steps 2 and 3 until the change in e_o = K volts.

Output Voltage Offset – Output voltage offset must be adjusted after the desired scale factor is established as indicated above. To adjust the offset, inject equal dc input currents into the reference and signal channels. The value of the input currents should approximate the average input current levels expected to be encountered in normal operation. Adjust the potentiometer shown in Figure 3 until the output voltage is zero.

INTERCHANGEABILITY WITH MODEL 756

Model 757 is a functional, pin compatible replacement for model 756 in applications that do not require external trims. The user need only short pin 7 to pin 9 in order to establish a scale factor of 1V/decade. In applications requiring external adjustments, the scale factor and offset trims should be configured to the model 757 requirements as outlined above.

LOG CONFORMITY

Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the theoretical value of the log of a ratio and the actual value that appears at the output of the log-ratio module after scale factor errors have been eliminated. Measurement of this error is made after initially zeroing the module at unity-ratio and adjusting the desired scale factor.

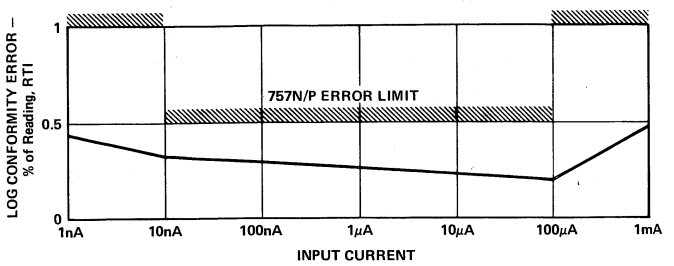


Figure 4. Log Conformity Error for Model 757. Curve is for Either Input Channel with Current Held Constant at 10μA On Other Channel

Figure 4 shows the log conformity performance of model 757 over a 6 decade input range. Log conformity for each channel does not vary noticeably as the current is varied in the other channel.

FREQUENCY CHARACTERISTICS

Figure 5 shows a plot of small signal response (-3dB) as a function of input signal current. The graph demonstrates the frequency response performance for each input channel over the range of 1nA to 1mA, independent of current on the other channel.

As shown in the graph, the reference channel is faster than the signal channel at low input levels. If an application requires higher speed in the input signal channel than in the reference channel, then the channels can be interchanged with a resulting polarity reversal of the output signal

$$(\log \frac{I_{SIG}}{I_{REF}} = \log I_{SIG} - \log I_{REF} = -\log \frac{I_{REF}}{I_{SIG}}).$$

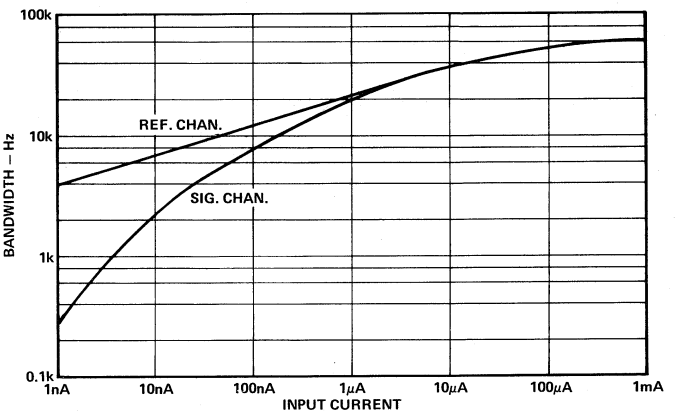


Figure 5. Small Signal Bandwidth (-3dB) vs. Input Signal Level

OUTPUT OFFSET VOLTAGE DRIFT

The curves of Figure 6 illustrate the output offset voltage changes over the operating temperature range of 0 to +70°C, at K = 1V/decade. Since output offset voltage changes are minimum at +25°C, best accuracy operation is obtained over the range of +25°C ±20°C.

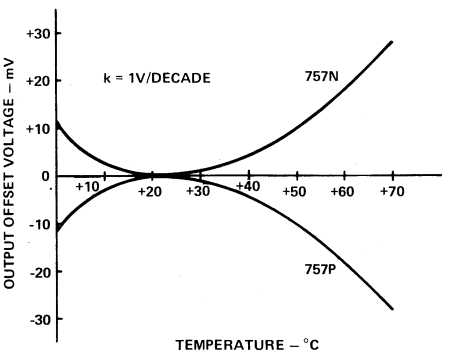


Figure 6. Output Offset Voltage vs. Temperature

ANTILOG OPERATION

The antilogarithm is the inverse of the logarithm. It is by definition the exponential in which the logarithmic base (B) is raised to a power (Y). That is,

$$X = \log^{-1}_B (Y) = B^Y$$

The model 757 log ratio module with the transfer function

$$E_O = -K \log_{10} \frac{E_{SIG}}{E_{REF}} \quad (R_1 = R_2)$$

can be connected as shown in Figure 7 to compute

$$E_O = E_{REF} \times 10^{(E_{SIG}/-K)}$$

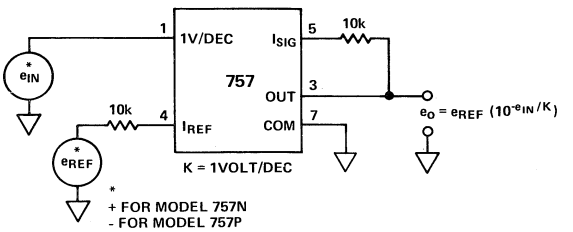


Figure 7. Model 757 Antilog Connection

Thus, when K = 1, the log ratio operation provides an output of 1 volt per decade of input ratio, while the antilog mode yields an output that changes 1 decade per volt of input.

In antilog operation, E_{REF} is the normalized value of the exponential and each volt of increase of the input multiplies E_{REF} by an additional factor of 10.

Exponential devices can be used when:

1. Compound multiplications involving roots and powers are performed.
2. Devices with logarithmic responses must be linearized.
3. Function fitting and generation is required to obtain relationships or generate curves having voltage-programmable rates of growth or decay. (e.g. if E_{SIG} is a ramp, E_O will be a widely varying exponential function of time that can be further modified by varying E_{REF} and K).

APPLICATIONS

Data Compression – Processing signals with wide dynamic range is a common problem in instrumentation and data transmission. For example, digitizing an analog signal with a range of 10nA to 100μA with 1% accuracy requires a 20 bit A/D converter. (Required resolution = 1/100 x 1/10,000 = $1/10^6 \cong 1/2^{20}$).

By using the 757 with I_{REF} adjusted to 10nA and K set for 5/4 V/decade, the input data can be compressed into a 5 volt output range. For a 1% resolution of any signal, the allowable output error is 4.32mV x K. Log conformity contributes 2.17mV x K (0.5%) over this range. The remaining error with K = 5/4 is 2.69mV and should correspond to less than the LSB of the converter. With a 5 volt output range 2.69mV corresponds just over the LSB of an 11-bit converter. Thus the 757 module can compress the data for use with a 12 bit A/D (such as Analog Devices ADC-12QZ) to obtain the desired 1% resolution.

Absorbance Measurements – Critical properties of materials, which are of particular interest in the fields of chemistry, medicine, spectrometry and pollution control are characterized by absorbance. The relationship between absorbance, A, and light intensity, I, is: $A = \log I_O/I_T$ where I_O = intensity of incident light, and I_T = intensity of transmitted light.

Figure 8 shows the 757 log-ratio module used in such a photometer application. Two inputs represent the intensities of light transmitted through space and through a medium that absorbs light. The absorbance of the medium is given by the formula

$$A = \log \frac{I_{SIGNAL}}{I_{REFERENCE}}$$

where I_{SIGNAL} and $I_{REFERENCE}$ are the currents representing the light intensities.

The transducers used in this application are photodiodes, which provide a short-circuit current proportional to the intensity of applied light. The lowest value of absorbance is determined by the value of I_{REF}, since when $I_{SIG} = I_{REF}$, A = 0. The output of the log-ratio module is externally trimmed to 1V/decade and applied to the input of a 3½-digit DPM through the scaling network R1 and R2.

Model 757 was chosen for this design because it makes available both amplifier summing junctions. When the photodiodes are connected to the summing junctions, they are operated in the short-circuit mode, that is, with zero volts across the diodes. Short-circuit loading is necessary, because accuracy of the photodiodes can be degraded several percent when operated with as little as 100mV across the diode junction.

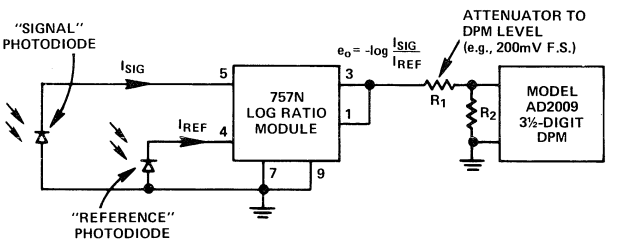


Figure 8. Model 757N Applied to Absorbance Measurements

INTERCONNECTION GUIDELINES

Model 757 is a complete log ratio module that requires no additional frequency compensation for proper operation.

Input Capacitance – Model 757 is able to operate with 1000pF at both input terminals. Therefore, the 757 can be used in applications requiring long cable lengths between the module and the signal transducers.

Input-to-Output Capacitance – When using a log ratio module the user should take care in system configurations to avoid excessive stray capacitance between input and output terminals. Such precautions include avoiding running input and output signal lines close together. If long cable runs are required where inputs and output are closely bundled together, it is advisable to enclose the inputs and/or output in separate, grounded electrostatic shields. By observing simple rules of good circuit layout, problems with oscillations that may result from excessive input-to-output capacitance can easily be avoided. Model 757 can accommodate up to 150pF of input-to-output capacitance without oscillation.

Leakage Resistance – Since model 757 can operate at extremely low input current levels, precautions must be taken to prevent current leakage into the input terminals. Such leakage can cause errors when small input or reference currents are used. This problem may arise on printed circuit layouts if the inputs are run too close to the power supply busses. Providing an etched guard around the input lines, connected to analog signal ground will also reduce unwanted current leakage.

Economy, Wideband Log/Antilog Amplifiers

MODELS 759N, 759P

FEATURES

- Low Cost, Complete Log/Antilog Amplifier.
  - External Components Not Required;
  - Internal Reference; Temperature Compensated
- Small Size: 1.1″ x 1.1″ x 0.4″
- Fast Response: 200kHz Bandwidth (I_{SIG} = 1μA)
- 6 Decades Current Operation – 1nA to 1mA
  - 1% max Error – 20nA to 200μA
  - 2% max Error – 10nA to 1mA
- 4 Decades Voltages Operation – 1mV to 10V
  - 1% max Error – 1mV to 2V
  - 2% max Error – 1mV to 10V
- Log Current or Voltage
- Antilog Voltage
- Data Compression or Expansion

GENERAL DESCRIPTION

Models 759N and 759P are low cost, fast response, dc logarithmic amplifiers offering 1% conformance to ideal log operation over four decades of current operation – 20nA to 200μA, as well as 2% conformance over four decades of voltage operation – 1mV to 10V. Featuring 200kHz bandwidth at I_{SIG} = 1μA, these new economy designs are the industry's fastest log/antilog amplifiers and offer an attractive alternative to in-house designs.

Designed for ease of use, models 759N/P are complete, temperature compensated, log or antilog amplifiers packaged in a small 1.1″ x 1.1″ x 0.4″ epoxy encapsulated module. External components are not required for logging currents over the complete six decade operating range from 1nA to 1mA. Both the scale factor (K = 2, 1, 2/3 volt/decade) and log/antilog operation can be selected by simple pin interconnection. In addition both the internal 10μA reference current as well as the offset voltage may be externally adjusted to improve overall accuracy performance.

MODEL SELECTION

Model 759N computes the log of positive input signals (voltage or current), while model 759P computes the log of negative input signals (voltage or current). In the antilog mode of operation, both models accept bipolar voltage input signals ($-2V \leq E_{SIG}/K \leq 2V$), with model 759N producing a positive output signal and model 759P producing a negative output signal.

APPLICATIONS

Model 759N and 759P can operate with either current or voltage inputs when connected as shown in Figure 1. To illustrate the logarithmic transfer characteristics, a plot of input current versus output voltage is also presented. Model 759 is ideally suited for log applications whenever low cost implementation of logarithmic natural relationships is advantages. Examples are absorbence measurements, data compression and expansion, chemical analysis of liquids, computing powers, roots and ratios and conversion of exponential quantities to linear form.

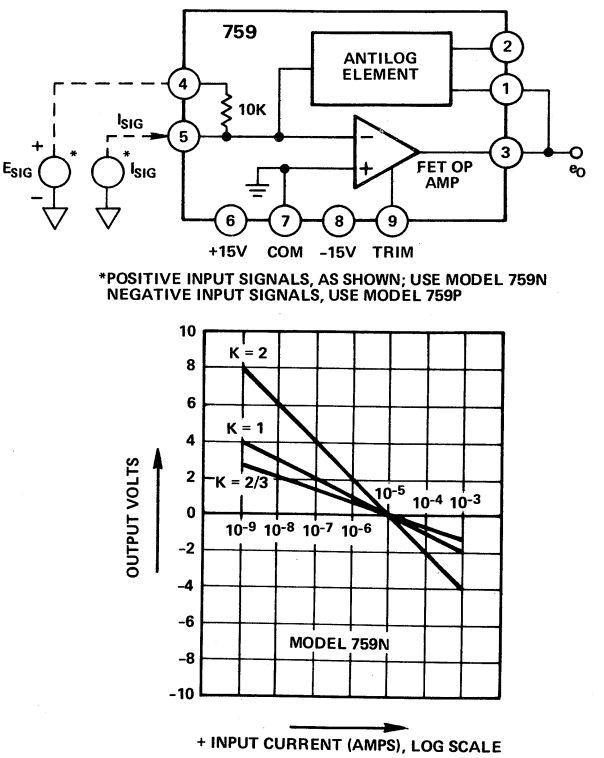


Figure 1. Functional Block Diagram and Transfer Function

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	759N/P
TRANSFER FUNCTIONS	
Current Mode	$e_O = -K\log_{10}\frac{I_{SIG}}{I_{REF}}$
Voltage Mode	$e_O = -K\log_{10}\frac{E_{SIG}}{E_{REF}}$
Antilog Mode	$e_O = E_{REF}\ 10^{-\left(\frac{E_{SIG}}{K}\right)}$
TRANSFER FUNCTION PARAMETERS	
Scale Factor (K) Selections[1, 2]	2, 1, 2/3 Volt/Decade
Error @ +25°C	±1% max
vs. Temperature (0 to +70°C)	±0.04%/°C max
Reference Voltage (E_{REF})[2]	0.1V
Error @ +25°C	±4% max
vs. Temperature (0 to +70°C)	±0.05%/°C
Reference Current (I_{REF})[2]	10μA
Error @ +25°C	±3% max
vs. Temperature (0 to +70°C)	±0.05%/°C

LOG CONFORMITY ERROR			
I_{SIG} Range	E_{SIG} Range	R.T.I.	R.T.O. (K = 1)
20nA to 200μA	1mV to 2V	±1% max	±4.3mV max
10nA to 1mA	1mV to 10V	±2% max	±8.64mV max
1nA to 10nA		±5%	±21mV

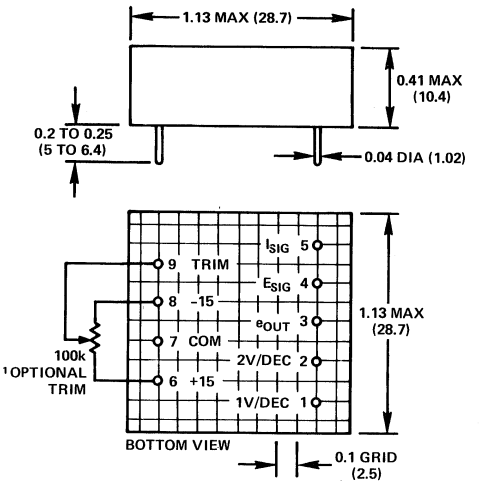
INPUT SPECIFICATIONS	
Current Signal Range	
Model 759N	+1nA to +1mA min
Model 759P	−1nA to −1mA min
Max Safe Input Current	±10mA max
Bias Current @ +25°C	(0, +) 200pA max
vs. Temperature (0 to +70°C)	x2/+10°C
Voltage Signal Range	
Model 759N	+1mV to +10V min
Model 759P	−1mV to −10V min
Offset Voltage @ +25°C (Adjustable to 0)	±2mV max
vs. Temperature (0 to +70°C)	±10μV/°C
vs. Supply Voltage	±15μV/%
FREQUENCY RESPONSE, Sinewave	
Small Signal Bandwidth, −3dB	
I_{SIG} = 1nA	250Hz
I_{SIG} = 10nA	1.8kHz
I_{SIG} = 100nA	25kHz
I_{SIG} = 1μA	200kHz
I_{SIG} = 10μA	300kHz
I_{SIG} = 100μA	300kHz
I_{SIG} = 1mA	300kHz
RISE TIME	
Increasing Input Current	
10nA to 100nA	20μs
100nA to 1μA	3μs
1μA to 100μA	2.5μs
100μA to 1mA	2.5μs
Decreasing Input Current	
1mA to 100μA	3μs
100μA to 1μA	3μs
1μA to 100nA	10μs
100nA to 10nA	80μs
INPUT NOISE	
Voltage, 10Hz to 10kHz	10μV rms
Current, 10Hz to 10kHz	10pA rms
OUTPUT SPECIFICATIONS[3]	
Rated Output	
Voltage	±10V min
Current	
Log Mode	±5mA
Antilog Mode	±4mA
Resistance	0.5Ω
POWER SUPPLY	
Rated Performance	±15V dc
Operating	±(12 to 18)V dc
Current, Quiescent	±4mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	−25°C to +85°C
Storage	−55°C to +125°C
CASE SIZE	1.125" x 1.125" x 0.4"

[1] Use terminal 1 for K = 1V/decade; terminal 2 for K = 2V/decade; terminals 1 and 2 (shorted together) for K = 2/3V/decade.
[2] Specification is + for model 759N; − for model 759P.
[3] No damage due to any pin being shorted to ground.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

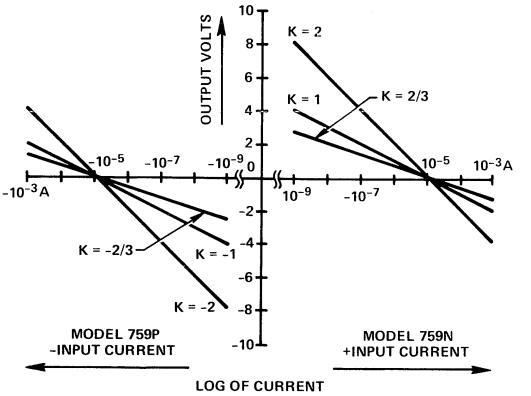
Dimensions shown in inches and (mm).



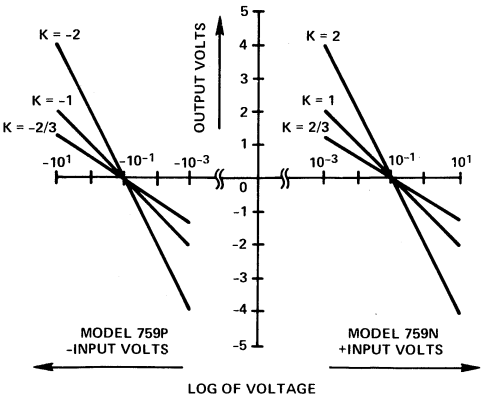
WEIGHT: 10 GRAMS
MATING SOCKET AC1016

[1] Optional 100kΩ external trim pot. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim terminal 9 left open, input offset voltage will be ±2mV maximum.

TRANSFER CURVES



Plot of Output Voltage vs Input Current for Model 759 Connected in the Log Mode



Plot of Output Voltage vs Input Voltage for Model 759 Connected in the Log Mode

PRINCIPLE OF OPERATION

Log operation is obtained by placing the antilog element in the feedback loop of the op amp as shown in Figure 1. At the summing junction, terminal 5, the input signal current to be processed is summed with the output current of the antilog element. To attain a balance of these two currents, the op amp provides the required output voltage to the antilog feedback element. Under these conditions the ideal transfer equation (K = 1) is:

$$e_{OUT} = 1V \log_{10} I_{SIG}/I_{REF}$$

The log is a mathematical operator which is defined only for numbers, which are dimensionless quantities. Since an input current would have the dimensions of amperes it must be referenced to another current, I_{REF}, the ratio being dimensionless. For this purpose a temperature compensated reference of 10μA is generated internally.

The scale factor, K, is a multiplying constant. For a change in input current of one decade (decade = ratio of 10:1), the output changes by K volts. K may be selected as 1V or 2V by connecting the output to pin 1 or 2, respectively. If the output is connected to both pins 1 and 2, K will be 2/3V.

REFERRING ERRORS TO INPUT

A unique property of log amplifiers is that a dc error of any given amount at the output corresponds to a constant percent of the input, regardless of input level. To illustrate this, consider the output effects due to changing the input by 1%.

The output would be:

$$e_{OUT} = 1V \log_{10} (I_{SIG}/I_{REF})(1.01) \text{ which is equivalent to:}$$

$$e_{OUT} = \underbrace{1V \log_{10} (I_{SIG}/I_{REF})}_{\text{Initial Value}} \quad \underbrace{\pm 1V \log_{10} (1.01)}_{\text{Change}}$$

The change in output, due to a 1% input change is a constant value of ±4.3mV. Conversely, a dc error at the output of ±4.3mV is equivalent to a change at the input of 1%. An abbreviated table is presented below for converting between errors referred to output (R.T.O.), and errors referred to input (R.T.I.).

	ERROR R.T.O.		
ERROR R.T.I.	K = 1	K = 2	K = 2/3
0.1%	0.43mV	0.86mV	0.28mV
0.5	2.17	4.34	1.45
1.0	4.32	8.64	2.88
3.0	12.84	25.68	8.56
4.0	17.03	34.06	11.35
5.0	21.19	42.38	14.13
10.0	41.39	82.78	27.59

Table 1. Converting Output Error in mV to Input Error in %

SOURCES OF ERROR

Log Conformity Error — Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the value of the transfer equation and the actual value which occurs at the output of the log module, after scale factor, reference and offset errors are eliminated or taken into account. Figure 2 below illustrates the log conformity performance of model 759 over a 6 decade input range. The best linearity performance is obtained in the 5 decades from 10nA to 1mA. To obtain optimum performance, the input data should be scaled to this range.

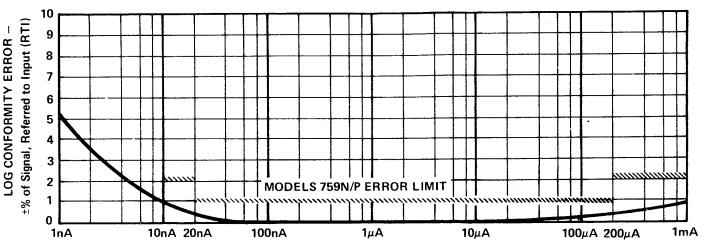


Figure 2. Log Conformity Error for Models 759N and 759P

Offset Voltage — The offset voltage, E_{os}, of model 759 is the offset voltage of the internal FET amplifier. This voltage appears as a small dc offset voltage in series with the input terminals. For current logging applications, its error contribution is negligible. However, for log voltage applications, best performance is obtained by an offset trim adjustment.

Bias Current — The bias current of model 759 is the bias current of the internal FET amplifier. This parameter can be a significant source of error when processing signals in the nanoamp region. For this reason, the bias current for model 759 is 200pA, maximum.

Reference Current — I_{REF} is the internally generated current source to which all input currents are compared. I_{REF} tolerance errors appear as a dc offset at the output. The specified value of I_{REF} is ±3% referred to the input, and, from Table 1, corresponds to a dc offset of ±12.84mV for K = 1. This offset is independent of input signal and may be removed by injecting a current into terminal 1 or 2.

Reference Voltage — E_{REF} is the effective internally generated voltage to which all input voltages are compared. It is related to I_{REF} through the equation:
$E_{REF} = I_{REF} \times R_{IN}$, where R_{IN} is an internal 10kΩ, precision resistor. Virtually all tolerance in E_{REF} is due to I_{REF}. Consequently, variations in I_{REF} cause a shift in E_{REF}.

Scale Factor — Scale factor is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope, and is specified in per cent of the nominal value. An external adjustment may be performed if fine trimming is desired for improved accuracy.

OPTIONAL EXTERNAL ADJUSTMENTS FOR LOG OPERATION

Trimming E_{OS} — The amplifier's offset voltage, E_{OS}, may be trimmed for improved accuracy with the model 759 connected in its log circuit. To accomplish this, a 100kΩ, 10 turn pot is connected as shown in Figure 3. The input terminal, Pin 4, is connected to ground. Under these conditions the output voltage is:

$$e_{OUT} = -K \log_{10} E_{OS}/E_{REF}$$

To obtain an offset voltage of 100μV or less, for K = 1, the trim pot should be adjusted until the output voltage is between +3 and +4 volts for model 759N, and -3 to -4V for model 759P.

For other values of K, the trim pot should be adjusted for an output of e_{OUT} = 3 x K to 4 x K where K is the scale factor.

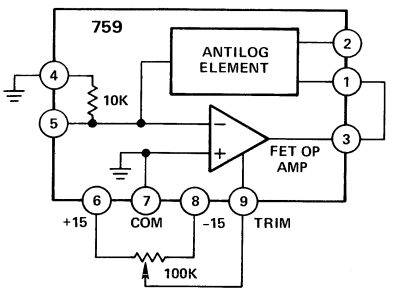


Figure 3. Trimming E_{OS} in Log Mode

Reference Current or Reference Voltage — The reference current or voltage of model 759 may be shifted by injecting a constant current into the unused scale factor terminal (Pin 1 or Pin 2). Each 330μA of current injected will shift the reference one decade, in accordance with the expression: I_I = 330μA log 10μA/I_{REF}, where I_I = current to be injected and I_{REF} = the desired reference current.

By changing I_{REF}, there is a corresponding change in E_{REF} since, $E_{REF} = I_{REF} \times R_{IN}$. An alternate method for rescaling E_{REF} is to connect an external R_{IN}, at the I_{IN} terminal (Pin 5) to supplant the 10kΩ supplied internally (leaving it unconnected). The expression for E_{REF} is then, $E_{REF} = R_{IN} I_{REF}$. Care must be taken to choose R_{IN} such that $(e_{SIG}\ max)/R_{IN} \leqslant 1mA$.

Scale Factor (K) Adjustment — Scale factor may be increased from its nominal value by inserting a series resistor between the output terminal, Pin 3, and either terminal 1 or 2. The table below should be consulted when making these scale factor changes.

RANGE OF K	CONNECT SERIES R TO PIN	VALUE OF R	NOTE
2/3V to 1.01V	1	3kΩ x (K − 2/3)	use pins 1, 2
1.01V to 2.02V	1	3kΩ x (K − 1)	use pin 1
>2.02V	2	3kΩ x (K − 2)	use pin 2

Table 2. Resistor Selection Chart for Shifting Scale Factor

ANTILOG OPERATION

The model 759 may be used to develop the antilog of the input voltage when connected as shown in Figure 4. The antilog transfer function (an exponential), is:

$$e_{OUT} = E_{REF}\ 10^{-e_{IN}/K} \qquad [-2 \leqslant e_{IN}/K \leqslant 2]$$

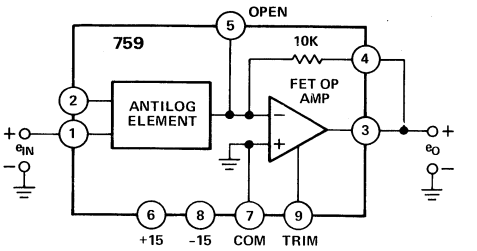


Figure 4. Functional Block Diagram

Principle of Operation — The antilog element converts the voltage input, appearing at terminal 1 or 2, to a current which is proportional to the antilog of the applied voltage. The current-to-voltage conversion is then completed by the feedback resistor in a closed-loop op amp circuit.

A more complete expression for the antilog function is:

$$e_{OUT} = E_{REF}\ 10^{-e_{IN}/K} + E_{OS}$$

The terms K, E_{OS}, and E_{REF} are those described previously in the LOG section.

Offset Voltage (E_{OS}) Adjustment — Although offset voltage of the antilog circuit may be balanced by connecting it in the log mode, and using the technique described previously, it may be more advantageous to use the circuit of Figure 5. In this configuration, offset voltage is equal to $e_{OUT}/100$. Adjust for the desired null, using the 100k trim pot. After adjusting, turn power off, remove the external 100Ω resistor, and the jumper from Pin 1 to +15V. For 759P use the same procedure but connect Pin 1 to -15V.

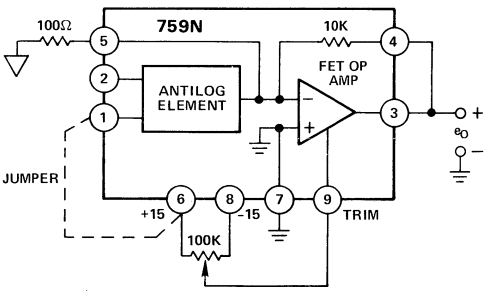


Figure 5. Trimming E_{OS} in Antilog Mode

Reference Voltage (E_{REF}) Adjustment — In antilog operation, the voltage reference appears as a multiplying constant. E_{REF} adjustment may be accomplished by connecting a resistor, R, from Pin 5 to Pin 3, in place of the internal 10kΩ. The value of R is determined by:

$$R = E_{REF}\ \text{desired}/10^{-5}\ A$$

Scale Factor (K) Adjustment — The scale factor may be adjusted for all values of K greater than 2/3V by the techniques described in the log section. If a value of K, less than 2/3V is desired for a given application, an external op amp would be required as shown in Figure 6. The ratio of the two resistors is approximately:

$$R1/R_G = (1/K - 1) \text{ where K = desired scale factor}$$

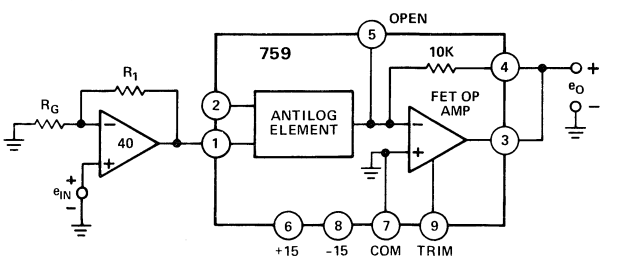


Figure 6. Method for Adjusting K< 2/3V

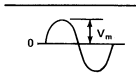
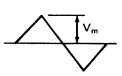
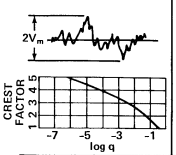
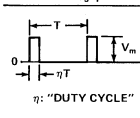
RMS Converters

Orientation
RMS Converters

The devices catalogued here are high-accuracy true-rms-to-dc-conversion IC's and modules. Devices of this class compute the instantaneous square of the input signal, average it, and take the square root of the result, to provide a dc voltage that is proportional to the rms of the input (and, in the case of the AD536, an additional dc voltage that is proportional to the *log* of the rms, for dB measurements).

Excellent pre-trimmed performance, improvable by simple optional trims, makes these devices ideal for all types of laboratory and OEM rms instrumentation where amplitude measurements must be made with high accuracy, independently of waveshape.

An alternative to rms that has been widely used in the past, principally for measurements on sine waves, is mean absolute-deviation, or "ac average." It is performed by taking the absolute value of (i.e., full-wave or half-wave rectifying) a signal, filtering it, and scaling it by the ratio of rms to m.a.d. for sine waves, 1.111, so that it reads correctly (for undistorted sine waves). Unfortunately, this ratio varies widely as a function of the waveform and will give grossly incorrect results in many cases. The table shows a few representative examples comparing rms with m.a.d.

WAVEFORM		RMS	MAD	RMS / MAD	CREST FACTOR
	SINE WAVE	$\frac{V_m}{\sqrt{2}}$ 0.707 V_m	$\frac{2}{\pi} V_m$ 0.637 V_m	$\frac{\pi}{2\sqrt{2}}$ = 1.111	$\sqrt{2}$ = 1.414
	SYMMETRICAL SQUARE WAVE OR DC	V_m	V_m	1	1
	TRIANGULAR WAVE OR SAWTOOTH	$\frac{V_m}{\sqrt{3}}$	$\frac{V_m}{2}$	$\frac{2}{\sqrt{3}}$ = 1.155	$\sqrt{3}$ = 1.732
	GAUSSIAN NOISE CREST FACTOR IS THEORETICALLY UNLIMITED. q IS THE FRACTION OF TIME DURING WHICH GREATER PEAKS CAN BE EXPECTED TO OCCUR	RMS	$\sqrt{\frac{2}{\pi}}$ RMS = 0.798 RMS	$\sqrt{\frac{\pi}{2}}$ 1.253	C.F. / q 1 / 32% 2 / 4.6% 3 / 0.37% 3.3 / 0.1% 3.9 / 0.01% 4 / 63ppm 4.4 / 10ppm 4.9 / 1ppm 6 / 2x10⁻⁹
	PULSE TRAIN η / MARK/SPACE 1 / ∞ 0.25 / 0.3333 0.0625 / 0.0667 0.0156 / 0.0159 0.01 / 0.0101 η: "DUTY CYCLE"	$V_m\sqrt{\eta}$ V_m 0.5V_m 0.25V_m 0.125V_m 0.1V_m	$V_m\eta$ V_m 0.25V_m 0.0625V_m 0.0156V_m 0.01V_m	$\frac{1}{\sqrt{\eta}}$ 1 2 4 8 10	$\frac{1}{\sqrt{\eta}}$ 1 2 4 8 10

Examples of applications include noise measurement — for example, thermal noise, transistor noise, and switch-contact noise. True-rms measurement is a technique that provides consistent theoretically valid measurements of noise amplitude (standard deviation) from different sources having different properties.

True-rms devices are also useful for measuring electrical signals derived from mechanical phenomena, such as strain, stress, vibration, shock, expansion, bearing noise, and acoustical noise. The electrical signals produced by these mechanical actions are often noisy, non-periodic, nonsinusoidal, and superimposed on dc levels, and require true-rms for consistent, valid, accurate measurements. RMS converters are also useful for accurate measurements on low-repetition-rate pulse-trains having high *crest factors* (ratio of peak to rms), and for measurements of the energy content of SCR waveforms at differing firing angles.

The basic approach used in these converters for computing the rms (with design variations to harmonize the approach with the technology) is to take the absolute value, square it, and divide by the fed-back output (using the logarithmic characteristics of transistor junctions), and filter the result. The resulting approximation

$$E_o = \text{Avg.}\left[\frac{V_{in}^2}{E_o}\right] \cong \sqrt{\text{Avg.}\,(V_{in}^2)}$$

is valid if the averaging time-constant is sufficiently long compared with the periods of the lowest-frequency ac components of the signal.

The simplest form of averaging involves a single-pole filter. Both device families will accept external filtering capacitance; but the modular converters include an initial value of capacitance to provide an internal filter whose time constant is adequate for many applications. Increased values of capacitance for filtering will improve the accuracy for low frequency rms measurements and provide reduced ripple at the output, but at the cost of increased settling time. For fastest settling and minimum ripple, the data sheets and (2) show how an additional stage of 2-pole filtering is useful (the internal buffer amplifier of the AD536 permits this to be accomplished without external active elements). The additional filtering permits improvement of settling time or reduction of ripple (or both) because of substantial reduction of C_{ext}.

PERFORMANCE SPECIFICATIONS

Considerable information regarding rms-to-dc converter circuit design, performance, selection, and applications is to be found in the NONLINEAR CIRCUITS HANDBOOK.[1] In addition, useful applications information on auxiliary filtering can be found in the article "Measure RMS with Less Ripple in Less Time,"[2] and a discussion of the design of the AD536

[1] Analog Devices, Inc., 1974, 1976, 536pp, edited by D. H. Sheingold, $5.95; send check or complete Master-Charge data to P.O. Box 796, Norwood MA 02062

[2] ANALOG DIALOGUE 9-3, 1975, pp 21-22

can be found in the 1976 IEEE International Solid-State Circuits Conference *Digest of Technical Papers*, page 10.

The most-salient feature of a true rms-to-dc converter is that it ideally has no error due to an indirect approximation to the rms. Static errors are due only to scale-factor, linearity, and offset errors; dynamic errors are due to insufficient averaging time at the low end and finite bandwidth and slewing rate at the upper end. Linearity errors affect crest factor in midband. Dynamic errors are also a function of signal amplitude, due in part to the variation of bandwidth of the "log" transistors with signal level.

Total Error A specification for quick reference, this is the maximum deviation of the dc component of the output voltage from the theoretical output value over a specified range of signal amplitude and frequency. It is shown as the sum of a fixed error and a component proportional to the theoretical output ("% of reading"). It is specified for a sinusoidal input in a given frequency and amplitude range. The fixed error-component includes all offset errors and irreducible nonlinearities; the %-of-reading component includes the linear scale-factor error.

Total Error, external trim (adjustment) is the amount by which the output may differ from the theoretical value when the output offset and scale factor have been trimmed. Note that the fixed error-component cannot be reduced to zero, even though the output offset can be nulled at zero input. This is because of residual input offsets and inherent nonlinearities in the converter.

Total Error vs. Temperature is the average change of %-of-full-scale error component plus the average change of percent of reading error component per degree Celsius, over the rated temperature range.

Frequency for 1%-of-Reading Error is the minimum value of frequency (at the high end) at which the error increases from the midband value by 1% of reading. It is a function of peak-to-peak input amplitude.

Frequency for ±3dB Reading Error is the minimum value of frequency (at the high end) at which the error may equal 30% of reading. It is a function of amplitude.

Crest Factor (a property of the signal) is the ratio of peak signal voltage to the ideal value of rms; the specified value of crest factor is that for which the error is maintained within specified limits at a given rms level for a worst-case — rectangular pulse — input signal.

Filter Time Constant and External Capacitor: The time constant of the internal averaging filter, and the increase of time constant per μF of added external capacitance.

Input: The voltage range over which specified operation is obtained, the maximum voltage for which the unit operates, the maximum safe input voltage, and the effective input resistance.

Output: The maximum output range for rated performance, the minimum current guaranteed available at full-scale output voltage, and the source resistance of the output circuit.

Power Supply: Power-supply range for specified performance, power-supply range for operation, and quiescent current drain. Note that the AD536 can be operated from single or dual supplies.

Temperature Range: The range of temperature variation for operation within specifications. Temperature coefficients are determined by three-point measurements (T_H − 25°C), (25°C − T_L), when measured.

Selection Guide
RMS Converters

MODEL	CHARACTERISTICS	PAGE
442J/K/L	Wideband, low-drift, high-crest-factor module. Preadjusted for total max error ±2mV ±0.15% of reading, for sine waves, frequencies to 20kHz (100kHz typical), 0 to 2V rms input. User-trimmable to ±0.5mV ±0.05%, 10mV to 2V. Crest factor of 7 for 0.2% additional reading error. Bandwidth for 1% (rdg.) error 700kHz, and for -3dB 8MHz, for 2V rms signals. Averaging time-constant 1.5ms + C_{ext} • 15ms/μF. Total-error max tempco (±35μV ±0.01% rdg.)/°C (442L).	235
AD536J/K	Monolithic IC rms/dB converter. Laser-wafer-trimmed for total max error ±2mV ±0.2% of reading (AD536K), sine waves at 1kHz (20kHz typ), 0 to 7V rms. Crest factor of 6 for 1% additional error. ±3dB bandwidth 100kHz. Averaging time constant per μF of C_{ext}, 25ms/μF. Total-error tempco (±100μV ±0.01% rdg)/°C. Additional features include dB output with 60dB range, single- or dual-supply operation, and low power consumption — 1mA.	229

NOTE:
The devices listed above and catalogued here are recommended for new designs. Models 440 and 441 are popular earlier models that are still available. Data sheets will be provided upon request.

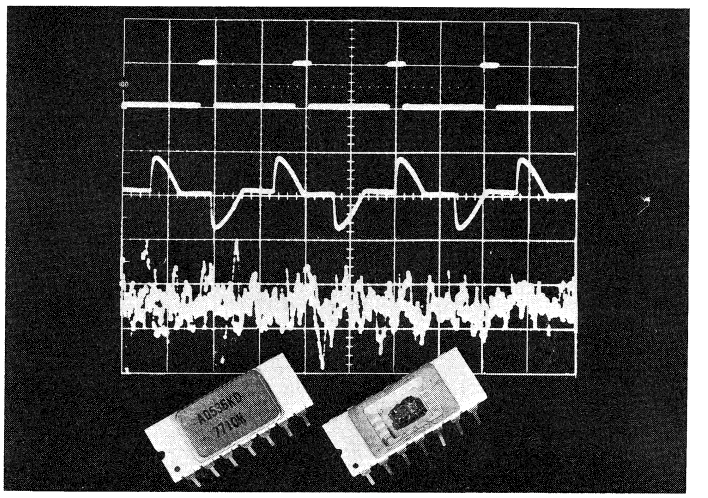
ANALOG DEVICES

Integrated Circuit True rms-to-dc Converter

AD536

FEATURES

- True rms-to-dc Conversion
- Laser-Trimmed to High Accuracy
  - 0.2% max Error (AD536K)
  - 0.5% max Error (AD536J)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 100kHz Bandwidth: $V_{rms} \geqslant 100mV$
  - Signal Crest Factor of 6 for 1% Error
- dB Output with 60dB Range
- Low Power: 1mA Quiescent Current
- Single or Dual Supply Operation
- Low Cost Integrated Circuit



PRODUCT DESCRIPTION

The AD536 is a complete integrated circuit true rms-to-dc converter. It is the first single chip monolithic circuit of this type and offers performance which is comparable or superior to that of hybrid or modular units costing much more. The AD536 directly computes the true rms value of any complex input waveform containing ac and dc components. It has a crest factor compensation scheme which allows measurements with 1% error at crest factors up to 6. The wide bandwidth of the device extends the measurement capability to 100kHz with 3dB error for signal levels above 100mV.

An important new feature of the AD536 not previously available in rms converters is an auxiliary dB output. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60dB. Using an externally supplied reference current, the 0dB level can be conveniently set by the user to correspond to any input level from 0.1 to 2 volts rms.

The AD536 is laser trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal), and full scale accuracy. As a result, no external trims are required to achieve the rated accuracy of the unit.

There is full protection for both inputs and outputs. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with inputs connected will not cause unit failure. The output is short-circuit protected.

The AD536 is available in two accuracy grades, the "K" version with a maximum total error of ±2mV ±0.2% of reading and the "J" with a maximum error of ±5mV ±0.5% of reading. Both versions are specified for rated performance from 0 to +70°C and supplied in a hermetically sealed 14-pin DIP.

PRODUCT HIGHLIGHTS

1. The AD536 computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it relates directly to a physical quantity, the power of the signal. The rms value of a statistical signal also relates to its standard deviation.
2. The crest factor of a waveform is the ratio of the peak signal swing to the rms value. The crest factor compensation scheme of the AD536 allows measurement of highly complex signals with wide dynamic range.
3. The only external component required to perform measurements to the fully specified accuracy is the capacitor which sets the averaging period. The value of this capacitor determines the low frequency ac accuracy, ripple level and settling time. Alternate two and three capacitor schemes are shown which give much faster settling time for the same level of ripple.
4. The AD536 will operate equally well from split supplies or a single supply with total supply levels from 5 to 36 volts. The quiescent supply current is only one milliampere at any supply voltage. This versatility and low power makes the device well-suited for a wide variety of remote controllers and battery powered instruments.
5. Every AD536 is baked for 48 hours at +150°C, and temperature cycled 10 times from -65°C to +200°C, prior to final test to assure reliability and long term stability.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	AD536J	AD536K
TRANSFER EQUATION	$V_{OUT} = \sqrt{avg.\ (V_{IN})^2}$	*
CONVERSION ACCURACY		
Total Error, Internal Trim[1] (Fig. 1)	±5mV ±0.5% of Reading, max	±2mV ±0.2% of Reading, max
vs. Temperature	±(0.1mV ±0.01% Reading)/°C	*
vs. Supply Voltage	±(0.1mV ±0.01% Reading)/V	*
dc Reversal Error	± 0.05% of Reading	*
Total Error, External Trim[1] (Fig. 2)	±3mV ±0.3% of Reading	±2mV ±0.1% of Reading
ERROR vs CREST FACTOR[2]		
Crest Factor 1 to 2	Specified Accuracy	*
Crest Factor = 3	-0.1% of Reading	*
Crest Factor = 6	-1% of Reading	*
FREQUENCY RESPONSE[3]		
Bandwidth for Specified Accuracy	20kHz	*
±3dB Bandwidth	100kHz	*
AVERAGING TIME CONSTANT (Fig. 4)	25ms/μF C_{AV}	*
INPUT CHARACTERISTICS (Pin 1)		
Signal Range, ±15V Supply	±20V Peak	*
Signal Range, +5V Supply (Fig. 16)	±5V Peak	*
Safe Input, All Supply Voltages	±25V max	*
Input Resistance	16.7kΩ ±25%	*
Input Offset Voltage	±2mV max	±1mV max
OUTPUT CHARACTERISTICS (Fig. 1, Pin 6)		
Offset Voltage	±2mV max	±1mV max
vs. Temperature	±0.1mV/°C	*
vs. Supply Voltage	±0.1mV/V	*
Voltage Swing, ±15V Supplies	0 to +10V min	*
±5V Supply	0 to +2V min	*
Output Current	(+5mA, -130μA) min	*
Short Circuit Current	+20mA	
Resistance	0.5Ω max	
dB OUTPUT (Fig. 12)		
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms	±0.5dB	±0.2dB
Scale Factor	-3mV/dB	*
Scale Factor TC (Uncompensated, see Fig. 12 for Temperature Compensation)	-0.3% Reading /°C (-0.03dB/°C)	*
I_{REF} for 0dB = 1V rms	20μA	*
I_{REF} Range	1μA to 100μA	*
I_{OUT} TERMINAL (Pin 8: Pin 9 Open)		
I_{OUT} Scale Factor	40μA/Volt rms	*
I_{OUT} Scale Factor Tolerance	±25%	*
Output Resistance	10^8Ω	*
Voltage Compliance	$-V_S$ to $(+V_S$ -3V)	*
BUFFER AMPLIFIER		
Input and Output Voltage Range	$-V_S$ to $(+V_S$ -3V) min	*
Input Offset Voltage, R_S = 25k	±4mV max	
Input Current	100nA typ, 300nA max	*
Input Resistance	10^8Ω	*
Output Current	(5mA, -130μA) min	*
Short Circuit Current	+20mA	*
Small Signal Bandwidth	1MHz	*
Slew Rate[4]	5V/μs	*
POWER SUPPLY		
Voltage, Rated Performance		
Dual Supply	±3.0V to ±18V	*
Single Supply	+5V to +36V	*
Quiescent Current		
Total V_S 5V to 36V	2mA max (1mA typ)	*
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	*
Storage	-55°C to +150°C	*

[1] Accuracy is specified for 0 to 7V rms, dc or 1kHz sinewave input to pin 1, with the AD536 connected as in Figure 1.
[2] Error vs crest factor is specified for 1V rms rectangular pulse input, pulse width = 200μs.
[3] Signal Range–100mV to 7V rms.
[4] With 2K external pulldown resistor.

*Specifications same as AD536J.
Specifications subject to change without notice.

STANDARD CONNECTION

The AD536 is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD536 will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 4. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy above these points will be according to specification. If it is desired to reject the dc level, a capacitor is added in series with the input, as shown in Figure 3; the capacitor must be non-polar. If the AD536 is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible.

The input and output signal ranges are a function of the supply voltages; these ranges are shown in Figure 16. The AD536 can also be used in an unbuffered voltage output mode by disconnecting pins 7 and 8; the output then appears unbuffered at pin 8. The buffer amplifier can then be used for other purposes. Further, the AD536 can be used in a current output mode by disconnecting pin 9 from ground. The output current is available at pin 8 with a nominal full scale of 400μA, positive out.

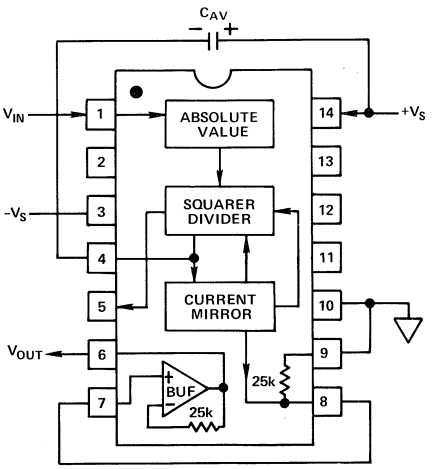


Figure 1. Standard rms Connection

OPTIONAL EXTERNAL TRIMS FOR HIGHER ACCURACY

If it is desired to improve the accuracy of the AD536, the external trims shown in Figure 2 can be added. R_1 is used to trim the gain of the device; R_4 is used to trim the offset. The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R_4 to give zero volts output from pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.

2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from pin 6, i.e., 1.000V dc input should give 1.000V dc output. Of course, a ±1.000 peak-to-peak sinewave should give a 0.707V dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

The major advantage of external trimming is to optimize device performance for a reduced signal range; the AD536 is internally trimmed for a 7V rms full scale range.

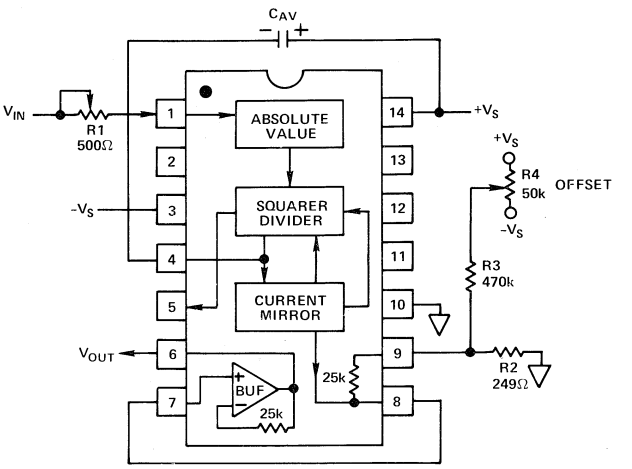


Figure 2. Optional External Gain and Output Offset Trims

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 require the use of approximately symmetrical dual supplies. The AD536 can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the differential input stage must be biased off ground for proper operation. This biasing is done at pin 10; thus it is critical that no extraneous signals be coupled into this point. AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 16.7kΩ; for a cut-off at 10Hz, C_2 should be 1μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The input and output signal ranges are shown in Figure 16. The load resistor, R_L, is necessary to provide output sink current.

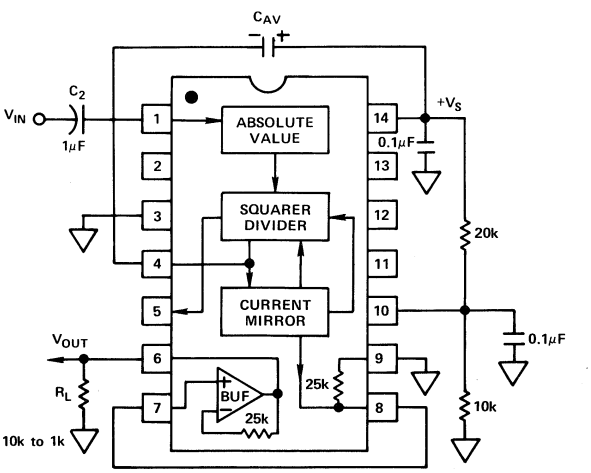


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

A computing rms-to-dc circuit of this type can respond to both ac and dc signals. The output will track a slowly varying dc input exactly and will track the rms *average* of a high frequency ac waveform; however there is a transition region at low frequencies where the circuit will respond in an intermediate fashion. The averaging time constant determines the frequency at which that transition occurs.

The important performance factors in this transition region are accuracy and ripple. In the low frequency transition region, the circuit output will try to follow the input exactly in a dc fasion and also try to perform the rms average; thus the output waveform will have a dc level which approximates the rms and also an ac ripple. For the standard connection of Figure 1, the value of the averaging capacitor, C_{AV}, determines these factors.

The deviation of the dc component of the output signal from the theoretically correct output is the dc error; it is shown in Figure 4 as a function of C_{AV} and frequency. The ac component of the output signal is the ripple; it will normally be a percentage of the input signal at a given frequency. The ripple effect for the standard circuit is shown in the first curve on the right in Figure 6. The ripple effect is a linear function of C_{AV} for the standard circuit. To minimize ripple and error effects when measuring signals with high crest factors (especially low-duty cycle pulse trains), C_{AV} should be chosen to give a time constant at least 10 times the signal period (e.g., use 100ms for a 100Hz pulse rate, thus a 4μF capacitor).

The settling time required to respond to a step change in rms input level is also an important consideration. Figure 4 also shows (on the right axis) the settling time to 1% for given values of C_{AV}. Thus, if C_{AV} is chosen as 10μF, the settling time (for a step change to full scale) is one second, the dc error is 0.1% at 3Hz (from Figure 4) and the peak-to-peak ripple is about 5% at 10Hz (extrapolated from Figure 6). The settling time will be twice as great for decreasing signals as for increasing and will increase at low signal levels.

This performance can be improved considerably for both ripple and settling time with the addition of a one- or two-pole "post" filter as shown in Figure 5. The relative performance of these various filter types is shown in Figure 6. The performance of filters using other capacitance values will scale properly if the same capacitance ratios between C_{AV}, C_2, and C_3 are used. The settling time of the two pole filter is 0.7 seconds; the three-pole filter is 0.3 seconds. Note that dc error performance is only a function of C_{AV}.

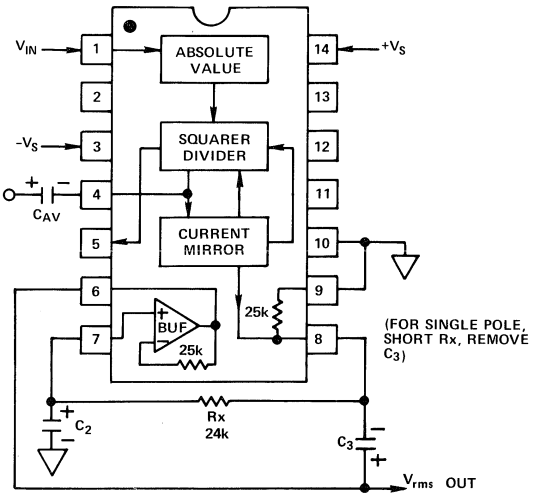


Figure 5. 2 Pole "Post" Filter

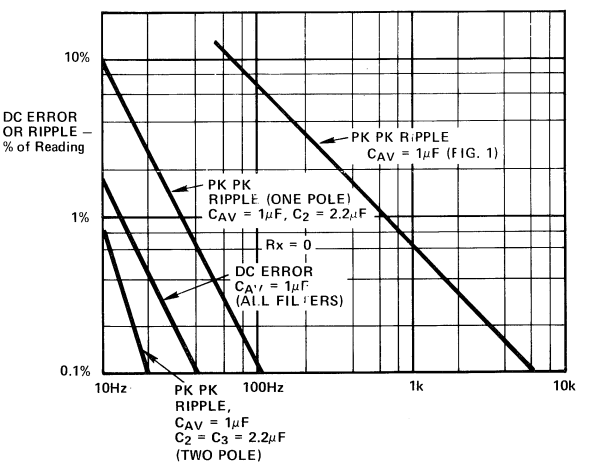


Figure 6. Performance Features of Various Filter Types

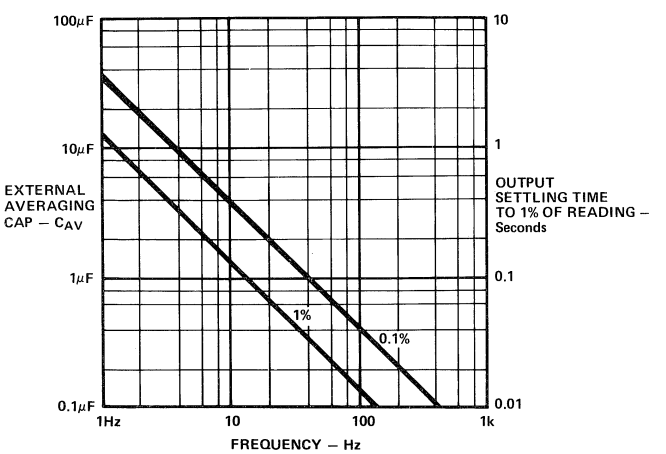


Figure 4. Lower Frequency for Stated % of Reading Error and Settling Time for Circuit Shown in Figure 1

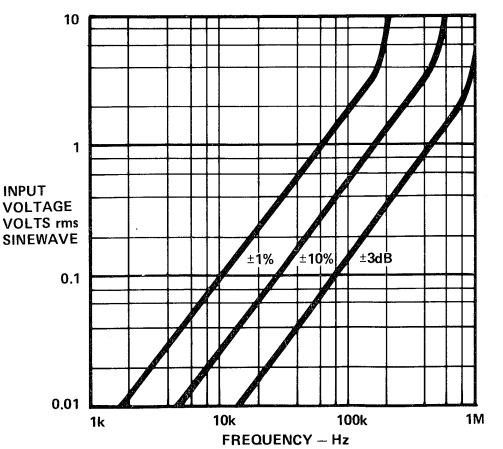


Figure 7. High Frequency Response

AD536 PRINCIPLE OF OPERATION

The AD536 embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD536 follows the equation:

$$V_{rms} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 8 is a simplified schematic of the AD536; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2 / I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{Avg.} [I_1^2/I_4] = I_1 \text{ rms}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD536 thus results:

$$V_{OUT} = 2R_2 I_{rms} = V_{IN} \text{ rms}$$

The dB output is derived from the emitter of Q_3, since the voltage at this point is proportional to -log V_{IN}. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

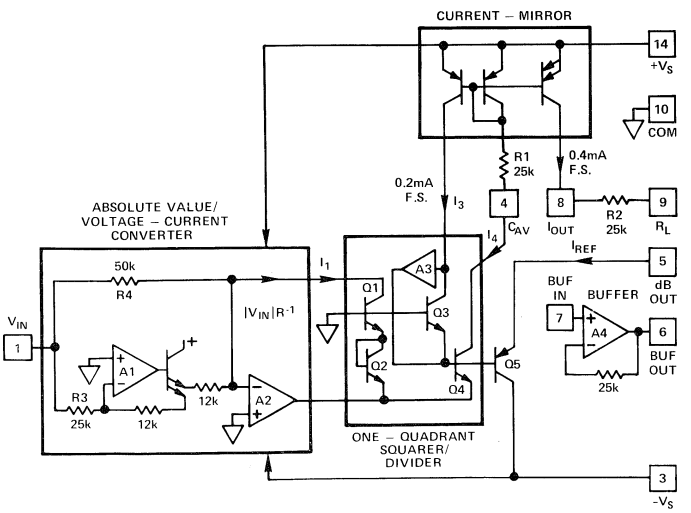


Figure 8. Simplified Schematic

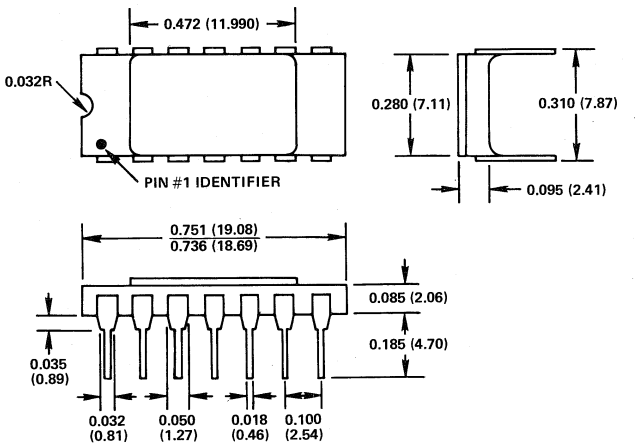
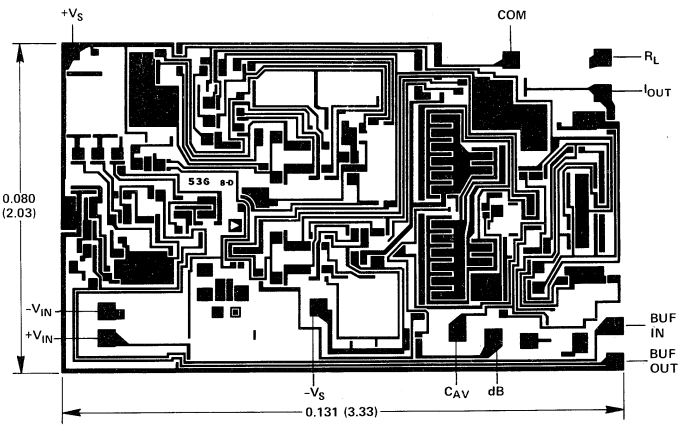


Figure 9. Physical Dimensions. Dimensions shown in inches and (mm).



THE AD536 IS AVAILABLE IN A LASER-TRIMMED CHIP FORM. THE CHIP CAN BE GUARANTEED TO J-LEVEL PERFORMANCE. CONSULT FACTORY FOR APPLICATION AND PRICING DETAILS.

Figure 10. Chip Dimensions and Pad Layout. Dimensions shown in inches and (mm).

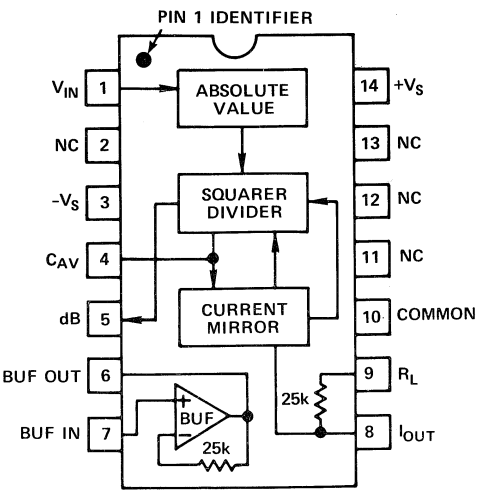


Figure 11. AD536 Pin Connections and Functional Diagram

CONNECTIONS FOR dB OPERATION

A powerful feature added to the AD536, which is not available in any other computing rms circuit, is the logarithmic or decibel output. The internal circuit which computes dB is very accurate and works well over a 60dB range. The connection for dB measurements is shown in Figure 12. The user selects the 0dB level by setting R_1 for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer-divider at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the 0.3%/°C temperature drift of the dB circuit. The special T.C. resistor, R_3, is available from Tel Labs, type number QB-1. The linear rms output is available at pin 8 with an output impedance of 25kΩ; thus many applications may require an additional buffer amplifier if this output is desired.

dB Calibration:

1. Set V_{IN} = 1.00V dc
2. Adjust R_1 for dB out = 0.00V
3. Set V_{IN} = +0.1V dc
4. Adjust R_2 for dB out = -2.00V

Any other desired 0dB reference level can be used by setting V_{IN} and adjusting R_1 accordingly. Note that adjusting R_2 for the proper gain automatically gives the correct temperature compensation.

An alternate circuit which operates on a single positive supply and gives direct dB display on a linear panel meter is shown in Figure 13.

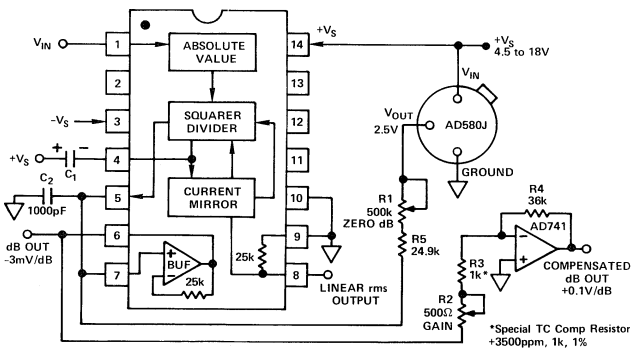


Figure 12. dB Connection

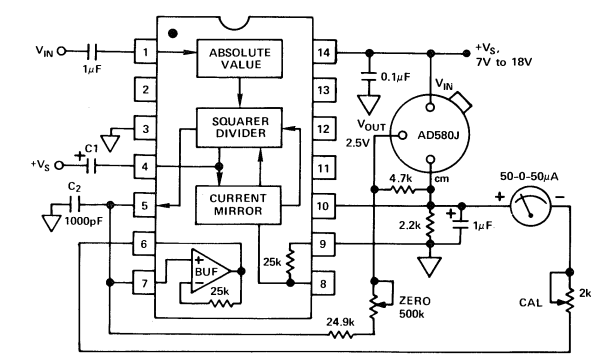
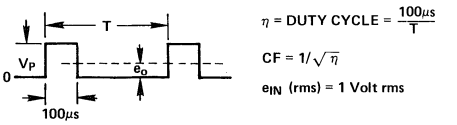


Figure 13. AD536 with dB Output Power to Linear Meter Display, Single Supply

RMS MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is frequently understated in importance for rms measurements, yet it is key to determining the accuracy of a true rms measurement on a specific waveform. Crest factor is defined as the ratio of the peak signal amplitude to the rms value (C.F. = V_p/V_{rms}). Most common waveforms have relatively low crest factors (<2). Waveforms such as low duty cycle pulse trains have high crest factors (e.g., for 1% duty cycle pulse train, crest factor is 10). Figure 14 is a curve of reading error for the AD536 with a one volt rms pulse train with variable duty cycle and peak amplitude. In this curve, pulse width (100μs) and rms level (1V) are held constant. The pulse train was selected because of its ability to generate a wide range of crest factors by varying the duty cycle (C.F. = $1\sqrt{\eta}$). At a crest factor of 10, the peak input amplitude is 10 Volts (V_p = (C.F.) (V_{rms}). Therefore a one volt rms level was selected for crest factors from 1 to 10 (V_p from 1 to 10 Volts).



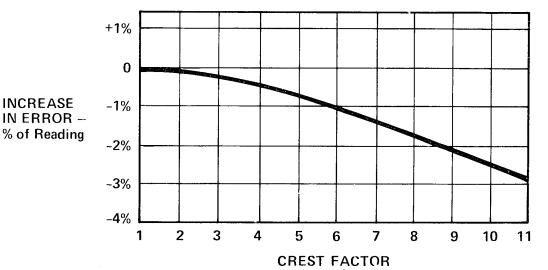


Figure 14. Error vs. Crest Factor

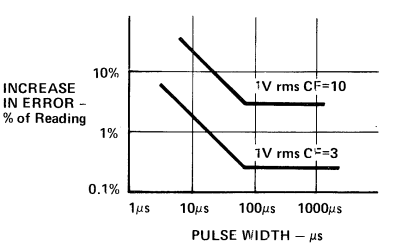


Figure 15. AD536 Error vs. Pulse Width Rectangular Pulse

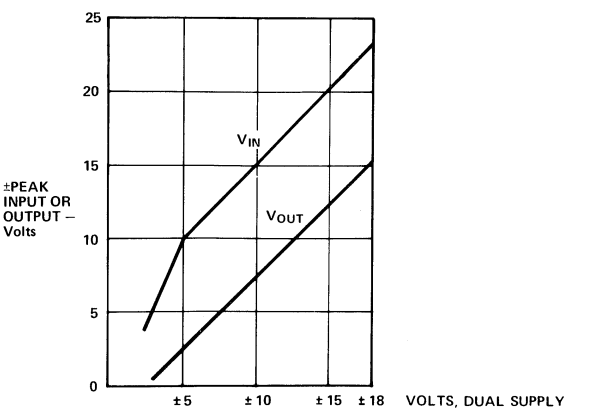


Figure 16. AD536 Input and Output Voltage Ranges vs. Supply

Wideband, High Accuracy True RMS-to-DC Converter

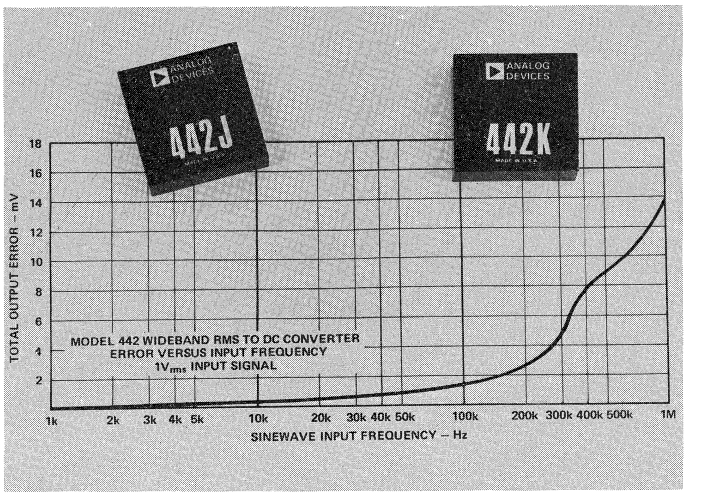
MODEL 442

FEATURES

Dc to 8MHz Response (-3dB)
High Accuracy:
With No Ext. Trim: ±2mV ±0.15% of Rdg., max
With Ext. Trim: ±1mV ±0.05% of Rdg., max
Low Drift: ±(35μV ±0.01% of Reading)/°C max, 442L
Fast Settling Time: 5ms to 1%
Small Size: 1.5" x 1.5" x 0.4"
All Hermetically Sealed Semiconductors

APPLICATIONS

Wideband rms Instrumentation
Telephone, Telegraph & Modem Test Equipment
Vibration Analysis
Sound & Noise Level Instrumentation
Mean Square Measurements



GENERAL DESCRIPTION

Model 442 is a high performance true rms-to-dc converter featuring 8MHz bandwidth, low drift to ±35μV/°C ±0.01% of reading/°C maximum, and ±1% reading error to 800kHz. Unlike competing designs, model 442 achieves its high accuracy over a very wide input signal range. With no external adjustment, accuracy is held to within ±2mV ±0.15% of reading for input signals of 0 to $2V_{rms}$. If optional adjustments are performed, this accuracy can be improved to ±1mV ±0.05% of reading. Model 442 is designed to be used in high performance instrumentation where response to low level, high speed signals, is of greatest importance.

The compact, log-antilog circuit design of model 442 results in high accuracy measurements on sinewave signals and complex waveforms such as pulse trains. Reading error increases 0.2% for signals with crest factors up to 7. In addition, true rms measurement can be performed directly on signals containing both ac and dc components.

Model 442 is available in three low drift selections offering maximum drift performance over 0 to +70°C range; model 442L: ±(35μV ±0.01% of rdg.)/°C max; model 442K: ±(50μV ±0.01% of rdg.)/°C max; model 442J: ±(100μV ±0.01% of rdg.)/°C max.

WHERE TO USE MODEL 442

Excellent untrimmed performance along with simple, optional trims make model 442 the ideal component for all types of laboratory and OEM rms instrumentation where wideband measurements must be made with high accuracy. Model 442 is ideally suited for measuring thermal noise, transistor noise and switch contact noise. True rms measurement is the only technique to accurately measure system noise and thereby assist the designer in reducing this noise. Model 442 is also useful for measuring mechanical phenomena such as strain, stress, vibration, shock, expansion and contraction. The electrical signals produced by these mechanical actions are often noisy, nonperiodic, nonsinusoidal and superimposed on dc levels, therefore requiring true rms devices for accurate measurements.

Model 442 is also required for accurate measurements on low repetition rate pulse trains. For pulse trains with crest factors of 10, a 3dB bandwidth of 400 times the pulse rate is required to achieve 1% accuracy and 4000 times the pulse rate is needed for 0.1% accuracy.

Model 442 may also be connected (see Figure 3) to measure the MEAN SQUARE of a signal ($e_o = e_{in}^2/V_R$). The Mean Square of a random signal is equal to the variance (σ^2).

TOTAL ACCURACY

Total output error is specified as the sum of two components; a fixed term plus a percentage of output signal. Model 442 has a rated sinewave accuracy of ±1mV ±0.05% max (externally trimmed), which for a one volt rms sinewave, results in a ±1.5mV maximum error (±1mV fixed error plus ±0.5mV reading error). The fixed error component is comprised of output offsets and linearity errors. Both of these error terms have been minimized in the model 442 as a result of special output circuit design and sophisticated factory offset trim procedures. Output offset can be adjusted for minimum error by means of an external adjustment (see Figure 2). The % of reading error is attributed to nonlinearity and scale factor errors. Scale factor error may also be reduced by external adjustment of an optional 5kΩ potentiometer (see Figure 2).

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc, unless otherwise noted)

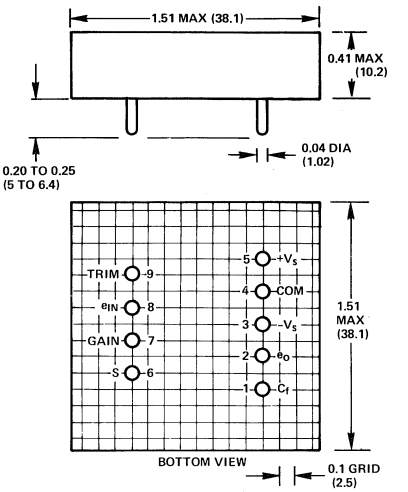
MODEL	442J	442K	442L
TRANSFER EQUATION	$e_o = \sqrt{avg\ (e_{in})^2}$	*	*
ACCURACY[1]			
Total Error, Sinewave Input, f ≤ 20kHz			
No External Adjustment			
Input Range: 0 to $2V_{rms}$	±2mV ±0.15% of Rdg., max	*	*
External Adjustment			
Input Range: 0 to $2V_{rms}$[2]	±1mV ±0.05% of Rdg., max	*	*
$10mV_{rms}$ to $2V_{rms}$[3]	±0.5mV ±0.05% of Rdg., max	*	*
Additional Error, Sinewave Input, 20kHz ≤ f ≤ 500kHz			
With or Without External Adjustment			
For Any Input Range	$(\pm 25\mu V \pm 0.0025\%\ of\ Rdg) \times \left(\frac{f(kHz) - 20kHz}{1kHz}\right)$, max	*	*
vs. Temperature (0 to +70°C), max	±100µV/°C plus ±0.01% of Rdg./°C	±50µV/°C plus ±0.01% of Rdg./°C	±35µV/°C plus ±0.01% of Rdg./°C
vs. Supply Voltage	±0.1mV/%	*	*
Warm-Up Time	5 minutes	*	*
FREQUENCY RESPONSE, SINEWAVE INPUT			
±1% Reading Error[3]			
Input: $7V_{rms}$	500kHz	*	*
$2V_{rms}$	700kHz	*	*
$1V_{rms}$	800kHz	*	*
$0.2V_{rms}$	120kHz	*	*
$0.1V_{rms}$	80kHz	*	*
$0.01V_{rms}$	25kHz	*	*
-3dB Reading Error			
Input: $7V_{rms}$	5MHz	*	*
$2V_{rms}$	8MHz	*	*
$1V_{rms}$	7MHz	*	*
$0.2V_{rms}$	3MHz	*	*
$0.1V_{rms}$	2MHz	*	*
$0.01V_{rms}$	300kHz	*	*
Internal Filter Time Constant	1.5ms	*	*
External Filter Time Constant[4]	15ms/µF	*	*
Total Averaging Time Constant[4]	1.5ms + 15ms/µF	*	*
CREST FACTOR			
±0.2% Additional Reading Error	7	*	*
±0.5% Additional Reading Error	10	*	*
INPUT SPECIFICATIONS			
Voltage			
Signal Range	$\pm 10V_{peak}$ min	*	*
Safe Input	$\pm V_S$	*	*
Impedance	2.5kΩ ±10%	*	*
OUTPUT SPECIFICATIONS[5]			
Rated Output			
Voltage	+10.0V min	*	*
Current	+5mA min	*	*
Impedance	0.1Ω	*	*
Offset Voltage, @ +25°C	±2mV max	*	*
With External 20kΩ Trim Pot	Adjustable to Zero	*	*
POWER SUPPLY[6]			
Voltage, Rated Specifications	±15V dc	*	*
Voltage, Operating	±(6 to 18)V dc	*	*
Current, Quiescent	±12mA	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	*
Operating	-25°C to +85°C	*	*
Storage	-55°C to +125°C	*	*
CASE SIZE	1.5" x 1.5" x 0.4"	*	*

*Specifications same as model 442J.
[1] Error is specified as the sum of two components: a fixed term plus a percentage of output signal (reading). Refer to TOTAL ACCURACY
[2] Refer to OPTIONAL AC CALIBRATION PROCEDURE
[3] Refer to AC CALIBRATION PROCEDURE.
[4] Connect optional filter capacitor between pin 1 and pin 2 (see Figure 2). Pin 1 is protected for shorts to ground and the positive supply voltage. Pin 1 is not protected for negative voltage greater than 1 volt.
[5] Protected for short circuit to ground and/or either supply voltage.
[6] Recommended power supply: Analog Devices' model 904

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Weight: 40 grams

MATING SOCKET AC1016

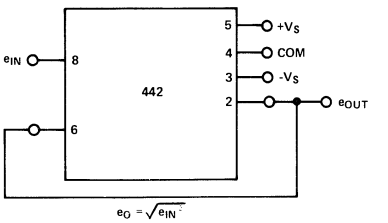
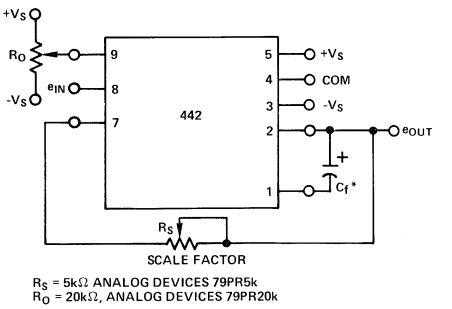


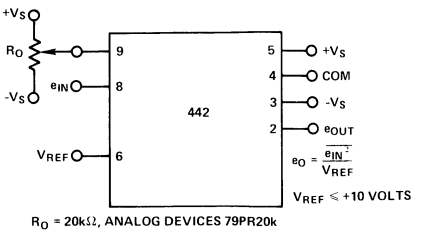
Figure 1. Wiring Connections for rms Measurements (No External Trim)



R_S = 5kΩ ANALOG DEVICES 79PR5k
R_O = 20kΩ, ANALOG DEVICES 79PR20k

*SELECT C_f FOR INCREASED AVERAGING TIME CONSTANT.
τ(ms) = 1.5 + 15C_f (µF)

Figure 2. Optional External Adjustment for rms Measurements



R_O = 20kΩ, ANALOG DEVICES 79PR20k

Figure 3. Wiring Connections for Mean Square Measurements with Adjustable Scale Factor (V_{REF})

OPTIONAL EXTERNAL ADJUSTMENT PROCEDURES

In rms designs, high accuracy is achieved by minimizing input and output offsets. Model 442 is internally trimmed for low input offsets and can accurately measure signals as low as 5mV. The optional adjustment trims outlined below (see Figure 2) minimize output error.

DC Calibration Procedure (Allow a 5 min. warm-up)

1. Ground pin 8 and adjust R_O for e_o = 0 volts.
2. Apply 1.000V_{dc} to pin 8; adjust R_S for e_o = 1.000V_{dc}.

AC Calibration Procedure (Allow a 5 min. warm-up)

The ac calibration procedure results in higher accuracy when compared to the DC CALIBRATION PROCEDURE. The AC PROCEDURE yields sinewave error of ±0.5mV ±0.05% of reading maximum, for 10mV_{rms} to 2V_{rms} inputs. When using the AC CALIBRATION PROCEDURE, use C_f = 1μF or larger in order to minimize low frequency errors.

1. Apply a precision 10mV_{rms}, 1kHz sinewave to pin 8. Adjust R_O for e_o = 10mV_{dc}.
2. Apply a precision 1.000V_{rms}, 1kHz sinewave input to pin 8 and adjust R_S for e_o = 1.000V_{dc}.

Optional AC Calibration Procedure

To minimize error at 0 volts and 1V_{rms}, step 1 above should be modified to read:

1. Ground pin 8 and adjust R_O for e_o = 0 volts.

Figure 4 illustrates the results of using the AC CALIBRATION PROCEDURE for zero error at 10mV_{rms} and 1V_{rms}.

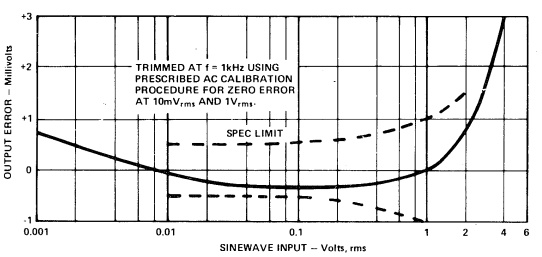


Figure 4. Trimmed Output Error Versus Sinewave Input Level (f = 1kHz)

HIGH FREQUENCY ACCURACY VERSUS SIGNAL LEVEL

Model 442's excellent wideband performance shown in Figure 5 results from its high speed input stage and from the use of reduced values of critical circuit resistance to minimize frequency response degradation due to stray capacitance. A special compensation circuit is also incorporated to extend the bandwidth for low level signals. Model 442 is optimized for operation from 10mV_{rms} to 2V_{rms} input levels, making it ideal for DVM applications.

The cross-over of the 100mV_{rms}, and 200mV_{rms} curves with the 10mV_{rms} curve in Figure 5 results from the nonlinearities that remain after performing the AC CALIBRATION PROCEDURE – refer to Figure 4.

LOW FREQUENCY ACCURACY VS. FILTER CAPACITOR

Figure 6 shows output error versus frequency with external filter capacitor (C_f) as a parameter. This capacitor reduces low frequency error without affecting high frequency accuracy. To select C_f, the lowest frequency component of the input signal (f_L) is determined. Model 442's averaging time constant, τ(ms) = 1.5 + 15C_f (μF), is selected to be approximately 10 times the period of f_L. Low leakage capacitors, such as tantalum electrolytic, are recommended.

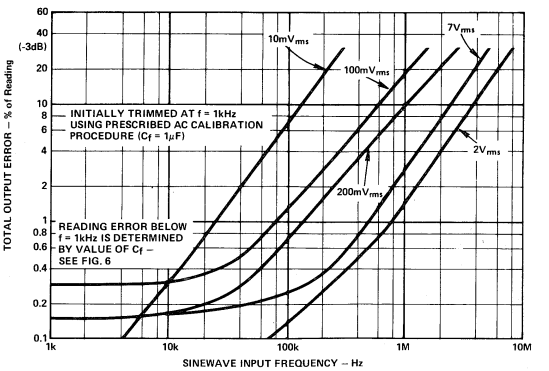


Figure 5. Trimmed Output Error at High Frequency Versus Input Signal Level

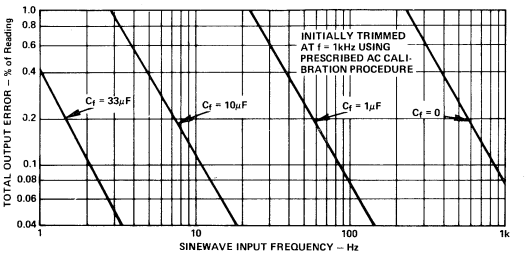


Figure 6. Trimmed Output Error at Low Frequency Versus C_f

SETTLING TIME AND OUTPUT RIPPLE VS. FILTER CAPACITOR

The external filter capacitor affects low frequency accuracy, ripple and settling time. Output ripple is reduced as C_f is increased (see Figure 7). There is no upper limit on the size of C_f, however settling time is increased as C_f increases. Figure 8 shows settling time to 1% accuracy for 1V_{rms} step changes. Increasing changes settle in about 3τ; decreasing step changes settle in about 5τ where τ is defined by: τ(ms) = 1.5 + 15C_f.

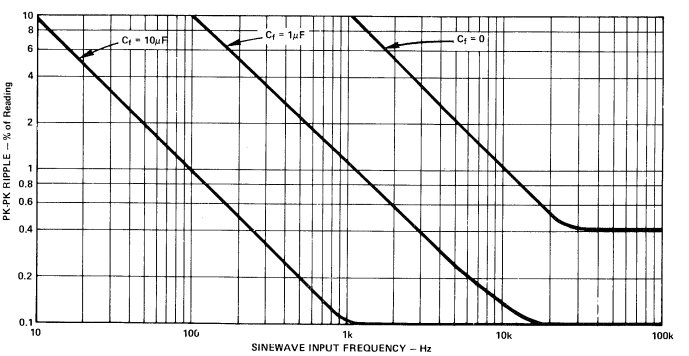


Figure 7. Output Ripple Versus External Filter Capacitor (C_f)

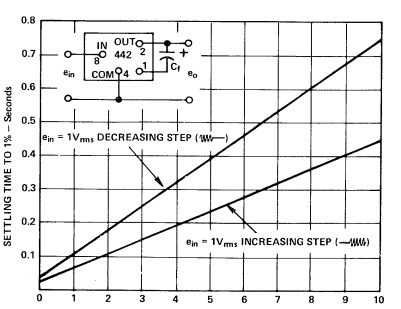


Figure 8. Settling Time Versus Filter Capacitor (C_f)

USING A TWO POLE FILTER FOR LOW RIPPLE AND FAST RESPONSE

The output of model 442 contains an ac ripple signal that introduces a small dc error. Adding external capacitance in parallel with the internal filter capacitor will reduce the ripple, but will result in a corresponding increase in settling time (see Figure 9).

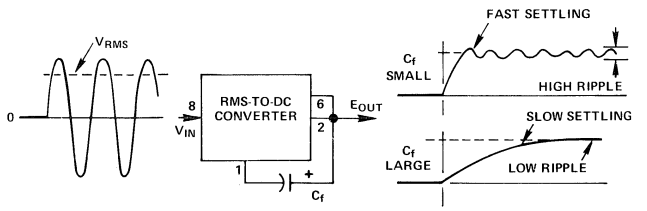


Figure 9. Settling Time and Low Frequency Ripple

A circuit which results in dramatic improvement in ripple while achieving fast settling time is shown in Figure 10. A comparison of ripple for the circuits of Figures 9 and 10 is shown in Figure 11. Percent ripple is plotted as a function of frequency. Note the dramatic reduction of ripple for Figure 10. The frequencies at which 0.1% and 1% ripple occur are reduced by factors of about 80 and 20 respectively.

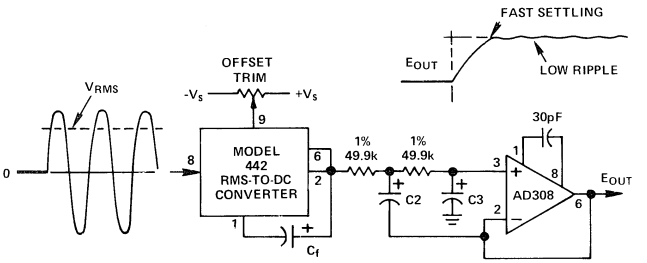


Figure 10. External 2-Pole Filter

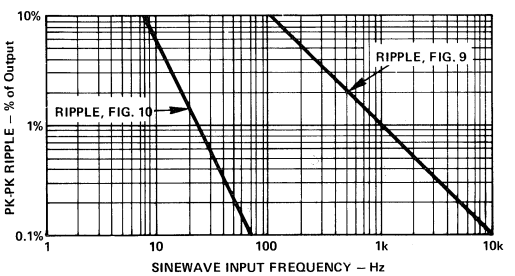


Figure 11. Ripple for Figures 9 & 10; C_f = 1μF

Figures 12 and 13 make it easy to determine capacitance and settling time to <1%, for a desired percentage ripple and a given lower input frequency, f_L.

1. Determine the lowest frequency, f_L, for which an output ripple of either 1% or 0.1% is desired.
2. Referring to Figure 12, find the value of capacitance, C_1, as the ordinate corresponding to the intersection of f_L and the 1% or 0.1% ripple lines.
3. Calculate values of C_f, C_2 and C_3: $C_f = C_1 - 0.1\mu F$; $C_2 = \frac{1}{2}C_1$; $C_3 = 0.7C_2$. Refer to Figure 6 to estimate the low frequency errors corresponding to the selected value of C_f.
4. To find the settling time to <1%, use f_L corresponding to 1% ripple for the chosen C_1, and consult Figure 13. Find the value for settling time at the intersection of f_L and each direction of input rms change (increasing and decreasing).
5. The capacitance values calculated are for signals with C.F. ≤ 2. For C.F. = 2 to 10, multiply the capacitance values by 10.

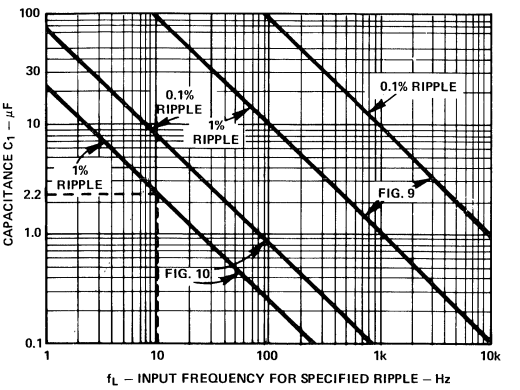


Figure 12. Total capacitance (C_1) as a function of f_L, for 0.1% and 1% pk-pk ripple. For the circuit shown in Figure 10 the resulting capacitor values for 1% ripple at f_L = 10Hz are: C_1 = 2.2μF; C_f = 2.1μF; C_2 = 1.1μF and C_3 = 0.7μF. The settling times are 0.2s (increasing) and 0.4s (decreasing). For corresponding conditions in the circuit of Figure 9, C_1 = 100μF and settling times are 2.8s (increasing) and 4.2s (decreasing).

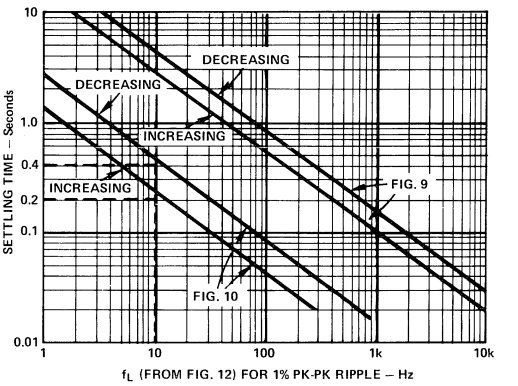


Figure 13. Settling Time to 1% of Step Change of RMS for the Circuits of Figures 9 and 10 as a Function of f_L.

ACCURACY AND SIGNAL CREST FACTOR

Accuracy of true rms measurements on waveforms other than sinewaves is determined from the signal crest factor. Figure 14 is a curve of reading error for crest factors from 1 to 10. In this figure, a $1V_{rms}$ pulse train with variable duty cycle and peak amplitude was selected because of its ability to generate a wide range of crest factors by simply varying the duty cycle (C.F. = $1/\sqrt{\eta}$.) Pulse width is held constant at 200μs to eliminate effects of high frequency error caused by narrow pulse width. RMS level is held constant at 1 volt by varying pulse amplitude. C_f was chosen to be 10μF to minimize the effects of low frequency error.

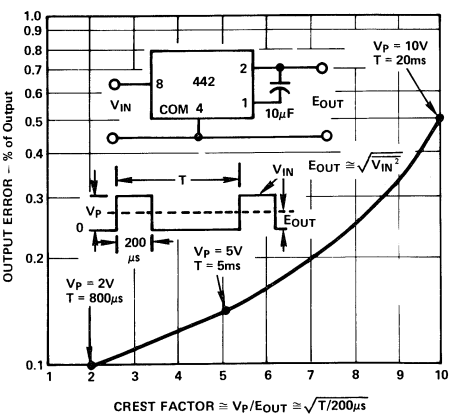


Figure 14. Trimmed Output Error Versus Crest Factor

Transducers and References

Selection Guide
Transducers and References

	MODEL	CHARACTERISTIC	PAGE
VOLTAGE REFERENCES	AD580J/K/L/M/S/T/U	Monolithic 3-terminal 2.5V @ 10mA reference. Output voltage to within ±1% (M, U), less than 10mV line regulation (4.5V to 30V), 10mV max load regulation (10mA change), and 10ppm/°C change with temperature (M, U).	241
	AD581J/K/L/S/T/U	Monolithic 3-terminal laser-trimmed 10.000V ±5mV @ 10mA voltage reference. Tempcos trimmed to within 5ppm/°C max (0 to +70°C – L), and 10ppm/°C max (–55°C to +125°C – U). Can be used in 2-terminal connection as high-performance "Zener diode" for positive or negative reference voltage.	245
	AD2700J/L/S	Hybrid high-accuracy +10V ±2.5mV (L, U) @ 10mA, 3ppm/°C (L, S, U).	265
	AD2701J/L/S	Hybrid high-accuracy –10V ±2.5mV (L, U) @ 10mA, 3ppm/°C (L, S, U)	265
	AD2702J/L/S	Hybrid high-accuracy dual ±10V ±2.5mV (L, U) @ 10mA, 3ppm/°C (U).	265
TRANSDUCERS	AD590J/K/L	Monolithic 2-terminal temperature-to-current transducer that passes a current numerically equal to the device temperature, in degrees Kelvin (1μA/°K), when a dc excitation voltage, from +4V to +30V is applied. Laser-trimmed to ±1°C calibration accuracy (L). Linear to within ±0.5°C over –55°C to +150°C temperature range (K, L). Low cost. Small TO-52 case, isolated from circuitry.	251
SCANNING DIGITAL THERMOMETER	AD2036	6-Channel scanning digital thermometer. Accepts inputs from six external thermocouples (J, K, or T), provides switching, cold-junction compensation, linearizing, conconversion, °F or °C display (0.5″, 13mm LED's), and parallel BCD output – including channel identification. Will drive printer. Scans continuously or one-cycle-at-a-time. Channels individually addressable or manually switchable. Line-powered with ±350V peak max isolation.	259
MISCELLANEOUS	AD537J/K/S	Monolithic V/f converter, can be configured as a T/V or T/f converter. 14-pin package, 0 to +70°C (J, K) or –55°C to +125°C (S), 1mV/°K output can be scaled for arbitrary T/f ranges. ±5mV initial error, ±0.1°K nonlinearity, ±0.02mV/°K slope error. Reference output voltage: 1V ± 5%, 100μV/°C max tempco.	475

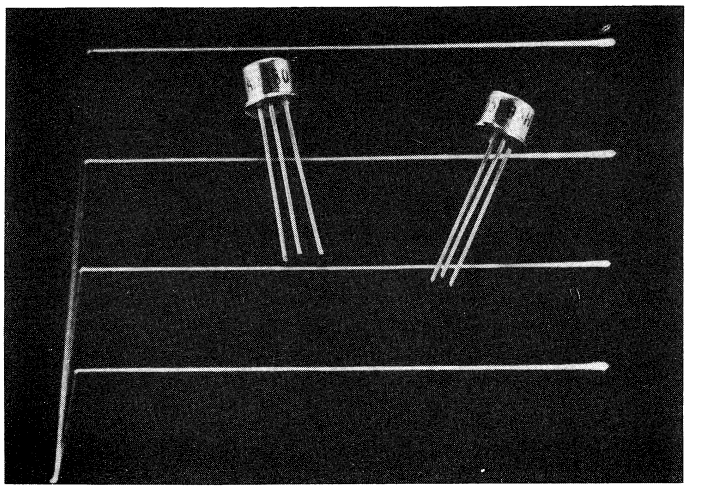
ANALOG DEVICES

Integrated Circuit Low Drift Voltage Reference

AD580

FEATURES

3-Terminal Device:
Voltage In/Voltage Out
V_{OUT} = 2.5V ±1%: 4.5V < V_{IN} < 30V
Excellent Temperature Stability:
10ppm/°C (AD580M)
10ppm/°C (AD580U)
Excellent Long Term Stability: 250μV (25μV/month)
Low Quiescent Current: 1.0mA max
Small IC Package: TO-52 Can
10mA Current Output Capability
Low Cost



PRODUCT DESCRIPTION

The AD580 is a three-terminal, low cost, temperature compensated, bandgap voltage reference which provides a fixed 2.5V output voltage for inputs between 4.5V and 30V. A unique combination of advanced circuit design and sophisticated thin film resistor processing capability provides the AD580 with a temperature stability of better than 10ppm/°C and long term stability of better than 250μV. In addition, the low quiescent current drain of 1.0mA max offers a clear advantage over classical zener techniques.

The AD580 is recommended as a stable reference for all 8, 10, and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD580, allowing operation with 5 volt logic supplies, makes the AD580 a good choice for all digital panel meter applications.

The AD580J, K, L and M are specified for operation over the 0 to +70°C temperature range; the AD580S, T and U are specified for operation over the extended temperature range of −55°C to +125°C.

PRODUCT HIGHLIGHTS

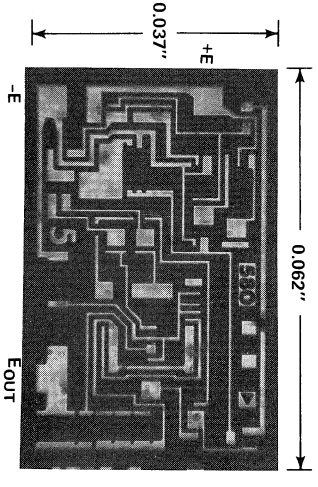
1. The three-terminal voltage in/voltage out operation of the AD580 provides regulated output voltage without any external components.
2. The AD580 provides a stable 2.5V output voltage for input voltages between 4.5V and 30V. The capability to provide a stable output voltage using a 5-volt input makes the AD580 an ideal choice for panel meter applications.
3. Thin film resistor technology and tightly controlled bipolar processing provide the AD580 with temperature stabilities below 10ppm/°C and long term stability better than 250μV.
4. The low quiescent current drain and fast turn-on time of the AD580 make it ideal for CMOS and other low power system applications.
5. Every AD580 is baked for 48 hours at +200°C, temperature cycled 10 times from −65°C to +150°C, and receives a high impact shock test.

SPECIFICATIONS (typical @ E_{in} = +15V and 25°C unless otherwise specified)

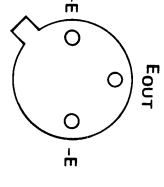
MODEL	AD580J	AD580K	AD580L	AD580M	AD580S	AD580T	AD580U
ABSOLUTE MAX RATINGS							
Input Voltage	40V E_{in}	*	*	*	*	*	*
Power Dissipation @ +25°C							
Ambient Temperature	350mW	*	*	*	*	*	*
Derate Above +25°C	2.8mW/°C	*	*	*	*	*	*
Operating Junction Temp Range	−55°C to +150°C	*	*	*	*	*	*
Storage Temperature Range	−65°C to +175°C	*	*	*	*	*	*
Lead Temperature (soldering, 10 sec)	+300°C	*	*	*	*	*	*
Thermal Resistance							
Junction-to-Case	100°C/W	*	*	*	*	*	*
Junction-to-Ambient	360°C/W	*	*	*	*	*	*
Operating Temperature Range	0 to +70°C	*	*	*	−55°C to +125°C	−55°C to +125°C	−55°C to +125°C
OUTPUT VOLTAGE	2.425V min (2.575V max)	2.450V min (2.550V max)	**	2.475 min (2.525 max)	2.425V min (2.575V max)	**	2.475 min (2.525 max)
OUTPUT TURN-ON SETTLING TIME[1]	6.0μs to 0.04%	*	*	*	*	*	*
OUTPUT VOLTAGE CHANGE							
T_{min} to T_{max}	15mV max (85ppm/°C)	7mV max (40ppm/°C)	4.3mV max (25ppm/°C)	1.75mV max (10ppm/°C)	25mV max (55ppm/°C)	11mV max (25ppm/°C)	4.5mV max (10ppm/°C)
LINE REGULATION							
$7V \leqslant V_{IN} \leqslant 30V$	6mV max (0.6mV typ)	4mV max (0.6mV typ)	2mV max	2mV max	6mV max (0.6mV typ)	2mV max	2mV max
$4.5V \leqslant V_{IN} \leqslant 7V$	3mV max (0.3mV typ)	2mV max (0.3mV typ)	1mV max	1mV max	3mV max (0.3mV typ)	1mV max	1mV max
LOAD REGULATION							
ΔI = 10mA	10mV max	*	*	*	*	*	*
QUIESCENT CURRENT	1.5mA max (1.0mA typ)	*	*	*	*	*	*
NOISE (0.1 to 10Hz)	60μV(p-p)	*	*	*	*	*	*
STABILITY							
Long Term	250μV	*	*	*	*	*	*
Per Month	25μV	*	*	*	*	*	*

NOTE 1: Self-heating time constant will depend on heat sinking, raw supply voltage and load conditions.

*Specification same as AD580J.
**Specification same as AD580K.
Specifications and prices subject to change without notice.



BONDING DIAGRAM

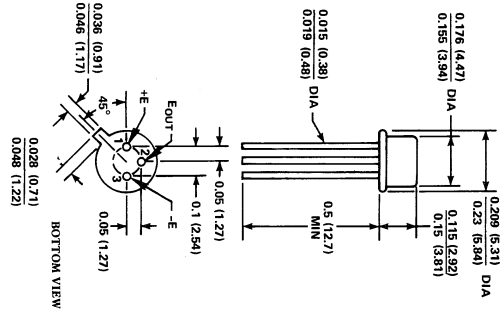


BOTTOM VIEW

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

CASE 27 TO-52 PACKAGE



VOLTAGE VARIATION VS. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references are characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of the inconsistent nonlinearities, in zener references (butterfly or "S" type characteristics), manufacturers began to use a maximum limit error band approach to characterize their references. This technique measures the output voltage at 3 to 5 different temperatures and guarantees that the output voltage deviation will fall within the guaranteed error band at these discrete temperatures. This approach, of course, makes no mention or guarantee of performance at any other temperature within the operating temperature range of the device.

The consistent Voltage vs. Temperature performance of a typical AD580 is shown in Figure 1. Note that the characteristic is quasi parabolic, eliminating the possible "S" type characteristics of classical zener references. This parabolic characteristic permits a maximum output deviation specification over the devices' full operating temperature range, rather than just at 3 to 5 discrete temperatures.

The AD580M guarantees a maximum deviation of 1.75mV over the 0 to +70°C temperature range. This can be shown to be equivalent to 40ppm/°C average maximum; i.e. . . . .

$$\frac{1.75\text{mV max}}{70^\circ\text{C}} \times \frac{1}{2.5\text{V}} = 10\text{ppm}/^\circ\text{C max average}$$

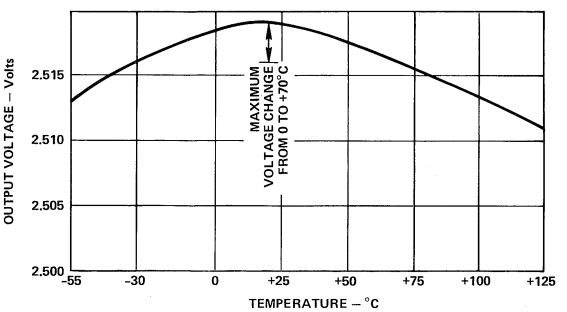


Figure 1. AD580K Output Voltage vs. Temperature

NOISE PERFORMANCE

Figure 2 represents the peak-to-peak noise of the AD580 from 1Hz (3dB point) to a 3dB high end shown on the horizontal axis. Peak-to-peak noise from 1Hz to 1MHz is approximately 600μV.

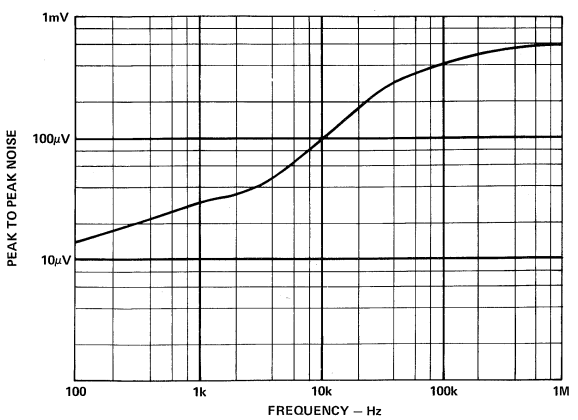


Figure 2. Peak-to-Peak Output Noise vs. Frequency

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for needed operation. Figure 3 displays the turn-on characteristic of the AD580. Note that the AD580 settles to within 1mV (0.04%) within 5μs after power turn-on.

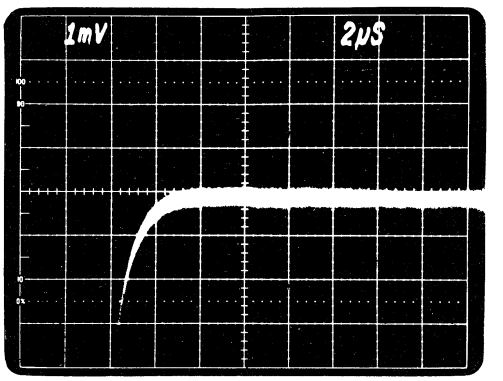


Figure 3. Turn-On Characteristic

APPLICATIONS INFORMATION

THE AD580 AS A REFERENCE FOR A 12-BIT D/A CONVERTER

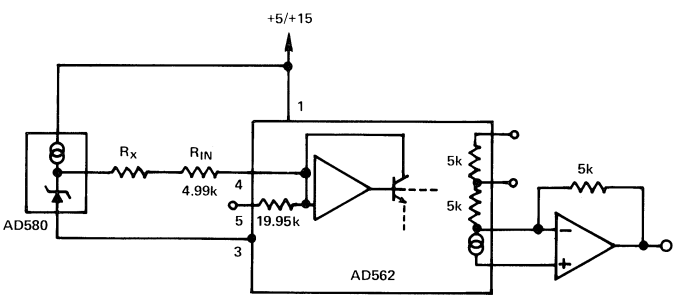


Figure 4. The AD580 As A Reference For The AD562 12-Bit D/A Converter

The AD562, like most D/A converters, is designed to operate with a +10 volt reference element. In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor. The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k span resistors.

As illustrated in Figure 4, the AD580 may be used to generate the 0.5mA reference current via an external 4.99k resistor. The external 5k span resistor, used as feedback in an op amp, converts the AD562's output current to an output voltage.

The overall DAC's worst case gain temperature coefficient in this configuration would be: T.C. of AD580 + T.C. of external resistors + T.C. of AD562. Using an AD580M, external resistors that track at 1ppm/°C, and an AD562K we get:

$$(10\text{ppm/°C} + 1\text{ppm/°C} + 3\text{ppm/°C}) = 14\text{ppm/°C},$$
worst case

or

$$\sqrt{(10)^2 + (1)^2 + (3)^2} = 10.5\text{ppm/°C RSS}$$

Note: Internal resistors of the AD562 display -30ppm/°C absolute temperature coefficient. Their tracking coefficient is less than 2ppm/°C.

THE AD580 AS A CURRENT LIMITER

The AD580 represents an excellent alternative to current limiter diodes which require factory-selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD580 approach is not limited to a specially selected factory set current limit; it can be programmed from 1 to 10mA with the insertion of a single external resistor. The approximate temperature coefficient of current limit for the AD580 used in this mode is 0.13%/°C for I_{Lim} = 1mA and 0.01%/°C for I_{Lim} = 13mA (see Figure 6). Figure 5 displays the high output impedance of the AD580 used as a current limiter for I_{Lim} = 1, 2, 3, 4, 5mA.

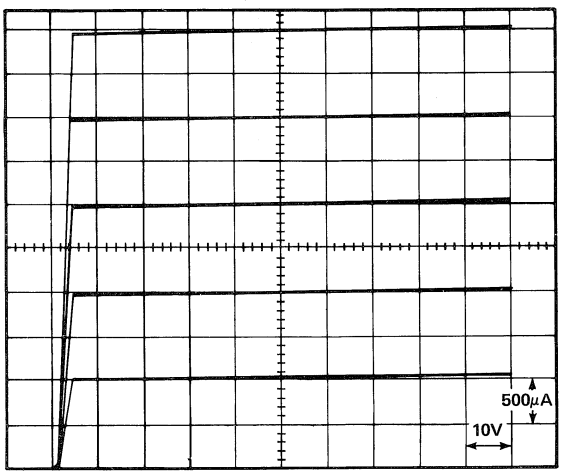


Figure 5. Input Current vs. Input Voltage (Integral Loads)

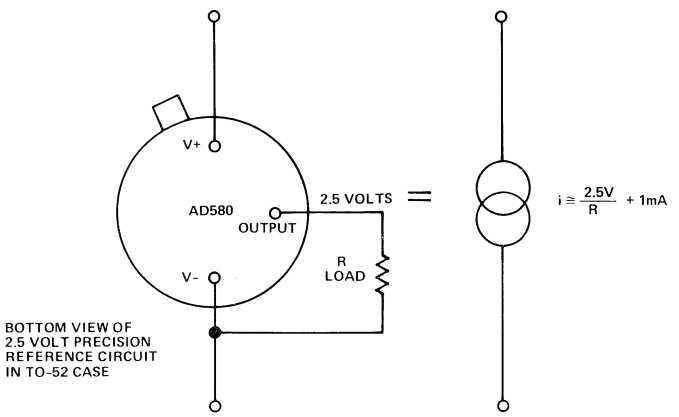


Figure 6. A Two-Component Precision Current Limiter

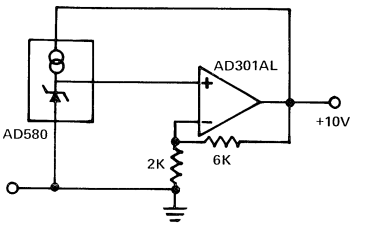


Figure 7. "Bootstrapped" 10 Volt Reference Using the AD580. (Circuit Configuration Courtesy of Walter G. Jung.)

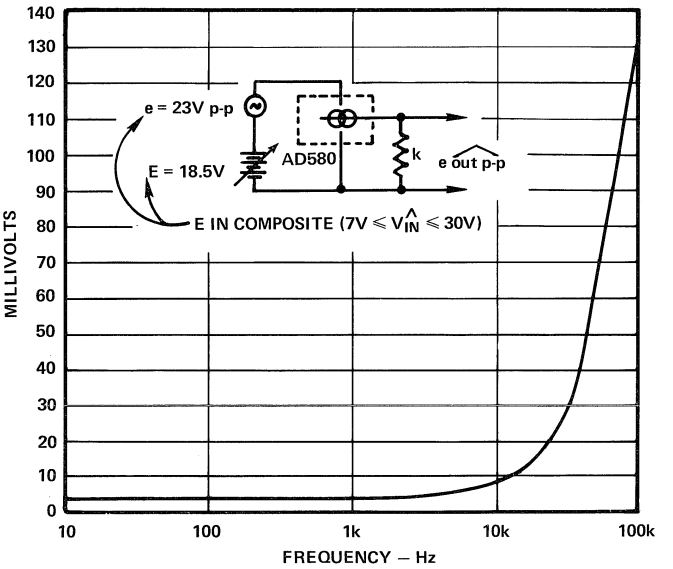
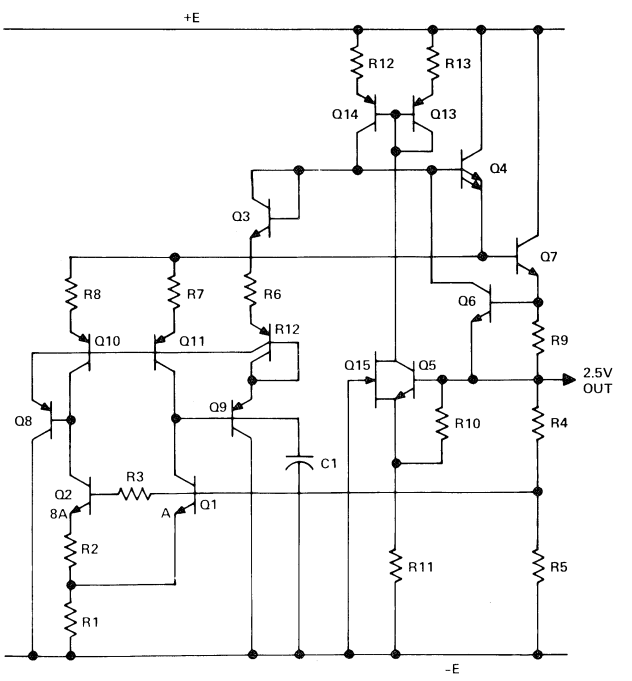


Figure 8. AD580 Line Regulation Plot

SCHEMATIC DIAGRAM



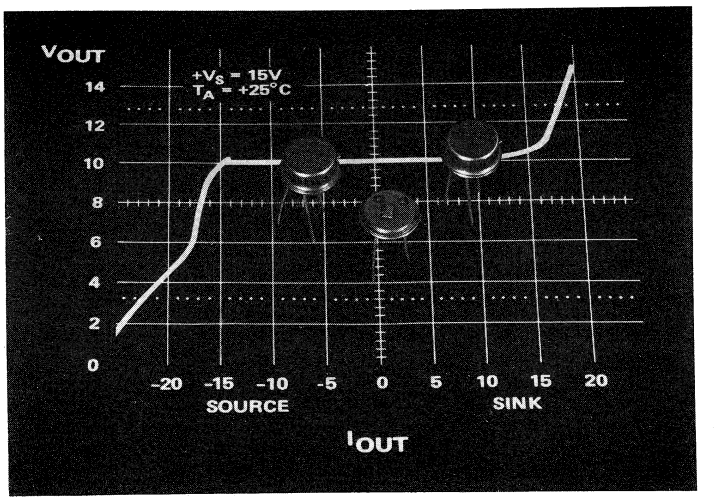
ANALOG DEVICES

High Precision 10 Volt IC Reference

AD581

FEATURES

Laser-Trimmed to High Accuracy:
10.000 Volts ±5mV (L and U)
Trimmed Temperature Coefficient:
5ppm/°C max, 0 to +70°C (L)
10ppm/°C max, -55°C to +125°C (U)
Excellent Long-Term Stability:
25ppm/1000 hrs. (Non-Cumulative)
Negative 10 Volt Reference Capability
Low Quiescent Current: 1.0mA max
10mA Current Output Capability
3-Terminal TO-5 Package
Low Cost



PRODUCT DESCRIPTION

The AD581 is a three-terminal, temperature compensated, monolithic band-gap voltage reference which provides a precise 10.00 volt output from an unregulated input level from 12 to 40 volts. Laser Wafer Trimming (LWT) is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in high precision performance previously available only in expensive hybrids or oven-regulated modules. The 5mV initial error tolerance and 5ppm/°C guaranteed temperature coefficient of the AD581L represent the best performance combination available in a monolithic voltage reference.

The band-gap circuit design used in the AD581 offers several advantages over classical zener breakdown diode techniques. Most important, no external components are required to achieve full accuracy and stability of significance to low power systems. In addition, total supply current to the device, including the output buffer amplifier (which can supply up to 10mA) is typically 750μA. The long-term stability of the band-gap design is equivalent or superior to selected zener reference diodes.

The AD581 is recommended for use as a reference for 8, 10 or 12 bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD581J, K, and L are specified for operation from 0 to +70°C; the AD581S, T, and U are specified for the -55°C to +125°C range. The AD581S, T, and U grades are also available processed to MIL-STD-883A, Level B. All grades are packaged in a hermetically-sealed three-terminal TO-5 metal can.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD581L has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C, while the AD581U guarantees ±15mV maximum total error without external trims from -55°C to +125°C.
2. Since the laser trimming is done on the wafer prior to separation into individual chips, the AD581 will be extremely valuable to hybrid designers for its ease of use, lack of required external trims, and inherent high performance.
3. The AD581 can also be operated in a two-terminal "Zener" mode to provide a precision negative 10 volt reference with just one external resistor to the unregulated supply. The performance in this mode is nearly equal to that of the standard three-terminal configuration.
4. Advanced circuit design using the band-gap concept allows the AD581 to give full performance with an unregulated input voltage down to 12 volts. With an external resistor, the device will operate with a supply as low as 11.4 volts.
5. Every AD581 is baked for 48 hours at +200°C, temperature cycled 10 times from -65°C to +150°C, burned-in under power for 48 hours at +125°C, and given a high G shock test prior to final test to ensure reliability and long-term stability.

SPECIFICATIONS (typical @ V_{IN} = +15V and +25°C unless otherwise noted)

MODEL	AD581J	AD581K	AD581L	AD581S	AD581T	AD581U
ABSOLUTE MAX RATINGS						
Input Voltage V_{IN} to Ground	40V	*	*	*	*	*
Power Dissipation @ +25°C	600mW	*	*	*	*	*
Operating Junction Temp. Range	−55°C to +150°C	*	*	*	*	*
Storage Temperature Range	−65°C to +175°C	*	*	*	*	*
Lead Temperature (Soldering, 10sec)	+300°C	*	*	*	*	*
Thermal Resistance Junction-to-Ambient	150°C/Watt	*	*	*	*	*
Operating Temperature Range	0 to +70°C	*	*	−55°C to +125°C	**	**
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10.000V output)	±30mV max	±10mV max	±5mV max	±30mV max	±10mV max	±5mV max
OUTPUT VOLTAGE CHANGE Maximum Deviation from +25°C Value T_{min} to T_{max} (Temperature Coefficient)	±13.5mV (30ppm/°C)	±6.75mV (15ppm/°C)	±2.25mV (5ppm/°C)	±30mV (30ppm/°C)	±15mV (15ppm/°C)	±10mV (10ppm/°C)
LINE REGULATION						
$15V \leq V_{IN} \leq 30V$	3mV max (0.002%/V)	*	*	*	*	*
$13V \leq V_{IN} \leq 15V$	1mV max (0.005%/V)	*	*	*	*	*
LOAD REGULATION						
$0 \leq I_{OUT} \leq 5mA$	500µV/mA max	*	*	*	*	*
	200µV/mA typ	*	*	*	*	*
QUIESCENT CURRENT	1.0mA max	*	*	*	*	*
	750µA typ	*	*	*	*	*
TURN-ON SETTLING TIME TO 0.1%[1]	200µs	*	*	*	*	*
NOISE (0.1 to 10Hz)	50µV p-p	*	*	*	*	*
LONG-TERM STABILITY	25ppm/1000 Hrs. (Non-Cumulative)	*	*	*	*	*
SHORT CIRCUIT CURRENT	30mA	*	*	*	*	*
OUTPUT CURRENT						
Source @ +25°C	10mA min	*	*	*	*	*
Source T_{min} to T_{max}	5mA min	*	*	*	*	*
Sink T_{min} to T_{max}	5mA min	*	*	200µA min	**	**
Sink −55°C to +85°C	—	—	—	5mA min	**	**

*Specifications same as AD581J.
**Specifications same as AD581S.
[1] See Figure 8.
Specifications and prices subject to change without notice.

APPLYING THE AD581

The AD581 is easy to use in virtually all precision reference applications. The three terminals are simply primary supply, ground, and output, with the case grounded. No external components are required even for high precision applications; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD581 requires less than 1mA quiescent current from an operating supply range of 12 to 40 volts.

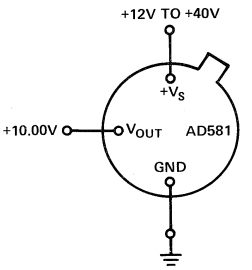
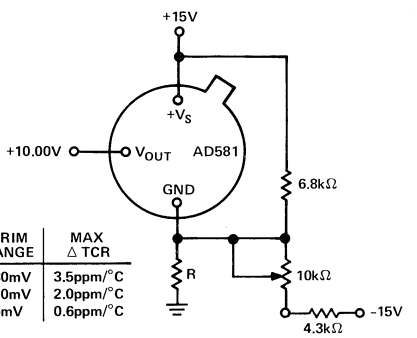


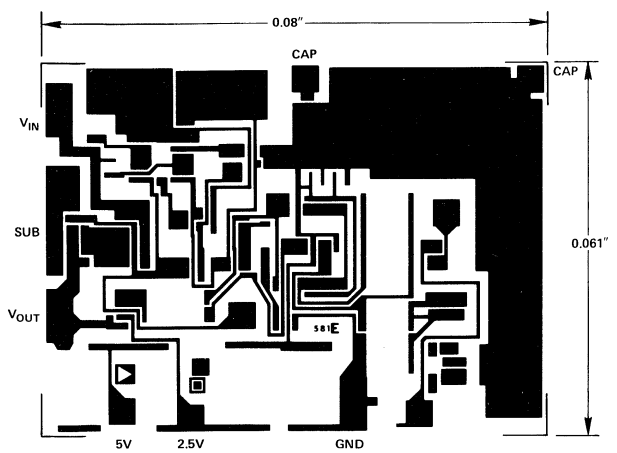
Figure 1. AD581 Pin Configuration (Top View)

An external fine trim may be desired to set the output level to exactly 10.000 volts within less than a millivolt (calibrated to a main system reference). System calibration may also require a reference slightly different from 10.00 volts. In either case, the optional trim circuit shown in Figure 2 can offset the output by up to ±30 millivolts (with the 22Ω resistor), if needed, with minimal effect on other device characteristics.



R	TRIM RANGE	MAX Δ TCR
22Ω	±30mV	3.5ppm/°C
12Ω	±10mV	2.0ppm/°C
3.9Ω	±5mV	0.6ppm/°C

Figure 2. Optional Fine Trim Configuration



THE AD581 IS ALSO AVAILABLE IN LASER-TRIMMED CHIP FORM WITH ALL SPECIFICATIONS GUARANTEED TO J-GRADE. THE CHIP HAS ADDITIONAL APPLICATION FLEXIBILITY NOT AVAILABLE IN THE THREE-TERMINAL PACKAGED DEVICE. CONSULT FACTORY FOR FURTHER DETAILS.

Figure 3. AD581 Bonding Diagram

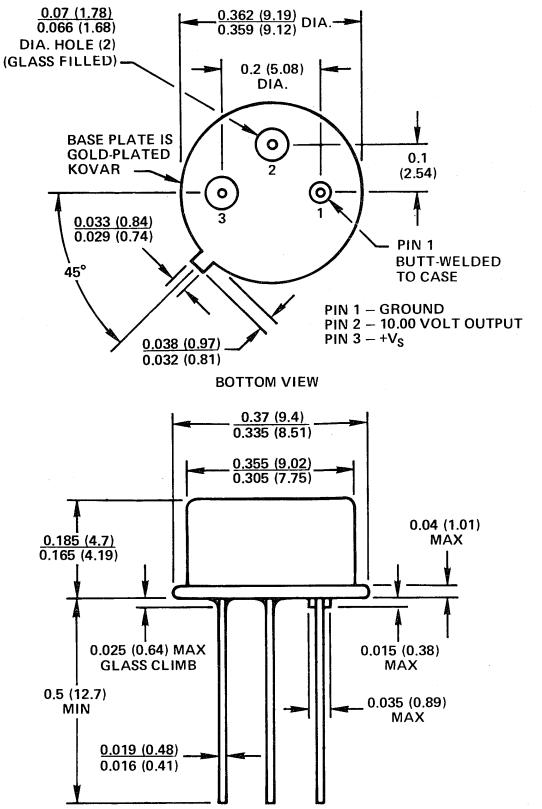


Figure 4. Outline Dimensions and Pin Designations. Dimensions shown in inches and (mm).

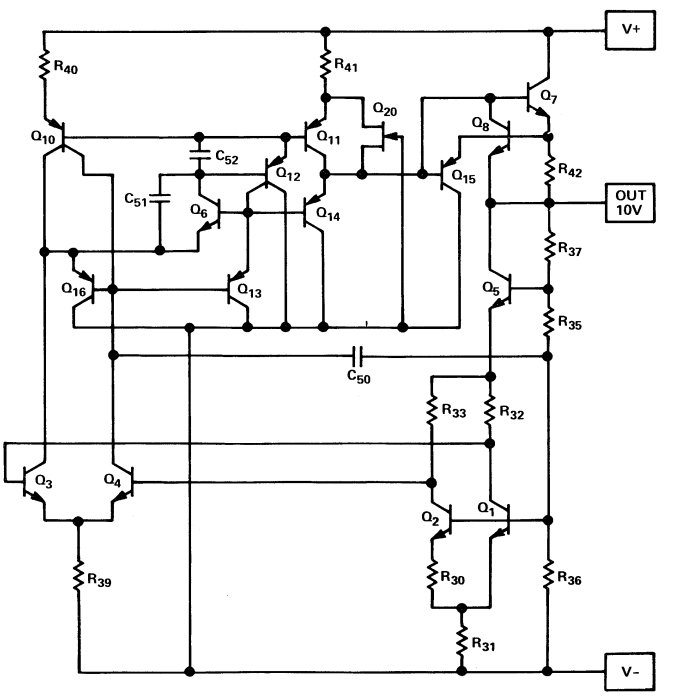


Figure 5. Simplified Schematic

VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD581 consistently follows the S-curve shown in Figure 6. Five-point measurement of each device guarantees the error band over the -55°C to +125°C range; three-point measurement guarantees the error band from 0 to +70°C.

The error band which is guaranteed with the AD581 is the maximum deviation from the initial value at +25°C; this error band is of more use to a designer than one which simply guarantees the maximum total change over the entire range (i.e., in the latter definition, all of the changes could occur in the positive direction). Thus, with a given grade of the AD581, the designer can easily determine the maximum total error from initial tolerance plus temperature variation (e.g., for the AD581T, the initial tolerance is ±10mV, the temperature error band is ±15mV, thus the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C).

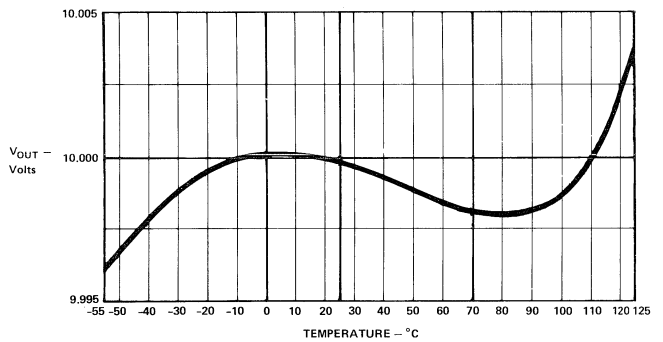


Figure 6. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD581 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device are shown in Figure 7. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

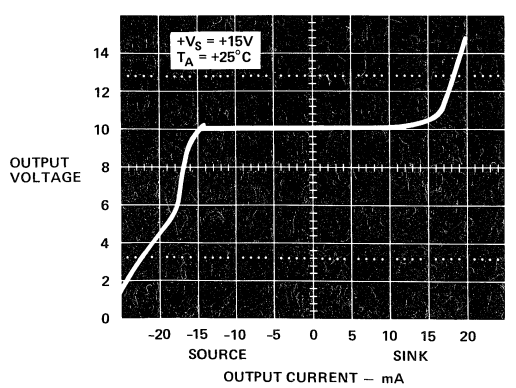


Figure 7. AD581 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 8 displays the turn-on characteristic of the AD581. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 180μs, and there is no long thermal tail appearing after the point.

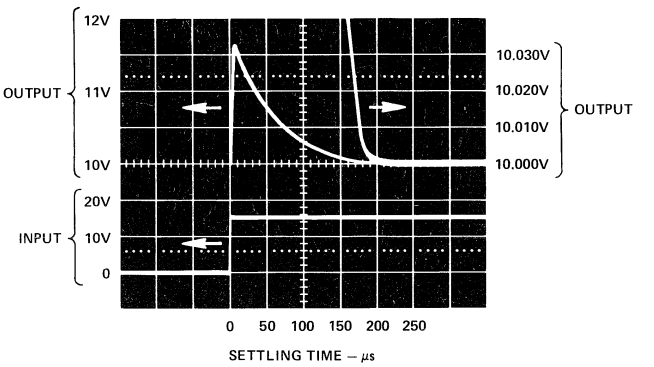


Figure 8. Output Settling Characteristic

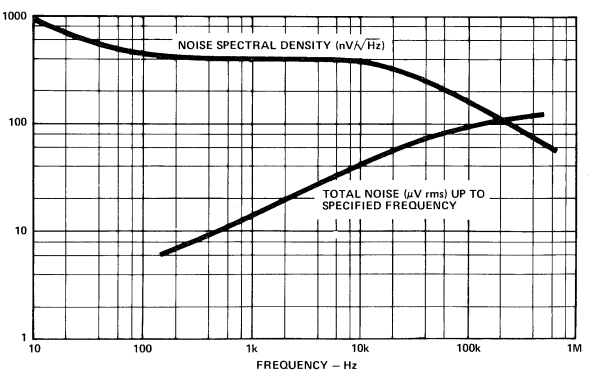


Figure 9. Spectral Noise Density and Total rms Noise vs. Frequency

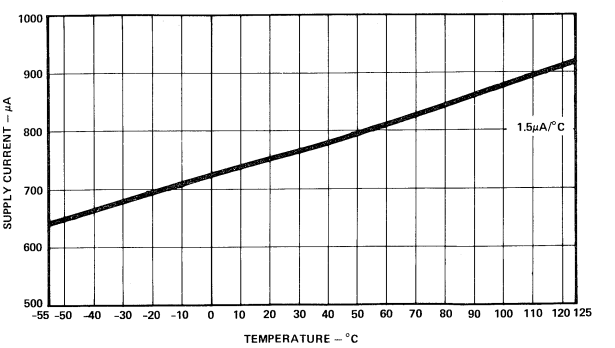


Figure 10. Quiescent Current vs. Temperature

PRECISION HIGH CURRENT SUPPLY

The AD581 can be easily connected with power pnp or power darlington pnp devices to provide much greater output current capability. The circuit shown in Figure 11 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

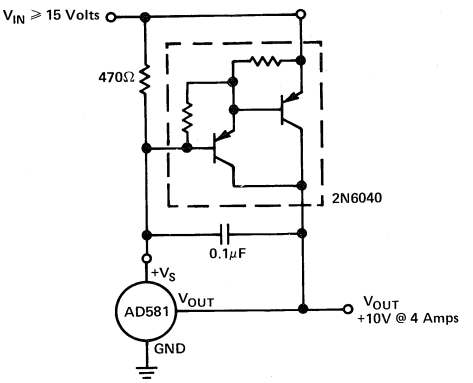


Figure 11. High Current Precision Supply

CONNECTION FOR REDUCED PRIMARY SUPPLY

While line regulation is specified down to 13 volts, the typical AD581 will work as specified down to 12 volts or below. The current sink capability allows even lower supply voltage capability such as operation from 12V ±5% as shown in Figure 12. The 560Ω resistor reduces the current supplied by the AD581 to a manageable level at full 5mA load. Note that other bandgap references, without current sink capability, may be damaged by use in this circuit configuration.

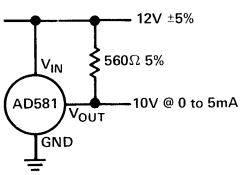


Figure 12. 12 Volt Supply Connection

THE AD581 AS A CURRENT LIMITER

The AD581 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD581 approach is not limited to a defined set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor. Of course, the minimum voltage required to drive the connection is 13 volts. The AD580, which is a 2.5 volt reference, can be used in this type of circuit with compliance voltage down to 4.5 volts.

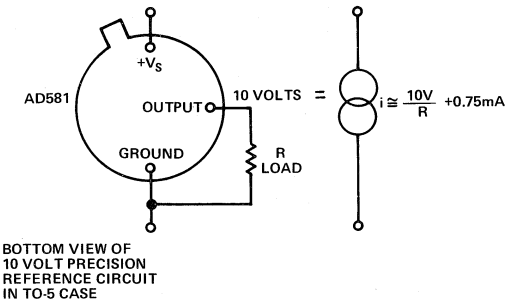


Figure 13. A Two-Component Precision Current Limiter

NEGATIVE 10-VOLT REFERENCE

The AD581 can also be used in a two-terminal "zener" mode to provide a precision -10.00 volt reference. As shown in Figure 14, the V_{IN} and V_{OUT} terminals are connected together to the high supply (in this case, ground). The ground pin is connected through a resistor to the negative supply. The output is now taken from the ground pin instead of V_{OUT}. With 1mA flowing through the AD581 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2 ohms. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD581 is always between 1 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD581 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 10.5 volts. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD581 always remains within its regulating range of 1 to 5mA.

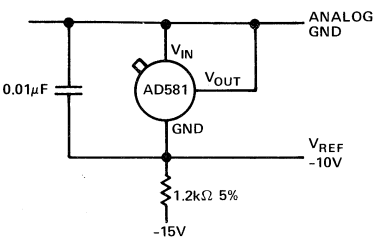


Figure 14. Two-Terminal -10 Volt Reference

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD581 is ideal for application with the entire AD7520 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7570 10-bit A/D converter. In the standard hook-up, as shown in Figure 15, the +10 volt reference is inverted by the amplifier/DAC configuration to produce a 0 to -10 volt range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. If a 0 to +10 volt full scale range is desired, the AD581 can be connected to the CMOS DAC in its -10 volt "zener" mode, as shown in Figure 14 (the $-10V_{REF}$ output is connected directly to the $V_{REF\ IN}$ of the CMOS DAC). The AD581 will normally be used in the -10 volt mode with the AD7570 to give a 0 to +10 volt ADC range. This is shown in Figure 16. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

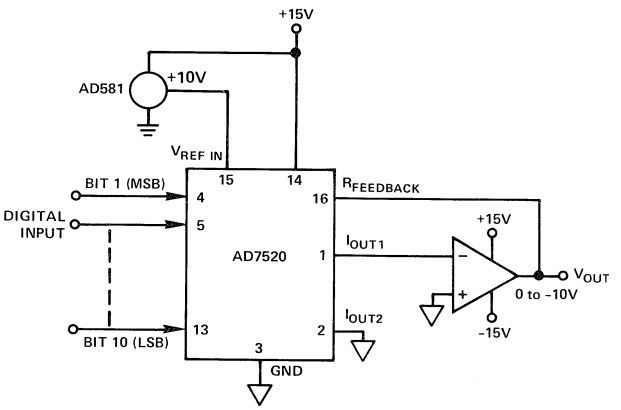


Figure 15. Low Power 10-Bit CMOS DAC Application

PRECISION 12-BIT D/A CONVERTER REFERENCE

The AD562, like most D/A converters, is designed to operate with a +10 volt reference element. In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD581L (at 5ppm/°C) as the 10 volt reference guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C.

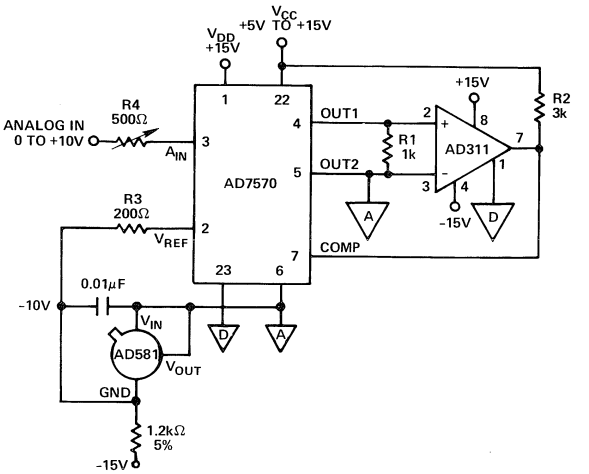


Figure 16. AD581 as Negative 10 Volt Reference for CMOS ADC

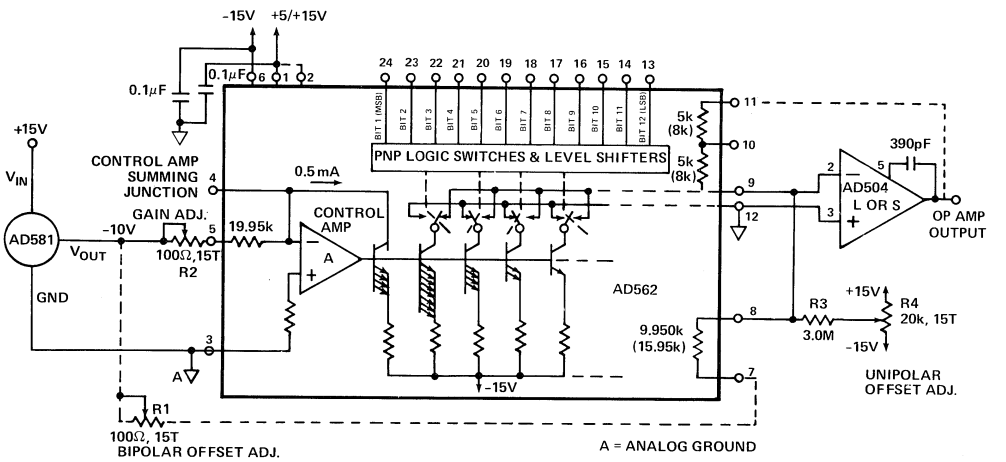
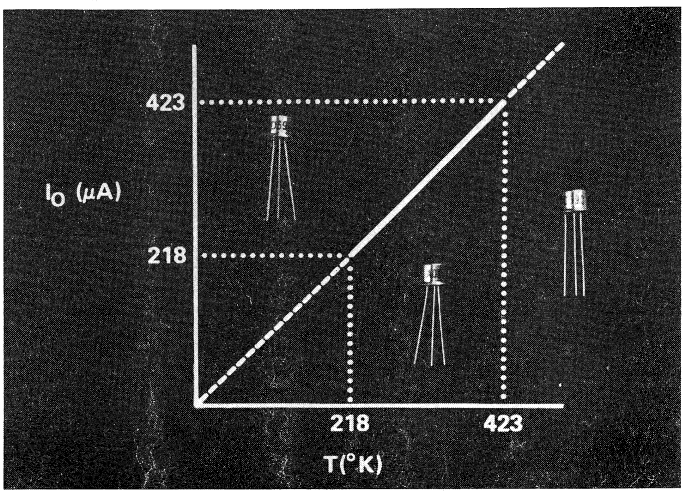


Figure 17. Precision 12-Bit D/A Converter

Two-Terminal IC Temperature Transducer

AD590

FEATURES
Linear Current Output: 1μA/°K
Wide Range: -55°C to +150°C
Two-Terminal Device: Voltage In/Current Out
Laser Trimmed to ±1°C Calibration Accuracy (AD590L)
Excellent Linearity: ±0.5°C Over Full Range (AD590K, L)
Wide Power Supply Range: +4V to +30V
Sensor Isolation from Case
Low Cost



PRODUCT DESCRIPTION

The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between +4V and +30V the device acts as a high impedance, constant current regulator passing 1μA/°K. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2°K (+25°C).

The AD590 should be used in any temperature sensing application below +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance–measuring circuitry and cold junction compensation are not needed in applying the AD590. In the simplest application a resistor, a power source and any voltmeter can be used to measure Kelvin temperature.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, and biasing proportional to absolute temperature. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

PRODUCT HIGHLIGHTS

1. The AD590 is a calibrated two terminal temperature sensor requiring only a dc voltage supply (+4V to +30V). Costly transmitters, filters, lead wire compensation and linearization circuits are all unnecessary in applying the device.
2. State-of-the-art laser trimming at the wafer level in conjunction with extensive final testing insures that AD590 units are easily interchangeable. The absolute calibration of the device is excellent (±1°C, AD590L).
3. The device enjoys excellent linearity (±0.5°C, AD590L) over the entire temperature range.
4. Superior interference rejection results from the output being a current rather than a voltage. In addition, power requirements are low (1.5mW's @ 5V @ +25°C). These features make the AD590 easy to apply as a remote sensor.
5. The high output impedance (>10MΩ) provides excellent rejection of supply voltage drift and ripple. For instance, changing the power supply from 5V to 15V results in only a 1μA maximum current change, or 1°C equivalent error.
6. The AD590 is electrically durable: it will withstand a forward voltage up to 44V and a reverse voltage of 20V. Hence, supply irregularities or pin reversal will not damage the device.
7. The device is hermetically sealed in the TO–52 package. All AD590 grades, J, K and L, are specified over the -55°C to +150°C temperature range. MIL-STD-883 processing to level B is available. The device is also available in chip form; please consult the factory for details.

SPECIFICATIONS (typical @ +25°C and V_S = +5V unless otherwise specified)

MODEL	AD590J	AD590K	AD590L
ABSOLUTE MAXIMUM RATINGS			
Forward Voltage (E+ to E–)	+44V	*	*
Reverse Voltage (E+ to E–)	–20V	*	*
Breakdown Voltage (Case to E+ or E–)	±200V	*	*
Rated Performance Temperature Range	–55°C to +150°C	*	*
Storage Temperature Range	–65°C to +175°C	*	*
Lead Temperature (Soldering, 10sec)	+300°C	*	*
POWER SUPPLY			
Operating Voltage Range	+4V to +30V	*	*
OUTPUT			
Nominal Current Output @ +25°C (298.2°K)	298.2μA	*	*
Nominal Temperature Coefficient	1μA/°C	*	*
Calibration Error[1] @ +25°C	±5.0°C max	±2.0°C max	±1.0°C max
Absolute Error[1] (–55°C to +150°C)			
Without External Calibration Adjustment	±9.0°C max	±3.8°C max	±2.4°C max
With +25°C Calibration Error Set to Zero	±2.0°C max	±1.0°C max	**
Nonlinearity[1] (–55°C to +150°C)	±2.0°C max	±0.5°C max	**
Current Noise	40pA/$\sqrt{\text{Hz}}$	*	*
Power Supply Rejection			
+4V ≤ V_S ≤ +5V	0.5μA/V	*	*
+5V ≤ V_S ≤ +15V	0.2μA/V	*	*
+15V ≤ V_S ≤ +30V	0.1μA/V	*	*
Case Isolation to Either Lead	$10^{10}\Omega$	*	*
Effective Shunt Capacitance	100pF	*	*
Electrical Turn-On Time[2]	20μs	*	*
Reverse Bias Leakage Current[3]			
(Reverse Voltage = 10V)	10pA	*	*

NOTES:
[1] See error explanations page.
[2] Does not include self-heating effects; see page on explanation of these effects.
[3] Leakage current doubles every 10°C.

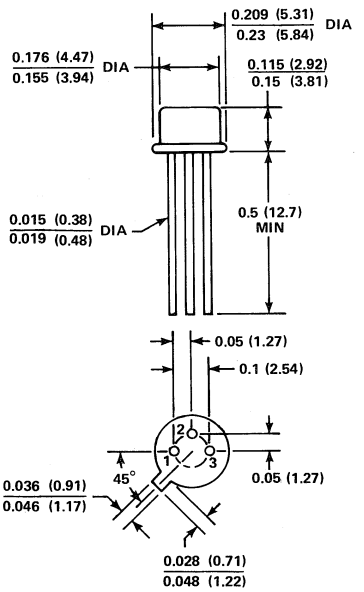
*Specifications same as AD590J.
**Specifications same as AD590K.

Specifications subject to change without notice.

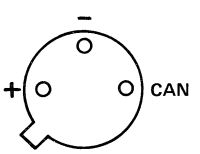
OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).

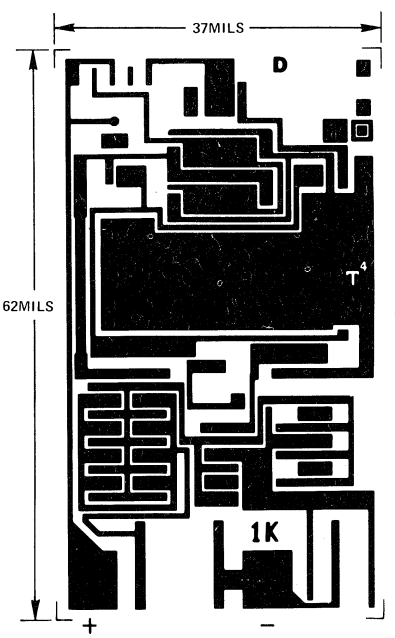
TO-52 PACKAGE



BOTTOM VIEW



BOTTOM VIEW



Metalization Diagram

CIRCUIT DESCRIPTION[1]

The AD590 uses a fundamental property of the silicon transistors from which it is made to realize its temperature proportional characteristic: if two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in their base-emitter voltages will be (kT/q)(In r). Since both k, Boltzman's constant and q, the charge of an electron, are constant, the resulting voltage is directly proportional to absolute temperature (PTAT).

In the AD590, this PTAT voltage is converted to a PTAT current by low temperature coefficient thin film resistors. The total current of the device is then forced to be a multiple of this PTAT current. Referring to Figure 1, the schematic diagram of the AD590, Q8 and Q11 are the transistors that produce the PTAT voltage. R5 and R6 convert the voltage to current. Q10, whose collector current tracks the collector currents in Q9 and Q11, supplies all the bias and substrate leakage current for the rest of the circuit, forcing the total current to be PTAT. R5 and R6 are laser trimmed on the wafer to calibrate the device at +25°C.

Figure 2 shows the typical V–I characteristic of the circuit at +25°C and the temperature extremes.

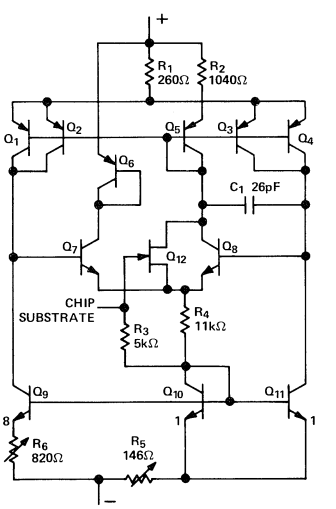


Figure 1. Schematic Diagram

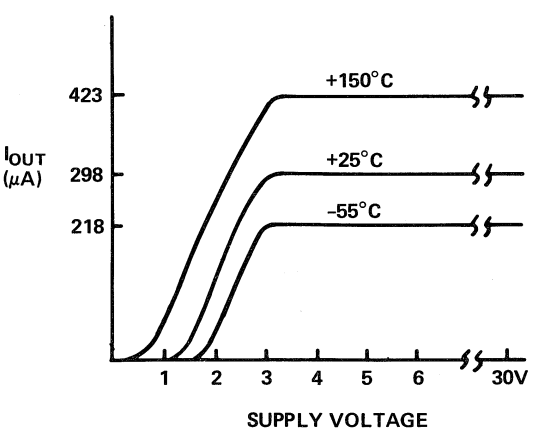


Figure 2. V–I Plot

[1] For a more detailed circuit description see M.P. Timko, "A Two-Terminal IC Temperature Transducer," IEEE J. Solid State Circuits, Vol. SC-11, p. 784-788, Dec. 1976.

EXPLANATION OF TEMPERATURE SENSOR SPECIFICATIONS

The way in which the AD590 is specified makes it easy to apply in a wide variety of different applications. It is important to understand the meaning of the various specifications and the effects of supply voltage and thermal environment on accuracy.

The AD590 is basically a PTAT (proportional to absolute temperature)[1] current regulator. That is, the output current is equal to a scale factor times the temperature of the sensor in degrees Kelvin. This scale factor is trimmed to 1μA/°K at the factory, by adjusting the indicated temperature (i.e. the output current) to agree with the actual temperature. This is done with 5V across the device at a temperature within a few degrees of 25°C (298.2°K). The device is then packaged and tested for accuracy over temperature.

CALIBRATION ERROR

At final factory test the difference between the indicated temperature and the actual temperature is called the calibration error. Since this is a scale factor error, its contribution to the total error of the device is PTAT. For example, the effect of the 1°C specified maximum error of the AD590L varies from 0.73°C at -55°C to 1.42°C at 150°C. Figure 3 shows how an exaggerated calibration error would vary from the ideal over temperature.

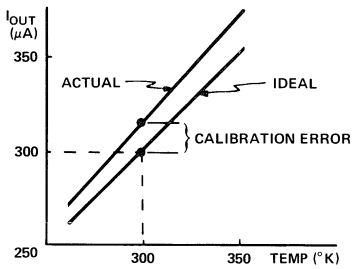


Figure 3. Calibration Error vs. Temperature

The calibration error is the major contributor to maximum total error in all AD590 grades. However, since it is a scale factor error, it is particularly easy to trim. Figure 4 shows the most elementary way of accomplishing this. To trim this circuit the temperature of the AD590 is measured by a reference temperature sensor and R is trimmed so that V_T = 1mV/°K at that temperature. Note that when this error is trimmed out at one temperature, its effect is zero over the entire temperature range. In most applications there is a current to voltage conversion resistor (or, as with a current input ADC, a reference) that can be trimmed for scale factor adjustment.

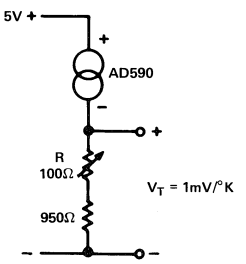


Figure 4. One Temperature Trim

[1] T(°C) = T(°K) - 273.2; Zero on the Kelvin scale is "absolute zero"; there is no lower temperature.

ERROR VERSUS TEMPERATURE: WITH CALIBRATION ERROR TRIMMED OUT

Each AD590 is also tested for error over the temperature range with the calibration error trimmed out. This specification could also be called the "variance from PTAT" since it is the maximum difference between the actual current over temperature and a PTAT multiplication of the actual current at 25°C. This error consists of a slope error and some curvature, mostly at the temperature extremes. Figure 5 shows a typical AD590K temperature curve before and after calibration error trimming.

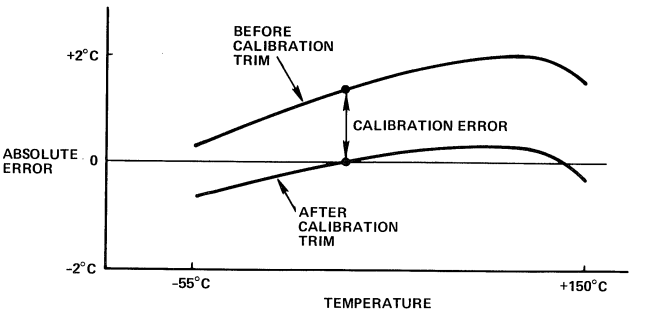


Figure 5. Effect of Scale Factor Trim on Accuracy

ERROR VERSUS TEMPERATURE: NO USER TRIMS

Using the AD590 by simply measuring the current, the total error is the "variance from PTAT" described above plus the effect of the calibration error over temperature. For example the AD590L maximum total error varies from 1.73°C at -55°C to 2.42°C at 150°C. For simplicity, only the larger figure is shown on the specification page.

NONLINEARITY

Nonlinearity as it applies to the AD590 is the maximum deviation of current over temperature from a best-fit straight line. The nonlinearity of the AD590 over the -55°C to +150°C range is superior to all conventional electrical temperature sensors such as thermocouples, RTD's and thermistors. Figure 6 shows the nonlinearity of the typical AD590K from Figure 5.

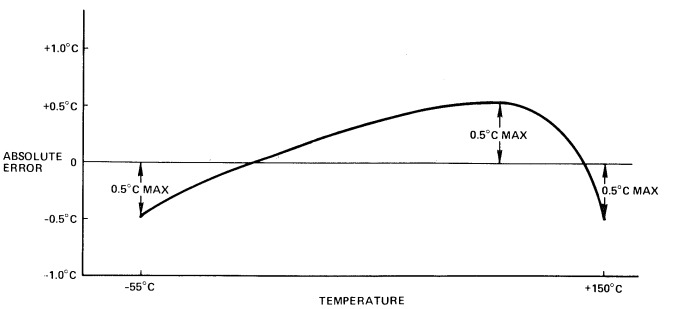


Figure 6. Nonlinearity

Figure 7A shows a circuit in which the nonlinearity is the major contributor to error over temperature. The circuit is trimmed by adjusting R_1 for a 0V output with the AD590 at 0°C. R_2 is then adjusted for 10V out with the sensor at 100°C. Other pairs of temperatures may be used with this procedure as long as they are measured accurately by a reference sensor. Note that for +15V output (150°C) the V+ of the op amp must be greater than 17V.

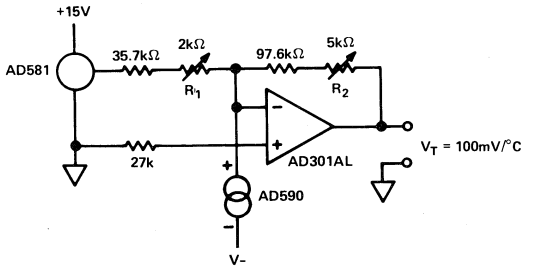


Figure 7A. Two Temperature Trim

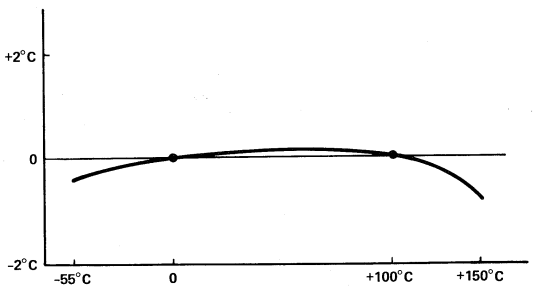


Figure 7B. Typical Two-Trim Accuracy

VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The AD590 specifications are guaranteed for use in a low thermal resistance environment with 5V across the sensor. Changes in these conditions will change the output of the device in such a way that the normal scale factor trim described on previous page will compensate for them.

The power supply rejection specifications given show the maximum expected change in output current versus input voltage changes. The insensitivity of the output to input voltage allows the use of unregulated supplies. It also means that hundreds of ohms of resistance (such as a CMOS multiplexer) can be tolerated in series with the device.

It is important to note that using a supply voltage other than 5V does not change the PTAT nature of the AD590. Thus an output error resulting from the use of a different power supply level is equivalent to a calibration error and can be removed by the scale factor trim (see previous page).

The thermal environment in which the AD590 is used determines two important characteristics: the effect of self heating and the response of the sensor with time.

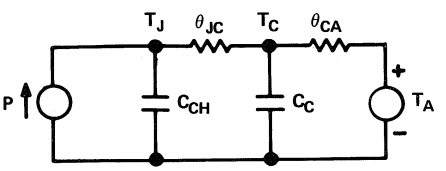


Figure 8. Thermal Circuit Model

Figure 8 is a model of the AD590 which demonstrates these characteristics. θ_{JC} is the thermal resistance between the chip and the case, about 26°C/watt. θ_{CA} is the thermal resistance between the case and its surroundings and is determined by the characteristics of the thermal connection. Power source P represents the power dissipated on the chip. The rise of the junction temperature, T_J, above the ambient temperature T_A is:

$$T_J - T_A = P(\theta_{JC} + \theta_{CA}). \qquad \text{Eq. 1}$$

Table 1 gives the sum of θ_{JC} and θ_{CA} for several common thermal media. The heat-sink used was a common clip-on. Using Equation 1, the temperature rise of an AD590 in a stirred bath at 25°C, when driven with a 5V supply will be 0.06°C. However, for the same conditions in still air the temperature rise is 0.72°C. For a given supply voltage, the temperature rise varies with the current and is PTAT. Therefore, if an application circuit is trimmed with the sensor in the same thermal environment in which it will be used, the scale factor trim compensates for this effect over the entire temperature range.

MEDIUM	$\theta_{JC} + \theta_{CA}$	τ
Aluminum Block	28°C/watt	1.2sec
Stirred Liquid Bath	39°C/watt	3.4sec
Moving Air[1] — Heat Sink	45°C/watt	5.0sec
Moving Air[1] — No Heat Sink	115°C/watt	12.0sec
Still Air — Heat Sink	191°C/watt	108.0sec
Still Air — No Heat Sink	480°C/watt	60.0sec

[1] Air velocity ≅ 9ft/sec

Table 1. Thermal Resistances

The time response of the AD590 to a step change in temperature is determined by the thermal resistances and the thermal capacities of the chip, C_{CH}, and the case, C_C. C_{CH} is about 0.04 watt-sec/°C for the AD590. C_C varies with the measured medium since it includes anything that is in direct thermal contact with the case. In most cases, the single time constant exponential curve of Figure 9 is sufficient to describe the time response, T (t). Table 1 shows the effective time constant, τ for several media.

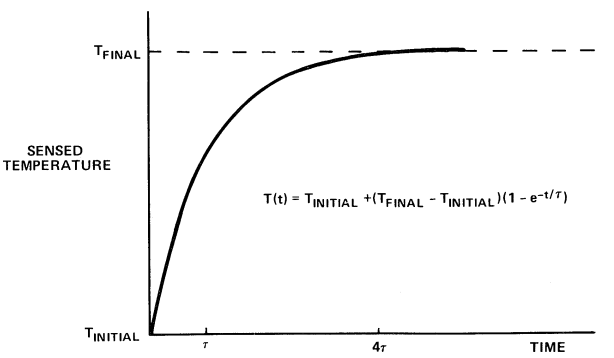
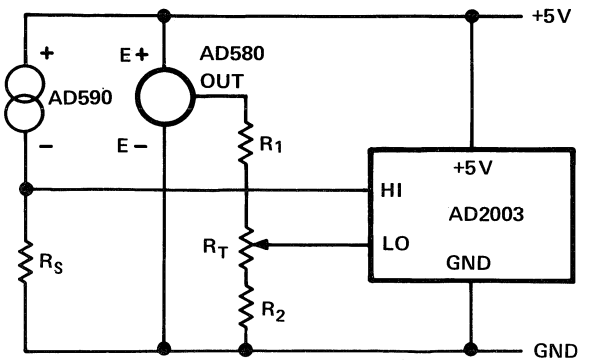


Figure 9. Time Response Curve



	R_S	R_1	R_2	R_T
°K	1kΩ	OPEN	SHORT	SHORT
°C	1kΩ	9.09kΩ	1kΩ	200Ω
°R	1.8kΩ	OPEN	SHORT	SHORT
°F	1.8kΩ	9.53kΩ	1.95kΩ	500Ω

Figure 10. Variable Scale Display

Figure 10 demonstrates the use of a standard Digital Panel Meter for the display of temperature on any of the standard scales. If only Kelvin or Rankin temperature is to be displayed then the AD580 and the resistive divider are not required since no offset voltage is needed. For Celsius and Fahrenheit, R_T should be trimmed at a midrange reference temperature. For specified accuracy, R_T should be within 0.1% of its value listed in the table above.

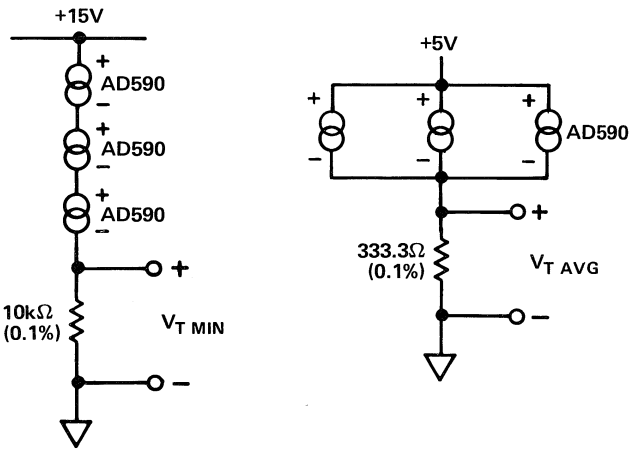


Figure 11. Series & Parallel Connection

Connecting several AD590 units in series as shown in Figure 11 allows the minimum of all the sensed temperatures to be indicated. In contrast, using the sensors in parallel yields the average of the sensed temperatures.

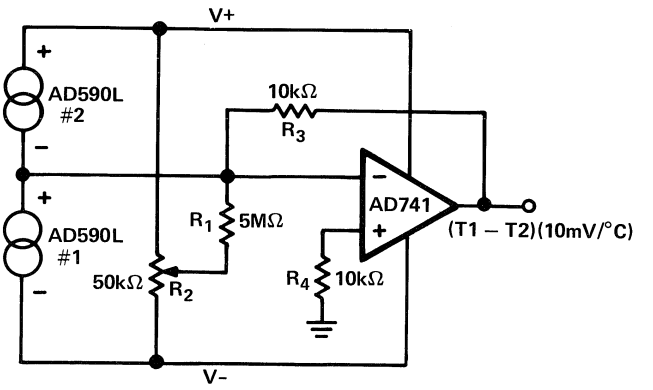


Figure 12. Differential Measurements

The circuit of Figure 12 demonstrates one method by which differential temperature measurements can be made. R_1 and R_2 can be used to trim the output of the op amp to indicate a desired temperature difference. For example, the inherent offset between the two devices can be trimmed in. If V+ and V– are radically different, then the difference in internal dissipation will cause a differential internal temperature rise. This effect can be used to measure the ambient thermal resistance seen by the sensors in applications such as fluid level detectors or anemometry.

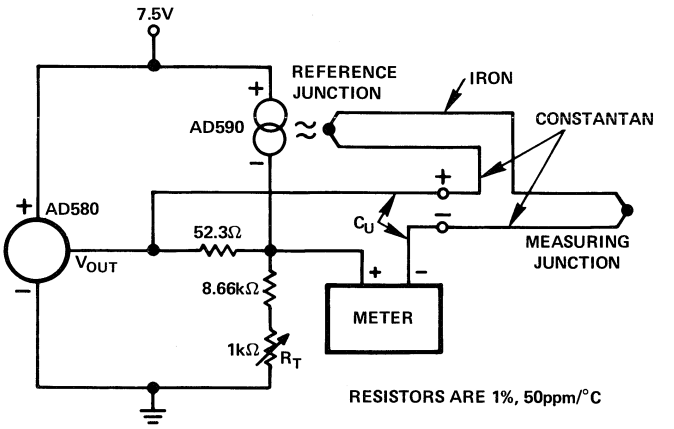


Figure 13. Cold Junction Compensation Circuit for Type J Thermocouple

Figure 13 is an example of a cold junction compensation circuit for a Type J Thermocouple using the AD590 to monitor the reference junction temperature. This circuit replaces an ice-bath as the thermocouple reference for ambient temperatures between +15°C and +35°C. The circuit is calibrated by adjusting R_T for a proper meter reading with the measuring junction at a known reference temperature and the circuit near +25°C. Using components with the T.C.'s as specified in Figure 13, compensation accuracy will be within ±0.5°C for circuit temperatures between +15°C and +35°C. Other thermocouple types can be accommodated with different resistor values. Note that the T.C.'s of the voltage reference and the resistors are the primary contributors to error.

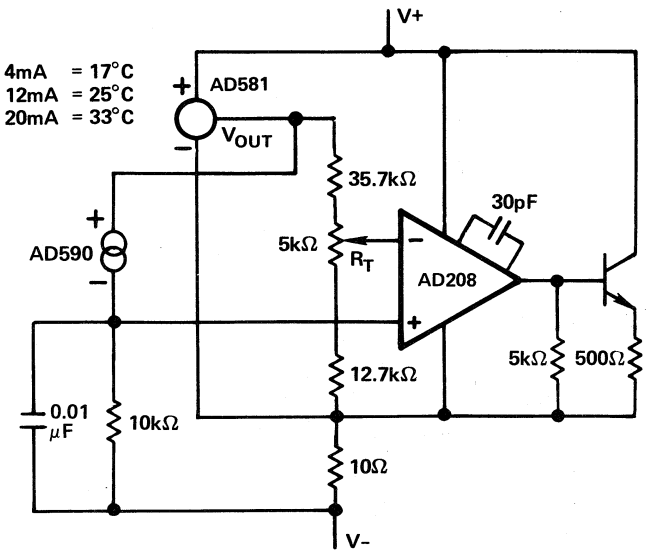


Figure 14. 4 to 20mA Current Transmitter

Figure 14 is an example of a current transmitter designed to be used with 40V, 1kΩ systems; it uses its full current range of 4mA to 20mA for a narrow span of measured temperatures. In this example the 1μA/°K output of the AD590 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C. R_T is trimmed for proper reading at an intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD590 may be chosen.

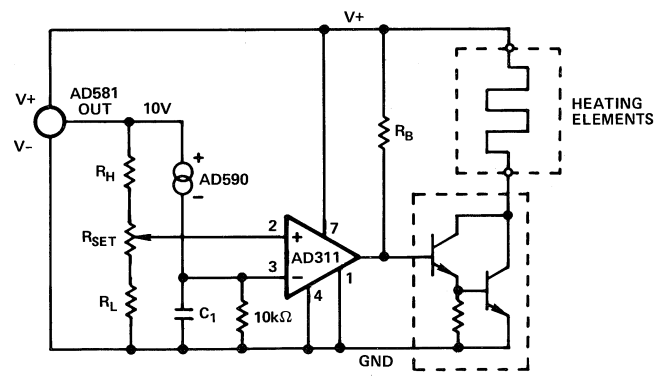


Figure 15. Simple Temperature Control Circuit

Figure 15 is an example of a variable temperature control circuit (thermostat) using the AD590. R_H and R_L are selected to set the high and low limits for R_{SET}. R_{SET} could be a simple pot, a calibrated multi-turn pot or a switched resistive divider. Powering the AD590 from the 10V reference isolates the AD590 from supply variations while maintaining a reasonable voltage (~7V) across it. Capacitor C_1 is often needed to filter extraneous noise from remote sensors. R_B is determined by the β of the power transistor and the current requirements of the load.

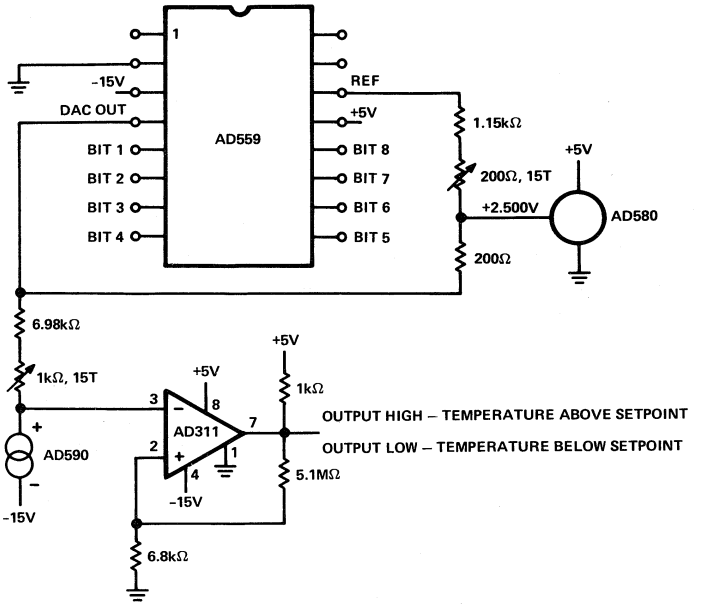


Figure 16. DAC Setpoint

Figure 16 shows how the AD590 can be configured with an 8 bit DAC to produce a digitally controlled setpoint. This particular circuit operates from 0 (all inputs high) to +51°C (all inputs low) in 0.2°C steps. The comparator is shown with 1°C hysteresis which is usually necessary to guard-band for extraneous noise; omitting the 5.1MΩ resistor results in no hysteresis.

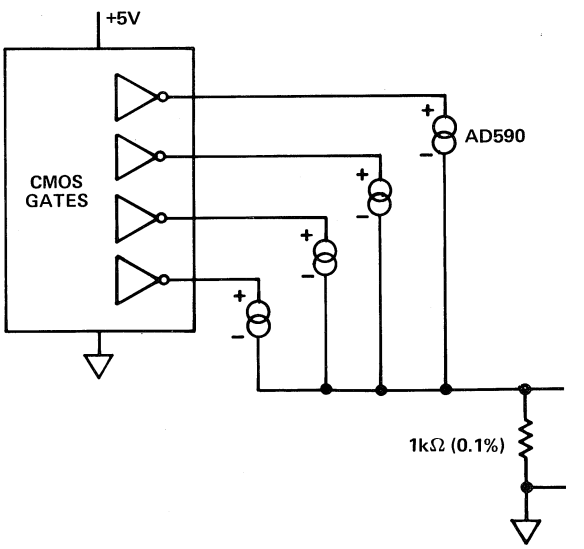


Figure 17. AD590 Driven from CMOS Logic

The voltage compliance and the reverse blocking characteristic of the AD590 allows it to be powered directly from +5V CMOS logic. This permits easy multiplexing, switching or pulsing for minimum internal heat dissipation. In Figure 17 any AD590 connected to a logic high will pass a signal current through the current measuring circuitry while those connected to a logic zero will pass insignificant current. The outputs used to drive the AD590's may be employed for other purposes, but the additional capacitance due to the AD590 should be taken into account.

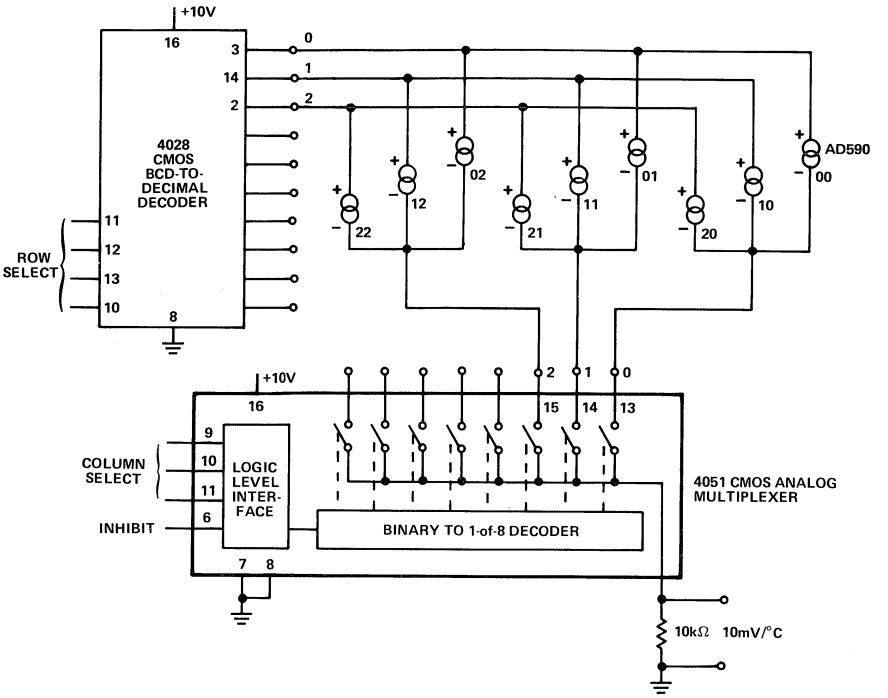


Figure 18. Matrix Multiplexer

CMOS Analog Multiplexers can also be used to switch AD590 current. Due to the AD590's current mode, the resistance of such switches is unimportant as long as 4V is maintained across the transducer. Figure 18 shows a circuit which combines the principal demonstrated in Figure 17 with an 8 channel CMOS Multiplexer. The resulting circuit can select one of eighty sensors over only 18 wires with a 7 bit binary word. The inhibit input on the multiplexer turns all sensors off for minimum dissipation while idling.

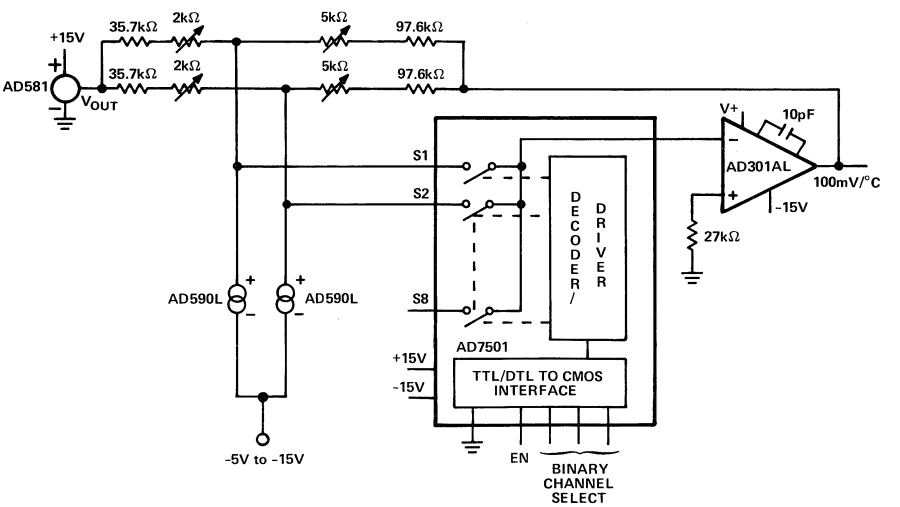


Figure 19. 8-Channel Multiplexer

Figure 19 demonstrates a method of multiplexing the AD590 in the two-trim mode (Figure 7). Additional AD590's and their associated resistors can be added to multiplex up to 8 channels of ±0.5°C absolute accuracy over the temperature range of −55°C to +125°C. The high temperature restriction of +125°C is due to the output range of the op amps; output to +150°C can be achieved by using a +20V supply for the op amp.

6 Channel Scanning Digital Thermometer

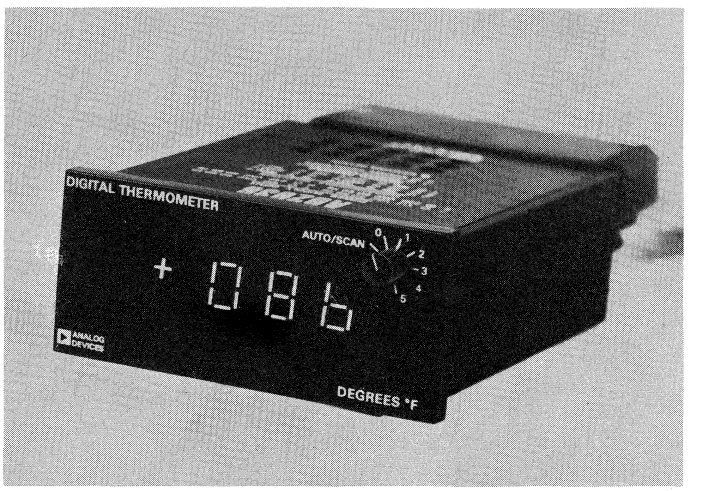
AD2036

FEATURES

Automatic Scan of 6 Thermocouples (TC's)
Manual Selection of Individual TC's
External Channel Selection by BCD Code
J, K, or T Thermocouple
°C or °F Readout
Self Contained Linearization
Isolated Analog Input
Parallel BCD Output
1° Resolution
+5V dc at 10mA for External Logic

APPLICATIONS

Multi-Point Temperature Measurements for Remote Data Acquisition and Data Logging
Temperature Monitoring in Design, Laboratory, Manufacturing and Quality Control



GENERAL DESCRIPTION

The AD2036 is a low cost 3½ digit, ac line powered digital readout temperature meter. Inputs for six thermocouples of identical types, either J, K, or T and calibrated temperature ranges in °C or °F, make up a total of six available models.

Cycling on an internal clock, the AD2036 can continually scan 6 input channels. Individual channels can be manually selected via a small switch on the front. Channel selection can also be made via an external BCD input at the rear connector. A separate channel select output identifies the selected channel independent of selection mode. The channel select output together with the BCD Output provides complete information for automatic data collection. The Isolated Parallel BCD Output provides an easy interface to conventional recording and controlling instruments. For applications where there are high common mode voltages (CMV) present, the AD2036 has as a standard feature a floating opto isolated analog front end that will withstand CMV's up to 250V rms.

The AD2036 displays readings on large 0.5″ (13mm) high LED displays. Both (+) and (−) polarities are indicated. Controls are provided for blanking the display.

AUTO/SCAN

The AD2036, while in the Auto/Scan mode, will permit unattended scanning of all six input channels. The rate of the channel select is 3.2 seconds. 1.6 seconds and 0.8 second channel select rates are available upon special request. The AD2036 can be used as a stand-alone instrument and with the Scan input held high will continually scan six channels. When the Scan input is brought low the AD2036 will continue to cycle and stop at channel 0. When used with a printer the channel select number in addition to the converted BCD value can be recorded.

MANUAL CHANNEL SELECTION

A switch on the front enables the user to manually select an individual thermocouple. As in the Auto/Scan mode, the BCD Output of the selected channel and the channel number are available. Selection of an individual TC channel automatically disables Scan and external channel selection is overridden. The Mode Output pin indicates when the switch is in this condition. On special order, meters can be supplied with card edge control for disabling the switch.

EXTERNAL CHANNEL SELECTION

For remote control of channel selection the AD2036 provides an input for an external BCD code selection. This feature enables external BCD switch, automatic microprocessor or computer control.

STANDARD PACKAGING

The AD2036 is packaged in Analog Devices' ac line powered DPM case which uses the same panel cutout as most other ac line powered DPMs from other manufacturers. In addition, the pin connections for the AD2036 converter board are the same as for the AD2022, AD2009, AD2016 and DPM's available from several other manufacturers.

SPECIFICATIONS (typical @ +25°C and nominal line voltage unless otherwise specified)

TYPES OF THERMOCOUPLE (TCs): J, K, or T

ACCURACY

°C		Error ±½LSB	°F		Error ±½LSB
J	-60 to 0	±1.4	J	-76 to 32	±2.5
	0 to 500	±1.4		32 to 932	±2.5
	500 to 760	±2.2		932 to 1400	±4.0
K	-60 to 0	±1.4	K	-76 to 32	±2.5
	0 to 150	±1.4		32 to 302	±2.5
	150 to 1350	±2.6		302 to 2000	±4.7
T	-100 to 0	±1.3	T	-148 to 32	±2.3
	0 to 250	±1.5		32 to 450	±2.7
	250 to 400	±2.0		450 to 752	±3.6

DISPLAY OUTPUT

- Light emitting diode (LED), seven segment display readouts, 0.5″ (13mm) high for 3 data digits, 100% overrange and polarity indication. Overload >1999 indicated by flashing display, polarity remains valid. There is no overload indication for out of range readings.
- Decimal points (3) selectable at input connector.
- Display Blanking

SIGNAL INPUT

- Input Impedance: 100MΩ
- Bias Current: 10nA
- Overvoltage Protection Between Channels: ±18V peak max
- Common Mode Voltage: ±350V peak max
- CMV Between Channels: ±6V peak max
- Temperature Coefficient: Span: +temp, 100ppm; -temp, 120ppm Zero: 0.03degrees/degree C or F
- Settling Time to Rated Accuracy: 2.0 seconds (full span step input)
- Normal Mode Rejection: 60dB at 50 – 400Hz
- Common Mode Rejection: 120dB @ 250V rms max CMV (Between TCs and digital gnd), $dv_{cm}/dt < 10^6$ V/sec, 250Ω imbalance

CONVERSION RATE

- 5 conversions per second
- Hold and read on command

CONTROL INPUTS

Display Blanking (TTL Compatible, 3 LSTTL Load) - Logic "0" or grounding blanks entire display except for decimal points; Logic "1" or open circuit for normal operation. Display blanking has no effect on output data. Display is valid immediately upon removal of blanking input.

Converter Hold (CMOS, TTL Compatible, 1 LSTTL Load) - Logic "0" or grounding causes DPM to cease conversions and display data from last conversion; Logic "1" or open circuit for normal operation. After "Converter Hold" is removed, one or two conversions are needed before reading and BCD are valid.

Decimal Points (Not TTL Compatible) - Logic "0" or grounding illuminates desired decimal point. External drive circuitry must sink 35mA peak at a 25% duty cycle, when decimal point is illuminated.

Data Hold (TTL Compatible, 1 TTL Load) - Logic "0" or grounding inhibits updating of latched parallel output data of AD2036. Logic "1" or open circuit allows data to be updated after each DPM conversion. This input has no effect on the normal conversion of the DPM and its display.

Scanner Enable (CMOS/TTL Compatible 1 LSTTL Load) - Logic "1" will enable Scanner to control the channel selection. External channel input BCD lines can remain connected. A Logic "0" enables external channel selection.

Scan (Scan) (CMOS/TTL Compatible, 1 LSTTL Load) - A Logic "1" ("0") for <12 seconds will initiate a scan of six channels. To use Scan input, the Scan input must be a Logic "0". Both inputs have debounce circuitry. A momentary scan pulse while in the switch or external selection mode will initiate a sequence of six readings of the channel that is addressed then stop.

Channel BCD Input (CMOS/TTL Compatible 1 LSTTL Load) - Logic "0" on Scanner Enable will allow use of external control. All other control inputs remain the same.

Channel Increment (CMOS/TTL Compatible 1 LSTTL Load) - Positive going edge will initiate sequence to the next channel.

Spare Inverter Input (CMOS, TTL Compatible 1 LSTTL Load) - Spare inverter supplied for customer convenience.

DATA OUTPUTS

Isolated Parallel BCD Outputs - 3 BCD digits, Overrange, Overload and Data Ready Outputs (TTL Compatible, 4 TTL Loads). BCD data outputs are latched positive true logic. Overload Output is Logic "0" for inputs greater than full scale range, Logic "1" when other data outputs are valid. Polarity Output (TTL Compatible, 4 TTL Loads latched) indicates positive polarity when high (Logic "1"). Digital outputs are fully isolated from input circuitry; all logic levels are referenced to digital ground.

Channel BCD Outputs (CMOS/TTL Compatible 2 TTL Loads) - BCD Channel number data outputs are positive true.

Mode Output (CMOS/TTL Compatible 2 TTL Loads) - Logic "1" indicates channel selection is by switch. Logic "0" indicates selection is by scanner or external control.

Data Ready (Data Ready) (CMOS/TTL Compatible 2 TTL Loads) - Logic "1" ("0") indicates data from Temperature Card is ready.

Spare Inverter Output (CMOS/TTL Compatible 2 TTL Loads) - Spare inverter supplied for customer convenience.

Clock OUT (CMOS, TTL Compatible, 2 TTL Loads) - Clock OUT pulse is disabled when Data Hold line is low.

TEMPERATURE RANGE[1]

- 0 to +50°C Operating
- -25°C to +85°C Storage

POWER INPUT

- AC line 50 – 400Hz, See Voltage Options below
- Power Consumption - 5.8W @ 50 – 400Hz

CALIBRATION ADJUSTMENTS

- Span
- Zero
- Recommended Recalibration Interval: six months

SIZE

- 3.92″ x 1.67″H x 5.80″D (100 x 42 x 147mm)
- Panel cutout 3.930″ x 1.682″ (99.8 x 42.7mm)

WEIGHT

- 1.25 pounds (0.568 kg)

OPTIONS

- 0.1° Resolution (consult factory)
- AC Power Inputs[2]

  AD2036 – 117V ac
  AD2036/E – 220V ac
  AD2036/F – 100V ac
  AD2036/H – 240V ac
  } ±10%

- Thermocouples Types

  AD2036/J – -60°C to 760°C -76°F to 1400°F
  AD2036/K – -60°C to 1350°C -76°F to 2000°F
  AD2036/T – -100°C to 400°C -148°F to 752°F

- Degree Readout

  AD2036/1 – Celsius
  AD2036/2 – Fahrenheit

ORDERING DIRECTIONS

- Sequence of options following model number AD2036 will be: Power Input, Thermocouple Type, Degree Readout, e.g. AD2036/E/J/1 (220V ac, J Thermocouple, Degree C).
- Display Lens[3]

  Lens 22 – Red with ADI Logo
  Lens 23 – Red without ADI Logo

- Connectors (2)

  2 each, 30 pin, 0.156″ spacing card edge connector.
  Viking 2VK15D/1-2 or equivalent.
  Optional: order AC1501

NOTES

1. Guaranteed
2. Only one ac power supply option may be specified.
3. Lens 22 is supplied if no lens option is specified.

Specifications subject to change without notice.

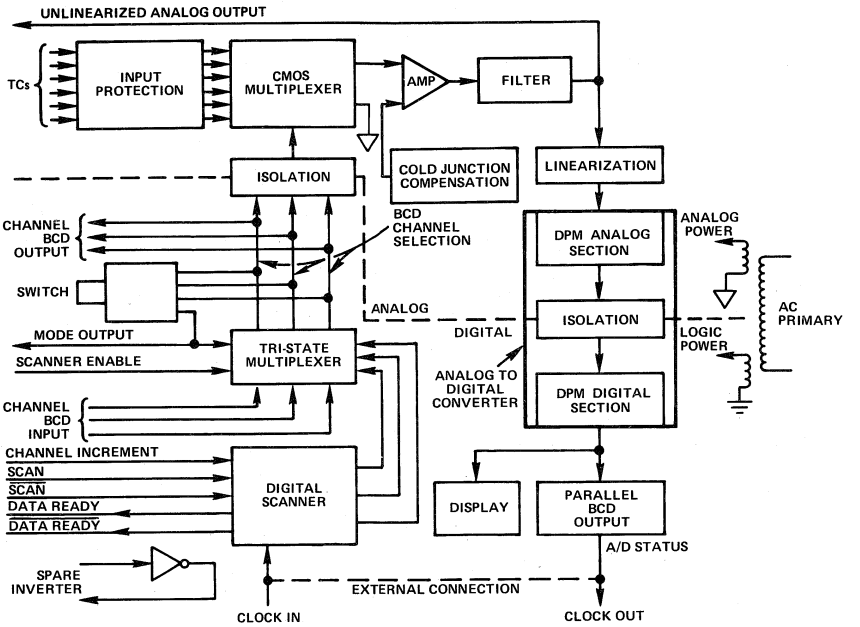


Figure 1. Block Diagram

DESIGNED AND BUILT FOR RELIABILITY

Even beyond the inherent advantages of the LSI IC design and LED displays, the AD2036 has had extreme care taken in its design and manufacture to insure reliability. Manufacturing processes are monitored by continual quality assurance inspections to insure proper workmanship and testing. Automatic equipment is used to test each DPM, both at the board level and at final assembly, to assure fault free performance. And, prior to shipment, each AD2036 must pass one full week of failure-free +50°C cycled power burn-in.

APPLYING THE AD2036

Description of Operation

The AD2036 Block Diagram is shown in Figure 1. Thermocouple selection is made by the CMOS Multiplexer which is comprised of two sets of six switches. The output of the Multiplexer is on two lines. One is connected to Analog Ground. The other is fed into an Amplifier that provides for Cold-Junction Compensation. The signal is then filtered and linearized and processed by the Analog to Digital Converter. The converter drives the Display and the Parallel BCD Output circuitry.

BCD Channel Selection is obtained from the Switch or the output of the Tri-State Multiplexer. In standard units, switch selection of individual TC Channels always takes precedence over the Tri-State Multiplexer. On special order, units can be wired for card edge enable/disable of the Switch. Under control of the Scanner Enable input, the Tri-State Multiplexer switches between channel selection from the Digital Scanner and the external Channel BCD Input. A logic low enables external selection. A logic high enables input from the Scanner.

As shown in the Timing Diagram of Figure 2, a Channel Scan is initiated by a logic high on the Scan input (pin S). The conclusion of the previous scan cycle will have resulted in Channel "0" already being selected. Conversions take place 5 times per second but 3.2 seconds are allowed to elapse before the Data Ready output indicates the data is valid. A minimum of 2 seconds is required for worst case settling

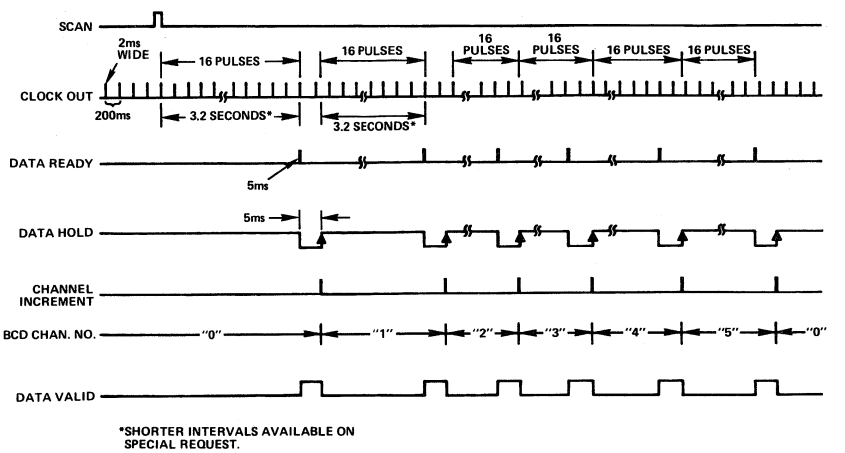


Figure 2. SCAN Timing Diagram

time of a full span step change as could take place in switching channel selection. On special order, where conditions do not warrant the 3.2 second delay, units can be provided with Data Ready occurring after 1.6 seconds or 0.8 seconds. Data can actually be taken up to the maximum 5 per second conversion rate (contact factory for further information).

In the standard unit, the Data Ready line switches high 16 clock pulses after Scan initiation (approximately 3.2 seconds). The Data Hold input can then be switched low if it is desired to retain the data unchanged for more than the minimum interval of 200ms. Upon releasing the Hold, it is necessary to produce a positive going pulse change on the Channel Increment input in order to step the Channel Selection. In many cases the Data Hold and Channel Increment inputs can be tied together so that release of the Hold will automatically step the Channel Selection.

In this fashion (and as shown in Figure 2) a complete cycle of the six channels can be obtained with the AD2036 stopping on Channel "0" and awaiting another Scan input pulse to signal the start of another cycle.

Operation with Printer

Input and output connections for operating with a printer are shown in Figure 3. A scan of the channels is initiated via push button or other pulse source. When Data Ready goes high, Busy from the printer goes low. This "holds" the Data and Channel Number Outputs until the printer raises the $\overline{\text{Busy}}$. When $\overline{\text{Busy}}$ goes high the "hold" is released and the channel counter is incremented. After 3.2 seconds (in the standard unit), the Data Ready again goes high and the interlocking of signals repeat 5 times until data has been printed for all six channels. Each automatic or manual initiation of the scan causes the sequence to repeat.

To continuously scan all six channels with a printer, set up as in Figure 3 except $\overline{\text{Scan}}$ must be held at Logic "0". .

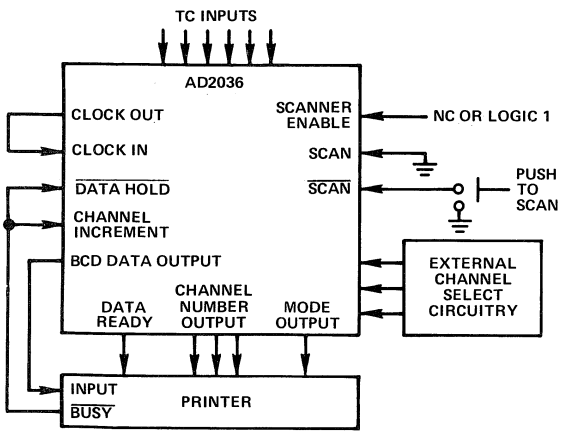


Figure 3. AD2036 with Printer

For continuous printing of a single channel set up as in Figure 3 except fix $\overline{\text{Scan}}$ at Logic "0". Channel can be selected by switch or externally.

For external Channel Selection, the Scanner Enable line should be held low. Under external BCD control, Channel Selection occurs immediately. If the Scan line is pulsed to a logic low, the printer will print the selected channel data 6 times and stop. If held low, a continuous printout of the selected channel will result. +5V power is provided at the rear connector to power external control logic.

Stand-Alone Operation

The AD2036 can at any time under switch control be operated so as to allow examination of individual channels. When used as a stand-alone instrument, it may also be desirable to be able to initiate a single scan of all six inputs. Figure 4 shows the necessary interconnections to obtain this operation. As before, the cycle is initiated via a pulse from a push button or other source. In this case, however, the Data Hold and Channel Increment inputs are controlled by the Data Ready. Each time Data Ready goes from low to high, the channel is incremented and conversions are made on the newly selected channel. The process continues until the meter is back on channel "0". The meter then waits for another scan initiation. During a scan each channel is displayed for 3.2 seconds (the whole scan takes approximately 20 seconds). Simultaneous display of channel number and converted value requires implementation of a separate display for channel number.

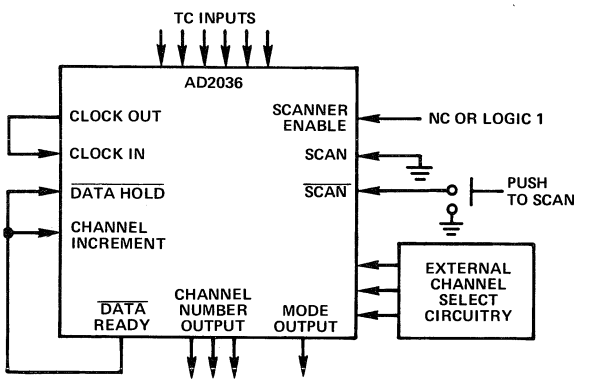


Figure 4. Stand-Alone Operation

To continuously scan, set up as per Figure 4 except fix the $\overline{\text{Scan}}$ input at Logic "0".

Opto Isolation

The AD2036 has as a standard feature Opto Isolation. This prevents external digital load currents from entering the analog circuitry via common ground paths and also enables safe temperature monitoring of equipment where there is no isolation from ac. As shown in the block diagram, Figure 1, digital and analog circuitry as well as the ac are isolated.

Wiring Connections

Power connections, thermocouple connections and control and digital connections are accessible at the rear. All but the thermocouple connections are via card edge (see Figures 6 and 7). Thermocouple wires are connected to a barrier strip on the top board (see Figure 5).

To install thermocouple wires, remove shroud from rear of unit by removing the screw. Feed thermocouple wires through slots in the shroud (see Figure 9). Thermocouple input wires are attached directly to the barrier strip. For easy access turn AD2036 upside down. (+) and (–) polarities are designated on the P.C.B. Care must be taken when connecting input wires to insure correct polarity. Figure 5 shows proper polarity and channel designations. Replace shroud after connecting TC's.

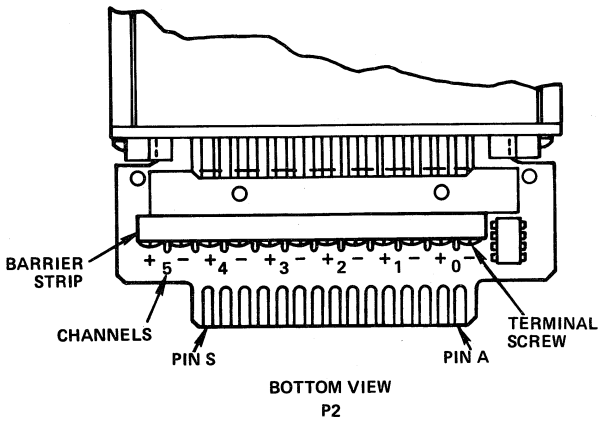


Figure 5. Thermocouple Connections

Power connections, control inputs and digital connections are contained in the pin out diagrams in Figures 6 and 7.

PIN REF	PIN FUNCTION
1	DATA HOLD
2	NC
3	CLOCK OUT
4	POLARITY
5	BCD 8
6	BCD 2
7	BCD 80
8	BCD 20
9	BCD 800
10	ANALOG GROUND
11	BCD 400
12	BCD 200
13	DISPLAY BLANK
14	OVERRANGE
15	AC LINE HIGH

KEY

PIN REF	PIN FUNCTION
A	NC (HOLE Y4)
B	NC (HOLE Y5)
C	OVERLOAD
D	CONVERTER HOLD
E	BCD 1
F	BCD 4
H	BCD 10
J	BCD 40
K	BCD 100
L	DP3 XX.X
M	DP2 X.XX
N	DIGITAL GROUND
P	DP1 .XXX
R	SHIELD (EARTH GROUND)
S	AC LINE LOW

Figure 6. Converter Card Pin Designations, P1

PIN REF	PIN FUNCTION
1	ANALOG GND
2	DATA READY
3	SPARE INVERTER OUTPUT
4	RESERVED FOR FUTURE FUNCTION
5	FACTORY USE
6	MODE OUTPUT
7	CHANNEL INPUT BCD 1
8	NC
9	NC
10	NC
11	NC
12	CLOCK IN
13	CHANNEL OUTPUT BCD 4
14	DIGITAL GND
15	FACTORY USE

KEY

PIN REF	PIN FUNCTION
A	ANALOG OUTPUT
B	DATA READY
C	CHANNEL INCREMENT
D	CHANNEL OUTPUT BCD 1
E	FACTORY USE
F	SPARE INVERTER INPUT
H	CHANNEL INPUT BCD 2
J	RESERVED FOR FUTURE FUNCTION
K	CHANNEL OUTPUT BCD 2
L	SCANNER ENABLE
M	RESERVED FOR FUTURE FUNCTION
N	CHANNEL INPUT BCD 4
P	SCAN
R	+5V dc (REF. TO DIG. GRD)
S	SCAN

Figure 7. Temperature Card Pin Designations, P2

Calibration Procedure

A precision voltage source and pure water Ice Bath are required. Location of the calibration adjusts are shown in Figure 8.

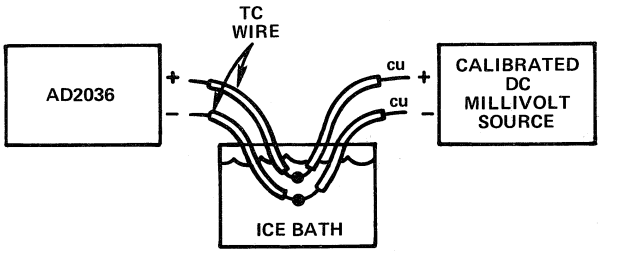


Figure 8. Calibration Diagram

With the voltage source set to zero, adjust the Zero control (top left) for a reading of 000 for Celsius or 032 for Fahrenheit units.

Using Table 1 for the proper thermocouple, set the calibrated voltage source to the appropriate number of millivolts and set span adjust (outer bottom right) for a correct reading.

				Zero Adjust		Span Adjust	
TC	Sensor Type	Color Code	Polarity	Input	Reading	Input/mV	Reading
J	Iron	White	+	0.0mV	0°C	41.013	730°C
	Constantan	Red	−	0.0mV	32°F	41.013	1346°F
K	Chromel	Yellow	+	0.0mV	0°C	52.049	1290°C
	Alumel	Red	−	0.0mV	32°F	42.303	1880°F
T	Copper	Blue	+	0.0mV	0°C	19.516	373°C
	Constantan	Red	−	0.0mV	32°F	19.536	713°F

Table 1. Calibration Chart

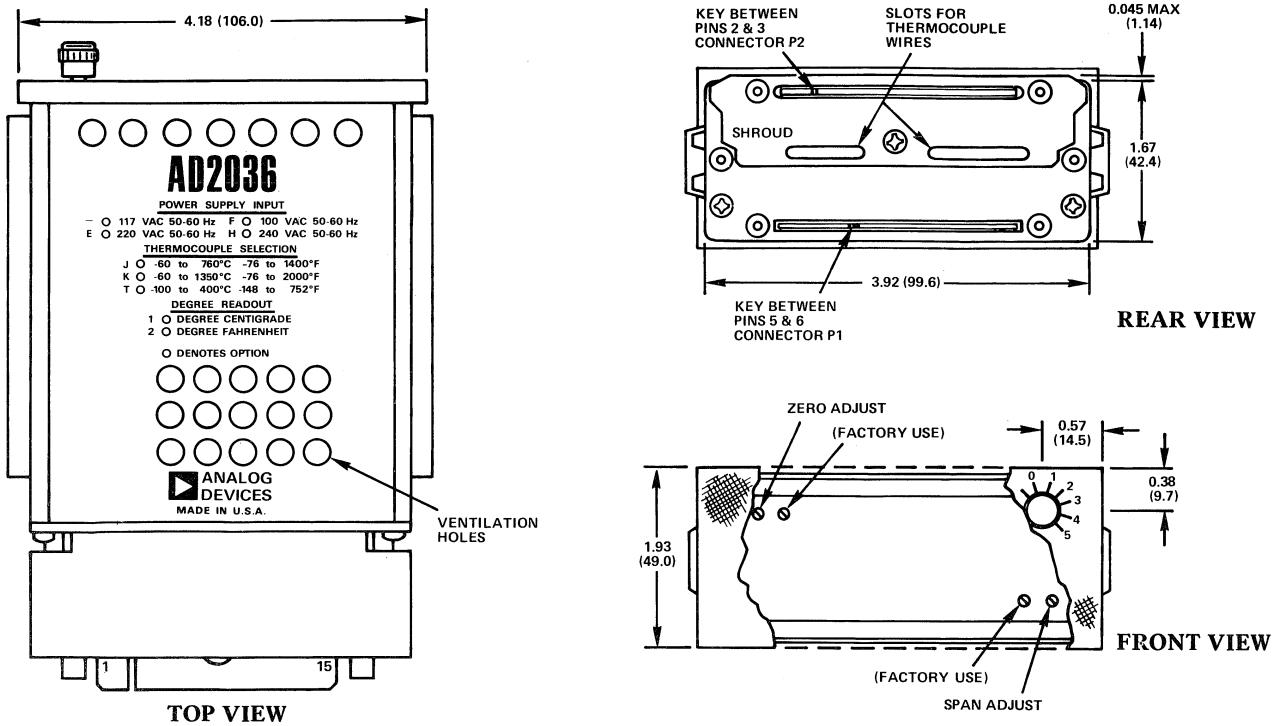


Figure 9. AD2036 Mechanical Outline
(Dimensions shown in inches and (mm))

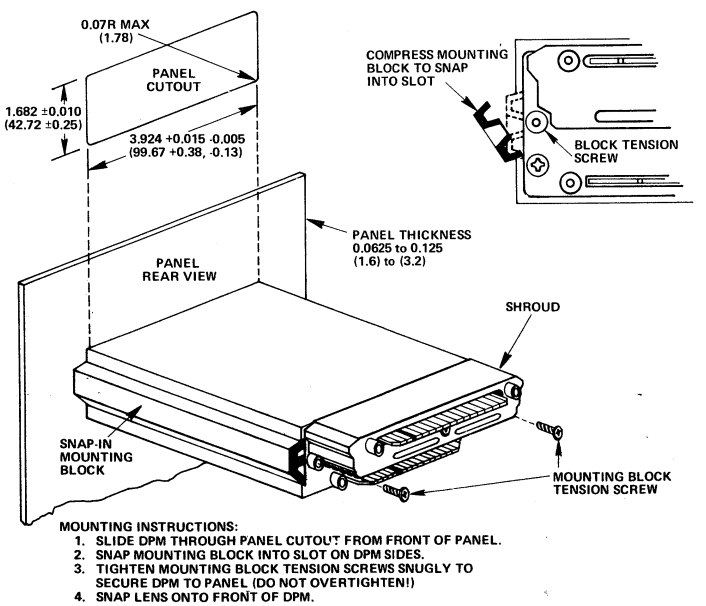


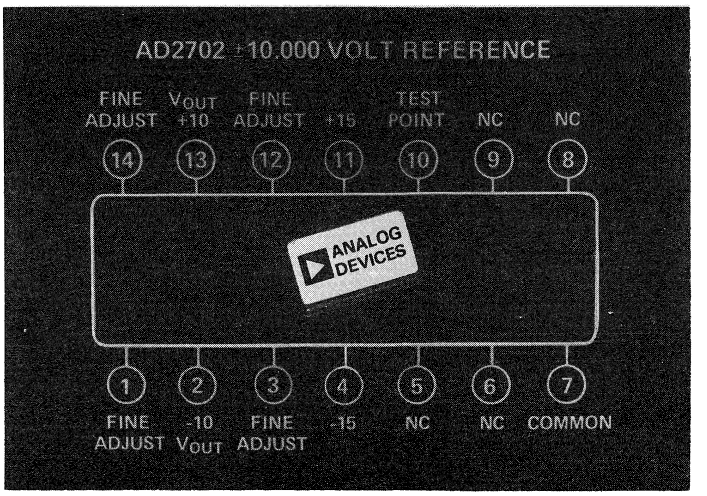
Figure 10. AD2036 Mounting Instructions
(Dimensions shown in inches and (mm))

±10 Volt Precision Reference Series

AD2700, AD2701, AD2702

FEATURES

Very High Accuracy: 10.000 Volts ±2.5mV (L and U)
Low Temperature Coefficient: 3ppm/°C
Performance Guaranteed -55°C to +125°C
10mA Output Current Capability
Low Noise
Short Circuit Protected



PRODUCT DESCRIPTION

The AD2700 family of precision 10 volt references offer the user excellent accuracy and stability at a moderate price by combining the recognized advantages of thin film technology and active laser trimming. The low temperature drift (3ppm/°C) achieved with these technologies can be matched only by the use of ovens, chip heaters for temperature regulation, or with hand selected components and manual trimming. In addition, temperature-regulated devices are guaranteed only up to +85°C operation, whereas the U- and S-grade devices in the AD2700 family are guaranteed to +125°C. The AD2700U and AD2700S series are also available with full screening to MIL-STD-883A, Class B.

The AD2700 is a +10 volt reference which is designed to interface with high accuracy bipolar D/A converters of 10 and 12 bit resolution. The 10mA output drive capability also makes the AD2700 ideal for use as a general positive system reference.

The AD2701 is a negative 10 volt reference especially designed to interface with CMOS D/A and A/D converters, as shown in the applications. For systems requiring a dual tracking reference, the AD2702 offers both positive and negative precision 10 volt outputs in a single package.

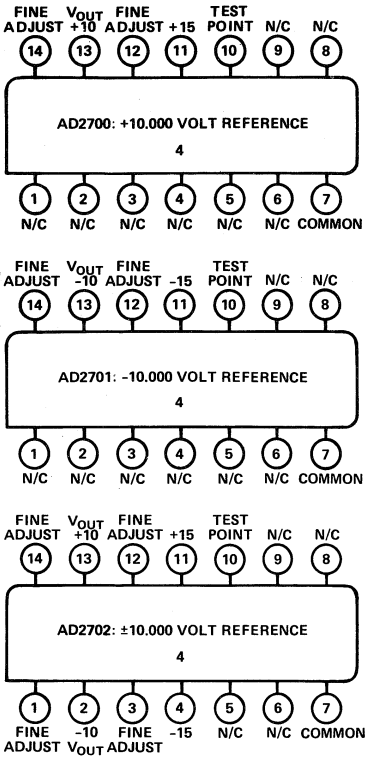
All three devices are offered in "J" and "L" grades for operation from -25°C to +85°C and "S" and "U" grades for the -55°C to +125°C temperature range. All units are packaged in a 14-pin dual-in-line welded metal package which offers excellent reliability, hermeticity, as well as EMI/RFI shielding.

Model	Output
AD2700	+10.000V
AD2701	-10.000V
AD2702	±10.000V

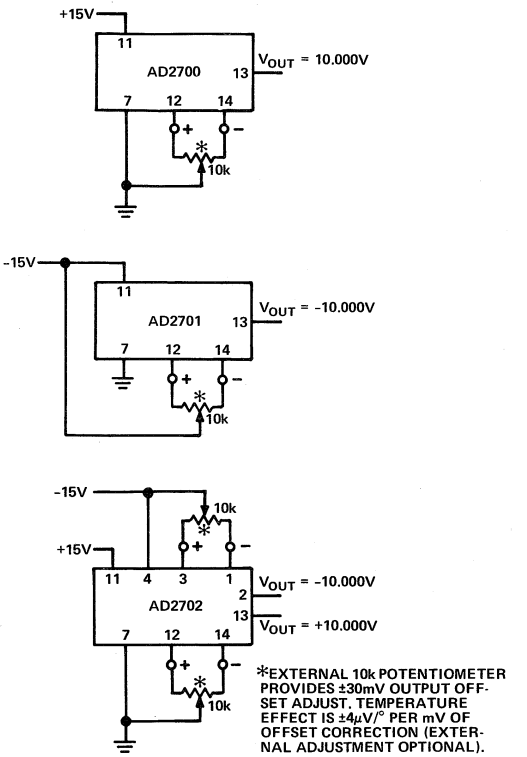
SPECIFICATIONS (maximum or minimum @ E_{in} -15V @ +25°C, R_L = 2kΩ unless otherwise noted)

MODEL	J	L	S	U
ABSOLUTE MAX RATINGS				
Input Voltage (for applicable supply)	±20V	*	*	*
Power Dissapation @ +25°C — AD2700, 01	300mW	*	*	*
— AD2702	450mW	*	*	*
Operating Temperature Range	-25°C to +85°C	*	-55°C to +125°C	***
Storage Temperature Range	-65°C to +150°C	*	*	*
Lead Temperature (soldering, 10s)	+300°C	*	*	*
Short Circuit Protection (to GND)	Continuous	*	*	*
OUTPUT VOLTAGE				
AD2700	10.000V ±0.005V	±0.0025V	*	**
AD2701	-10.000V ±0.005V	±0.0025V	*	**
AD2702	±10.000V ±0.005V	±0.0025V	*	**
OUTPUT CURRENT — @ +25°C	±10mA	*	*	*
(V_{IN} = ±13 to ±18V) over op. range	±5mA	+5mA, -2mA	**	**
OUTPUT VOLTAGE CHANGE[1] — AD2700,01	10ppm/°C	3ppm/°C	**	**
T_{min} to T_{max} AD2702	10ppm/°C	5ppm/°C	**	3ppm/°C
LINE REGULATION				
V_{IN} = ±13 to ±18V	100μV/V	*	*	*
LOAD REGULATION				
0 to ±10mA	50μV/mA	*	*	*
OUTPUT RESISTANCE	0.05Ω	*	*	*
INPUT VOLTAGE, OPERATING	±13V to ±18V	*	*	*
QUIESCENT CURRENT — AD2700, 01	±14mA	*	*	*
— AD2702	+17mA, -3mA	*	*	*
NOISE				
(0.1 to 10Hz)	50μV p-p typ	*	*	*
LONG TERM STABILITY (@ +55°C)	100ppm/1000 Hrs. typ	*	*	*
OFFSET ADJUST RANGE				
(See Diagrams)	±20mV (min)	*	*	*
OFFSET ADJUST TEMP DRIFT EFFECT	±4μV/°C per mV of Adjust typ	*	*	*

*Same as "J" grade performance.
**Same as "L" grade performance.
***Same as "S" grade performance.
[1] Output voltage change as a function of temperature is determined using the box method. Each unit is tested at -55, -25, +25, +85, +125°C. All readings must fall within the rectangular area bounded by the minimum and maximum temperature and whose diagonal has a slope equal to the stated Drift in ppm/°C: (V_{OUT} max − V_{OUT} min) ÷ (Operating temp. range).
Specifications subject to change without notice.



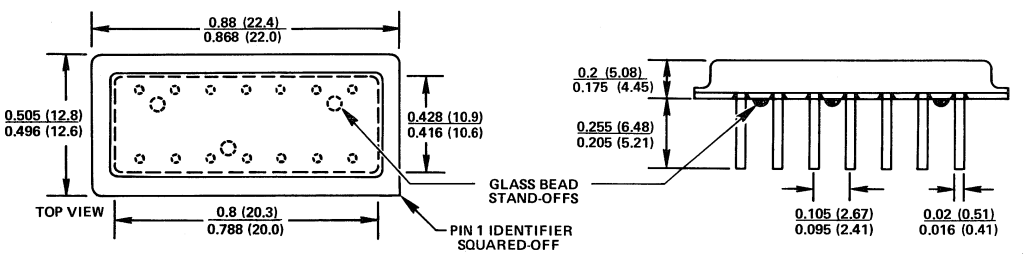
Pin Designations



Fine Trim Connections

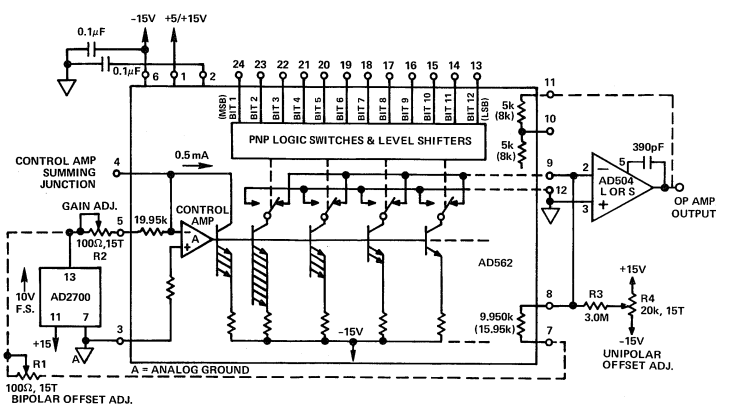
PACKAGE DIMENSIONS

Dimensions shown in inches and (mm).



Hermetically sealed 14 Pin Dual-In-Line (Fine & Gross leak tested per MIL-STD-883A, Method 1014)
Pin 7 is electrically connected to the case. Case has metal bottom surface.

14-Pin Dual-In-Line

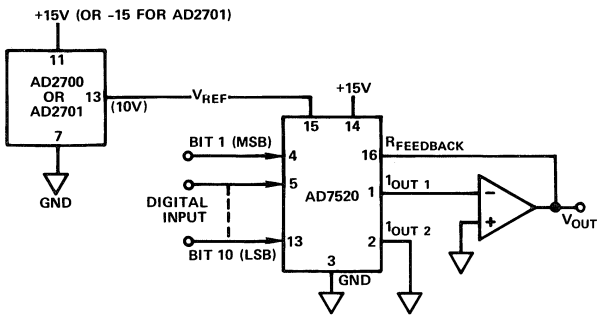


SEE AD562 DATA SHEET FOR ADDITIONAL APPLICATION INFORMATION

Using AD2700 Reference With the AD562 – 12 Bit D/A Converter

USING AD2700 REFERENCE WITH THE AD7520 AND AN IC AMPLIFIER TO BUILD A DAC

The AD2700 series is ideal for use with the AD7520 series of CMOS D/A converters. A CMOS converter in a unipolar application as shown below performs an inversion of the voltage reference input. Thus, use of the +10 volt AD2700 reference will result in a 0 to -10 volt output range. Alternatively, using the -10 volt AD2701 will result in a 0 to +10 volt range. Two operational amplifiers are used to give a bipolar output range of -10 volt to +10 volt, as shown in the lower figure. Either the AD2700 or AD2701 can be used, depending on the transfer code characteristic desired. For more detailed applications information, refer to the AD7520 data sheet.

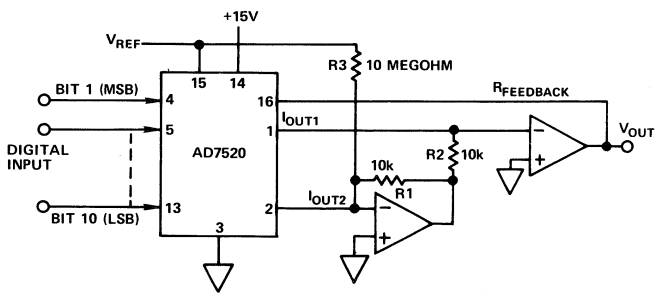


Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table 1. Code Table — Unipolar Binary Operation



Bipolar Operation (4-Quadrant Multiplication)

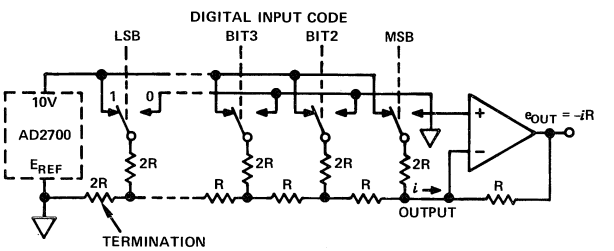
DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

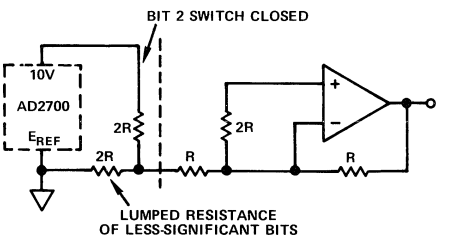
Table 2. Code Table — Bipolar (Offset Binary) Operation

USING THE AD2700 VOLTAGE REFERENCE WITH D/A CONVERTER

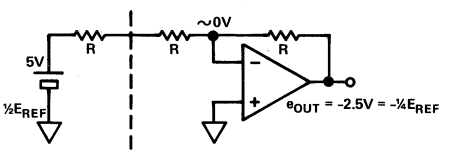
An AD2700 Voltage Reference can be used with an inverting operational amplifier and an R-2R ladder network. If all bits but the MSB are off (i.e., grounded), the output voltage is $(-R/2R)E_{REF}$. If all bits but Bit 2 are off, it can be shown that the output voltage is $\frac{1}{2}(-R/2R)E_{REF} = \frac{1}{4}E_{REF}$: The lumped resistance of all the less-significant-bit circuitry (to the left of Bit 2) is 2R; the Thevenin equivalent looking back from the MSB towards Bit 2 is the generator, $E_{REF}/2$, and the series resistance 2R; since the grounded MSB series resistance, 2R, has virtually no influence — because the amplifier summing point is at virtual ground — the output voltage is therefore $-E_{REF}/4$. The same line of thinking can be employed to show that the nth bit produces an increment of output equal to 2^{-n} E_{REF}.



a. Basic Circuit



b. Example: Contribution of Bit 2; All Other Bits "0"



c. Simplified Equivalent of Circuit (b.)

D/A Converters

Orientation
D/A Converters

FACTORS IN CHOOSING A D/A CONVERTER

In the current issue of this catalog, there are listed some 20 different families of digital-to-analog converters (DACs). If one were to consider all the variations, there would be nearly 100 types to choose among. The reason for so many different types is the number of degrees of freedom in selection—technological, functional, and performance. A selection guide follows these introductory notes.*

TECHNOLOGICAL FACTORS

The technologies represented here include modules (cards and potted circuits) and integrated circuits—monolithic and hybrid. Modules generally can provide the extremes of performance (resolution—e.g., the 18-bit DAC1138— and speed), as well as arbitrary levels of functional completeness. ICs are small and high in performance-per-dollar. They often require external components for performance of the complete function, but if they otherwise meet the required specifications, they will tend to supplant modules in new designs, because IC prices start low and tend to decrease further with time.

The three most-important IC technologies in current use at Analog Devices are thin-film-on-CMOS, thin-film on bipolar, and hybrids. *Hybrid* provides the most-complete high-performance devices. *Thin-film-on-bipolar* provides stable references, high-performance current switches, and laser-wafer-trimmed resistance networks; an outstanding example is the 10-bit AD561, with its high-compliance current output, trimmed-tempco buried-Zener reference, and fast response. *Thin-film-on-CMOS* uses voltage switches in a current-steering mode for full four-quadrant multiplying operation. In addition, the inherent high-density logic-capability and low dissipation of CMOS make possible such devices as the 10-bit AD7522, a microprocessor-compatible double-buffered DAC that can also be used as a digital gain-control with very low feedthrough and high linearity for bipolar analog signals.

FUNCTIONAL CHARACTERISTICS

The basic structure of all conventional D/A converters involves a network of precision resistors, a set of switches, and some form of level-shifting to adapt the switch drives to the specified logic levels. In addition, the device may contain output-conditioning circuitry, an output amplifier, a reference amplifier, an on-board reference, on-board buffer-registers (single- or dual-rank), and/or configuration conditioning.

*Complete information on converters may be found in the 250-page book, ANALOG-DIGITAL CONVERSION NOTES, published by Analog Devices and available for $5.95 from P.O. Box 796, Norwood MA 02062.

Basic DAC

This form is used principally for high-speed devices, such as the 25-50ns DAC1106; any elements likely to slow down the overall conversion (such as an output op amp) are furnished by the user to meet overall system specs. Some popular IC devices, such as the AD7520 and the AD7530, are quite simple (and correspondingly low in cost).

Output Conditioning

The analog quantity that is the "output" of a DAC, representing the input digital data, may be a "gain" (multiplying DAC), a current, and/or a voltage. In order to obtain a substantial voltage output at low impedance, an op amp is required. It is generally provided on-board in modular and hybrid DACs, but there are many ICs and other types that permit the user to choose an external op amp that will meet the particular needs of the application in stability, speed, and cost.

Almost all types of DACs provide one or more feedback resistors; they are matched to, and thermally track, resistances in the network, so that an external op amp, if used, will not require an external feedback resistor that might introduce tracking errors. If more than one feedback resistor is provided, a choice of analog output voltage ranges becomes available, e.g., 0–5V full-scale or 0–10V full-scale. If bipolar output-voltage ranges are specified, a bipolar-offset output is provided to subtract a half-scale value from the current flowing through the op amp summing point; it is usually derived from the DACs reference (or analog) input to avoid additional tracking error. Multiplying DACs use an internal or external op amp for bipolar offset.

In order to avoid difficulties, the user must pay especial attention to the specified output polarity, its relationship to the reference (if external) and to the input digital code. This can be especially tricky if the output is bipolar and the input requires a complementary (negative-true) digital coding. Another such case is where a current-output DAC, specified for a particular output-voltage polarity when used with an inverting op amp, is used in a mode that develops an output voltage passively (without the op amp) across an external resistive load. In addition to polarity, in this case, the user should be aware of the output-compliance constraint and the specified resistive component of output impedance.

Reference Input

The reference may be specified as external or internal, fixed or variable, single-polarity or bipolar. If internal, it may be permanently connected (as in the AD561) or optionally connectible (as in the DAC1122). If the DAC is a 4-quadrant multiplying type, the reference (or "analog input") is external, variable, and bipolar (AD7520/21/22/30/31—ICs, or DAC1125 self-

contained module, 12-bits). The user should check the specifications to determine whether the full-scale accuracy specifications are overall or subdivided into a converter-gain spec and a reference spec.

Digital Data
There are a number of ways in which converters differ in regard to the input data: First, the *coding* must be appropriate (binary, offset-binary, two's-complement, BCD, etc.), and its sense should be understood (positive-true, negative-true). The *resolution* (number of bits) must be sufficient; in addition, the specifications must be checked to ascertain that the 2^n distinct binary input codes will not only be accepted, but that also they will (if necessary) correspond to 2^n output values in a monotonic progression at any temperature in the operating range, with sufficient accuracy. The *data levels* accepted by the converter must be checked (TTL, low-voltage CMOS, high-voltage CMOS), as must the input loading imposed by the converter, and the supply conditions under which the converter will respond to the data. Check the data notation—misinterpretation can lead to connecting the data bits in backward order.

If *buffer registers* are desired, the converter should have an appropriate buffer configuration (for example, the 12-bit DAC1132 has a set of TTL buffers, the AD7522 has two ranks of CMOS buffering). In the case of the AD7522, not only is it double-buffered; it will also accept either serial or parallel data, and the parallel data can be loaded in two bytes (2 MSBs and 8 LSBs), or the serial data can be clocked in, while the DAC output remains unchanged.

Controls
If the DAC has external digital controls—for example, register strobes— their drive levels, digital sense (true or false), loading, and timing must be considered. The function and use of configuration controls (where present), such as serial/parallel, short-cycle, or chip-select decoding should be understood, and the appropriate ways of disabling them when not needed should be employed.

Power Supplies
Appropriate power supplies should be made available, considering the logic levels and analog output signals to be employed in the system. The appropriate degree of power-supply stability to meet the accuracy specs should be employed. Any recommended external protection circuitry (e.g., Schottky diodes, to ensure than V_{CC} is never more than 0.4V above V_{DD} in the AD7522) should be planned for. In almost all cases, separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals, while ensuring that a connection between the grounds can always exist at one point, even if the "mecca" point is inadvertently unplugged from the system.

SPECIFICATIONS

Definitions of the performance specifications, and related information, are provided on the next few pages, in alphabetical order.

Accuracy, Absolute
Error of a D/A converter is the difference between the actual analog output and the output that is expected when a given digital code is applied to the converter. Sources of error include gain error, zero error, linearity error, and noise. Error is usually commensurate with resolution, e.g., less than $2^{-(n+1)}$, or "½ LSB" of full scale. However, accuracy may be much better than resolution in some applications; for example, a 4-bit reference supply having only 16 discrete digitally chosen levels would have a resolution of 1/16, but it might have an accuracy to within 0.01% of each ideal value.

Absolute-accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

Accuracy, Relative
Relative accuracy error, expressed in %, ppm, or fractions of 1 LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristics) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated. Since the discrete analog output values corresponding to the digital input values ideally lie on a straight line, the relative-accuracy error can be interpreted as a measure of nonlinearity (see *Linearity).*

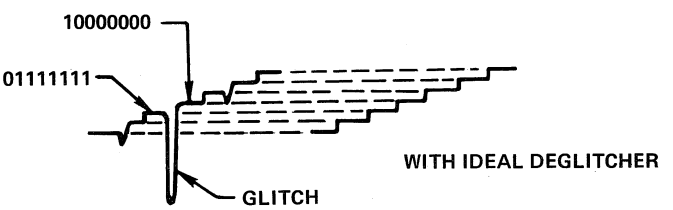
Compliance-Voltage Range
For a current-output DAC, the maximum range of (output) terminal voltage for which the device will provide the specified current-output characteristics.

Common-Mode Rejection (CMR)
The ability of an amplifier to reject the effect of voltage applied to both input terminals simultaneously. Usually a logarithmic expression representing a "common-mode rejection ratio" e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 10^6:1 means that a 1V common-mode voltage passes through the device as though it were a differential input signal of 1 microvolt.

Common-Mode Voltage
An undesirable signal picked up in a circuit by both wires making up the circuit, with reference to an arbitrary "ground." Amplifiers differ in their ability to amplify a desired signal accurately in the presence of a common-mode voltage.

Deglitcher
As the input code to a DAC is increased or decreased by small changes, it passes through what is known as major and minor

transitions. The most major transition is at half-scale, when the DAC switches around the MSB, and all switches change state, i.e., 01111111 to 10000000. If, at major transitions, the switches are faster (or slower) to switch off than on, this means that, for a short time, the D/A will give a zero (or full-scale) output, and then return to the required 1 LSB above the previous reading. Such large transient spikes are commonly known as "glitches", hence, a deglitcher is a device which removes these glitches. It normally consists of a fast sample-hold circuit, which holds the output constant until the switches reach equilibrium. Glitch energy is smallest in fast-switching DACs driven by fast logic gates that have little time-skew between 0-1 and 1-0 transitions.



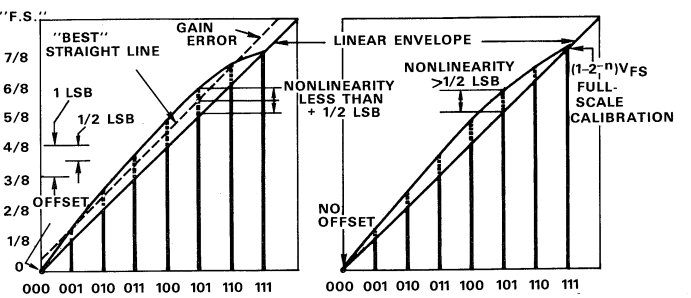
Feedthrough
Undesirable signal coupling around switches or other devices that are supposed to be turned off or provide isolation, e,g,. *feedthrough error* in a multiplying DAC. It is variously specified in %, ppm, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.

Four-Quadrant
In a multiplying DAC, "four quadrant" refers to the fact that both the reference signal and the number represented by the digital input may be of either positive or negative polarity. A four-quadrant multiplier is expected to obey the rules of multiplication for algebraic sign.

Gain
The "gain" of a converter is that analog scale-factor setting that provides the nominal conversion relationship, e.g., 10V span for a full-scale code change, in a fixed-reference converter. Gain- and zero-adjustment are discussed under *Zero*.

Least-Significant Bit (LSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the LSB is that bit that carries the smallest value, or weight. For example, in the natural-binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost digit is the LSB. Its analog weight, relative to full scale, is 2^{-n}, where n is the number of binary digits. It represents the smallest analog change that can be resolved by an n-bit converter.

Linearity
Linearity error of a converter (also, *integral nonlinearity*), expressed in % or ppm of full-scale range, or (sub)multiples of 1 LSB, is a deviation of the analog values, in a plot of the measured conversion relationship, from a straight line. The straight line can be either a "best straight line", determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristic from this straight line; or it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated (sometimes referred to as "end-point" linearity). End-point linearity error is similar to *relative-accuracy* error.



a. ½LSB Nonlinearity Achieved By Arbitrary Location of "Best Straight Line".

b. Nonlinearity Reference is Straight Line Through End Points. Nonlinearity >½LSB for Curve of a.

Comparison of Linearity Criteria for 3-Bit D/A Converter. Straight Line Through End Points is Easier to Measure, Gives More-Conservative Specification.

For multiplying D/A converters, the *analog* linearity error, at a specified digital code, is defined in the same way as for multipliers, i.e., by deviation from a "best straight line" through the plot of the analog output-input response.

Linearity, Differential
Any two adjacent digital codes should result in measured output values that are exactly 1 LSB apart (2^{-n} of full scale for an n-bit converter). Any deviation of the measured "step" from the ideal difference is called *differential nonlinearity*, expressed in (sub)multiples of 1 LSB. It is an important specification, because a differential linearity error greater than 1 LSB can lead to non-monotonic response in a D/A converter and missed codes in an A/D converter (see *Differential Linearity* in the A/D converter section for an illustration).

Monotonic
A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases, with the

result that the output will always be a single-valued function of the input. The specification "monotonic" (over a given temperature range) is sometimes substituted for a *differential nonlinearity* specification.

Most-Significant Bit (MSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the MSB is that digit (or bit) that carries the largest value of weight. For example, in the natural-binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the leftmost "1" is the MSB, with a weight of 2^{n-1}, or 8 LSBs. Its analog weight, relative to a DACs full-scale span, is ½. In bipolar DACs, the MSB indicates the polarity of the number represented by the rest of the bits.

Multiplying DAC
A multiplying DAC differs from a fixed-reference DAC in being designed to operate with varying (or ac) reference signals. The output signal of such a DAC is proportional to the product of the "reference" (i.e., analog input) voltage and the fractional equivalent of the digital input number (see *four-quadrant*).

Noise, Peak
The peak noise output of a DAC can be an important consideration in high-resolution DACs. The resolution is not confidently assignable when the peak noise in a given bandwidth exceeds the LSB value.

Noise, rms
For Gaussian noise, the rms noise should be one-seventh of the specified peak-to-peak noise, for less than 0.1% probability of encountering greater noise peaks. Both peak and rms specs should be looked at very carefully, as large spikes could be coupled into the device from elsewhere in the system. These spikes may have little effect on the rms noise value, though considerable in magnitude. If such a DAC were used in a display system, the noise would cause distortion of the pattern, and hence, loss of useful resolution.

Offset
For almost all bipolar converters (e.g., ±10 volts output), instead of actually generating negative currents to correspond to negative numbers, a unipolar DAC is used, and the output is offset by half full scale (1 MSB). For best results, this offset voltage or current is derived from the same reference supply that determines the gain of the converter.

This makes the zero point of the converter independent of thermal drift of the reference, because the ½ scale offset cancels the weight of the MSB at zero, independently of the amplitude of both.

Power-Supply Sensitivity
The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog output value (or fractions of 1 LSB) for a 1% dc change in the power supply, e.g., $0.05\%/\%\Delta V_S$). Power supply sensitivity may also be expressed in relation to a specified dc shift of supply voltage. A converter may be considered "good" if the change in reading at full scale does not exceed ±½ LSB for a 3% change in power supply. Even better specs are necessary for converters designed for battery operation.

Quantizing Uncertainty (or "Error")
The analog continuum is partitioned into 2^n discrete ranges for n-bit processing. All analog values within a given range of output (of a DAC) are represented by the same digital code, usually assigned to the nominal midrange value. For applications in which an analog continuum is to be restored, there is an inherent quantization uncertainty of ±½ LSB, due to limited resolution, in addition to the actual conversion errors. For applications in which discrete output levels are desired (e.g., digitally controlled power supplies or digitally controlled gains), this consideration is not relevant.

Resolution
An n-bit binary converter should be able to provide 2^n distinct and different analog output values corresponding to the set of n-bit binary words. A converter that satisfies this criterion is said to have a *resolution* of n bits. The smallest output change that can be resolved is 2^{-n} of the full-scale span.

Settling Time
The time required, following a prescribed data change, for the output of a DAC to reach and remain within a given fraction (usually ±½ LSB) of the final value. Typical prescribed changes are full-scale, 1 MSB, and 1 LSB at a major carry. Settling time of current-output DACs is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of the output op-amp circuit.

Slew Rate (or Slewing Rate)
Slew rate of a device or circuit is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration, such as limited current to charge a capacitor. Amplifiers with slew rate of a few volts/μs are common, and moderate in cost. Slew rates greater than about 75 volts/μs are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output.

Stability
Stability of a converter usually applies to the insensitivity of

its characteristics to time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion of temperature coefficients in tables of specifications (see "Temperature Coefficient").

Staircase
A voltage or current, increasing in equal increments as a function of time and having the appearance of a staircase (in a time plot), generated by applying a pulse train to a counter, and the output of the counter to the input of a DAC.

A very simple A/D converter can be built by comparing a staircase from a DAC with the unknown analog input. When the DAC output exceeds the analog input by a fraction of 1 LSB, the count is stopped, and the code corresponding to the count is the digital output.

Switching Time
In a DAC, the switching time is the time it takes for the switch to change from one state to the other ("delay time" plus "rise time" from 10%-90%), but does not include settling time, e.g. to <½ LSB.

Temperature Coefficients
In general, temperature instabilities are expressed as %/°C, ppm/°C, as fractions of 1 LSB/°C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include *gain, linearity, offset* (bipolar), and *zero*.

Gain Tempco: Two factors principally affect converter gain stability with temperature.

a) In fixed-reference converters the reference source will vary with temperature. For example, the tempco of a good Zener reference diode is generally less than 5ppm/°C
b) The reference circuitry and switches may add another 3ppm/°C in good 12-bit converters. High-resolution converters require much better tempcos for accuracy commensurate with the resolution.

Linearity Tempco: Sensitivity of linearity ("integral" and/or differential linearity) to temperature (in % FSR/°C or ppm FSR/°C) over the specified range. Monotonic behavior requires that the differential nonlinearity be less than 1 LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a temperature range, and/or implied by a statement that the device is monotonic over the specified temperature range.

Offset Tempco: The temperature coefficient of the all-DAC-switches-off (minus full scale) point of a bipolar converter (in % FSR/°C or ppm FSR/°C) depends on three major factors:

a) The tempco of the reference source
b) The voltage zero-stability of the output amplifier
c) The tracking capability of the bipolar-offset resistors and the gain resistors

Unipolar Zero Tempco (in % FSR/°C or ppm FSR/°C): The temperature stability of a unipolar fixed-reference DAC is principally affected by current leakage (current-output DAC), and offset voltage and bias current of the output op-amp (voltage-output DAC).

Zero- and Gain-Adjustment Principles
The output of a unipolar DAC is set to zero volts in the all-bits-off condition. The gain is set for F.S. $(1 - 2^{-n})$ with all bits on. The "zero" of an offset-binary bipolar DAC is set to -F.S. with all bits off, and the gain is set for +F.S. $(1 - 2^{-(n-1)})$ with all bits on. The data sheet instructions should be followed.

Selection Guide
D/A Converters

Description		Model §	Resolution (Bits)	Other	See Page
General Purpose	•	AD7523	8	CMOS IC, 4-quadrant multiplying, lowest cost	313
	•	AD1408	8	IC, replaces Motorola 1408/1508 directly	295
	•	AD559	8	IC, high-performance alternative to Motorola 1408/1508	277
	•	AD7524	8	CMOS IC, 4-quadrant multiplying, with register	317
	•	AD7533	10	CMOS IC, 4-quadrant multiplying, low cost	327
		AD7530	10	CMOS IC, 4-quadrant multiplying	323
		AD561	10	IC, internal reference, 250ns current settling	281
		DAC-10Z	10	Module, voltage output 5μs settling to 0.05%	377
		MDA-10Z	10	Module, 300ns settling to 0.05% current output	377
		AD7531	12	CMOS IC, 4-quadrant multiplying, low cost	323
		DAC1009	12	Module, voltage output, BCD optional	339
		DAC-12QZ	12	Module, voltage output, complementary coding, BCD optional, 5μs settling	375
		DAC1118	12	Module, voltage output, BCD optional	347
High Performance	•	AD7541	12	CMOS IC, 4-quadrant multiplying, pretrimmed	333
		AD562	12	IC, current output	289
		AD563	12	IC, current output, internal reference	289
		DAC-QS	12, 10, 8	Module, voltage output, BCD optional	373
		DAC-QM	12, 10, 8	Module, voltage output, BCD optional with input registers	367, 373
		DAC1132	12	Module, voltage output, 2μs settling to 0.01%	353
High Speed		AD561	10	IC, 250ns current settling, internal reference	281
		DAC-1106/08	10, 8	Module, 50/25ns current-settling to 0.05/0.2%	343
		DAC-10DF	10	Module, deglitched, voltage output, 200ns max to ±0.05%	365
High Resolution		DAC-QM	16, 14	Module, voltage output, BCD optional	367, 373
		DAC1136	16	Module, voltage output, 18μs settling to ±0.0015%	357
		DAC1138	18	Module, voltage output 60μs settling to ±0.00038%	357
Low Power † & Multiplying	•	AD7523	8	CMOS IC, 4-quadrant multiplying, low cost	313
	•	AD7524	8	CMOS IC, 4-quadrant multiplying, with register	317
	•	AD7533	10	CMOS IC, 4-quadrant multiplying, low cost	327
		AD7530	10	CMOS IC, 4-quadrant multiplying	323
		AD7520	10	CMOS IC, 4-quadrant multiplying	299
		AD7522	10	CMOS IC, 4-quadrant multiplying, double-buffered, serial-parallel	307
		AD7531	12	CMOS IC, 4-quadrant multiplying, low cost	323
	•	AD7541	12	CMOS IC, 4-quadrant multiplying, pretrimmed	333
		AD7521	12	CMOS IC, 4-quadrant multiplying	299
		DAC1125	12	Module, 4-quadrant, voltage out, low feedthrough 8.5mW power drain	349

• These devices have been added since publication of the 1977 CONVERSION PRODUCTS CATALOG.
† All CMOS IC's are low power.
§ The products cataloged in this volume are those considered to be the most cost-effective for new designs.
A number of popular older products are still available; they are listed on page 599.
Data sheets are available upon request.

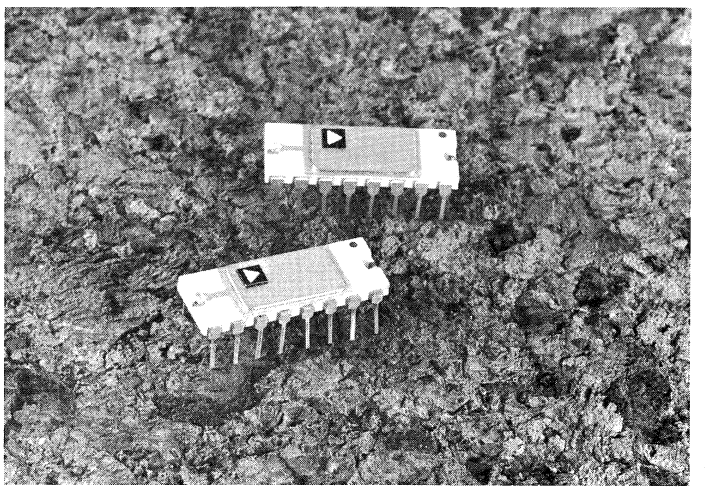
ANALOG DEVICES

8 Bit Monolithic D/A Converter

AD559

FEATURES

- Replaces the Motorola 1408/1508 8-Bit DAC
- Guaranteed Monotonicity and Relative Accuracy Over Full Temperature Range
- Single Chip Monolithic Construction
- Hermetic 16 Pin Ceramic DIP
- High Stability SiCr Thin Film Resistors
- Low Cost



PRODUCT DESCRIPTION

The AD559 is a low cost integrated circuit 8-bit digital-to-analog converter consisting of specially designed, precision bipolar switches, a control amplifier, and high stability silicon chromium thin-film resistors, all on a single monolithic chip. The single chip is mounted in a hermetically-sealed ceramic 16 lead dual in-line package.

A unique combination of advanced circuit design, and high stability SiCr thin film resistor processing provides the AD559 with true 8-bit accuracy at low I.C. costs. The maximum error over the full operating temperature range is limited to ½LSB and the gain temperature coefficient is 20ppm/°C typical. Monotonicity is guaranteed over the full operating temperature range of the devices.

The AD559 is recommended for all low cost, 8-bit DAC requirements and as a replacement for the Motorola 1408/1508 8-bit DAC, in most applications. The AD559K is specified for operation over the 0 to +75°C temperature range and the AD559S for operation over the full extended temperature range, -55°C to +125°C.

PRODUCT HIGHLIGHTS

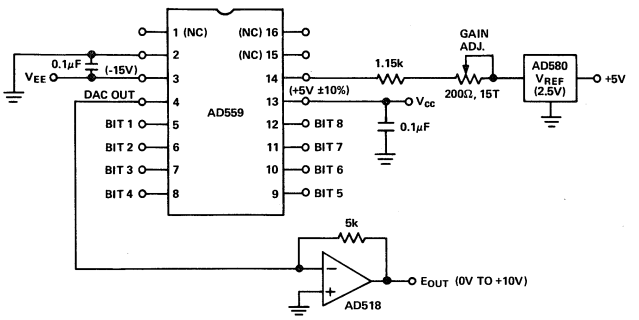
1. Monolithic I.C. construction makes the AD559 a logical choice where low cost is a prime consideration.
2. The AD559 replaces the Motorola 1408/1508 8-bit DAC in most applications. However, the capacitor needed to stabilize the 1408/1508 is not required when using the AD559.
3. High stability, thin film resistors enable the AD559 to provide low differential nonlinearity temperature coefficients, thus guaranteeing monotonicity and relative accuracy over the full operating temperature range.
4. Low digital input currents make the AD559 low voltage CMOS as well as TTL/DTL compatible.
5. The AD559 multiplies in two quadrants when a varying reference voltage is applied. When multiplication is not required, a fixed reference is used.
6. The device incorporates a newly developed, fully differential non-saturating precision current switching cell structure which provides increased immunity to supply voltage variations and also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation.

SPECIFICATIONS (typical @ +25°C, V_{CC} = +5V dc, V_{EE} = -15V dc and I_{REF} = 2mA, unless otherwise specified)

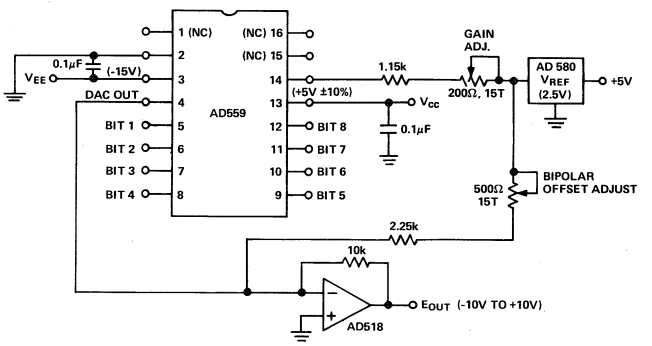
Model	AD559KD/BIN	AD559SD/BIN
DATA INPUTS		
Bit ON "Logic" 1	⩾2.0V @ 1μA max	*
Bit OFF "Logic" 0	⩽0.8V @ -100μA max	*
OUTPUT		
Current (All Bits ON and I_{REF} = +2.00mA)	1.99mA, ±2% max Over Operating Temp Range	*
Resistance	4MΩ	*
Capacitance	33pF	*
Compliance Voltage (See Fig. 3)	-1.5 to +10.5V	*
Zero (All Bits OFF)	200nA max Over Operating Temp Range	1μA max Over Operating Temp Range
Full Scale Power Supply Sensitivity (V_{CC} or V_{EE})	1μA/V max	*
RESOLUTION	8 Bits	*
ACCURACY (Error Relative to Full Scale)	½LSB max (0.19% of F.S.)	*
DIFFERENTIAL NONLINEARITY	½LSB max	*
SETTLING TIME TO ½LSB (All Bits ON-to-OFF or OFF-to-ON)	300ns Current Settling into Short Circuit	*
MAJOR CARRY SWITCHING TRANSIENT TO 90% COMPLETE	100ns	*
NOISE		
0.1 to 10Hz (All Bits ON)	8nA (p-p)	*
POWER REQUIREMENT Over Full Operating Range		
V_{CC}	+4.5V dc to +5.5V dc @ 8mA max	*
V_{EE}	-11.5V dc to -16.5V dc @ 16mA max	*
TEMPERATURE RANGE		
Operating	0 to +75°C	-55°C to +125°C
Storage	-55°C to +150°C	*
TEMPERATURE COEFFICIENT		
Gain	20ppm of F.S./°C	*
Differential Nonlinearity	2ppm of F.S./°C	*
MONOTONICITY	Guaranteed for 8 Bits Over Operating Temp Range	*
RATIOMETRIC PERFORMANCE		
Reference Current	0 to +3mA, Unipolar	*
Accuracy @ 200μA Ref. Current	2LSB	*
Accuracy @ 2mA, ±1mA Ref. Current	½LSB	*
Reference Feedthrough (All Bits OFF and 0 to +2mA p-p Sine Wave Ref. Current) Frequency for ½LSB p-p Output	24kHz	*
Reference Amp Slew Rate (All Bits ON and 2mA Step Change in Ref. Current)	4mA/μs	*
Output Settling Time to ½LSB (All Bits ON and 2mA Step Change in Ref. Current)	1μs	*
Control Amplifier Small-Signal Closed Loop Bandwidth	1.5MHz	*
Control Amplifier Full-Power Bandwidth	500kHz	*

*Specifications same as AD559KD.
Specifications subject to change without notice.

Figure 1 shows a typical connection scheme for the AD559. The control amplifier input current of +2.0mA is obtained from an AD580, 2.5V voltage reference. Pin 14, the summing node of the control amplifier, is maintained at 0V (virtual ground). Reference voltages other than +2.5V may be used by selecting $R_{REF} + R_g$ such that $V_{REF}/(R_{REF} + R_g) = 2mA$. Note, however, that increasing $R_{REF} + R_g$ above 3.5kΩ (or $V_{REF} > 7V$) makes the control amplifier transient response underdamped and increases the settling time. The settling time can be restored to its specified value by connecting a resistor R_X between pins 14 and 2 where $R_X \| (R_{REF} + R_g) = 1.25k\Omega$. R_X returns the control amplifier bandwidth to the value which minimizes settling time. (Since R_X is connected across 0V, the device gain is unaffected.)



a) Unipolar Output



b) Bipolar Output

Figure 1. Typical Connection Diagram for the AD559

CALIBRATION PROCEDURE FOR UNIPOLAR OUTPUTS

1. With all bits OFF, adjust the external operational amplifier null pot for E_{OUT} = 0.000V.
2. With all bits ON, adjust the gain trim for E_{OUT} = Nominal Full Scale -1LSB = +9.961V. (1LSB = 10V/256 = 39.1mV).

CALIBRATION PROCEDURE FOR BIPOLAR OUTPUTS

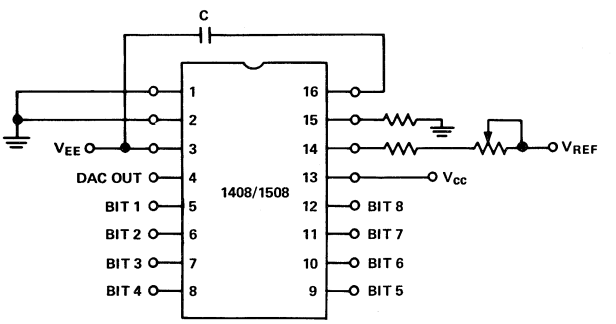
1. With all bits OFF, adjust the bipolar offset trim for E_{OUT} = -10.000V.
2. With Bit 1 (MSB) ON and Bits 2 through 8 OFF, adjust the gain trim for E_{OUT} = 0.000V.
3. With all bits ON, check that E_{OUT} = +10V -1LSB = +9.921V. (1LSB = 20V/256 = 78.2mV.)

THE AD559 AS A REPLACEMENT FOR THE 1408/1508 8-BIT DAC

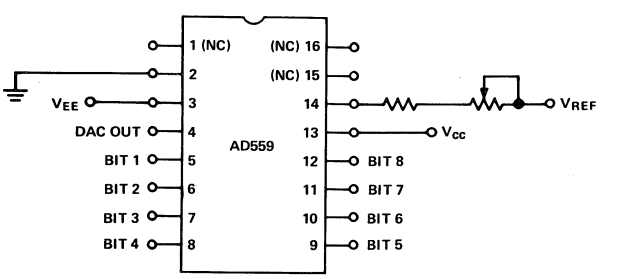
The AD559 is a superior alternative to the Motorola 1408/1508 8-bit DAC in most applications. Internal compensation is provided, thus eliminating the need for the external capacitor required by the Motorola device. Furthermore, the AD559's digital input currents are several orders of magnitude lower than the 1408/1508, making the AD559 completely CMOS compatible. The AD559 has the additional advantage of guaranteeing not only relative accuracy, but also differential nonlinearity (±½LSB max at +25°C) and complete monotonicity over the full operating temperature range.

Figure 2 is a comparative connection diagram for use in 1408/1508 replacement applications. The compensation capacitor, reference amplifier, balance resistor and compliance range control (pins 16, 15, and 1, respectively) are not required by the AD559; these pins are left uncommitted, enabling the user to plug the AD559 into existing circuits containing these components as well as to design it into new applications where these parts are omitted.

The AD559 is unconditionally stable for all reference voltages up to +10V. For reference voltages greater than +7V, a resistor, R_X (where $R_X \| R_{REF} + R_g$) = 1.25k may be used to minimize device settling time by compensating for the larger input resistance required at the control amplifier.



a) 1408/1508



b) AD559

Figure 2. 1408/1508 — AD559 Pin Out Comparison

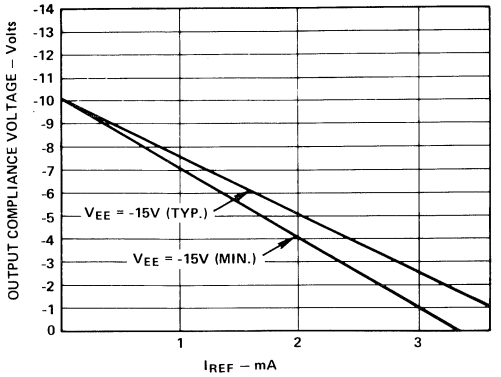


Figure 3. AD559 Output Compliance Voltage vs. Reference Current for V_{EE} = -15V

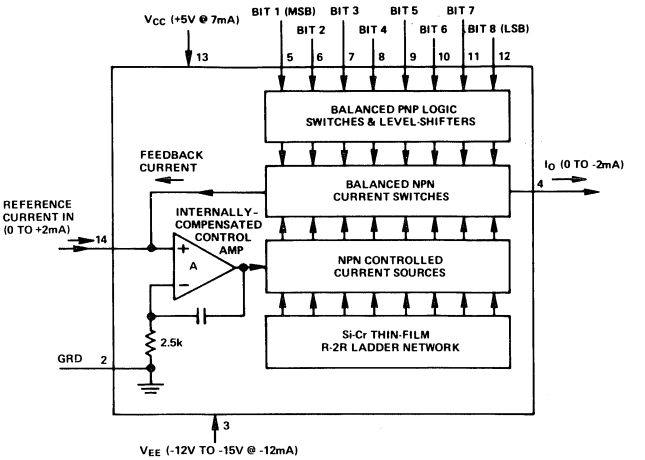
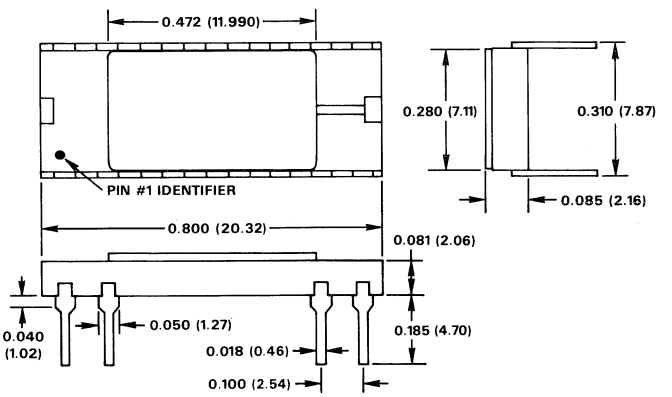


Figure 4. AD559 Block Diagram



Dimensions shown in inches and (mm)

Figure 5. Physical Dimensions

ANALOG DEVICES

Low Cost 10-Bit Monolithic D/A Converter

AD561

FEATURES

- Low Cost
- Complete Current Output Converter
- High Stability Buried Zener Reference
- Laser Trimmed to High Accuracy (1/4LSB Max Error, AD561K, T)
- Trimmed Output Application Resistors for 0 to +10, ±5 Volt Ranges
- Fast Settling — 250ns to 1/2LSB
- Guaranteed Monotonicity Over Full Operating Temperature Range
- TTL/DTL and CMOS Compatible (Positive True Logic)
- Single Chip Monolithic Construction
- Hermetically-Sealed Ceramic DIP (All Grades)

PRODUCT DESCRIPTION

The AD561 is an integrated circuit 10-bit digital-to-analog converter combined with a high stability voltage reference fabricated on a single monolithic chip. Using 10 precision high-speed current-steering switches, a control amplifier, voltage reference, and laser-trimmed thin-film SiCr resistor network, the device produces a fast, accurate analog output current. Laser trimmed output application resistors are also included to facilitate accurate, stable current-to-voltage conversion; they are trimmed to 0.1% accuracy, thus eliminating external trimmers in many situations.

Several important technologies combine to make the AD561 the most accurate and most stable 10-bit DAC available. The low temperature coefficient, high stability thin-film network is trimmed at the wafer level by a fine resolution laser system to 0.01% typical linearity. This results in an accuracy specification of ±1/4LSB max for the K and T versions, and 1/2LSB max for the J and S versions.

The AD561 also incorporates a low noise, high stability subsurface zener diode to produce a reference voltage with excellent long term stability and temperature cycle characteristics which challenge the best discrete zener references. A temperature compensation circuit is laser-trimmed to allow custom correction of the temperature coefficient of each device. This results in a typical full-scale temperature coefficient of 15ppm/°C; the T.C. is tested and guaranteed to 30ppm/°C max for the K and T versions, 60ppm/°C max for the S, and 80ppm/°C for the J.

All grades are packaged in a 16-pin hermetically-sealed ceramic dual-in-line package. The AD561J and K versions are specified for operation over the 0 to +70°C temperature range, the AD561S and T for operation over the full military temperature range from -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Advanced monolithic processing and laser trimming at the wafer level have made the AD561 the most accurate 10-bit converter available while keeping costs consistent with large volume integrated circuit production. The AD561K and T have 1/4LSB max relative accuracy and 1/2LSB max differential nonlinearity. The low T.C. R-2R ladder guarantees that all AD561 units will be monotonic over the entire operating temperature range.
2. Digital system interfacing is simplified by the use of a positive true straight binary code. The digital input voltage threshold is a function of the positive supply level; connecting V_{CC} to the digital logic supply automatically sets the threshold to the proper level for the logic family being used. Logic sink current requirement is only 25μA.
3. The high speed current steering switches are designed to settle in less than 250ns for the worst case digital code transition. This allows construction of successive-approximation A/D converters in the 3 to 5μs range.
4. The AD561 has an output voltage compliance range from -2 to +10 volts, thus allowing direct current-to-voltage conversion with just an output resistor, omitting the op amp. The 40MΩ open collector output impedance results in negligible errors due to output leakage currents.
5. Every AD561 is subjected to long term stabilization bakes and temperature cycled ten times from -65°C to +150°C prior to final test to insure reliability and long-term stability.

SPECIFICATIONS (T_A = +25°C, V_{CC} = +5V, V_{ee} = -15V, unless otherwise specified)

MODEL	AD561J MIN	AD561J TYP	AD561J MAX	AD561K MIN	AD561K TYP	AD561K MAX	UNITS
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			*			V
Bit OFF Logic "0"			+0.8			*	V
CMOS, 10V ≤ V_{CC} ≤ 16.5V (See Figure 1)							
Bit ON Logic "1"	70% V_{CC}			*			V
Bit OFF Logic "0"			30% V_{CC}			*	V
Logic Current (Each Bit) (T_{min} to T_{max})							
Bit ON Logic "1"		+5	+100		*	*	nA
Bit OFF Logic "0"		-5	-25		*	*	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	*	*	*	mA
Bipolar	±0.75	±1.0	±1.2	*	*	*	mA
Resistance (Exclusive of Application Resistors)		40M			*		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		*	*	% of F.S.
Capacitance		25			*		pF
Compliance Voltage	-2	-3	+10	*	*	*	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			*		ns
POWER REQUIREMENTS							
V_{CC}, +4.5V dc to +16.5V dc		8	10		*	*	mA
V_{EE}, -10.8V dc to -16.5V dc		12	16		*	*	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5V dc to +16.5V dc		2	10		*	*	ppm of F.S./%
V_{EE}, -10.8V dc to -16.5V dc		4	25		*	*	ppm of F.S./%
TEMPERATURE RANGE							
Operating		0 to +70			*	*	°C
Storage		-65 to +150			*	*	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of F.S./°C
Bipolar Zero		2	20		2	10	ppm of F.S./°C
Full Scale		15	80		15	30	ppm of F.S./°C
Differential Nonlinearity		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
PROGRAMMABLE OUTPUT		0 to +10			*		V
RANGES (See Figs. 5, 6)		-5 to +5			*		V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			*		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			*		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			*		% of F.S.
Bipolar Zero (With 20Ω Trimmer)		±0.2			*		% of F.S.

***Specifications same as AD561J specs.**
Specifications subject to change without notice.

MODEL	AD561S MIN	AD561S TYP	AD561S MAX	AD561T MIN	AD561T TYP	AD561T MAX	UNITS
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			**			V
Bit OFF Logic "0"			+0.8			**	V
CMOS, 10V ≤ V_{CC} ≤ 16.5V (See Figure 1)							
Bit ON Logic "1"	70% V_{CC}			**			V
Bit OFF Logic "0"			30% V_{CC}			**	V
Logic Current (Each Bit) (T_{min} to T_{max})							
Bit ON Logic "1"		+20	+100		**	**	nA
Bit OFF Logic "0"		-25	-100		**	**	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	**	**	**	mA
Bipolar	±0.75	±1.0	±1.2	**	**	**	mA
Resistance (Exclusive of Application Resistors)		40M			**		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		**	**	% of F.S.
Capacitance		25			**		pF
Compliance Voltage	-2	-3	+10	**	**	**	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			**		ns
POWER REQUIREMENTS							
V_{CC}, +4.5V dc to +16.5V dc		6	10		**	**	mA
V_{EE}, -10.8V dc to -16.5V dc		11	16		**	**	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5V dc to +16.5V dc		2	10		**	**	ppm of F.S./%
V_{EE}, -10.8V dc to -16.5V dc		4	25		**	**	ppm of F.S./%
TEMPERATURE RANGE							
Operating		-55 to +125			**	**	°C
Storage		-65 to +150			**	**	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of F.S./°C
Bipolar Zero		2	20		2	10	ppm of F.S./°C
Full Scale		15	60		15	30	ppm of F.S./°C
Differential Nonlinearity		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
PROGRAMMABLE OUTPUT		0 to +10			**		V
RANGES (See Figs. 5, 6)		-5 to +5			**		V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			**		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			**		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			**		% of F.S.
Bipolar Zero (With 20Ω Trimmer)		±0.2			**		% of F.S.

****Specifications same as AD561S specs.**
Specifications subject to change without notice.

DIGITAL LOGIC INTERFACE

All standard positive supply logic families interface easily with the AD561. The digital code is positive true binary (all bits high, Logic "1", gives positive full scale output). The logic input load factor (100nA max at Logic "1", -25μA max at Logic "0", 3pF capacitance), is less than one equivalent digital load for all logic families, including unbuffered CMOS. The digital threshold is set internally as a function of the positive supply, as shown in Figure 1. For most applications, connecting V_{CC} to the positive logic supply will set the threshold at the proper level for maximum noise immunity. For nonstandard applications, refer to Figure 1 for threshold levels. Uncommitted bit input lines will assume a "1" state (similar to TTL), but they are high impedance and subject to noise pickup. Unused digital inputs should be connected directly to ground or V_{CC}, as desired.

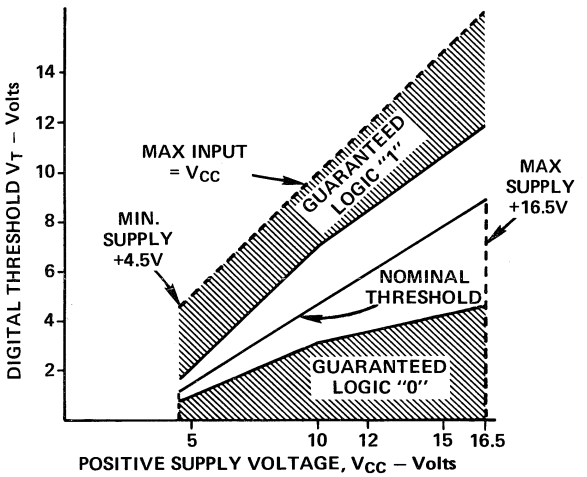
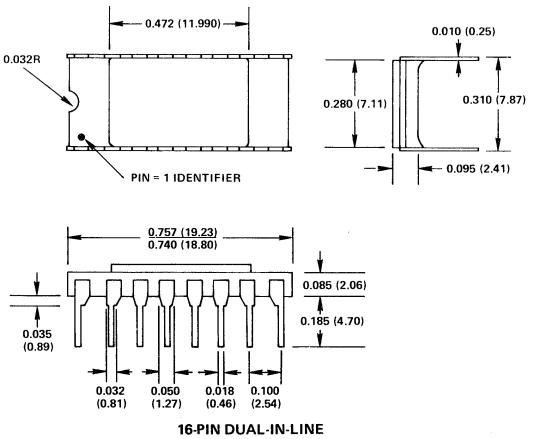


Figure 1. Digital Threshold Vs. Positive Supply



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Figure 2.

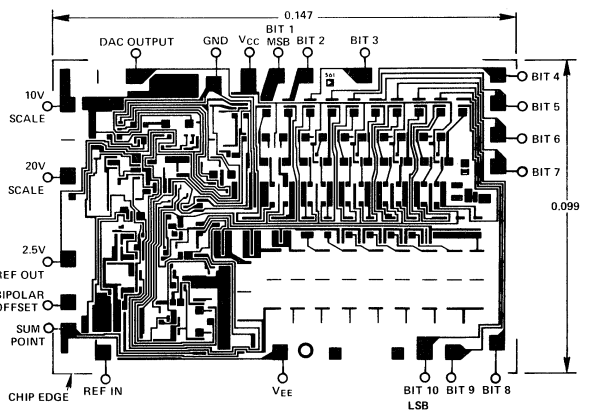
THE AD561 OFFERS TRUE 10-BIT RESOLUTION OVER FULL TEMPERATURE RANGE

ACCURACY: Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output (see following page) from the ideal analog output (a straight line drawn from 0 to F.S. – 1LSB) for any bit combination. The AD561 is laser trimmed to 1/4LSB (0.025% of F.S.) maximum error at +25°C for the K and T versions – 1/2LSB for the J and S.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a single-valued function of the input. All versions of the AD561 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential nonlinearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 9.8mV change in the analog output (1LSB = 10V x 1/1024 = 9.8mV). If in actual use, however, a 1LSB change in the input code results in a change of only 2.45mV (1/4LSB) in analog output, the differential nonlinearity error would be 7.35mV, or 3/4LSB. The AD561K and T have a max differential linearity error of 1/2LSB.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 2.5ppm/°C could under worst case conditions for a temperature change of +25°C to +125°C add 0.025% (100 x 2.5ppm/°C of error). The resulting error could then be as much as 0.025% + 0.025% = 0.05% of F.S. (1/2LSB represents 0.05% of F.S.). To be sure of accurate performance all versions of the AD561 are therefore 100% tested to be monotonic over the full operating temperature range.



THE AD561 IS AVAILABLE IN A LASER TRIMMED CHIP FORM. THE CHIP OFFERS MORE APPLICATION FLEXIBILITY THAN THE 16-PIN PACKAGED DEVICE. PLEASE CONSULT FACTORY FOR CHIP APPLICATION DETAILS.

Figure 3. Chip Bonding Diagram

AD561 ORDERING GUIDE

MODEL	TEMP RANGE	ACCURACY @ +25°C	GAIN T.C. (of F.S./°C)
AD561J	0 to +70°C	±½LSB max	80ppm max
AD561K	0 to +70°C	±¼LSB max	30ppm max
AD561S	-55 to +125°C	±½LSB max	60ppm max
AD561S/883B*	-55 to +125°C	±½LSB max	60ppm max
AD561T	-55 to +125°C	±¼LSB max	30ppm max
AD561T/883B*	-55 to +125°C	±¼LSB max	30ppm max

*The AD561S/883B and AD561T/883B are fully processed to MIL-STD-883A, Method 5004, Class B. The complete procedure list is available on request.

CONNECTING THE AD561 FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510, AD741L, AD301AL) is used, excellent performance can be obtained in many situations without trimming. (A 5mV op amp offset is equivalent to 1/2LSB on a 10 volt scale). If a 25Ω fixed resistor is substituted for the 50Ω trimmer, unipolar zero will typically be within ±1/10LSB (plus op amp offset), and full scale accuracy will be within ±1LSB. Substituting a 10Ω resistor for the 20Ω bipolar offset trimmer will give a bipolar zero error typically within ±1LSB.

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±½LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25picofarad DAC output capacitance.

FIGURE 5. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust op amp trimmer, R_1, until the output reads 0.000 volts (1LSB = 9.76mV).

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 50Ω gain trimmer, R_2, until the output is 9.990 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.23V full scale is desired (exactly 10mV/bit), insert a 120Ω resistor in series with R_2.

FIGURE 6. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.990 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . ZERO ADJUST

Turn ON MSB only, turn OFF all other bits. Adjust 20Ω trimmer R_3, to give 0.000 output volts.

STEP II . . . GAIN ADJUST

Turn OFF all bits, adjust 50Ω gain trimmer to give a reading of -5.000 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, the op amp trimmer is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 7. ±10 VOLT BUFFERED BIPOLAR OUTPUT

The AD561 can also be connected for a ±10 volt bipolar range with an additional external resistor as shown in Figure 7. A larger value trimmer is required to compensate for tolerance in the thin film resistors (which are trimmed to match the full scale current). For best full scale temperature coefficient performance, the external resistors should have a T.C. of -50ppm/°C. For applications requiring optimum performance, a ±10 volt bonding option is available on special order.

PIN CONFIGURATION
TOP VIEW

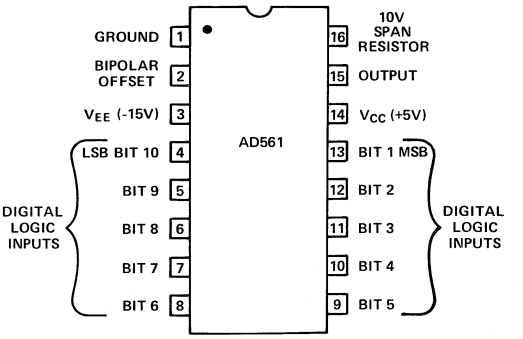


Figure 4.

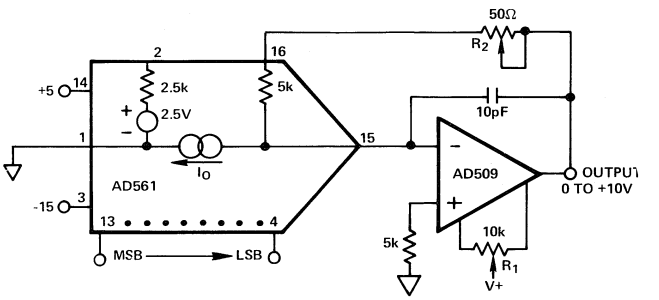


Figure 5. 0 to +10V Unipolar Voltage Output

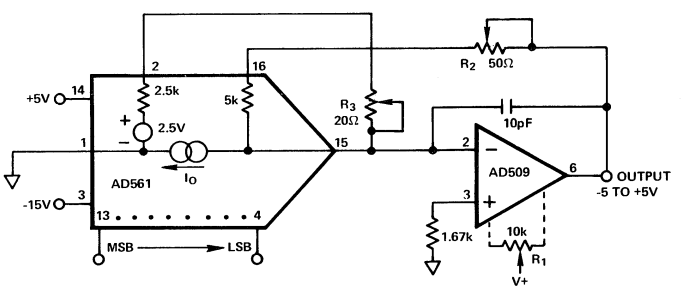


Figure 6. ±5V Buffered Bipolar Voltage Output

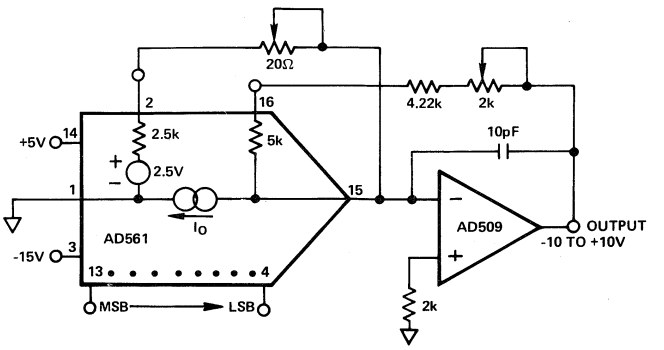


Figure 7. ±10V Buffered Voltage Output

CIRCUIT DESCRIPTION

A simplified schematic with the essential circuit features of the AD561 is shown in Figure 8. The voltage reference, CR1, is a buried zener (or subsurface breakdown diode). This device exhibits far better all-around performance than the NPN base-emitter reverse-breakdown diode (surface zener), which is in nearly universal use in integrated circuits as a voltage reference. Greatly improved long term stability and lower noise are the major benefits the buried zener derives from isolating the breakdown point from surface stress and mobile oxide charge effects. The nominal 7.5 volt device (including temperature compensation circuitry) is driven by a current source to the negative supply so that the positive supply can be allowed to go as low as 4.5 volts. The temperature coefficient of each diode is determined individually; this data is then used to laser trim a compensating circuit to balance the overall T.C. to zero. The typical resulting T.C. is 0 to ±15ppm/°C.

The negative reference level is inverted and scaled by A_1 to give a +2.5 volt reference (which can be driven by the low positive supply). The AD561, packaged in the 16-pin DIP, has the +2.5 volt reference (REF OUT) connected directly to the input of the control amplifier (REF IN). The buffered reference is not directly available externally except through the 2.5kΩ bipolar offset resistor; it can still be used as a voltage reference as shown below in Figure 9.

The 2.5kΩ scaling resistor and control amplifier A_2 then force a 1mA reference current to flow through reference transistor Q1, which has a relative emitter area of 8A. This is accomplished by forcing the bottom of the ladder to the proper voltage. Since Q_1 and Q_2 have equal emitter areas and have equal 5kΩ emitter resistors, Q_2 also carries 1mA. The ladder voltage drop constrains Q_7 (with area 4A) to carry only 0.5mA; Q_8 carries 0.25mA, etc.

The first four significant bit cells are scaled exactly in emitter area to match Q_1 for optimum V_{BE} and V_{BE} drift match, as well as for beta match. These effects are insignificant for the lower order bits, which account for a total of only 1/16 of full scale. However, the 18mV V_{BE} difference between two matched transistors carrying emitter currents in a ratio of 2:1 must be corrected. This is done by forcing 120μA through the 150Ω interbase resistors. These resistors and the R-2R ladder resistors are actively laser-trimmed at the wafer level to bring total device accuracy to better than ¼LSB. Sufficient ratio accuracy in the last two bits is obtained by simple emitter area ratio such that it is unnecessary to use additional area for ladder resistors. The current in Q_{16} is added to the ladder to balance it properly but is not switched to the output; thus full scale is 1023/1024 x 2mA.

The switching cell of Q_3, Q_4, Q_5 and Q_6 serves to steer the cell current either to ground (BIT 1 low) or to the DAC output (BIT 1 high). The entire switching cell carries the same current whether the bit is on or off, thus minimizing thermal transients and ground current errors. The logic threshold, which is generated from the positive supply (see Digital Logic Interface) is applied to one side of each cell.

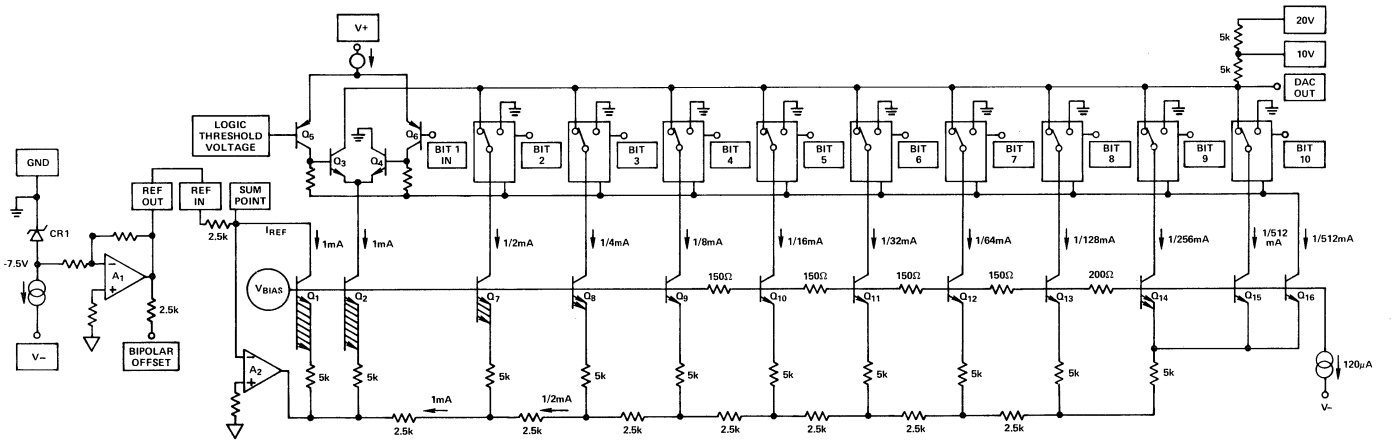


Figure 8. Circuit Diagram Showing Reference, Control Amplifier, Switching Cell, R-2R Ladder, and Bit Arrangement of AD561

PRECISION LOW-NOISE REFERENCE

The precision reference of the AD561 can be brought out separately from the DAC to serve as a master system reference. Since the reference is connected through the 2.5kΩ bipolar offset resistor, it must be buffered externally, as shown here in Figure 9. The DAC section can still be operated independently in a unipolar mode, but internal thermal and ground loop effects will create crosstalk of about 0.01% with an ideal ground. The long term stability of this reference will be especially good, typically ±0.01% per year or better. If the filter capacitor, C is not used, wideband output noise will be about 120ppm p-p (1.2mV p-p for 10 volts). If C is 4.7μF, wideband noise will be about 25μV p-p (10 volts out) and 15μV p-p from 0.1 to 10Hz.

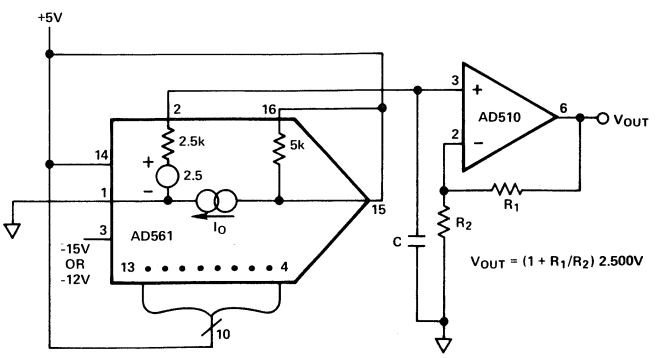


Figure 9. Precision Ultra Low Noise Reference

SETTLING TIME

The high speed NPN current steering switching cell and internally compensated reference amplifier of the AD561 are specifically designed for fast settling operation. The typical settling time to ±0.05% (½LSB) for the worst case transition (major carry, 0111111111 to 1000000000) is less than 250ns; the lower order bits all settle in less than 200ns. (Worst case settling occurs when all bits are switched, especially the MSB.) But full realization of this high speed performance requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD561 is specified in terms of the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter (see next page), or in many display applications. This form of conversion can give very fast operation if proper design and layout is done. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 12. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD561 output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.05% of full scale (for a full scale transition) requires 7.6 time constants. This effect is important for $R > 1k\Omega$.

If an op amp must be used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits are shown in the applications circuits using the fast settling AD509. The circuits shown settle to ±½LSB in 600ns unipolar and 1.1μs bipolar. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor, as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. Both supplies should be bypassed near the devices; 0.1μF will be sufficient since the AD561 runs at constant supply current regardless of input code.

POWER SUPPLY SELECTION

The AD561 will operate over a wide range of power supply voltages, with a total supply from 15.3 to 33 volts. Symmetrical supplies are not required, and in many applications not recommended.

The positive supply level determines the digital threshold level, as explained previously and shown in Figure 1. It is therefore recommended that V_{CC} be connected directly to the digital supply for best threshold match.

Positive output voltage compliance range is unaffected by the positive supply level because of the open collector output stage design; thus the full +10 volt compliance is available even with a +5 volt V_{CC} level. Power supply rejection is excellent, so that digital supply noise will not be reflected to the output. but use of a 0.1μF bypass capacitor near the AD561 is recommended for decoupling.

The nominal negative supply level is -15 volts, with an allowable range of -10.8 to -16.5 volts. The negative supply level affects the negative compliance range, as shown in Figure 10.

OUTPUT VOLTAGE COMPLIANCE

The AD561 has a typical output compliance range from -3 to +10 volts. The output current is unaffected by changes in the output terminal voltage over that range. This results from the use of open collector output switching stages in a cascode configuration, and gives an output impedance of 40MΩ. Positive compliance range is limited only by collector breakdown (and is independent of positive supply level), but the negative range is limited by the required bias levels and resistor ladder voltage. Negative compliance varies with negative supply, as shown in Figure 10. The compliance range is guaranteed to be -2 to +10 volts with V_{EE} = -15 volts.

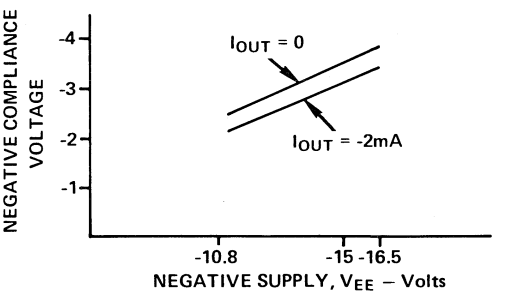


Figure 10. Typical Negative Compliance Range Vs. Negative Supply.

DIRECT UNBUFFERED VOLTAGE OUTPUT

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 1 shows a connection using the gain and bipolar output resistors to give a ±1.66 volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to -2mA unipolar output current and using the 2.5 volt reference voltage for bipolar offset. For example, setting R_X = 2.5kΩ gives a ±1 volt range with a 1kΩ equivalent output impedance. A 0 to +10 volt output can be obtained by connecting the 5kΩ gain resistor to 9.99 volts; again the digital code is complementary binary.

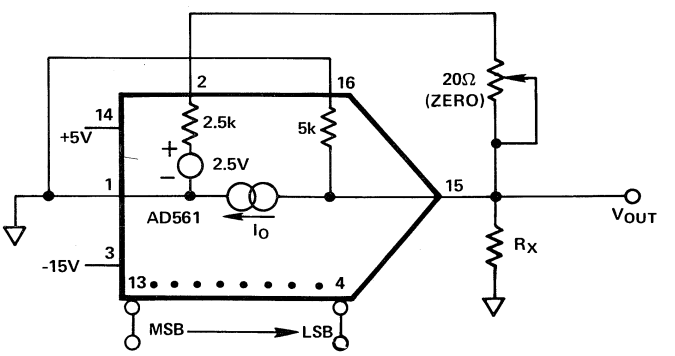


Figure 11. Unbuffered Bipolar Voltage Output

HIGH SPEED 10-BIT A/D CONVERTERS

The fast settling characteristics of the AD561 make it ideal for high speed successive approximation A/D converters. The internal reference and trimmed application resistors allow a 10-bit converter system to be constructed with a minimum parts count. Shown here is a configuration using standard components; this system completes a full 10-bit conversion in 5.5μs unipolar or 12μs bipolar. This converter will be accurate to ±1/2LSB of 10 bits and have a typical gain T.C. of 10ppm/°C.

In the unipolar mode, the system range is 0 to 9.99 volts, with each bit having a value of 9.76mV. For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from 1/2LSB below to 1/2LSB above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of +4.9mV; trim R_1 until the LSB just begins to appear in the output code (all other bits "0"). For full scale, use an input voltage of +9.9985 volts (10 volts − 1LSB − 1/2LSB); then trim R_2 again until the LSB just begins to appear (all other bits "1").

The bipolar signal range is -5.0 to +4.99 volts. Bipolar offset trimming is done by applying a +4.9mV input signal and trimming R_1 for the LSB transition (MSB "1", all other bits "0"). Full scale is set by applying -4.995 volts and trimming R_2 for the LSB transition (all other bits "0"). In many applications, the pretrimmed application resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 10-bit ±½LSB accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized, as mentioned in the section on settling time. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance of 1kΩ, 1LSB = 2mV) to the point that comparator performance will be sacrificed. A 1kΩ resistor is the optimum value for this application for 10-bit accuracy. The chart shown in the figure gives the speed of the ADC for ±1/2LSB accuracy (and no missing codes) for 6, 8 and 10-bit resolution.

A much faster converter can be constructed by using higher performance external components. Each individual high-order bit settles in less than 250ns; the low-order bits less than 200ns. Because of this, a staged clock which speeds up for lower bits will improve the speed. Also, a faster comparator and Schottky TTL or ECL logic would be necessary. 10-bit converters in the 3 to 5μs range could be built around the AD561 with these techniques.

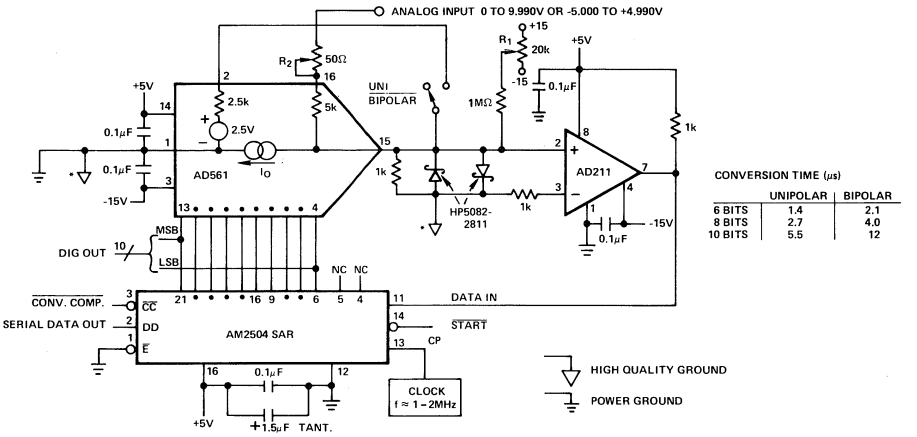


Figure 12. Fast Precision Analog to Digital Converter

DIGITAL 4 TO 20mA OR 1 TO 5 VOLT CONVERTER

A direct digital 4 to 20mA or 1 to 5 volt line driver can be built with the AD561 as shown in Figure 13. The 2.5 volt reference is divided to provide 1 volt at the op amp noninverting input − thus a zero input code results in a 1 volt output at the Darlington emitter (V_{OUT}). The 2k feedback resistance converts the nominal 2mA (±20%) full scale output from the AD561 to 4 volts, for a total output of 5 volts F.S. The voltage at the emitter forces a proportional current through the 250Ω (which appears at the collector as I_{OUT}). The AD561 current is added to the 4−20mA line; thus 5 volts full scale gives 22mA in the current loop. For exactly 20mA, trim the 1k pot for 4.5V F.S. (A single op amp circuit will not produce both 1 to 5 volt and 4 to 20mA outputs simultaneously.)

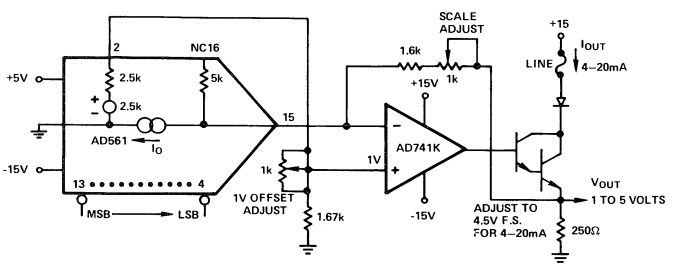


Figure 13. Digital 4 to 20mA or 1 to 5 Volt Line Driver

DIGITALLY PROGRAMMABLE SETPOINT COMPARATOR

Figure 15 demonstrates a high accuracy systems-oriented setpoint comparator. The 2.5 volt reference is buffered and amplified by the AD741K to produce an exact 10.000 volt reference which could be used as a primary system reference for several such circuits. The +10 volt compliance of the AD561 then allows it to generate a zero to +10 volt output swing through the 5kΩ application resistor without an additional op amp. The digital code for this system will be complementary binary (all 1's give 0.00 volts out).

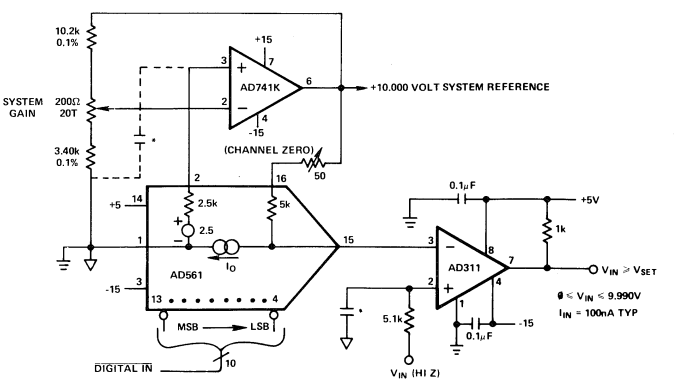


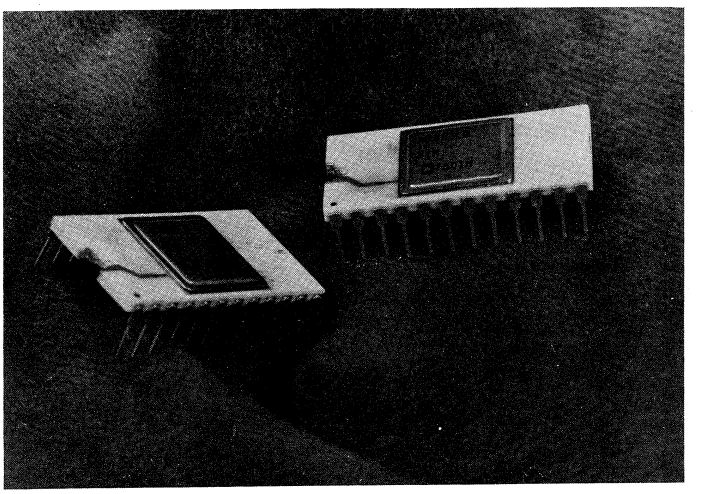
Figure 14. Digitally Programmable Set Point Comparator

ANALOG DEVICES

IC 12-Bit D/A Converter

AD562/AD563

FEATURES
Low Cost
True 12 Bit Accuracy
Guaranteed Monotonicity Over Full Temperature Range
Hermetic 24 Pin DIP
TTL/DTL and CMOS Compatibility



PRODUCT DESCRIPTION

The AD562/AD563 are integrated circuit 12 bit digital-to-analog converters consisting of a specially designed precision bipolar switch and control amplifier chip and a compatible high stability silicon chromium thin film resistor chip. The AD563 also includes its own internal voltage reference chip. All chips are internally connected and mounted in a hermetically sealed ceramic 24 lead dual-in-line package to produce a self-contained current output DAC.

A unique combination of advanced circuit design, high stability SiCr thin film resistor processing and laser trimming technology provide the AD562/AD563 with true 12 bit accuracy. The maximum error at +25°C is limited to ±½LSB on all versions and monotonicity is guaranteed over the full operating temperature range.

The AD562 and AD563 are recommended for high accuracy 12 bit D/A converter applications where true 12 bit performance is required, but low cost and small size are considerations. Both devices are also ideal for use in constructing A/D conversion systems and as building blocks for higher resolution D/A systems. J and K versions are specified for operation over the 0 to +70°C temperature range, the S and T for operation over the military temperature range, −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. True 12 bit resolution is achieved with guaranteed monotonicity over the full operating temperature range. Voltage outputs are easily implemented by using an external operational amplifier and the AD562/AD563's internally provided feedback resistors.
2. The devices incorporate a newly developed and fully differential, non-saturating precision current switching cell structure which provides increased immunity to supply voltage variation and also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation.
3. The thin film resistor network contains gain, range, and bipolar offset resistors so that various output voltage ranges can be programmed by changing connections to the device terminal leads. Thin film resistors are laser trimmed while the device is powered to accurately calibrate all scale factors. The scale factors are dependent upon the tracking coefficient (<±2ppm/°C) of these resistors, rather than upon their absolute temperature coefficients.

SPECIFICATIONS (T_A = +25°C, unless otherwise specified)

MODEL	AD562K	AD562S
DATA INPUTS		
TTL, V_{CC} = +5V, Pin 2		
Open Circuit		
Bit ON Logic "1"	+2.0V	*
Bit OFF Logic "0"	+0.8V max	*
CMOS, 4.75 ≤V_{CC} ≤15.8,		
Pin 2 Tied to Pin 1		
Bit ON Logic "1"	70%V_{CC} min	*
Bit OFF Logic "0"	30%V_{CC} max	*
Logic Current (Each Bit)		
Bit ON Logic "1"	+20nA typ, +100nA max	*
Bit OFF Logic "0"	−50μA typ, −100μA max	*
OUTPUT		
Current		
Unipolar	−1.6mA min, −2.0mA typ, −2.4mA max	*
Bipolar	±0.8mA min, ±1.0mA typ, ±1.2mA max	*
Resistance (Exclusive of		
Span Resistors)	5.3kΩ min, 6.6kΩ typ, 7.9kΩ max	*
Unipolar Zero (All Bits OFF)	0.01% of F.S. typ, 0.05% of F.S. max	*
Capacitance	33pF typ	*
Compliance Voltage	−1.5V to +10V typ	*
RESOLUTION	12 Bits	*
ACCURACY (Error Relative		
To Full Scale)	±1/2LSB max (0.012)% of F.S. max	±1/4LSB max (0.006)% of F.S. max
DIFFERENTIAL NONLINEARITY	±1/2LSB max	*
SETTLING TIME TO 1/2LSB		
All Bits ON-to-OFF or OFF-to-ON	1.5μs typ	*
POWER REQUIREMENTS		
V_{CC}, +4.75 to +15.8V dc	15mA typ, 18mA max	*
V_{EE}, −15V dc ±5%	20mA typ, 25mA max	*
POWER SUPPLY GAIN SENSITIVITY		
V_{CC} @ +5V dc	2ppm of F.S./% max	*
V_{CC} @ +15V dc	2ppm of F.S./% max	*
V_{EE} @ −15V dc	6ppm of F.S./% max	
TEMPERATURE RANGE		
Operating	0 to +70°C typ	−55°C to +125°C typ
Storage	−65°C to +150°C typ	−65°C to +150°C
TEMPERATURE COEFFICIENT		
Unipolar Zero	2ppm of F.S./°C max	*
Bipolar Zero	4ppm of F.S./°C max	*
Gain	5ppm of F.S./°C max	*
Differential Nonlinearity	2ppm of F.S./°C typ	1ppm of F.S./°C typ
MONOTONICITY	Guaranteed Over Full Operating	*
	Temperature Range	*
EXTERNAL ADJUSTMENTS[1]		
Gain Error with Fixed 50Ω Resistor	±0.2% of F.S. typ	*
Bipolar Zero Error with Fixed		
10Ω Resistor	±0.1% of F.S. typ	*
Gain Adjustment Range	±0.25% of F.S. typ	*
Binary Bipolar Zero Adjustments		
Range	±0.25% of F.S. typ	*
BCD Bipolar Offset Adjustment		
Range	±0.17% of F.S. typ	*
PROGRAMMABLE OUTPUT		
RANGES (See Figs. 1a, 1b)	0 to +5V typ	*
	−2.5V to +2.5V typ	*
	0V to +10V typ	*
	−5V to +5V typ	*
	−10V to +10V typ	*
REFERENCE INPUT		
Input Impedance	20kΩ typ	*

*Specifications same as AD562K. **Specifications same as AD562J. ***Specifications same as AD562S. [1] Device calibrated with internal reference.

AD563J	AD563K	AD563S	AD563T
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
5.0kΩ min, 6.6kΩ typ, 8.0kΩ max	*	**	*
*	*	*	*
*	*	*	*
-1.5V	**	*	*
*	*	*	*
±½ LSB max	***	***	***
*	*	*	*
*	*	*	*
15mA typ, 20mA max	**	**	**
*	*	*	*
3ppm of F.S./% typ, 10ppm of F.S./% max	***	**	**
3ppm of F.S./% typ, 10ppm of F.S./% max	**	**	**
14ppm of F.S./% typ, 25ppm of F.S./% max	**	**	**
*	*	***	***
*	*	***	***
With Internal Reference			
1ppm of F.S./°C typ, 2ppm of F.S./°C max	**	**	**
10ppm of F.S./°C max	**	**	**
50ppm of F.S./°C max	20ppm of F.S./°C max	30ppm of F.S./°C max	10ppm of F.S./°C max
*	*	*	*
*	*	*	*
*	*	*	*
With Fixed 10Ω Resistor			
±0.2% of F.S. typ	**	**	**
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
5kΩ typ	**	**	**

Specifications subject to change without notice.

THE AD562/AD563 OFFERS TRUE 12-BIT RESOLUTION OVER FULL TEMPERATURE RANGE

Accuracy: Analog Devices defines accuracy as the maximum deviation of the actual DAC output from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) *for any bit combination.* The AD563, for example, is laser trimmed to ¼LSB (0.006% of F.S.) maximum error at +25°C for K, S and T versions . . . ½LSB for the J version.

Monotonicity: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a single-valued function of the input. All versions of the AD562/AD563 are monotonic over their full operating temperature range.

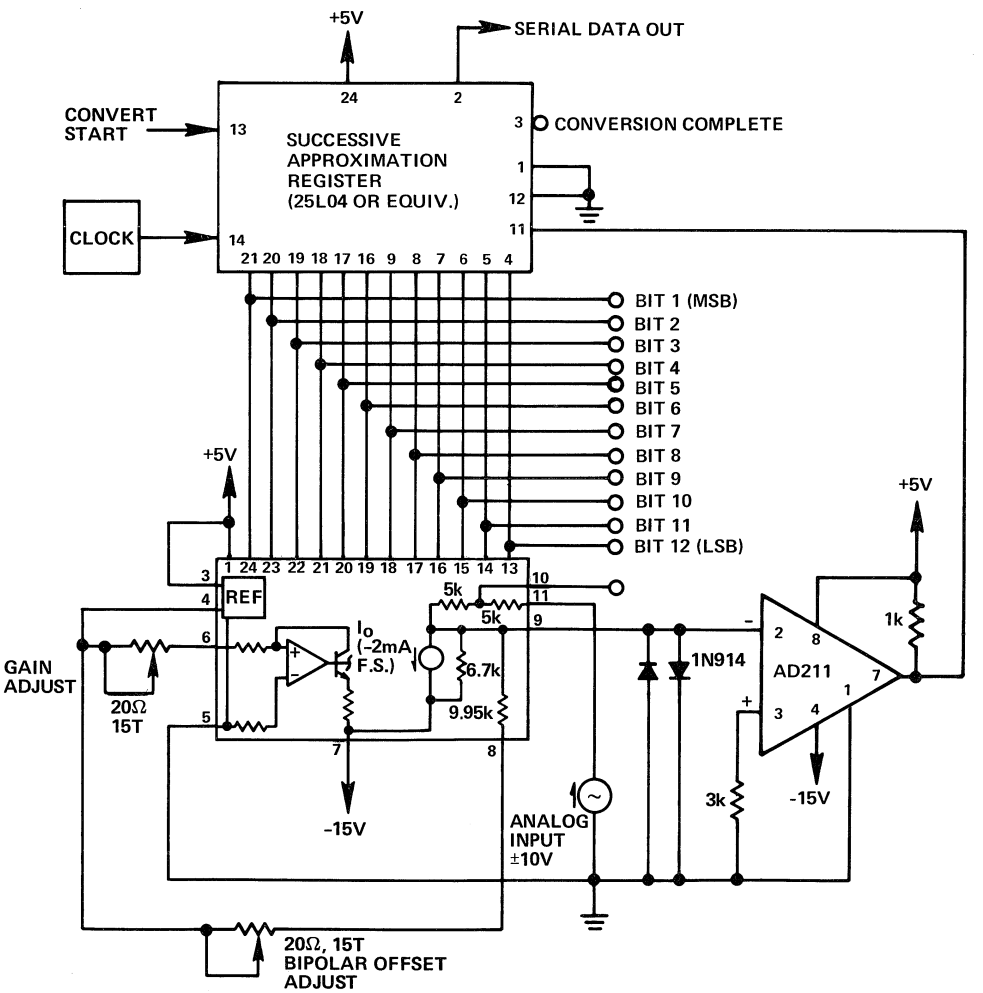
Differential Nonlinearity: Monotinic behavior requires that the differential nonlineearity error be <1LSB both at 25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variaion in analog value, normalized to full scale, associated with a one LSB change in digital input code. For example, for a 10V full-scale output, a change of one LSB in the digital input code should result in a 2.4mV change in the analog output (10V x 1/4096 = 2.4mV). If in actual use, however, a one LSB change in the input code results in a change of 1.3mV in analog output, the differential nonlinearity would be 1.1mV, or 0.011% of F.S.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1ppm/°C could, under worst case conditions for a temperature change of +25°C to +125°C, add 0.01% (100°C x 1ppm/°C) of error. The resulting error could then be as much as 0.006% + 0.01% = 0.016% of F.S. (1LSB represents 0.024% of F.S.). All versions of the AD562/AD563 are 100% tested to be monotonic over the full operating temperature range.

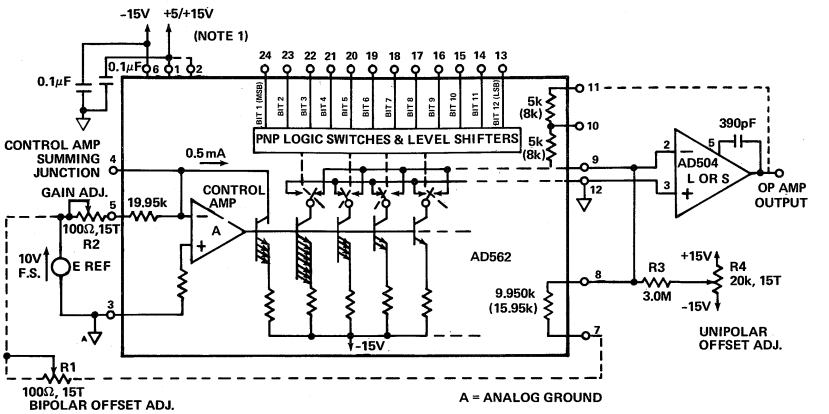
12-BIT SUCCESSIVE APPROXIMATION A/D CONVERTER USING THE AD563

The most popular medium speed (1 to 10μs/bit) A/D converter is the successive approximation type, in which the digital output equivalent of the analog input is formed by comparing a programmed D/A converter output with the analog input. The digital output is successively compared, one bit at a time, until the final comparison is within ½LSB.

The convertions speed of a successive approximation A/D converter is primarily determined by the settling time of each bit to ½LSB, the speed of the comparator, and the switching speed of the "SAR". The A/D converter configuration shown in Figure 5 will convert at a 40kHz rate for 12 bits.



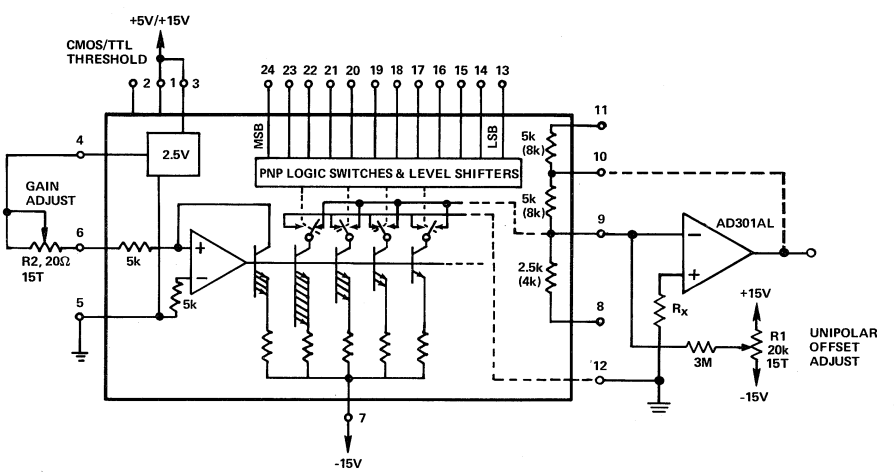
12-Bit Successive Approximation A/D Converter



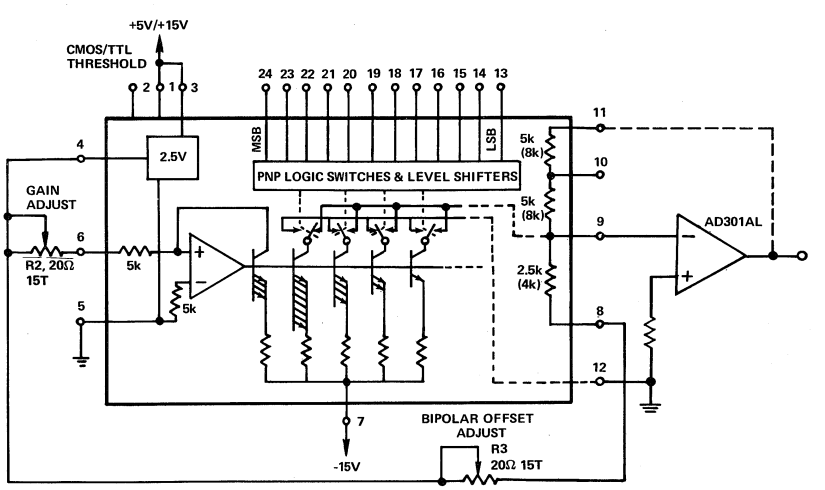
NOTE 1.
- A. FOR TTL AND DTL COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND LEAVE PIN 2 OPEN.
- B. FOR LOW VOLTAGE CMOS COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.
- C. FOR HIGH VOLTAGE CMOS COMPATIBILITY, CONNECT +15 VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.

NOTE 2. RESISTOR VALUES IN PARENTHESES ARE FOR BCD VERSION.

AD562 in Typical Unipolar and Bipolar Connection Scheme



AD563 in Typical Unipolar Connection Scheme



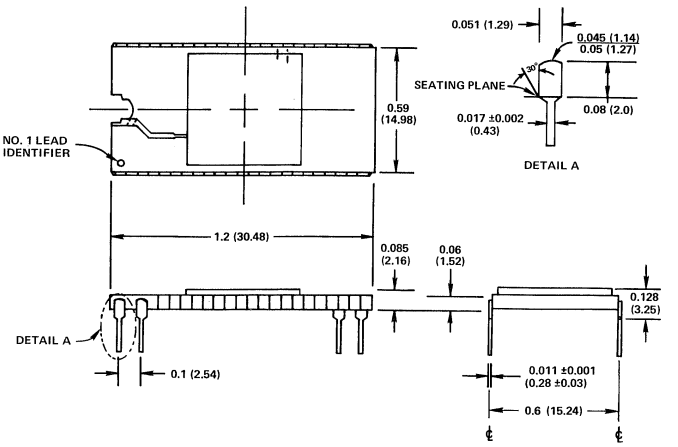
NOTE 1.
- A. FOR TTL AND DTL COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND LEAVE PIN 2 OPEN.
- B. FOR LOW VOLTAGE CMOS COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.
- C. FOR HIGH VOLTAGE CMOS COMPATIBILITY, CONNECT +15 VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.

NOTE 2. RESISTOR VALUES IN PARENTHESES ARE FOR BCD MODEL.
NOTE 3. SUPPLIES MAY BE BYPASSED WITH 0.1μF CAPACITORS.
NOTE 4. IN UNIPOLAR OPERATION, R_X SHOULD BE MADE EQUAL TO THE PARALLEL COMBINATION OF THE INTERNAL FEEDBACK RESISTOR AND 6.6k. IN BIPOLAR, R_X EQUALS THE FEEDBACK RESISTOR IN PARALLEL WITH 1.8k.

AD563 in Typical Bipolar Connection Scheme

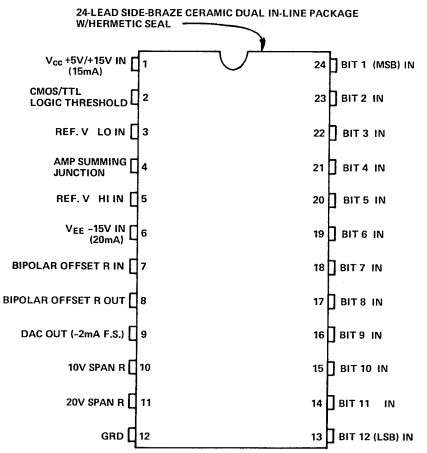
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

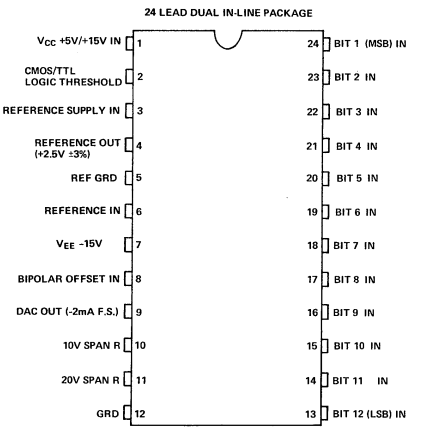


24 Lead Dual-in-Line Package

PIN CONFIGURATIONS
TOP VIEW



AD562



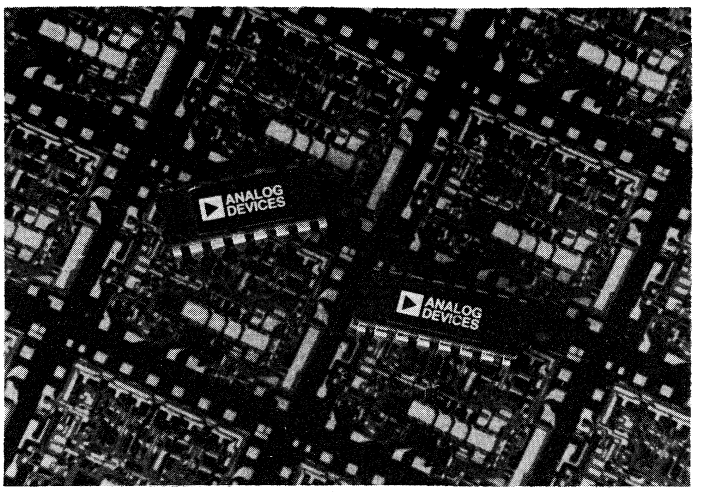
AD563

8 Bit Monolithic Multiplying D/A Converter

AD1408/AD1508

FEATURES

- **Improved Replacement for Industry Standard 1408/1508**
- **Improved Settling Time: 250ns typ**
- **Improved Linearity: ±0.1% Accuracy Guaranteed Over Temperature Range (-9 Grade)**
- **High Output Voltage Compliance: +0.5V to -5.0V**
- **Low Power Consumption: 157mW typ**
- **High Speed 2-Quadrant Multiplying Input: 4.0mA/μs Slew Rate**
- **Single Chip Monolithic Construction**
- **Hermetic 16 Pin Ceramic DIP**
- **Low Cost**



PRODUCT DESCRIPTION

The AD1408 and AD1508 are low cost monolithic integrated circuit 8-bit multiplying digital-to-analog converters, consisting of matched bipolar switches, a precision resistor network and a control amplifier. The single chip is mounted in a hermetically sealed ceramic 16 lead dual-in-line package.

Advanced circuit design and precision processing techniques result in significant performance advantages over older industry standard 1408/1508 devices. The maximum linearity error over the specified operating temperature range is guaranteed to be less than ±¼LSB (-9 grade) while settling time to ±½LSB is reduced to 250ns typ. The temperature coefficient of gain is typically 20ppm/°C and monotonicity is guaranteed over the entire operating temperature range.

The AD1408/AD1508 is recommended for all low-cost 8-bit DAC requirements; it is also suitable for upgrading overall performance where older, less accurate and slower 1408/1508 devices have been designed in. The AD1408 series is specified for operation over the 0 to +75°C temperature range, the AD1508 series for operation over the entire military temperature range of -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Monolithic IC construction makes the AD1408/AD1508 an optimum choice for applications where low cost is a major consideration.
2. The AD1408/AD1508 directly replaces other devices of this type.
3. Versatile design configuration allows voltage or current outputs, variable or fixed reference inputs, CMOS or TTL logic compatibility and a wide choice of accuracy and temperature range specifications.
4. Accuracies within ±¼LSB allow performance improvement of older applications without redesign.
5. Faster settling time (250ns typ) permits use in higher speed applications.
6. Low power consumption improves stability and reduces warm-up time.
7. The AD1408/AD1508 multiplies in two quadrants when a varying reference voltage is applied. When multiplication is not required, a fixed reference is used.
8. The AD1408/AD1508 is available in chip form; please consult factory for details.
9. The device is packaged in a hermetically-sealed ceramic 16 lead dual-in-line package. Processing to MIL-STD-883 level B is available.

SPECIFICATIONS (typical @ +25°C and V_{CC} = +5.0V dc, V_{EE} = -15V dc unless otherwise noted)

MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
POWER SUPPLY VOLTAGE	V_{CC}	+5.5	V dc
	V_{EE}	-16.5	V dc
DIGITAL INPUT VOLTAGE	V_5 thru V_{12}	+5.5, 0	V dc
APPLIED OUTPUT VOLTAGE	V_0	+0.5, -5.2	V dc
REFERENCE CURRENT	I_{14}	5.0	mA
REFERENCE AMPLIFIER INPUTS	V_{14}, V_{15}	V_{CC}, V_{EE}	V dc
POWER DISSIPATION			
(Package Limitation)		1000	mW
Derate above T_A = +25°C	P_D	6.7	mW/°C
OPERATING TEMPERATURE RANGE			
AD1408 Series	T_A	0 to +75	°C
AD1508 Series	T_A	-55 to +125	°C
STORAGE TEMPERATURE RANGE	T_{STG}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V dc, V_{EE} = -15V dc, $\frac{V_{REF}}{R14}$ = 2.0mA, **AD1508 Series:** T_A = -55°C to +125°C
AD1408 Series: T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
RELATIVE ACCURACY					
(Error Relative to Full Scale I_O)					
AD1508-9, AD1408-9	E_r	–	–	±0.10	%
AD1508-8, AD1408-8	E_r	–	–	±0.19	%
AD1408-7	E_r	–	–	±0.39	%
SETTLING TIME					
to Within 1/2LSB [Includes t_{PLH}]					
(T_A = +25°C)	t_S	–	250	–	ns
PROPAGATION DELAY TIME					
T_A = +25°C	t_{PLH}, t_{PHL}	–	30	100	ns
OUTPUT FULL SCALE CURRENT DRIFT	TCI_O	–	-20	–	ppm/°C
DIGITAL INPUT LOGIC LEVELS (MSB)					
High Level, Logic "1"	V_{IH}	2.0	–	–	V dc
Low Level, Logic "0"	V_{IL}	–	–	0.8	V dc
DIGITAL INPUT CURRENT (MSB)					
High Level, V_{IN} = 5.0V	I_{IH}	–	0	0.04	mA
Low Level, V_{IL} = 0.8V	I_{IL}	–	-0.4	-0.8	mA
REFERENCE INPUT BIAS CURRENT					
(Pin 15)	I_{15}	–	-1.0	-3.0	μA
OUTPUT CURRENT RANGE					
V_{EE} = -5.0V	I_{OR}	0	2.0	2.1	mA
V_{EE} = -6.0V to -15V	I_{OR}	0	2.0	4.2	mA
OUTPUT CURRENT					
V_{REF} = 2.000V, R14 = 1000Ω	I_O	1.9	1.99	2.1	mA
OUTPUT CURRENT					
(All Bits Low)	I_O (min)	–	0	4.0	μA
OUTPUT VOLTAGE COMPLIANCE					
($E_1 \leq$ 0.19% at T_A = +25°C)					
V_{EE} = -5V	V_O	–	–	-0.6, +0.5	V dc
V_{EE} below -10V	V_O	–	–	-5.0, +0.5	V dc
REFERENCE CURRENT SLEW RATE	SRI_{REF}	–	4.0	–	mA/μs
OUTPUT CURRENT POWER SUPPLY					
SENSITIVITY	$PSSI_O$	–	0.5	2.7	μA/V
POWER SUPPLY CURRENT					
(All Bits Low)	I_{CC}	–	+9	+14	mA
	I_{EE}	–	-7.5	-13	mA
POWER SUPPLY VOLTAGE RANGE					
(T_A = +25°C)	V_{CCR}	+4.5	+5.0	+5.5	V dc
	V_{EER}	-4.5	-15	-16.5	V dc
POWER DISSIPATION					
All Bits Low					
V_{EE} = -5.0V dc	P_D	–	82	135	mW
V_{EE} = -15V dc	P_D	–	157	265	mW
All Bits High					
V_{EE} = -5.0V dc	P_D	–	70	–	mW
V_{EE} = -15V dc	P_D	–	132	–	mW

Specifications subject to change without notice.

APPLYING THE AD1408/1508

Reference Amplifier Drive and Compensation

Figures 2a and 2b are the connection diagrams for using the AD1408/AD1508 in basic voltage output modes. In Figure 2a, a positive reference voltage, V_{REF}, is converted to a current by resistor R14. This reference current determines the scale factor for the output current such that the full scale output is 1LSB (1/256) less than the reference current. R15 provides bias current compensation to the reference control amplifier to minimize temperature drift; it is nominally equal to R14 although it needn't be a stable precision resistor. This configuration develops a negative output voltage across R_L and requires a positive V_{REF}.

If a negative V_{REF} is to be used, connections to the reference control amplifier must be reversed as shown in Figure 2b. This circuit also delivers a negative output voltage, but presents a high impedance to the reference source. The negative V_{REF} must be at least 4 volts above the V_{EE} supply.

Two quadrant multiplication may be performed by applying a bipolar ac signal as the reference as long as pin 14 is positive relative to pin 15 (reference current must flow into pin 14). If the ac reference is applied to pin 14 through R14, a negative voltage equal to the negative peak of the ac reference must be applied through R15 to pin 15; if the ac reference is applied to pin 15 through R15, a positive voltage equal to the positive peak of the ac reference must be applied through R14 to pin 14.

When a dc reference is used, capacitive bypass from reference to ground will improve noise rejection.

The compensation capacitor, C, provides proper phase margin for the reference control amplifier. As R14 is increased, the closed-loop gain of the amplifier is decreased, therefore C must be increased. For R14 = 1.0kΩ, 2.5kΩ and 5.0kΩ, minimum values of capacitance are 15pF, 37pF and 75pF respectively. C may be tied to either V_{EE} or ground, but tying it to V_{EE} increases negative supply noise rejection. If the reference is driven by a high-impedance current source, heavy compensation of the amplifier is required; this causes a reduction in overall bandwidth.

Output Current Range

The nominal value for output current range is 0 to 1.992mA as determined by a 2mA reference current. If V_{EE} is more negative than -7.0 volts, this range may be increased to a maximum of 0 to 4.2mA. An increase in speed may be realized at increased output current levels, but power consumption will increase, possibly causing small shifts in linearity.

Pin 1, range control, may be grounded or unconnected. Although other older devices of this type require different terminations for various applications, the AD1408/AD1508 compensates automatically. This pin is not connected internally, therefore any previously installed connections will be tolerated.

Output Voltage Range

The voltage on pin 4 is restricted to a +0.5 to -0.6 volt range when V_{EE} = -5V. When V_{EE} is more negative than -10 volts, this range is extended to +0.5 to -5.0 volts. If the current into pin 14 is 2mA (full-scale output current = 1.992mA), a 2.5kΩ resistor between the output, pin 4, and ground will provide a 0 to -4.980 volt full-scale. If R_L exceeds 500Ω however, the settling time of the device is increased.

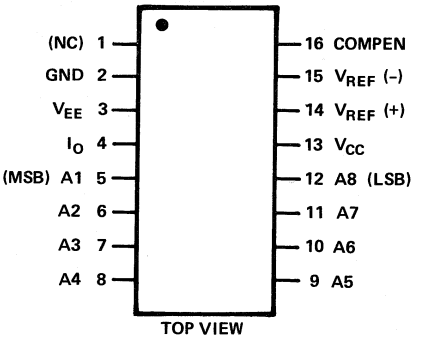
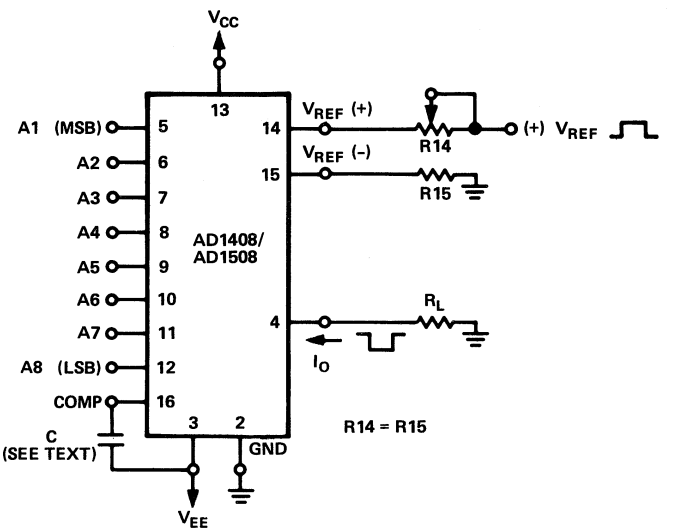
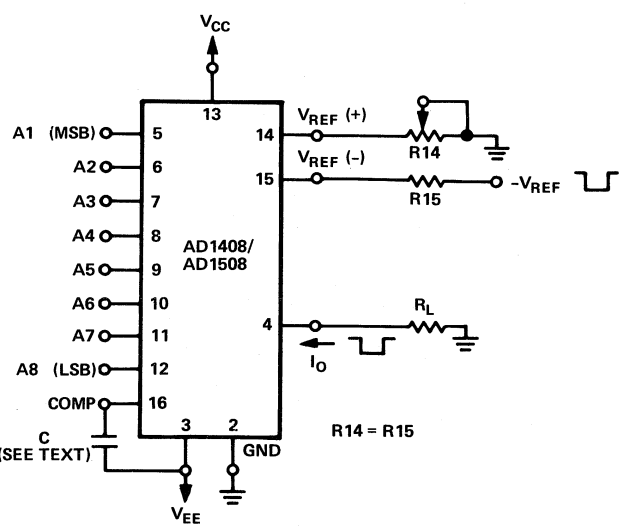


Figure 1. Pin Connections



a. Connections for Use with Positive Reference



b. Connections for Use with Negative Reference

Figure 2. Basic Connections

Voltage Output

A low impedance voltage output may be derived from the output current of the AD1408/AD1508 by using an output amplifier as shown in Figure 3. The output current I_O flows in R_O to create a positive-going voltage range at the output of amplifier A1. R_O may be chosen for the desired range of output voltage; the complete circuit transfer function is given in Figure 3.

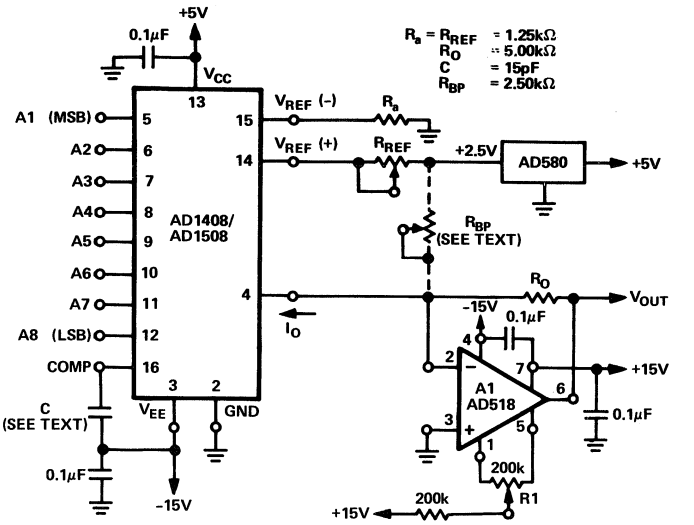
If a bipolar output voltage range is desired, R_{BP}, shown dotted, must be installed. Its purpose is to provide an offset equal to one-half of full-scale at the output of A1. The procedure for calibrating the circuit of Figure 3 is as follows:

Calibration for Unipolar Outputs (No R_{BP})

1. With all bits "OFF", adjust the A1 null-pot, R1, for V_{OUT} = 0.00V.
2. With all bits "ON", adjust R_{REF} for V_{OUT} = (Nominal Full Scale) − 1LSB = +9.961 volts

Calibration for Bipolar Outputs (R_{BP} installed, R1 not required)

1. With all bits "OFF", adjust R_{BP} for V_{OUT} = −F.S. = −5.000 volts
2. With Bit 1 (MSB) "ON", and all other Bits "OFF", adjust R_{REF} for V_{OUT} = 0.000V.
3. With all bits "ON", verify that E_{OUT} = +5.000V− 1LSB = 4.961V.



$$V_{OUT} = \frac{V_{REF}}{R_{REF}}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

ADJUST V_{REF}, R_{REF} OR R_O SO THAT WITH ALL DIGITAL INPUTS AT LOGIC "1", V_{OUT} = 9.961 VOLTS:

$$V_{OUT} = \frac{2.5}{1.25k\Omega}(5k\Omega)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right] = 9.961 \text{ VOLTS}$$

Figure 3. Typical Connection Diagram, AD1408/AD1508, Voltage Output, Fixed Reference

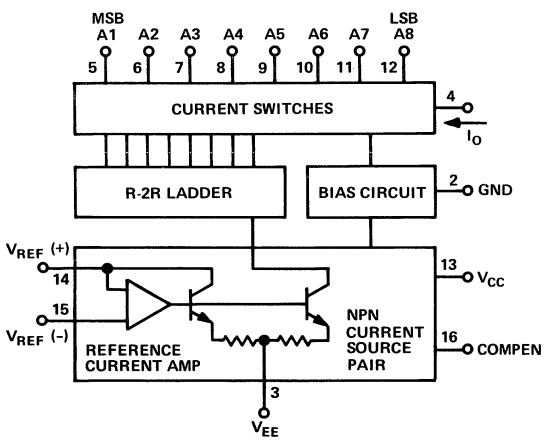
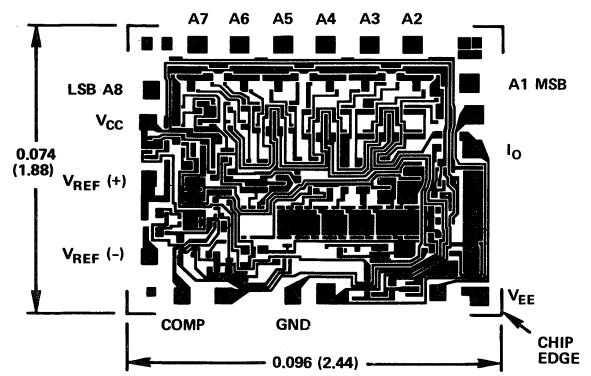


Figure 4. Simplified Block Diagram



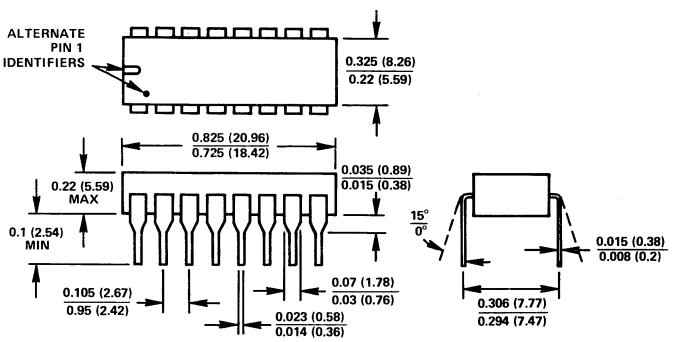
THE AD1408/AD1508 IS AVAILABLE IN CHIP FORM GUARANTEED TO -7 LEVEL PERFORMANCE. CONSULT FACTORY FOR APPLICATION AND PRICING DETAILS.

Figure 5. Chip Dimensions and Pad Layout. Dimensions shown in inches and (mm).

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-PIN DUAL-IN-LINE



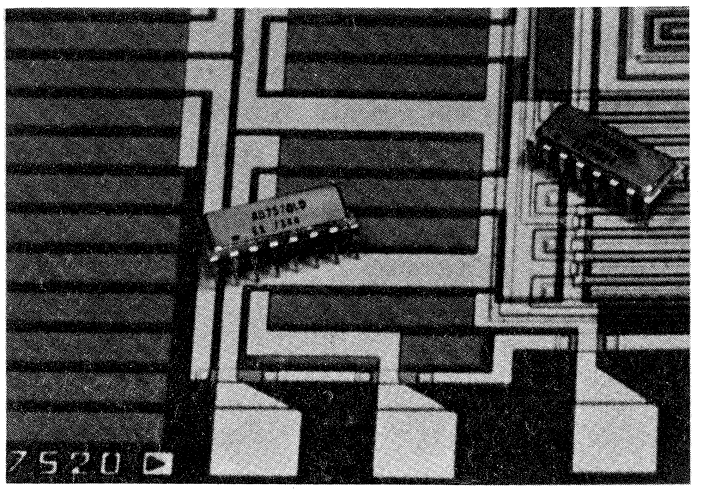
AD1408/AD1508 ORDERING GUIDE

MODEL	ACCURACY (±% F.S.)	TEMP. RANGE (°C)
AD1408-7D	0.39	0 to +75
AD1408-8D	0.19	0 to +75
AD1408-9D	0.10	0 to +75
AD1508-8D	0.19	-55 to +125
AD1508-9D	0.10	-55 to +125
AD1508-8D/ 883B	0.19	-55 to +125
AD1508-9D/ 883B	0.10	-55 to +125

CMOS 10&12-Bit Monolithic Multiplying D/A Converters

AD7520, AD7521

FEATURES
- **AD7520: 10 Bit Resolution**
- **AD7521: 12 Bit Resolution**
- **Linearity: 8, 9 and 10 Bit**
- **Nonlinearity Tempco: 2ppm of FSR/°C**
- **Low Power Dissipation: 20mW**
- **Current Settling Time: 500ns**
- **Feedthrough Error: 1/2LSB @ 100kHz**
- **TTL/DTL/CMOS Compatible**



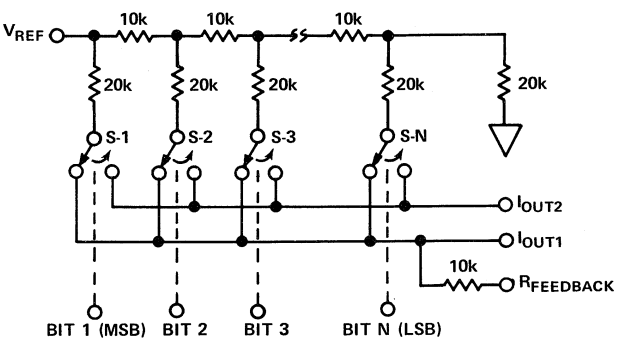
GENERAL DESCRIPTION

The AD7520 (AD7521) is a low cost, monolithic 10-bit (12-bit) multiplying digital-to-analog converter packaged in a 16-pin (18-pin) DIP. The devices use advanced CMOS and thin film technologies providing up to 10-bit accuracy with TTL/DTL/CMOS compatibility.

The AD7520 (AD7521) operates from +5V to +15V supply and dissipates only 20mW, including the ladder network.

Typical AD7520 (AD7521) applications include: digital/analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

FUNCTIONAL DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

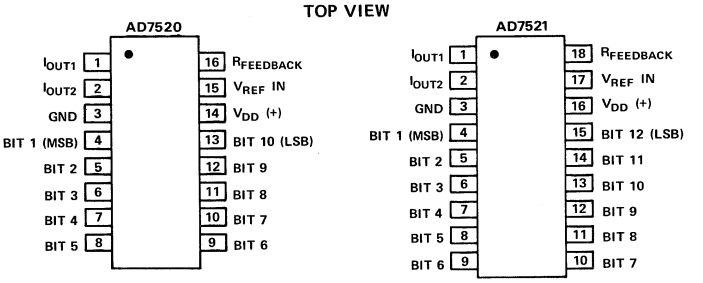
AD7520: N=10
AD7521: N=12
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0 to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8-Bit)	AD7520JN AD7521JN	AD7520JD AD7521JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7521KN	AD7520KD AD7521KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7521LN	AD7520LD AD7521LD	AD7520UD AD7521UD

PIN CONFIGURATION

TOP VIEW



PACKAGE IDENTIFICATION

Suffix D: Ceramic DIP package
Suffix N: Plastic DIP package

SPECIFICATIONS (V_{DD} = +15, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

PARAMETER	AD7520	AD7521	TEST CONDITIONS
DC ACCURACY[1]			
Resolution	10 Bits	12 Bits	
Nonlinearity (See Figure 5)			
	J, 0.2% of FSR max (8 Bit)	*	S,T,U: over -55°C to +125°C
	S, 0.2% of FSR max (8 Bit)	*	$-10V \leqslant V_{REF} \leqslant +10V$
	K, 0.1% of FSR max (9 Bit)	*	
	T, 0.1% of FSR max (9 Bit)	*	
	L, 0.05% of FSR max (10 Bit)	*	
	U, 0.05% of FSR max (10 Bit)	*	
Nonlinearity Tempco	2ppm of FSR/°C max	*	$-10V \leqslant V_{REF} \leqslant +10V$
Gain Error[2]	0.3% of FSR typ	*	$-10V \leqslant V_{REF} \leqslant +10V$
Gain Error Tempco[2]	10ppm of FSR/°C max	*	$-10V \leqslant V_{REF} \leqslant +10V$
Output Leakage Current (either output)	200nA max	*	Over specified temperature range
Power Supply Rejection (See Figure 6)	50ppm of FSR%/°C typ	*	
AC ACCURACY			To 0.05% of FSR
Output Current Settling Time (See Figure 10)	500ns typ	*	All digital inputs low to high and high to low
Feedthrough Error (See Figure 9)	10mV p-p max		V_{REF} = 20V p-p, 100kHz
		*	All digital inputs low
REFERENCE INPUT			
Input Resistance[4]	5kΩ min	*	
	10kΩ typ	*	
	20kΩ max	*	
ANALOG OUTPUT			
Output Capacitance (I_{OUT1}) (See Figure 8)	120pF typ	*	All digital inputs high
Output Capacitance (I_{OUT2}) (See Figure 8)	37pF typ	*	All digital inputs high
Output Capacitance (I_{OUT1}) (See Figure 8)	37pF typ	*	All digital inputs low
Output Capacitance (I_{OUT2}) (See Figure 8)	120pF typ	*	All digital inputs low
Output Noise (both outputs) (See Figure 7)	Equivalent to 10kΩ typ Johnson noise	*	
DIGITAL INPUTS[3]			
Low State Threshold	0.8V max	*	Over specified temperature range
High State Threshold	2.4V min	*	Over specified temperature range
Input Current (low to high state)	1μA typ	*	Over specified temperature range
Input Coding	Binary	*	See Tables 1 & 2 under Applications
POWER REQUIREMENTS			
Power Supply Voltage Range	+5V to +15V	*	
I_{DD}	5nA typ	*	All digital inputs at GND
	2mA max	*	All digital inputs high or low
Total Dissipation (Including ladder)	20mW typ	*	

NOTES:
[1] Full scale range (FSR) is 10V for unipolar mode and ±10V for bipolar mode.
[2] Using the internal $R_{FEEDBACK}$
[3] Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
[4] Ladder and feedback resistor tempco is approximately -150ppm/°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to GND) . . . . . +17V
V_{REF} (to GND) . . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Output Voltage (Pin 1, Pin 2) . . . . . -100mV to V_{DD}
Power Dissipation (package)
up to +75°C 450mW
derates above +75°C by . . . . . 6mW/°C
Operating Temperature
JN, KN, LN Versions . . . . . 0 to +70°C
JD, KD, LD Versions . . . . . -25°C to +85°C
SD, TD, UD Versions . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = +15V unless otherwise noted

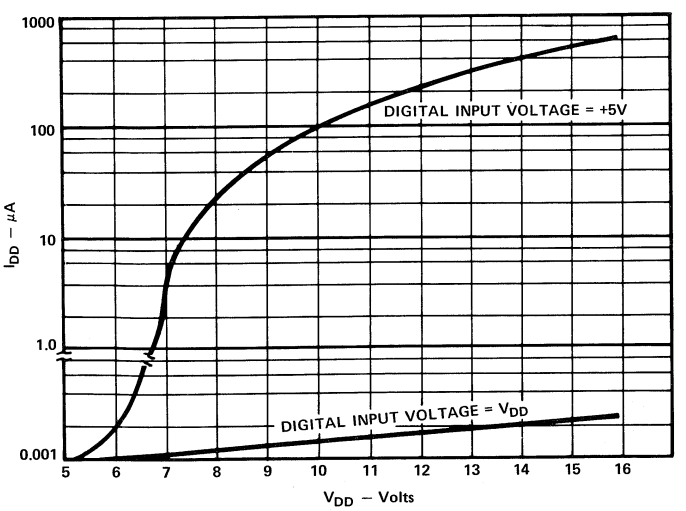


Figure 1. Supply Current vs. Supply Voltage

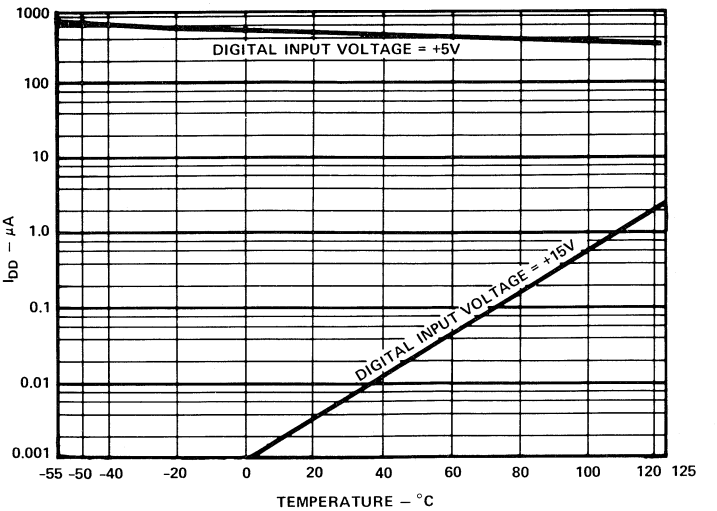


Figure 2. Supply Current vs. Temperature

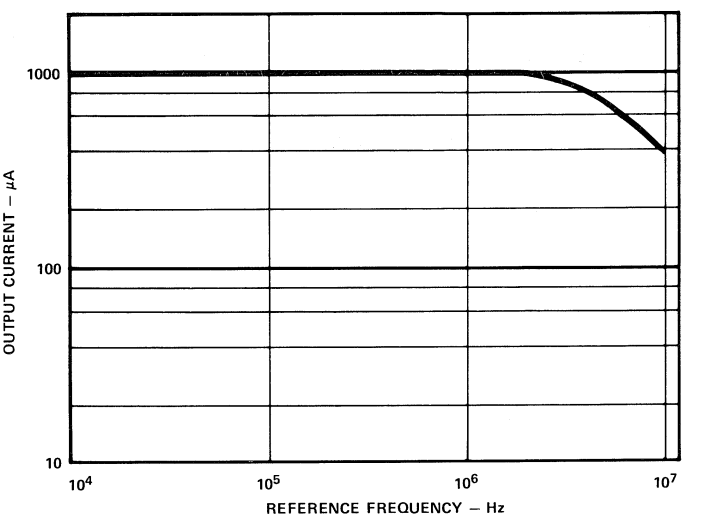


Figure 3. Output Current Bandwidth

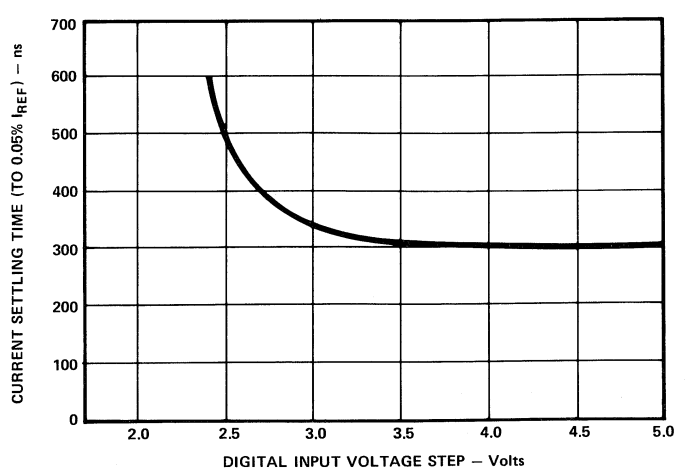


Figure 4. Output Current Settling Time vs. Digital Input Voltage

TEST CIRCUITS

Note: The following test circuits apply for the AD7520. Similar circuits can be used for the AD7521.

DC PARAMETERS

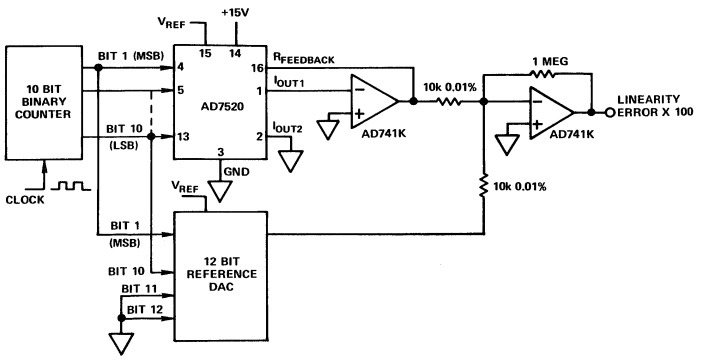


Figure 5. Nonlinearity

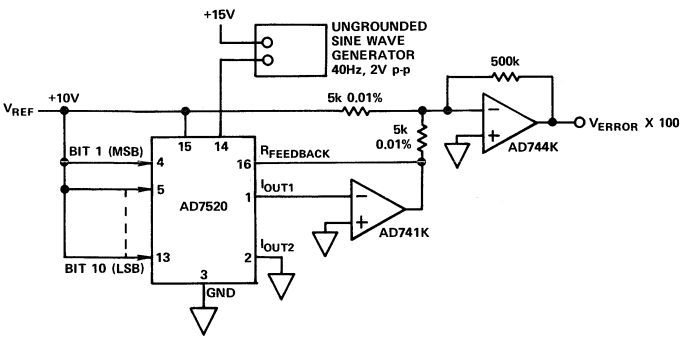


Figure 6. Power Supply Rejection

AC PARAMETERS

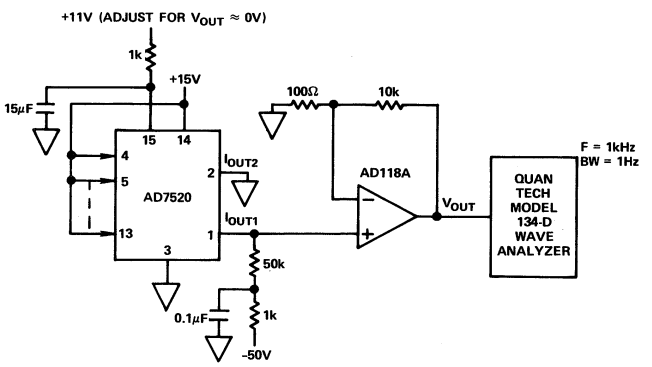


Figure 7. Noise

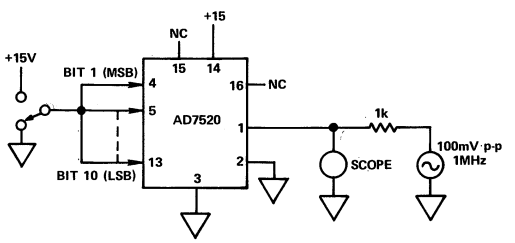


Figure 8. Output Capacitance

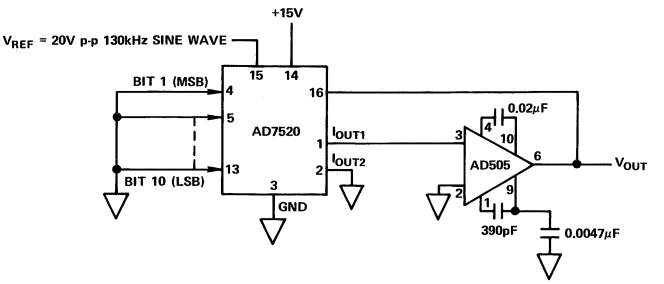


Figure 9. Feedthrough Error

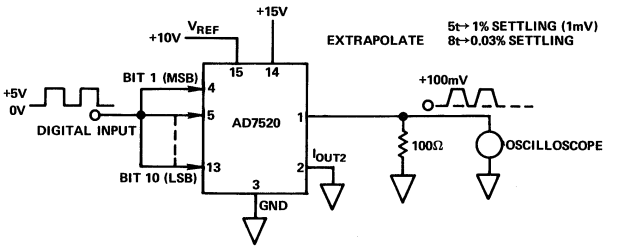


Figure 10. Output Current Settling Time

TERMINOLOGY

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

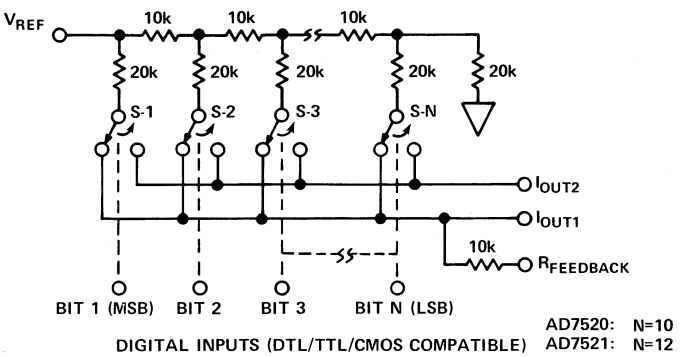
OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7520 (AD7521), a 10-bit (12-bit) multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten (twelve) CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 11. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.



(Switches shown for Inputs "High")

Figure 11. AD7520 (AD7521) Functional Diagram

One of the CMOS current switches is shown in Figure 12. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the first six switches are binarily scaled so the voltage drop across each switch is the same. For example, switch-1 of Figure 12 was designed for an "ON" resistance of 20 ohms, switch-2 of 40 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

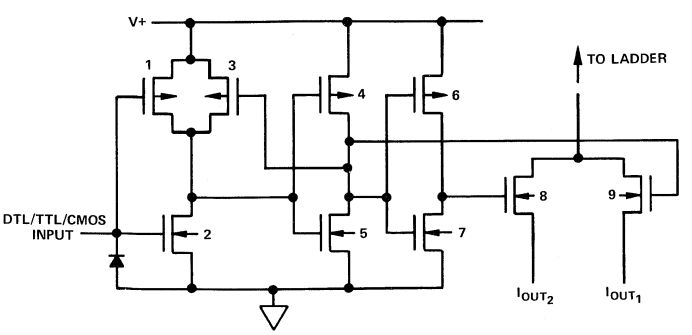


Figure 12. CMOS Switch

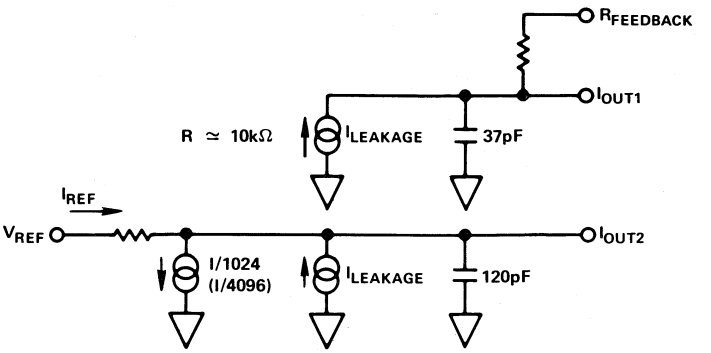


Figure 13. AD7520 (AD7521) Equivalent Circuit– All Digital Inputs Low

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 13 and 14. In Figure 13 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}\left(\frac{I}{4096}\right)$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 120pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 37pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 14 is similar to Figure 13; however, the "ON" switches are now on terminal I_{OUT1}, hence the 120pF at that terminal.

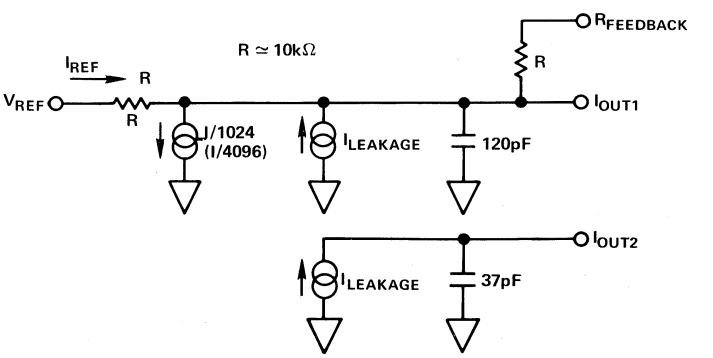


Figure 14. AD7520 (AD7521) Equivalent Circuit– All Digital Inputs High

APPLICATIONS

UNIPOLAR BINARY OPERATION

Figure 15 shows the circuit connections required for unipolar operation using the AD7520. Since V_{REF} can assume either positive or negative values, the circuit is also capable of 2-quadrant multiplication. The input code/output range table for unipolar binary operation is shown in Table 1.

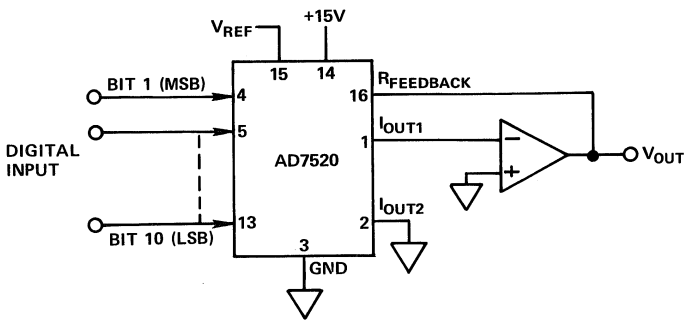


Figure 15. Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment

1. Tie all digital inputs to the AD7520 (AD7521) to GND potential.
2. Adjust the offset trimpot on the output operational amplifier for 0V ±1mV at V_{OUT}.

Gain Adjustment

1. Tie all digital inputs to the AD7520 (AD7521) to the +15V supply.
2. To increase V_{OUT}, place a resistor R in series with the amplifier output terminal and $R_{FEEDBACK}$ of the AD7520 (AD7521) (R = 0 to 500Ω)
3. To decrease V_{OUT}, place a resistor R in series with V_{REF}. (R = 0 to 500Ω)

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1 - 2^{-10})$
1000000001	$-V_{REF}\ (1/2 + 2^{-10})$
1000000000	$\frac{-V_{REF}}{2}$
0111111111	$-V_{REF}\ (1/2 - 2^{-10})$
0000000001	$-V_{REF}\ (2^{-10})$
0000000000	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table 1. Code Table — Unipolar Binary Operation

BIPOLAR (OFFSET BINARY) OPERATION

Figure 16 illustrates the AD7520 connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. Input coding is offset binary (modified 2's complement) as shown in Table 2.

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1 - 2^{-9})$
1000000001	$-V_{REF}\ (2^{-9})$
1000000000	0
0111111111	$V_{REF}\ (2^{-9})$
0000000001	$V_{REF}\ (1 - 2^{-9})$
0000000000	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

Table 2. Code Table — Bipolar (Offset Binary) Operation

When a switch's control input is a Logical "1", that switch's current is steered to I_{OUT1}, forcing the output of amplifier #1 to

$$V_{OUT} = -(I_{OUT1})(10k)$$

where 10k is the value of the feedback resistor.

A Logical "0" on the control input steers the switch's current to I_{OUT2}, which is terminated into the summing junction of amplifier #2. Resistors R1 and R2 need not track the internal R-2R circuitry; however, they should closely match each other to insure that the voltage at amplifer #2's output will force a current into R2 which is equal in magnitude but opposite in polarity to the current at I_{OUT2}. This creates a push-pull effect which halves the resolution but doubles the output range for changes in the digital input.

With the MSB a Logic "1" and all other bits a Logic "0", a 1/2 LSB difference current exists between I_{OUT1} and I_{OUT2}, creating an offset of 1/2 LSB. To shift the transfer curve to zero, resistor R-9 is used to sum 1/2 LSB of current into the I_{OUT2} terminal.

Offset Adjustment

1. Make V_{REF} approximately +10V.
2. Tie all digital inputs to +15V (Logic "1").
3. Adjust amplifier #2 offset trimpot for 0V ±1mV at amplifier #2 output.
4. Tie MSB (Bit 1) to +15V, all other bits to ground.
5. Adjust amplifier #1 offset trimpot for 0V ±1mV at V_{OUT}.

Gain Adjustment

Gain adjustment is the same as for unipolar operation.

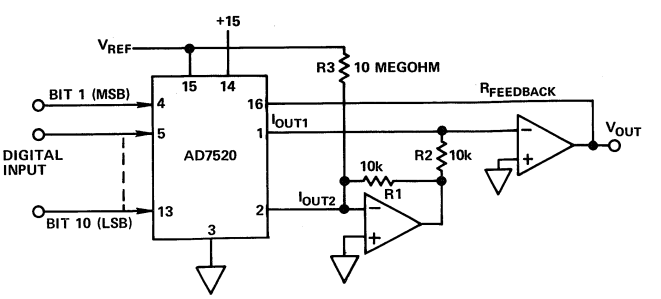


Figure 16. Bipolar Operation (4-Quadrant Multiplication)

DYNAMIC PERFORMANCE CHARACTERISTICS

The following circuits and associated waveforms illustrate the dynamic performance which can be expected using some commonly available IC amplifiers. All settling times are to 0.05% of 10V.

AD741J

Small Signal Bandwidth: 180kHz
Settling Time: 20μs

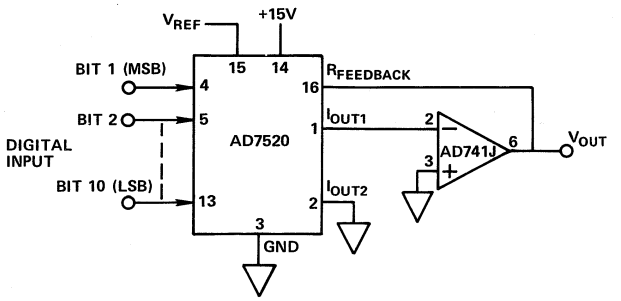


Figure 17. DAC Circuit Using AD741J

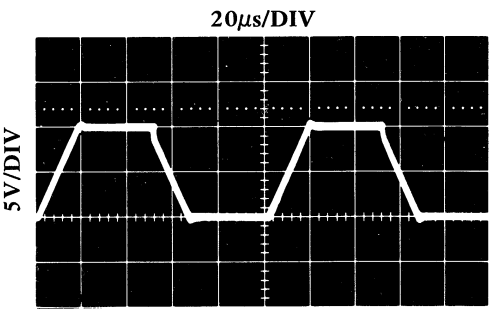


Figure 18. Output Waveform

AD518K

Small Signal Bandwidth: 1.0MHz
Settling Time: 6.0μs

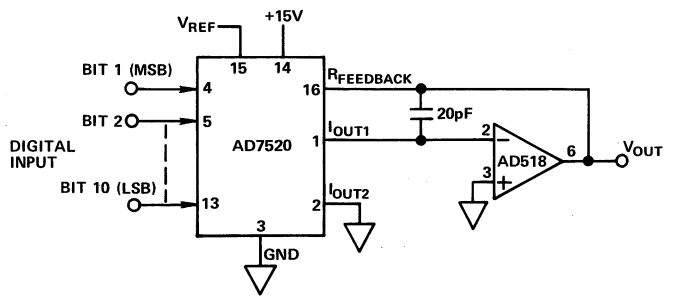


Figure 19. DAC Circuit Using AD518K

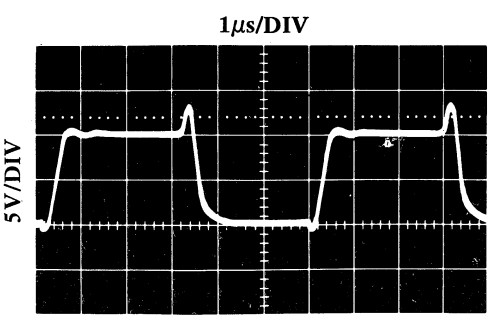


Figure 20. Output Waveform

AD505J

Small Signal Bandwidth: 1.0MHz
Settling Time: 2.5μs

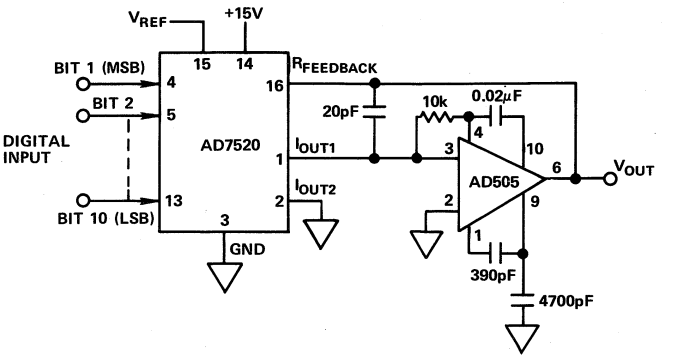


Figure 21. DAC Circuit Using AD505J

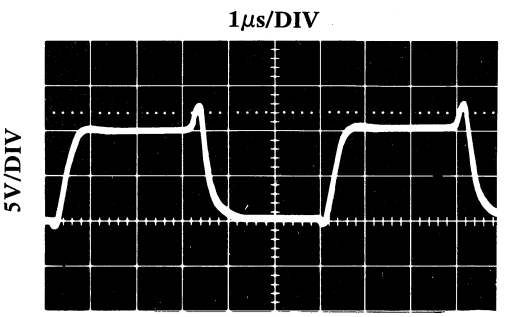


Figure 22. Output Waveform

AD509K

Small Signal Bandwidth: 1.6MHz
Settling Time: 2.0μs

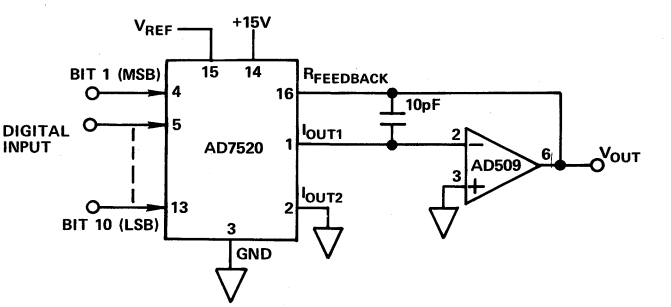


Figure 23. DAC Circuit Using AD509K

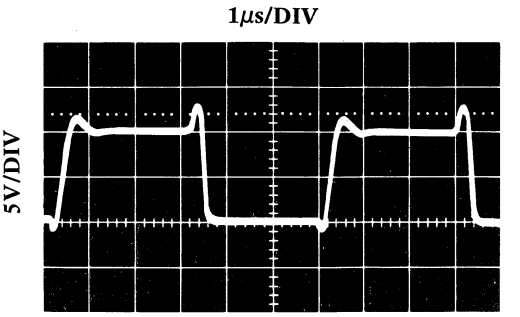


Figure 24. Output Waveform

ANALOG/DIGITAL DIVISION

With the AD7520 connected in its normal multiplying configuration as shown in Figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_X assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 25, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit 10) ON, the gain is 1024. With all bits ON, the gain is 1 (±1 LSB).

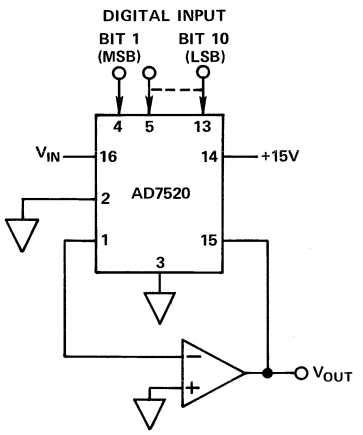
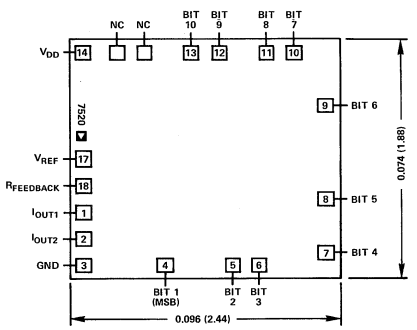


Figure 25. Analog/Digital Divider

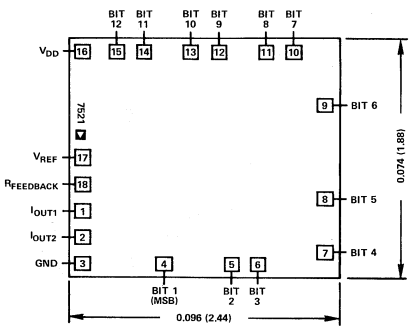
BONDING DIAGRAMS

Dimensions shown in inches and (mm).

AD7520



AD7521

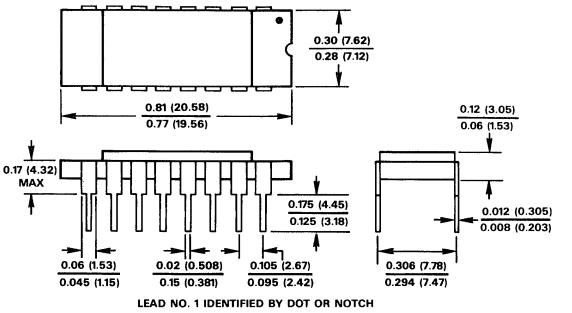


OUTLINE DIMENSIONS

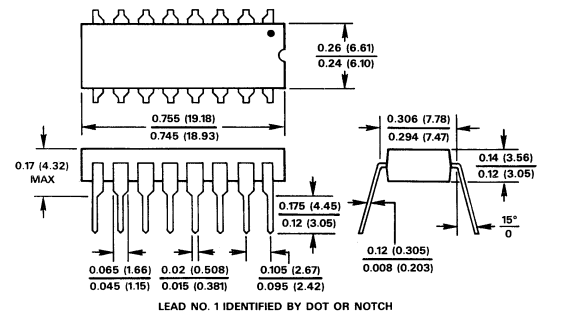
Dimensions shown in inches and (mm).

AD7520

16 PIN CERAMIC DIP

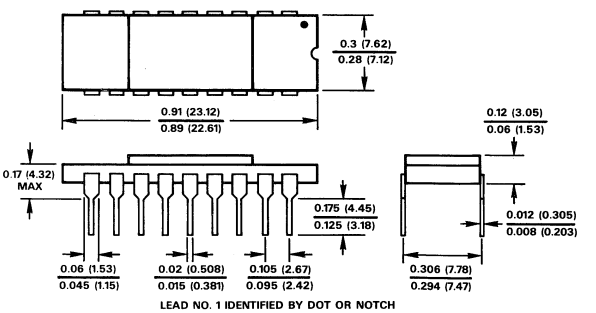


16 PIN PLASTIC DIP

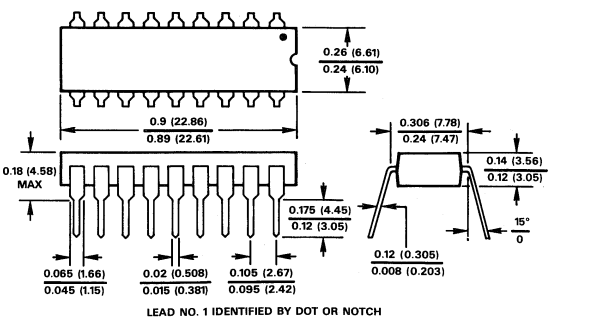


AD7521

18 PIN CERAMIC DIP



18 PIN PLASTIC DIP



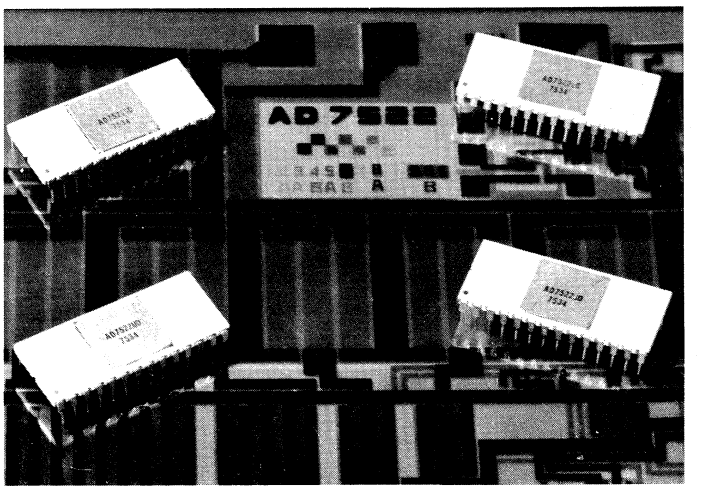
ANALOG DEVICES

CMOS 10-Bit, Buffered Multiplying D/A Converter

AD7522

FEATURES

- 10-Bit Resolution
- 8, 9, & 10-Bit Linearity
- Microprocessor Compatible
- Double Buffered Inputs
- Serial or Parallel Loading
- DTL/TTL/CMOS Direct Interface
- Nonlinearity Tempco: 2ppm of FSR/°C
- Gain Tempco: 10ppm of FSR/°C
- Very Low Power Dissipation
- Very Low Feedthrough



GENERAL DESCRIPTION

The AD7522 is a monolithic CMOS 10-bit multiplying D/A converter, with an input buffer and a holding register, allowing direct interface with microprocessors. Most applications require the addition of only an operational amplifier and a reference voltage.

The key to easy interface to a data bus is the AD7522's ability to load the input buffer in two bytes (an 8-bit and a 2-bit byte), and subsequently move this data to a holding register, where the digital word is converted into an analog current or voltage (with external operational amplifier). The input loading of either 8 or 10 bits can be done in a parallel or serial mode.

The AD7522 is packaged in a 28-pin DIP, and operates with a +15V main supply at 2mA max, and a logic supply of +5V for TTL interface, or +10 to +15V for CMOS interface.

A thin film on high density CMOS process, using silicon nitride passivation, ensures high reliability and excellent stability.

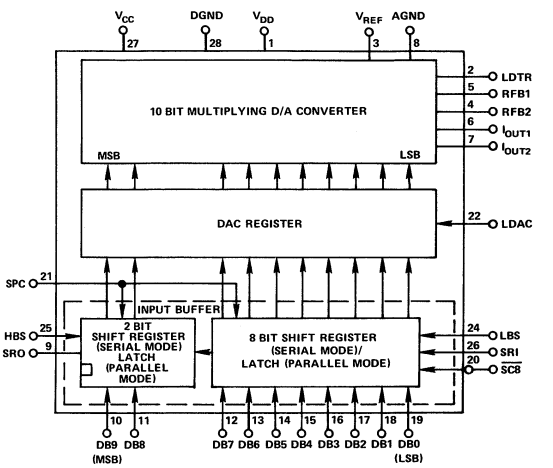
ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0 to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8-Bit)	AD7522JN	AD7522JD	AD7522SD
0.1% (9-Bit)	AD7522KN	AD7522KD	AD7522TD
0.05% (10-Bit)	AD7522LN	AD7522LD	AD7522UD

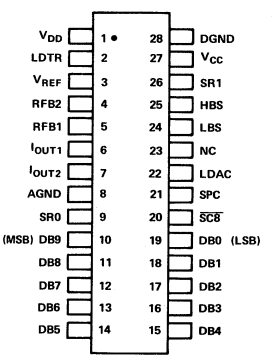
PACKAGE IDENTIFICATION

Suffix "D": Ceramic DIP Package
Suffix "N": Plastic DIP Package

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +15V, V_{CC} = +5V, V_{REF} = ±10V, TA = +25°C unless otherwise noted)

PARAMETER		TA = +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
STATIC ACCURACY				
Resolution	All	10 Bits min	10 Bits min	$\overline{SC8}$ = "1"
Nonlinearity	AD7522J	±0.2% FSR max		
	AD7522S	±0.2% FSR max	±0.2% FSR max	
	AD7522K	±0.1% FSR max		
	AD7522T	±0.1% FSR max	±0.1% FSR max	
	AD7522L	±0.05% FSR max		
	AD7522U	±0.05% FSR max	±0.05% FSR max	$-10V \leqslant V_{REF} \leqslant +10V$
Nonlinearity Tempco[1]	AD7522J,K,L	±1ppm FSR/°C typ	±2ppm FSR/°C max	
	AD7522S,T,U		±2ppm FSR/°C max	
Gain Error	AD7522J,K,L	±0.3% Reading typ		
Gain Error Tempco[1]	AD7522J,K,L	±5ppm of Reading/°C typ	±10ppm of Reading/°C max	
	AD7522S,T,U		±10ppm of Reading/°C max	
Output Leakage Current at I_{OUT1} or I_{OUT2}	All		200nA max	I_{OUT1}: DB0 through DB9 = 0 I_{OUT2}: DB0 through DB9 = 1
Power Supply Rejection	AD7522J,K,L	50ppm of Reading/% typ		
AC ACCURACY				
Feedthrough Error[1]	All	1mV p-p typ, 10mV p-p max		V_{REF}= 20V p-p; 10kHz
Output Current Settling Time	AD7522J,K,L	500ns typ		To 0.05% of FSR for a FSR Step. HBS and LBS Low to High LDAC = 1
REFERENCE INPUT				
Input Resistance	All	5kΩ min	20kΩ max	
ANALOG OUTPUT				
Output Capacitance				
C_{OUT1}	AD7522J,K,L	120pF typ		All Data Input High
C_{OUT2}	AD7522J,K,L	40pF typ		All Data Input High
C_{OUT1}	AD7522J,K,L	40pF typ		All Data Inputs Low
C_{OUT2}	AD7522J,K,L	120pF typ		All Data Inputs Low
DIGITAL INPUTS				
Low State Threshold	All	0.8V max	0.8V max	V_{CC} = +5V
	All	1.5V max	1.5V max	V_{CC} = +15V
High State Threshold	All	2.4V min	2.4V min	V_{CC} = +5V
	All	13.5V min	13.5V min	V_{CC} = +15V
Input Current	AD7522J,K,L	1μA typ		
LDAC Pulse Width[1]	All	500ns min	500ns min	LDAC: 0 to +3V
HBS, LBS Pulse Width[1]	All	500ns min	500ns min	HBS, LBS: 0 to +3V
Serial Clock Frequency[1]	All	1MHz max	1MHz max	
HBS, LBS Data Set Up[2]	All	250ns min	250ns min	
Data Hold Time[3]	All	500ns min, 200ns typ	500ns min	
POWER REQUIREMENTS				
I_{DD}	All	2mA max		In Quiescent State
I_{CC}	All	2mA max		In Quiescent State

Notes

[1] Guaranteed by design. Not tested.
[2] Data setup time is the minimum amount of time required for DB0 - DB9 to be stable prior to strobing HBS, LBS.
[3] Data hold time is the minimum amount of time required for DB0 - DB9 to be stable after strobing HBS, LBS.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{REF} to GND . . . . . ±25V
V_{DD} to GND . . . . . +17V
V_{CC} to GND . . . . . +17V
V_{CC} to V_{DD} . . . . . +0.4V
I_{OUT1}, I_{OUT2} . . . . . ±5mA
Operating Temperature
JN, KN, LN versions . . . . . 0 to +70°C
JD, KD, LD versions . . . . . -25°C to +85°C
SD, TD, UD versions . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Power Dissipation (Package)
Up to +50°C:
Plastic (Suffix N) 1200mW
Ceramic (Suffix D) 1000mW
Derate Above +50°C by
Plastic (Suffix N) . . . . . 12mW/°C
Ceramic (Suffix D) . . . . . 10mW/°C
Digital Input Voltage Range . . . . . V_{DD} to GND

CAUTION:

1. Do not apply voltages higher than V_{CC} to SRO.
2. Do not apply voltages higher than V_{DD} or less than GND to any other input/output terminal except V_{REF}, R_{FB1} or R_{FB2}.
3. The digital control inputs are zener protected, however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
4. V_{CC} should never exceed V_{DD} by more than 0.4V, especially during power ON or OFF sequencing.

TERMINOLOGY

RESOLUTION

Value of the LSB. For example, a unipolar n-bit converter has a resolution of (2^{-n}) (V_{REF}). A bipolar n-bit converter has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

NONLINEARITY

Error contributed by deviation of the DAC transfer function from a best straight line function. For a multiplying DAC, the nonlinearity should be independent of the sign or magnitude of V_{REF}. Nonlinearity is normally expressed as a percentage of full scale range (% FSR).

GAIN

The "gain" of a converter is that analog scale factor setting that establishes the nominal conversion relationship, e.g., 10V full scale. It is a linear error which can be externally adjusted (see gain adjustment on next page).

OUTPUT LEAKAGE CURRENT

Current which appears on the OUT1 terminal when the DAC register is loaded with all "0's" or on the OUT2 terminal when the DAC register is loaded with all "1's."

DAC CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7522's DAC functional block consists of a highly stable Silicon Chromium thin film R-2R ladder, and ten SPDT N-channel current steering switches. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

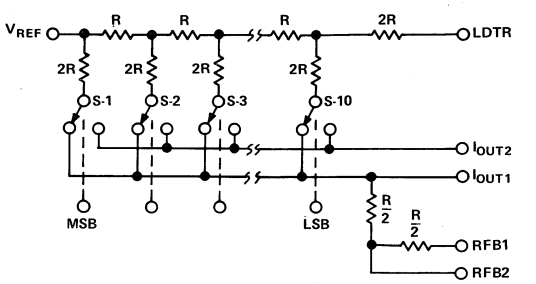


Figure 1. DAC Functional Diagram

EQUIVALENT CIRCUIT

The DAC equivalent circuit is shown in Figure 2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the $I_{REF}/1024$ current source represents the 1LSB of current lost through the ladder termination resistor to ground. The C_{OUT1} and C_{OUT2} output capacitances are as shown when the DAC latches feed the DAC with all "1's." If the DAC latches are loaded with all "0's," C_{OUT1} is 37pF, while C_{OUT2} is 120pF. In addition, C_{SD} is shunted by 10 ohms, and the 10 ohm R_{ON} in I_{OUT1} is replaced by a C_{SD} of 10pF. When fast amplifiers are used, it will be necessary to provide phase compensation (in the form of feedback capacitance) to cancel the pole formed by $R_{FEEDBACK}$ and C_{OUT} if stability is to be maintained.

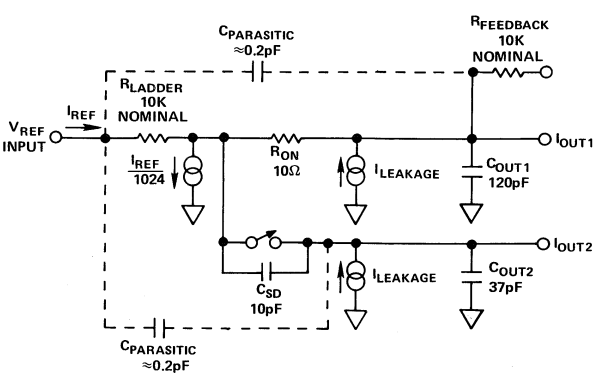


Figure 2. Equivalent Circuit (Shown for all Digital Inputs High)

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	V_{DD}	+15V (nominal) Main Supply.
2	LDTR	R-2R Ladder Termination Resistor. Normally grounded for unipolar operation or terminated at I_{OUT2} for bipolar operation.
3	V_{REF}	Reference Voltage Input. Since the AD7522 is a multiplying DAC, V_{REF} may vary over the range of ±10V.
4	RFB2	$R_{FEEDBACK} \div 2$; gives full scale equal to $V_{REF}/2$.
5	RFB1	$R_{FEEDBACK}$, used for normal unity gain (at full scale) D/A conversion.
6	I_{OUT1}	DAC Current OUT1 Bus. Normally terminated at virtual ground of output amplifier.
7	I_{OUT2}	DAC Current OUT2 Bus, terminated at ground for unipolar operation, or virtual ground of op amp for bipolar operation.
8	AGND	Analog Ground. Back gate of DAC N-channel SPDT current steering switches.
9	SRO	Serial Output. An auxiliary output for recovering data in the input buffer.
10	DB9	Data Bit 9. Most significant parallel data input.
11	DB8	Data Bit 8.
12	DB7	Data Bit 7.
13	DB6	Data Bit 6.
14	DB5	Data Bit 5.
15	DB4	Data Bit 4.
16	DB3	Data Bit 3.
17	DB2	Data Bit 2.
18	DB1	Data Bit 1.
19	DB0	Data Bit 0. Least significant parallel data input.
20	$\overline{SC8}$	8-Bit Short Cycle Control. When in serial mode, if $\overline{SC8}$ is held to Logic "0", the two least significant input latches in the input buffer are bypassed to provide proper serial loading of 8-bit serial words. If $\overline{SC8}$ is held to Logic "1", the AD7522 will accept a 10-bit serial word. Data bits 0 (LSB) and DB1 are in a parallel load mode when $\overline{SC8}$ = 0 and should be tied to a logic low state to prevent false data from being loaded.
21	SPC	Serial/Parallel Control. If SPC is a Logic "0", the AD7522 will load parallel data appearing on DB0 through DB9 into the input buffer when the appropriate strobe inputs are exercised (see HBS and LBS). If SPC is a Logic "1", the AD7522 will load serial data appearing on Pin 26 into the input buffers. Each serial data bit must be "strobed" into the buffer with the HBS and LBS.
22	LDAC	Load DAC: When LDAC is a Logic "0", the AD7522 is in the "hold" mode, and digital activity in the input buffer is locked out. When LDAC is a Logic "1", the AD7522 is in the "load" mode, and data in the input buffer loads the DAC register.
23	NC	No Connection.
24	LBS	Low Byte Strobe. When in "parallel load" mode (SPC = 0), parallel data appearing on the DB0 (LSB) through DB7 inputs will be "clocked" into the input buffer on the positive going edge of the LBS. When in "serial load" mode (SPC = 1), serial data bits appearing at the serial input terminal, Pin 26, will be "clocked" into the input buffer on the positive going edge of HBS and LBS. (HBS and LBS must be clocked simultaneously when in "serial load" mode.)
25	HBS	High Byte Strobe. When in "parallel load" mode (SPC = 0), parallel data appearing on the DB9 (MSB) and DB8 data inputs will be "clocked" into the input buffer on the positive going edge of HBS. When in "serial load" mode (SPC = 1), serial data bits appearing at the serial input terminal, Pin 26, will be "clocked" into the input buffer on the positive going edges of HBS and LBS. (HBS and LBS must be clocked simultaneously when in "serial load" mode.)
26	SRI	Serial Input.
27	V_{CC}	Logic Supply. If +5V is applied, all digital inputs/outputs are TTL compatible. If +10V to +15V is applied, digital inputs/outputs are CMOS compatible.
28	DGND	Digital Ground

Note 1: Logic "1" applied to a data bit steers that bit's current to the $I_{OUT}1$ terminal.

APPLICATIONS

UNIPOLAR OPERATION

Figure 3 shows the analog circuit connections required for unipolar operation. The input code/output voltage relationship is shown in Table 1.

Zero Offset Adjustment

1. Adjust the op amp's offset potentiometer for <1mV on the amplifier junction. (Each millivolt of amplifier V_{OS} causes ±0.66mV of differential nonlinearity which adds to the ladder nonlinearity.)

Gain Adjustment

1. Set R1 and R2 to 0Ω. Load the DAC register with all "1's."
2. If analog out is greater than $-V_{REF}$, increase R1 for required full scale output. If analog out is less than $-V_{REF}$, increase R2 for required full scale output.

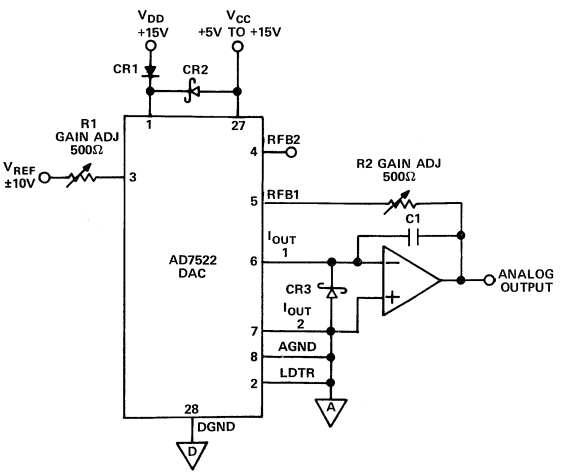


Figure 3. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1 - 2^{-10})$
1000000001	$-V_{REF}\ (1/2 + 2^{-10})$
1000000000	$-V_{REF}/2$
0111111111	$-V_{REF}\ (1/2 - 2^{-10})$
0000000001	$-V_{REF}\ (2^{-10})$
0000000000	0

Table 1. Unipolar Code Table

BIPOLAR OPERATION

Figure 4 shows the analog circuit connections required for bipolar operation. The input code/output voltage relationship is shown in Table 2.

Zero Offset Adjustment

1. Adjust the offset potentiometer of amplifier A1 and A2 for <1mV on the respective summing junctions. If the analog out for code 1000000000 is not zero, sum current into or out of the summing junction of A1 for 0V at analog out.

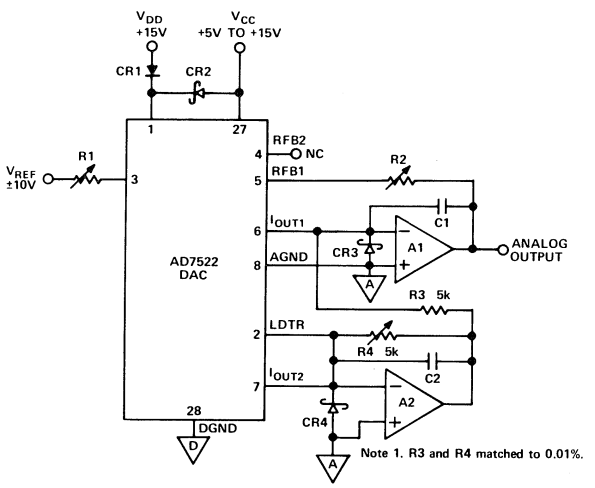


Figure 4. Bipolar Operation

Gain Adjustment

1. Load the DAC register with all "0's." Set R1 and R2 to 0Ω.
2. If analog out is greater than $+V_{REF}$, increase R2 until it reads precisely $+V_{REF}$. If analog out is less than $+V_{REF}$, increase R1 until it reads precisely V_{REF}.

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1 - 2^{-9})$
1000000001	$-V_{REF}\ (2^{-9})$
1000000000	0
0111111111	$V_{REF}\ (2^{-9})$
0000000001	$V_{REF}\ (1 - 2^{-9})$
0000000000	V_{REF}

Table 2. Bipolar Code Table

SINGLE BYTE PARALLEL LOADING

Figure 5 illustrates the logic connections for loading single byte parallel data into the input buffer. DB0 should be grounded on "K" and "T" versions, and DB0 and DB1 should be grounded on "J" and "S" versions for monotonic operation of the DAC. DB9 is always the MSB, whether 8-bit, 9-bit, or 10-bit linear AD7522's are used.

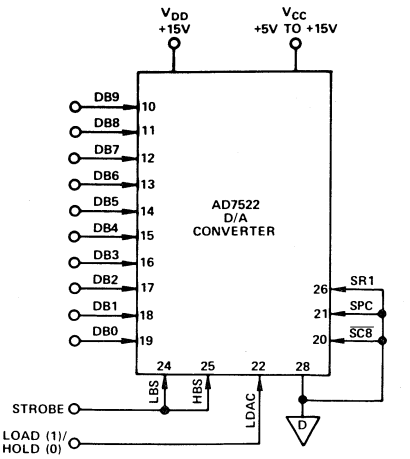


Figure 5. Single Byte Parallel Loading

When data is stable on the parallel inputs (DB0-DB9), it can be transferred into the input buffer on the positive edge of the strobe pulse.

Data is transferred from the input buffer to the DAC register when LDAC is a Logic "1." LDAC is a level-actuated (versus edge-triggered) function and must be held "high" at least 0.5μs for data transfer to occur.

TWO BYTE PARALLEL LOADING

Figures 6 and 7 show the logic connections and timing requirements for interfacing the AD7522 to an 8-bit data bus for two byte loading of a 10-bit word.

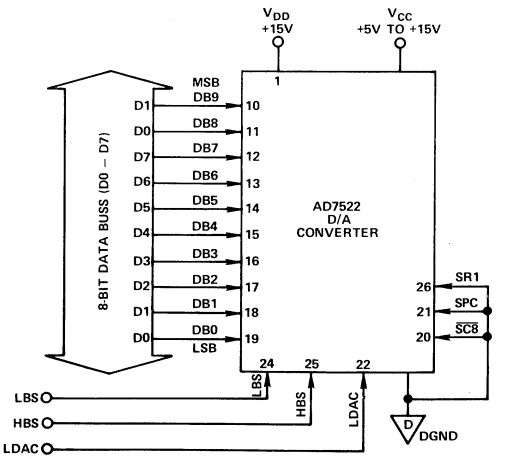


Figure 6. Two Byte Parallel Loading

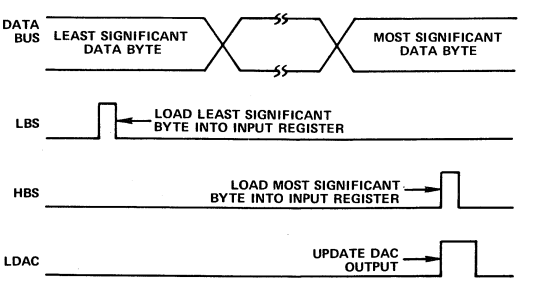


Figure 7. Timing Diagram

First, the least significant data byte (DB0 through DB7) is loaded into the input buffer on the positive edge of LBS. Subsequently, the data bus is used for status indication and

instruction fetching by the CPU. When the most significant data byte (DB8 and DB9) is available on the bus, the input buffer is loaded on the positive edge of HBS. The DAC register updates to the new 10-bit word when LDAC is "high." LDAC may be exercised coincident with, or at any time after HBS loads the second byte of data into the input buffer.

SERIAL LOADING

Figure 8 and Figure 9 show the connections and timing diagram for serial loading.

To load a 10-bit word ($\overline{SC8}$ = 1), HBS and LBS must be strobed simultaneously with exactly 10 positive edges to clock the serial data into the input buffer. For 8-bit words ($\overline{SC8}$ = 0), only 8 positive edges are required.

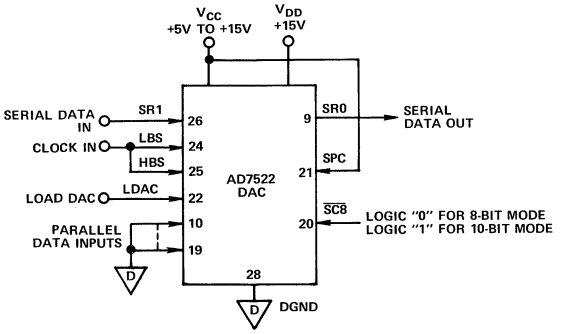


Figure 8. Serial 8- and 10-Bit Loading (Analog Outputs Not Shown for Clarity)

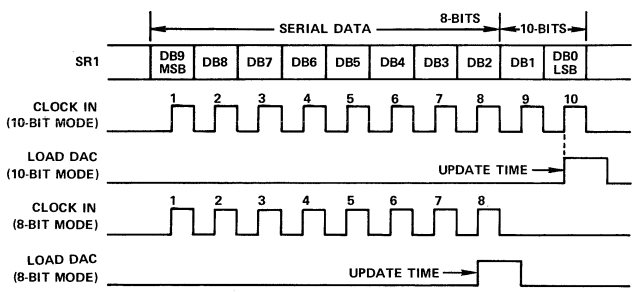


Figure 9. Timing Diagram for Serial 8- and 10-Bit Loading

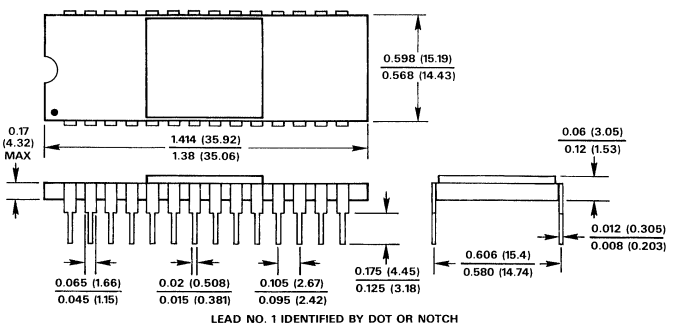
APPLICATION HINTS

1. CR1 and CR2 on Figures 3 and 4 protect the AD7522 against latch-up V_{CC} exceeds V_{DD}, and may be omitted if V_{DD} and V_{CC} are driven from the same voltage.
2. Diodes CR3 on Figure 3 and CR3 and CR4 on Figure 4 clamp the amplifier junction to -300mV if they attempt to swing negative during power up or power down. The input structures of some high-speed op amps can supply substantial current under the transient conditions encountered during power sequencing. It is recommended that the PC layout be able to accommodate the diodes.
3. Fast op amps will require phase compensation for stability due to the pole formed by C_{OUT1} or C_{OUT2} and $R_{FEEDBACK}$.
4. During serial loading, all data inputs (DB0 through BD9), should be grounded.

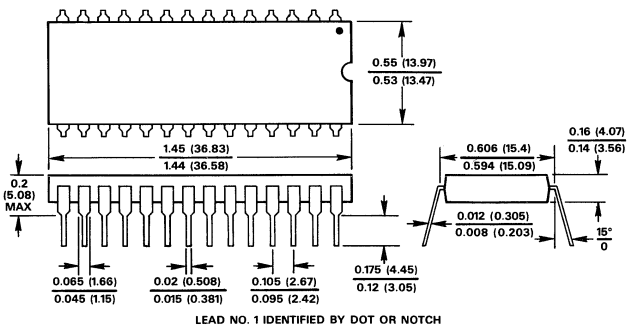
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

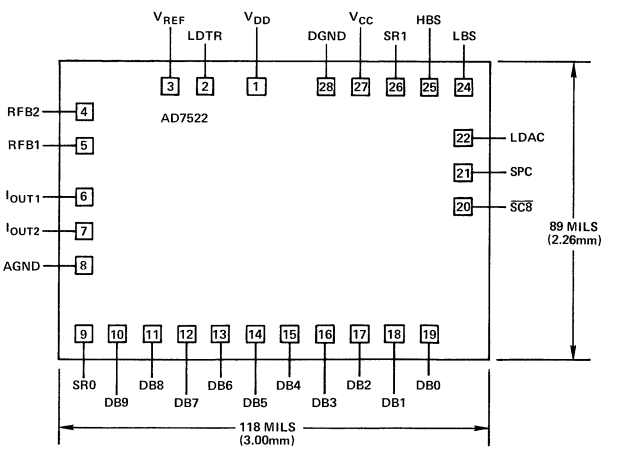
28 PIN CERAMIC DIP



28 PIN PLASTIC DIP



BONDING DIAGRAM



ANALOG DEVICES

CMOS 8-Bit Multiplying D/A Converter

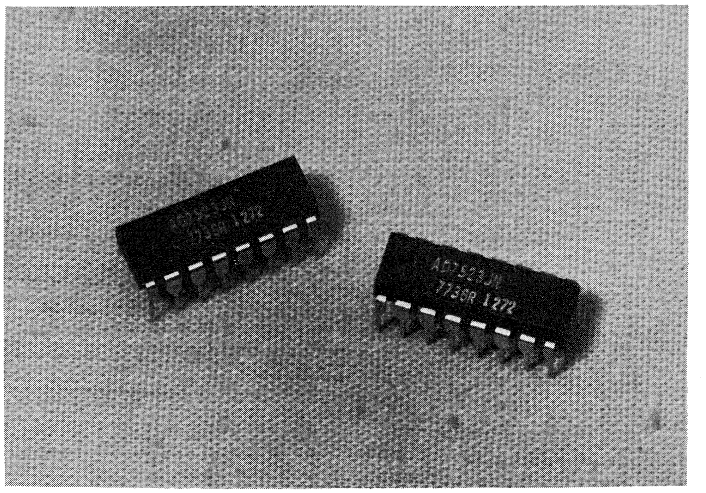
AD7523

FEATURES

- Low Cost
- Fast Settling: 100ns
- Low Power Dissipation
- Low Feedthrough: ½LSB @ 200kHz
- Full Four-Quadrant Multiplying

APPLICATIONS

- Battery Operated Equipment
- Low Power, Ratiometric A/D Converters
- Digitally Controlled Gain Circuits
- Digitally Controlled Attenuators
- CRT Character Generation
- Low Noise Audio Gain Control

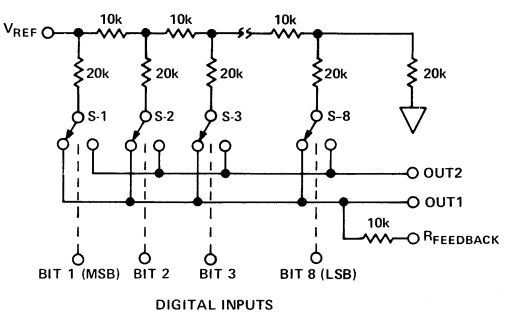


GENERAL DESCRIPTION

The AD7523 is a low cost, monolithic multiplying digital-to-analog converter packaged in a 16-pin DIP. The device uses an advanced monolithic, thin-film-on-CMOS technology to provide 8-bit resolution with accuracy to 10-bits and very low power dissipation.

The AD7523's excellent multiplying characteristics and low cost allow it to be used in a wide ranging field of applications such as: low noise audio gain control, CRT character generation, motor speed control, digitally controlled attenuators, etc.

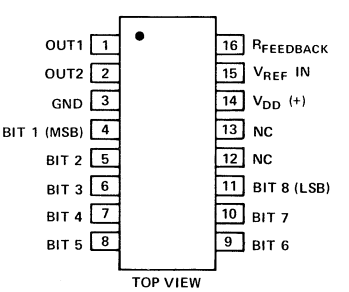
FUNCTIONAL DIAGRAM



ORDERING INFORMATION

Model	Linearity	Package	Operating Temperature Range
AD7523JN	±1/2LSB	16 pin Plastic	0 to +70°C
AD7523KN	±1/4LSB		
AD7523LN	±1/8LSB		

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +15V, V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = +25°C	T_A = 0 to +70°C	TEST CONDITION
STATIC ACCURACY			
Resolution	8 Bits min	8 Bits min	
Nonlinearity[1]			
AD7523JN	±1/2LSB max (±0.2% FSR max)	±1/2LSB max (±0.2% FSR max)	V_{OUT1} = V_{OUT2} = 0V
AD7523KN	±1/4LSB max (±0.1% FSR max)	±1/4LSB max (±0.1% FSR max)	
AD7523LN	±1/8LSB max (±0.05% FSR max)	±1/8LSB max (±0.05% FSR max)	
Monotonicity	Guaranteed over 0 to +70°C		V_{OUT1} = V_{OUT2} = 0V
Gain Error[1,2]	-1.5% of FSR min, +1.5% of FSR max	-1.8% of FSR min, +1.8% of FSR max	Digital Inputs = V_{INH}
Power Supply Rejection (Gain)[1,2]	0.02% per % max	0.03% per % max	V_{DD} = +14V to +15V Digital Inputs = V_{INH}
Output Leakage Current			
I_{OUT1} (pin 1)	±50nA max	±200nA max	V_{OUT1} = V_{OUT2} = 0V, V_{REF} = ±10V Digital Inputs = V_{INL}
I_{OUT2} (pin 2)	±50nA max	±200nA max	V_{OUT1} = V_{OUT2} = 0V, V_{REF} = ±10V Digital Inputs = V_{INH}
DYNAMIC PERFORMANCE			
Output Current			
Settling Time[3]	150ns max	200ns max	To 0.2% FSR, Load = 100Ω Digital Inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error[3]	±1/2LSB max	±1LSB max	Digital Inputs = V_{INL} V_{REF} = 20V p-p, 200kHz sinewave
REFERENCE INPUT			
Input Resistance (pin 15)	5kΩ min, 20kΩ max		V_{OUT1} = V_{OUT2} = 0V
Temperature Coefficient		-500ppm/°C max	
ANALOG OUTPUTS[3]			
Output Capacitance			
C_{OUT1} (pin 1)	100pF max	100pF max	Digital Inputs = V_{INH}
C_{OUT2} (pin 2)	30pF max	30pF max	
C_{OUT1} (pin 1)	30pF max	30pF max	Digital Inputs = V_{INL}
C_{OUT2} (pin 2)	100pF max	100pF max	
DIGITAL INPUTS			
Logic Thresholds			
V_{INH}	+14.5V min	+14.5V min	
V_{INL}	+0.5V max	+0.5V max	
Input Leakage Current			
I_{IN} (per input)	±1μA max	±1μA max	V_{IN} = 0V or +15V
Input Capacitance			
C_{IN}[3]	4pF max	4pF max	
Input Coding	Unipolar Binary or Offset Binary (see next page)		
POWER REQUIREMENTS			
V_{DD} Range	+5V min, +16V max	+5V min, +16V max	Device Functionality. Accuracy is tested and guaranteed only at V_{DD} = +15V
I_{DD}	100μA max	100μA max	Digital Inputs = V_{INH} or V_{INL}

NOTES:
[1] FSR is Full Scale Range.
[2] Using internal feedback resistor, Full Scale Range (FSR) is equal to (V_{REF} -1LSB) in the unipolar circuit on next page.
[3] Guaranteed by design. Not subject to test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . -0V, +17V
V_{REF} to GND. . . . . ±25V
Digital Input Voltage (V_{IN}) to GND . . . . . -0.3V to V_{DD}
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND. . . . . -0.3V to V_{DD}

Power Dissipation (package)
To +70°C 670mW
Derate Above +70°C by . . . . . .8.3mW/°C
Operating Temperature. . . . . 0 to +70°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not apply voltages lower than ground or higher the V_{DD} to any pin except V_{REF} (pin 15) and R_{FB} (pin 16).
3. The inputs of some IC amplifiers (especially wide bandwidth types) present a low impedance to V^- during power-up or power-down sequencing. To prevent the AD7523 OUT1 or OUT2 terminals from exceeding -300mV (which causes catastrophic substrate current) a Schottky diode (HP5082-2811 or equivalent) is recommended. The diode should be connected between OUT1 (OUT2) and ground as shown in Figures 1 and 2.

BASIC OPERATION

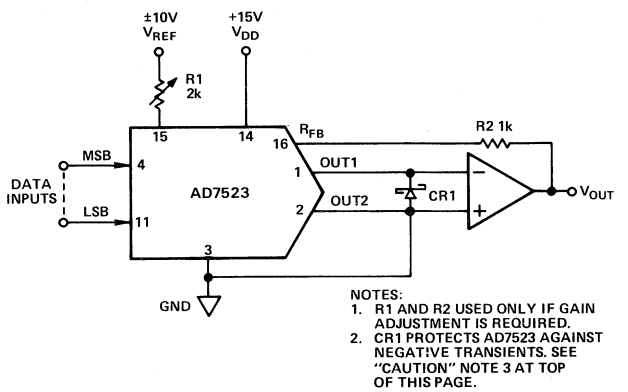


Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB	LSB	ANALOG OUTPUT
11111111		$-V_{REF}\left(\frac{255}{256}\right)$
10000001		$-V_{REF}\left(\frac{129}{256}\right)$
10000000		$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111		$-V_{REF}\left(\frac{127}{256}\right)$
00000001		$-V_{REF}\left(\frac{1}{256}\right)$
00000000		$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: $1LSB = (2^{-8})(V_{REF}) = \frac{1}{256}\ (V_{REF})$

Table 1. Unipolar Binary Code Table

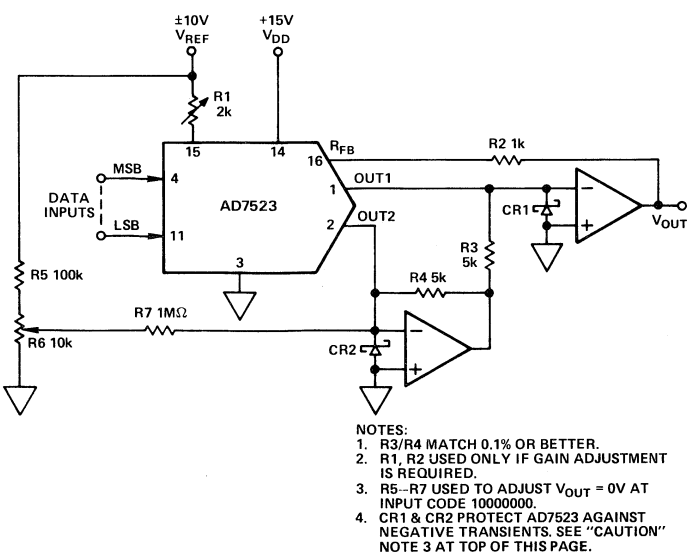


Figure 2. Bipolar (4-Quadrant) Operation

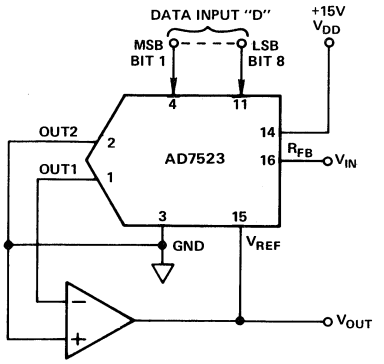
DIGITAL INPUT MSB	LSB	ANALOG OUTPUT
11111111		$-V_{REF}\left(\frac{127}{128}\right)$
10000001		$-V_{REF}\left(\frac{1}{128}\right)$
10000000		0
01111111		$+V_{REF}\left(\frac{1}{128}\right)$
00000001		$+V_{REF}\left(\frac{127}{128}\right)$
00000000		$+V_{REF}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{REF}) = \left(\frac{1}{128}\right)\ (V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table

APPLICATIONS

DIVIDER (DIGITALLY CONTROLLED GAIN)



EQUATIONS

$$V_{OUT} = -\frac{V_{IN}}{D}$$

$$A_V = \frac{V_{OUT}}{V_{IN}} = -\frac{1}{D}$$ where: A_V = Voltage Gain

and where:

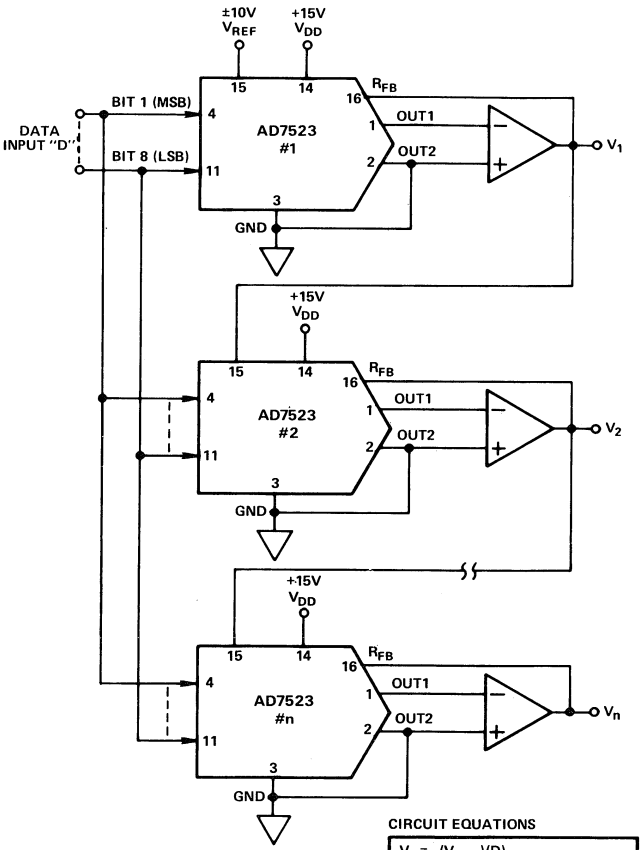
$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \frac{BIT\ 8}{2^8}$$

(BIT N = 1 or 0)

EXAMPLES

D = 00000000, $A_V = -A_{OL}$ (OP AMP)
D = 00000001, $A_V = -256$
D = 10000000, $A_V = -\frac{256}{128} = -2$
D = 11111111, $A_V = -\frac{256}{255}$

POWER GENERATION



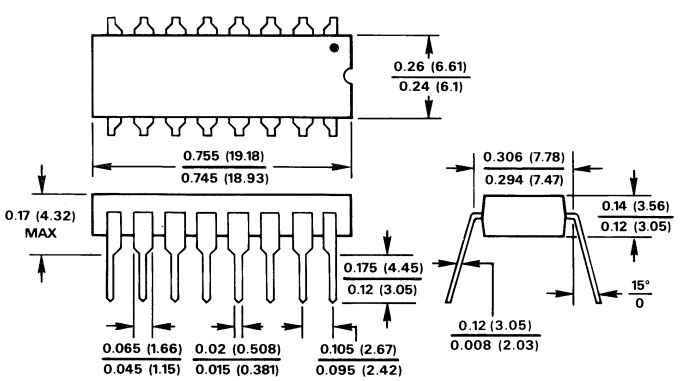
CIRCUIT EQUATIONS

$V_1 = -(V_{REF})(D)$
$V_2 = +(V_{REF})(D^2)$
$V_n = -(V_{REF})(D^n)$, n an odd integer
$V_n = +(V_{REF})(D^n)$, n an even integer

OUTLINE DIMENSIONS

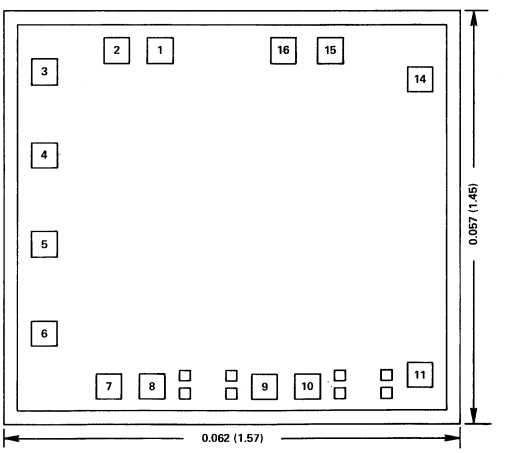
Dimensions shown in inches and (mm).

16 PIN PLASTIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH

BONDING DIAGRAM

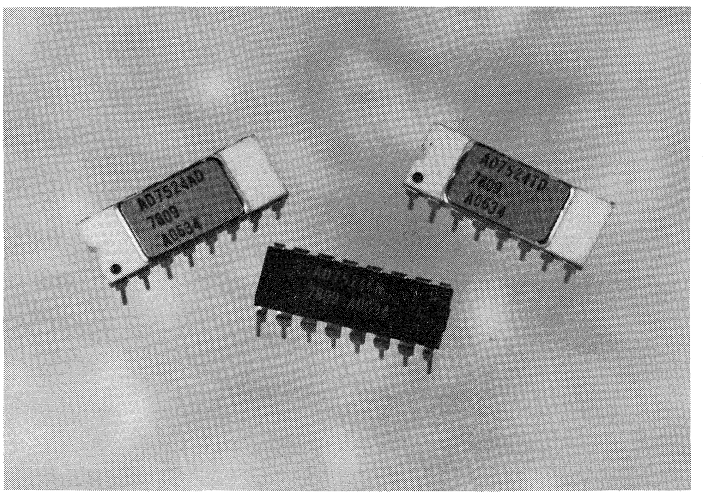


NOTES:
1. Pad numbers correspond to pin numbers shown on pin configuration, page 1.
2. Dimensions in inches (mm).
3. Pad 3, GND, should be bonded 1st.
4. Pads are 0.004" x 0.004" (0.102 x 0.102mm).

CMOS 8-Bit Buffered Multiplying DAC

AD7524

PRELIMINARY TECHNICAL DATA



FEATURES

- Low Cost
- On-Chip Bus Interface Logic
- Full Four-Quadrant Multiplication
- +5V to +15V Operation
- Low Power Consumption
- Monotonicity Guaranteed (Full Temperature Range)

APPLICATIONS

- Microprocessor Controlled Gain Circuits
- Microprocessor Controlled Attenuator Circuits
- Microprocessor Controlled Function Generation
- Precision AGC Circuits

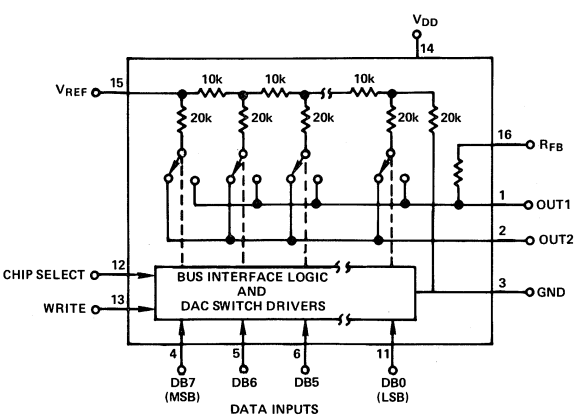
GENERAL DESCRIPTION

The AD7524 is a low cost, 8-bit monolithic CMOS DAC designed for direct interface to most microprocessors.

Basically an 8-bit DAC with input latches, the AD7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the AD7524 provides accuracy to 1/8 LSB with power dissipation of only 20 millivolts.

Featuring operation from +5V to +15V, the AD7524 interfaces directly to most microprocessor buses or output ports. Excellent multiplying characteristics (2 or 4-quadrant) make the AD7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

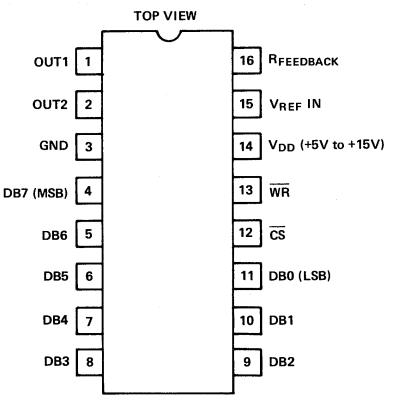
FUNCTIONAL DIAGRAM



ORDERING INFORMATION

	Temperature Range and Package		
Nonlinearity @ +15V	Plastic 0 to +70°C	Ceramic -25°C to +85°C	Ceramic -55°C to +125°C
±1/2 LSB	AD7524JN	AD7524AD	AD7524SD
±1/4 LSB	AD7524KN	AD7524BD	AD7524TD
±1/8 LSB	AD7524LN	AD7524CD	AD7524UD

PIN CONFIGURATION



SPECIFICATIONS (V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise noted)

PARAMETER	LIMIT, T_A = +25°C		LIMIT, T_A = OPERATING RANGE		UNITS	TEST CONDITION
	V_{DD} = +5V	V_{DD} = +15V	V_{DD} = +5V	V_{DD} = +15V		
STATIC ACCURACY						
Resolution	8	8	8	8	Bits min	
Nonlinearity						
AD7524JN, AD, SD	±1/2	±1/2	±1/2	±1/2	LSB max	
AD7524KN, BD, TD	±1/2	±1/4	±1/2	±1/4	LSB max	
AD7524LN, CD, TD	±1/2	±1/8	±1/2	±1/8	LSB max	
Monotonicity	guaranteed	guaranteed	guaranteed	guaranteed	—	
Gain Error[1]	±1.0	±0.5	±1.4	±0.6	% FSR max	
dc Supply Rejection, Gain[2]						
$\Delta Gain/\Delta V_{DD}$	0.08	0.02	0.16	0.04	% per % max	ΔV_{DD} = ±10%
Output Leakage Current						
I_{OUT1} (pin 1)	±50	±50	±400	±200	nA max	DB0 – DB7 = V_{IH}; $\overline{WR}$, $\overline{CS}$ = V_{IL}; V_{REF} = ±10V
I_{OUT2} (pin 2)	±50	±50	±400	±200	nA max	DB0 – DB7 = V_{IL}; $\overline{WR}$, $\overline{CS}$ = V_{IL}; V_{REF} = ±10V
DYNAMIC ACCURACY						
Output Current Settling Time (To 1/2 LSB)	150[3]	100[3]	200[2]	150[2]	ns max	OUT1 Load = 100Ω; $\overline{WR}$, $\overline{CS}$ = V_{IL} DB0 – DB7 = V_{IH} to V_{IL} or V_{IL} to V_{IH}
ac Feedthrough Current[2]						
@ OUT1 (pin 1)	±1/2	±1/2	±1	±1	LSB max	V_{REF} = 100kHz, 20V p-p sinewave
@ OUT2 (pin 2)	±1/2	±1/2	±1	±1	LSB max	DB0 – DB7 = V_{IL}; $\overline{CS}$, $\overline{WR}$ = V_{IL}
REFERENCE INPUT						
R_{in} (pin 15 to GND)[4]	5	5	5	5	kΩ min	
	20	20	20	20	kΩ max	
ANALOG OUTPUTS						
Output Capacitance[2]						
C_{OUT1} (pin 1)	90	90	90	90	pF max	DB0 – DB7 = V_{IH}; $\overline{WR}$, $\overline{CS}$ = V_{IL}
C_{OUT2} (pin 2)	30	30	30	30	pF max	
C_{OUT1} (pin 1)	30	30	30	30	pF max	DB0 – DB7 = V_{IL}; $\overline{WR}$, $\overline{CS}$ = V_{IL}
C_{OUT2} (pin 2)	90	90	90	90	pF max	
DIGITAL INPUTS (dc parameters)						
Logic Threshholds						
Input HIGH Voltage Requirement V_{IH}	+3.0	+13.5	+3.0	+13.5	V min	
Input LOW Voltage Requirement V_{IL}	+0.8	+1.5	+0.8	+1.5	V max	
Input Current (per input) I_{IN}	±1	±1	±10	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance[2] (per input) C_{IN}	20	20	20	20	pF max	
SWITCHING CHARACTERISTICS						
Chip Select to Write Setup Time t_{CS}[3]	280	250			ns min	
Chip Select to Write Hold Time t_{CH}[3]	60	50			ns min	
Write Pulse Width t_{WP}[3]	220	200			ns min	
Data Setup Time t_{DS}[3]	160	140			ns min	
Data Hold Time t_{DS}[3]	100	80			ns min	
POWER SUPPLY						
I_{DD}	25	25	25	25	μA	All Digital Inputs = 0V
	200	200	300	300	μA	All Digital Inputs = V_{IL}
	25	25	25	25	μA	All Digital Inputs = V_{DD}
	200	200	300	300	μA	All Digital Inputs = V_{IH}

NOTES:

[1] Gain error is measured when using internal feedback resistor. Ideal Full Scale Range (FSR) = (V_{REF} – 1 LSB) as shown in Table I.

[2] Guaranteed, not tested.

[3] AC parameter, sample tested @ +25°C to assure conformance to specifications.

[4] DAC thin film resistor temperature coefficient is approximately -300ppm/°C.

Specifications subject to change without notice.

CAUTION

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not apply voltages lower than ground or higher than V_{DD} to any pin except V_{REF} (pin 15) and R_{FB} (pin 16).
3. The inputs of some IC amplifiers (especially wide bandwidth types) present a low impedance to V^- during power-up or power-down sequencing. To prevent the AD7524 OUT1 or OUT2 terminals from exceeding -300mV (which causes catastrophic substrate current) a Schottky diode (HP5082-2811 or equivalent) is recommended. The diode should be connected between OUT1 (OUT2) and ground as shown in Figures 5 and 6.
4. Do not plug this device into sockets under power. Remove power before insertion or removal.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . -0.3V, +17V
V_{REF} to GND. . . . . ±25V
V_{RFB} to GND. . . . . ±25V
Digital Input Voltage to GND . . . . . -0.3V to V_{DD}
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND . . . . . -0.3V to V_{DD}
Power Dissipation (package)
Plastic (N. Suffix)
To +70°C. 670mW
Derates above +70°C by . . . . . .8.3mW/°C
Ceramic (D Suffix)
To +75°C. 450mW
Derates above +75°C by . . . . . .6mW/°C
Operating Temperature
Commerical (JN, KN, LN) Grades. . . . . 0 to +70°C
Industrial (AD, BD, CD) Grades . . . . . -25°C to +85°C
Military (SD, TD, UD) Grades . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

TERMINOLOGY

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a *best straight line* function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the reference voltage. "Zero" gain error (for an 8-bit DAC) is defined when V_{OUT} equals $-V_{REF}$ (255/256).

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from OUT1 and OUT2 terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on OUT1 terminal with all digital inputs LOW or on OUT2 terminal when all inputs are HIGH. This is an error current which contributs an offset voltage (at the amplifier output) of typically 0.2 LSB.

INTERFACE LOGIC INFORMATION

MODE SELECTION

AD7524 mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

WRITE MODE

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the AD7524 is in the WRITE mode, and the AD7524 analog output responds to data activity at the DB_0-DB_7 data bus inputs. In this mode, the AD7524 acts like a non-latched input D/A converter.

HOLD MODE

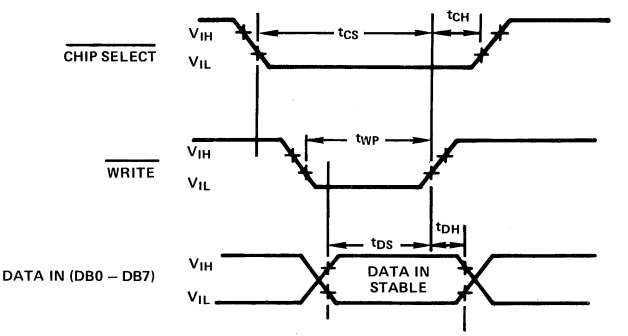
When either $\overline{CS}$ or $\overline{WR}$ are HIGH, the AD7524 is in the HOLD mode. The AD7524 analog output holds the value corresponding to the last digital input present at DB_0-DB_7 prior to $\overline{WR}$ or $\overline{CS}$ assuming the high state.

MODE SELECTION TABLE

$\overline{CS}$	$\overline{WR}$	MODE	DAC RESPONSE
L	L	Write	DAC responds to data bus (DB0 – DB7) inputs
H	X	Hold	Data bus (DB0 – DB7) is locked out;
X	H	Hold	DAC holds last data present when $\overline{WR}$ assumed HIGH state.

L = LOW state
H = HIGH state
Y = Don't care state

WRITE CYCLE TIMING DIAGRAM



NOTE: IF $\overline{CS}$ AND $\overline{WR}$ ARE EXERCISED SIMULTANEOUSLY, THE t_{DH} SPECIFICATION (AS SHOWN IN SPECIFICATION TABLE, MUST BE INCREASED BY 60ns.

ANALOG CIRCUIT DESCRIPTION

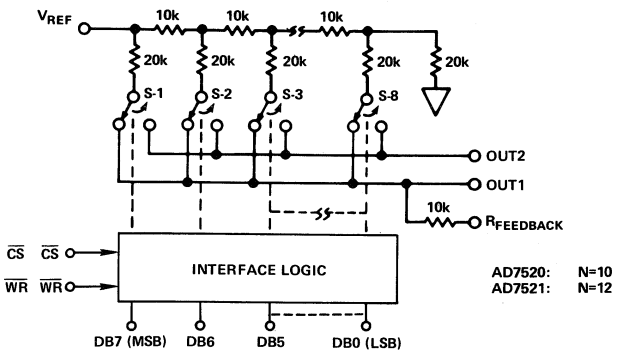
GENERAL CIRCUIT INFORMATION

The AD7524, an 8-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and eight N-channel MOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

One of the current switches is shown in Figure 2. The "ON" resistances of the first six switches are binarily scaled so the voltage drop across each switch is the same. For example, switch 1 of Figure 2 was designed for an "ON" resistance of 20 ohms, switch 2 of 40 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that

each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.



(Switches shown for Inputs "High")

Figure 1. AD7524 Functional Diagram

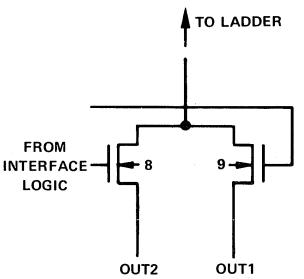


Figure 2. N-Channel Current Steering Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 3 and 4. In Figure 3 with all digital inputs low, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{256}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 90pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 30pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal OUT1, hence the 90pF at that terminal.

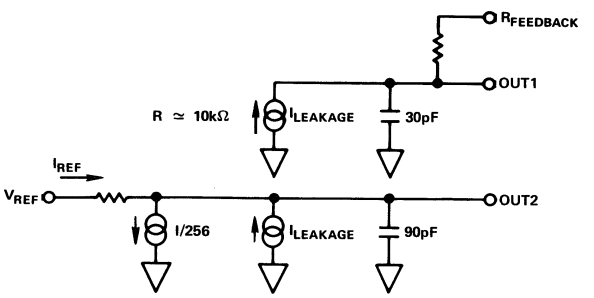


Figure 3. AD7524 DAC Equivalent Circuit – All Digital Inputs Low

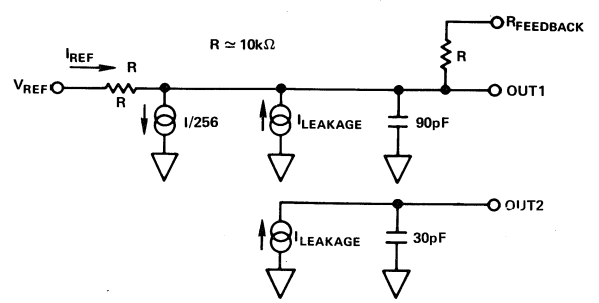


Figure 4. AD7524 DAC Equivalent Circuit – Digital Inputs High

APPLYING THE AD7524

ANALOG CIRCUIT CONNECTIONS

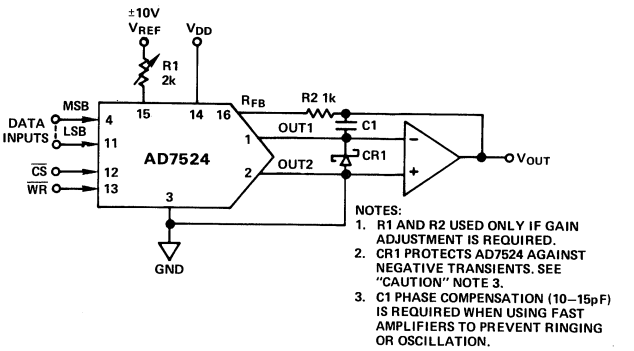
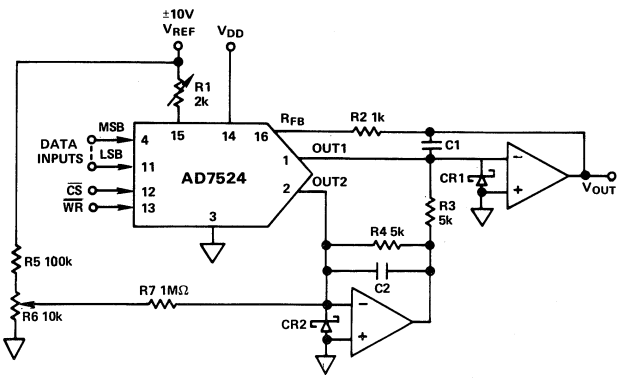


Figure 5. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT		ANALOG OUTPUT
MSB	LSB	
11111111		$-V_{REF}\left(\frac{255}{256}\right)$
10000001		$-V_{REF}\left(\frac{129}{256}\right)$
10000000		$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111		$-V_{REF}\left(\frac{127}{256}\right)$
00000001		$-V_{REF}\left(\frac{1}{256}\right)$
00000000		$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: $1LSB = (2^{-8})(V_{REF}) = \frac{1}{256}\ (V_{REF})$

Table 1. Unipolar Binary Code Table



NOTES:

1. R3/R4 MATCH 0.1% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. R5–R7 USED TO ADJUST V_{OUT} = 0V AT INPUT CODE 10000000.
4. CR1 & CR2 PROTECT AD7524 AGAINST NEGATIVE TRANSIENTS. SEE "CAUTION" NOTE 3.
5. C1 AND C2 PHASE COMPENSATION (10–15pF) IS REQUIRED WHEN USING FAST AMPLIFIERS TO PREVENT RINGING OR OSCILLATION.

Figure 6. Bipolar (4-Quadrant) Operation

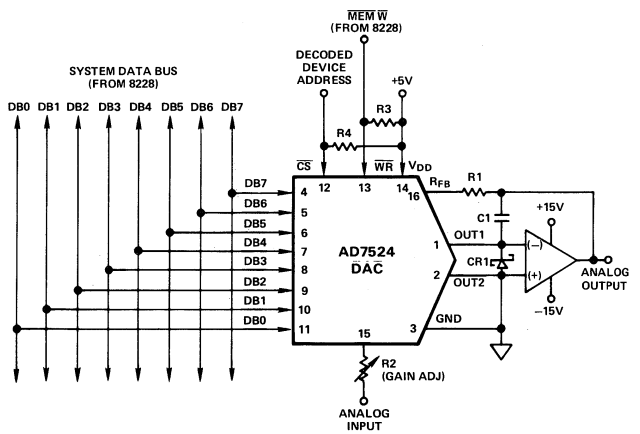
DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}\left(\frac{127}{128}\right)$
10000001	$-V_{REF}\left(\frac{1}{128}\right)$
10000000	0
01111111	$+V_{REF}\left(\frac{1}{128}\right)$
00000001	$+V_{REF}\left(\frac{127}{128}\right)$
00000000	$+V_{REF}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{REF}) = \left(\frac{1}{128}\right)(V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table

APPLICATIONS — MICROPROCESSOR INTERFACE

AD7524/8080A INTERFACE



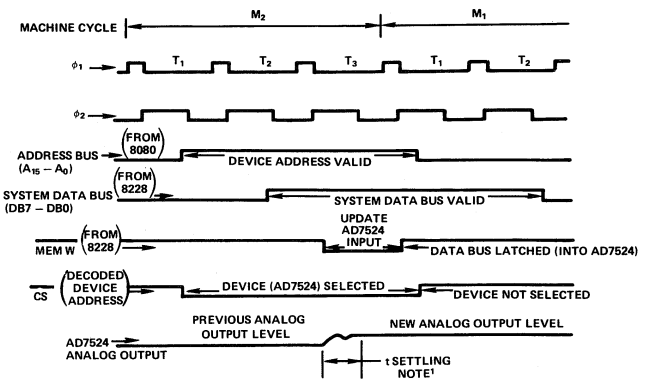
AD7524/8080A INTERFACE

The illustration above shows the AD7524 used in the MCS-80 microcomputer system as a Memory Mapped Output Device. The basic CPU group consists of the 8080A CPU, 8224 clock generator and 8228 system controller/bus driver. The AD7524 $\overline{WR}$ input is connected to the 8228 $\overline{MEMW}$ output and the DB0 – DB7 inputs are connected to the 8228 system data bus outputs. The $\overline{CS}$ input is connected to the system address decoding logic. Note that pullup resistors R3 and R4 are required to ensure that the $\overline{CS}$ and $\overline{WR}$ input HIGH states reach 3.0V min. Pullups are not required on the system data bus since the 8228 V_{OH} is 3.6V min for DB0 – DB7.

System timing is shown. Data is loaded into the AD7524 when the $\overline{WR}$ and $\overline{CS}$ inputs are both LOW. The data is latched into the AD7524 when $\overline{WR}$ returns HIGH. AD7524 updating is accomplished by using any of the 8080A memory write instructions (such as MOV M, r).

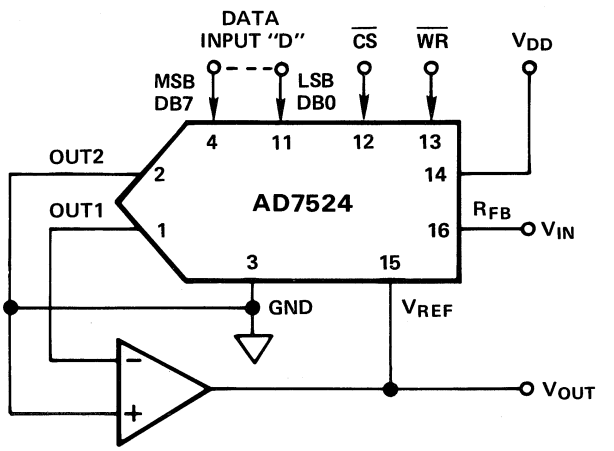
The AD7524 can also be addressed and loaded as an isolated Output Device by connecting the AD7524 $\overline{WR}$ input to the 8228 $\overline{I/O\ W}$ terminal (instead of $\overline{MEMW}$).

TIMING DIAGRAM



NOTE: 1SETTLING TIME IS DEPENDENT PRIMARILY UPON OUTPUT AMPLIFIER SLEWING AND SETTLING CHARACTERISTICS. WAVEFORM SHOWN IS NOT REPRESENTATIVE OF ANY SPECIFIC AMPLIFIER.

DIVIDER (DIGITALLY CONTROLLED GAIN)



EQUATIONS

$$V_{OUT} = -\frac{V_{IN}}{D}$$

$$A_V = \frac{V_{OUT}}{V_{IN}} = -\frac{1}{D}$$ where: A_V = Voltage Gain

and where:

$$D = \frac{DB7}{2^1} + \frac{DB6}{2^2} + \ldots \frac{DB0}{2^8}$$

DB_N = 1 or 0

EXAMPLES

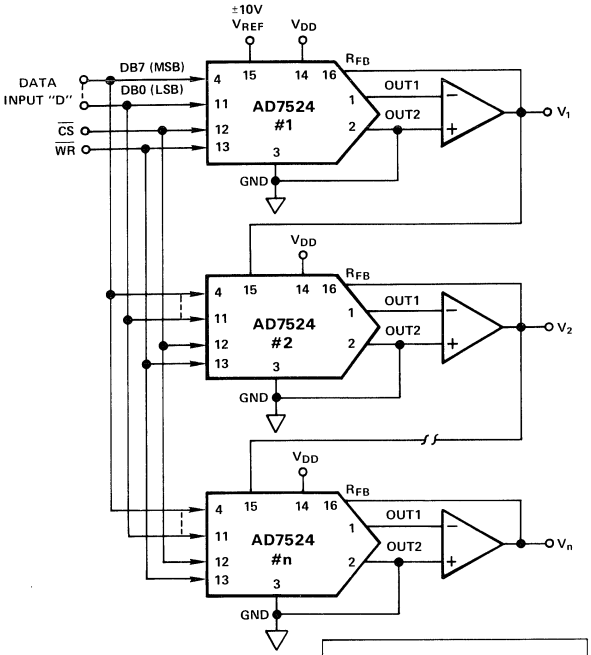
D = 00000000, $A_V = -A_{OL}$ (OP AMP)

D = 00000001, A_V = –256

D = 10000000, A_V = -2

D = 11111111, $A_V = -\frac{256}{255}$

POWER GENERATION



CIRCUIT EQUATIONS

$V_1 = -(V_{REF})(D)$

$V_2 = +(V_{REF})(D^2)$

$V_n = -(V_{REF})(D^n)$, n an odd integer

$V_n = +(V_{REF})(D^n)$, n an even integer

where:

$$D = \frac{DB7}{2^1} + \frac{DB0}{2^2} + \ldots \frac{DB0}{2^8}$$

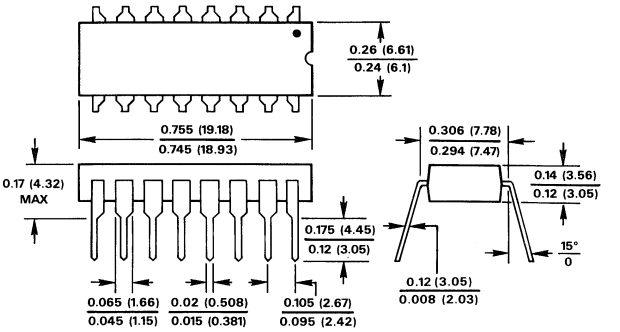
and

DB_n = 1 or 0

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

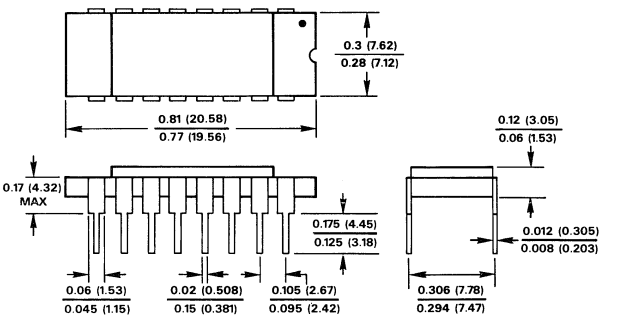
16 PIN PLASTIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH

LEADS ARE SOLDER PLATED KOVAR

16 PIN CERAMIC DIP

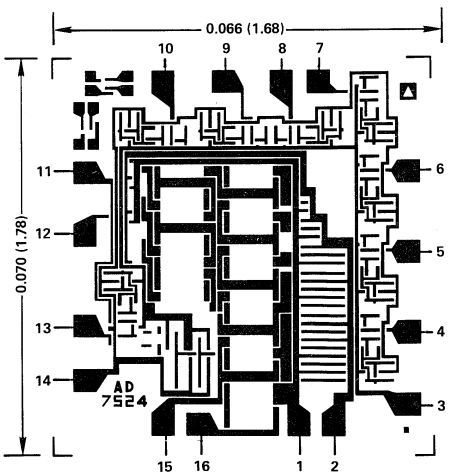


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH

LEADS ARE GOLD-PLATED (50 MICROINCHES MIN.) KOVAR

BONDING DIAGRAM

Dimensions shown in inches and (mm).

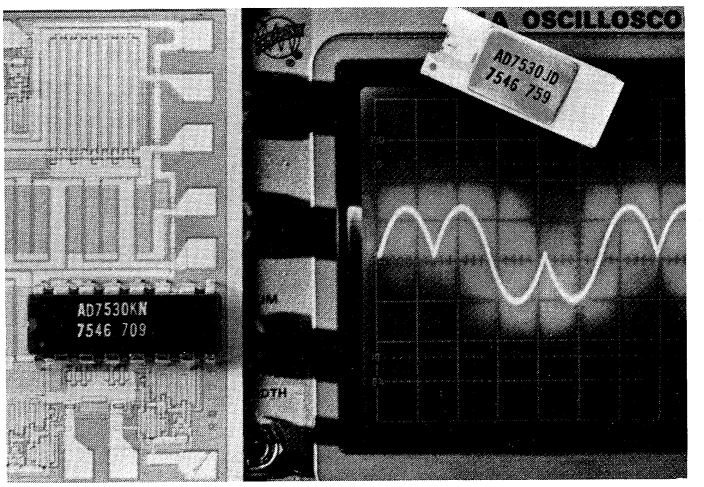


Notes:
1. Pad numbers correspond to pin numbers shown in pin configuration.
2. Pad 3 (GND) should be bonded first to minimize ESD hazards.
3. Pads are 0.004 in. x 0.004in. (0.102mm x 0.102mm).

CMOS 10 & 12 Bit Monolithic Multiplying D/A Converters

AD7530, AD7531

FEATURES
AD7530: 10-Bit Resolution
AD7531: 12-Bit Resolution
8, 9 and 10 Bit Linearity
DTL/TTL/CMOS Compatible
Nonlinearity Tempco: 2ppm of FSR/°C
Low Power Dissipation: 20mW
Current Settling Time: 500ns
Feedthrough Error: 10mV p-p @ 50kHz
Low Cost



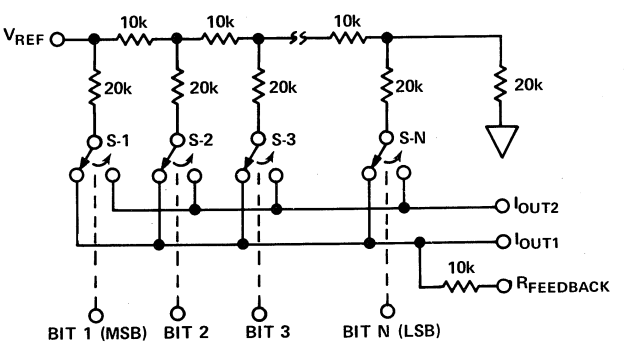
GENERAL DESCRIPTION

The AD7530 (AD7531) is a low cost, monolithic 10-bit (12-bit) multiplying digital-to-analog converter packaged in a 16-pin (18-pin) DIP. The device uses advanced CMOS and thin film technologies providing up to 10-bit accuracy with DTL/TTL/CMOS compatibility.

The AD7530 (AD7531) operates from a +5V to +15V supply and dissipates only 20mW, including the ladder network.

Typical applications include: digital/analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

FUNCTIONAL DIAGRAM



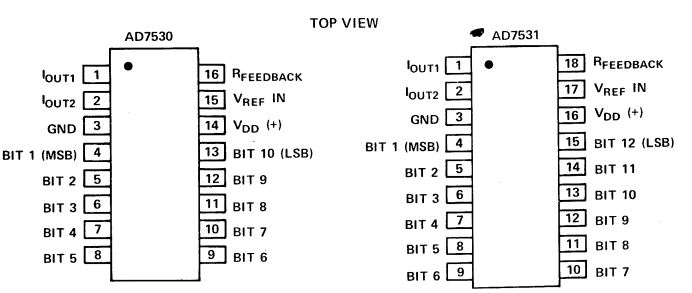
DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

AD7530: N = 10
AD7531: N = 12
(Switches shown in "High" state)

ORDERING INFORMATION

Nonlinearity	Temperature Range	
	0 to +70°C	−25°C to +85°C
0.2% (8-Bit)	AD7530JN	AD7530JD
	AD7531JN	AD7531JD
0.1% (9-Bit)	AD7530KN	AD7530KD
	AD7531KN	AD7531KD
0.05% (10-Bit)	AD7530LN	AD7530LD
	AD7531LN	AD7531LD

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +15, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

PARAMETER		AD7530	AD7531	TEST CONDITIONS
DC ACCURACY (Note 1)				
Resolution		10 Bits	12 Bits	
Nonlinearity	AD7530J	0.2% of FSR max (8 Bit)	*	
	AD7530K	0.1% of FSR max (9 Bit)	*	
	AD7530L	0.05% of FSR max (10 Bit)	*	
Nonlinearity Tempco		2ppm of FSR/°C max	*	$-10V < V_{REF} < +10V$
Gain Error		0.3% of FSR typ	*	
Gain Error Tempco		10ppm of FSR/°C max	*	
Output Leakage Current (Either Output)		300nA max	*	Over specified temperature range.
Power Supply Rejection		50ppm of FSR/% typ	*	
AC ACCURACY				To 0.05%
Output Current Settling Time		500ns typ	*	All digital inputs low to high and high to low
Feedthrough Error		10mV p-p max	*	V_{REF} = 20V p-p, 50kHz. All digital inputs low
REFERENCE INPUT		±10V	*	
Input Range		±1mA	*	
Input Resistance		10kΩ typ	*	
ANALOG OUTPUT				
Output Current Range (Both Outputs)		±1mA	*	
Output Capacitance	I_{OUT1}	120pF typ	*	All digital inputs high
	I_{OUT2}	37pF typ	*	
	I_{OUT1}	37pF typ	*	All digital input low
	I_{OUT2}	120pF typ	*	
Output Noise (Both Outputs)		Equivalent to 10kΩ Johnson noise typ	*	
DIGITAL INPUTS (Note 2)				
Low State Threshold		0.8V max	*	
High State Threshold		2.4V min	*	Over specified temperature range
Input Current (low to high state)		1μA typ	*	
Input Coding		Binary	*	See Tables 1 & 2
POWER REQUIREMENTS				
Power Supply Voltage Range		+5V to +15V	*	
I_{DD}		5nA typ	*	All digital inputs at GND
		2mA max	*	All digital inputs high or low
Total Dissipation		20mW typ	*	

NOTES:
[1] Full scale range (FSR) is 10V for unipolar mode and ±10V for bipolar mode.
[2] Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

*Same specifications as for AD7530.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to Gnd) . . . . . +17V
V_{REF} (to Gnd) . . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to Gnd
Voltage at Pin 1, Pin 2 . . . . . −100mV to V_{DD}
Power Dissipation (package)
up to +75°C 450mW
Operating Temperature
JN, KN, LN Versions . . . . . 0 to +75°C
JD, KD, LD Versions . . . . . −25°C to +85°C
Storage Temperature . . . . . −65°C to +150°C

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

APPLICATIONS

UNIPOLAR BINARY OPERATION

Figure 1 shows the circuit connections required for unipolar operation. Since V_{REF} can assume either positive or negative values, the circuit is also capable of 2-quadrant multiplication. The input code/output range table for unipolar binary operation is shown in Table 1.

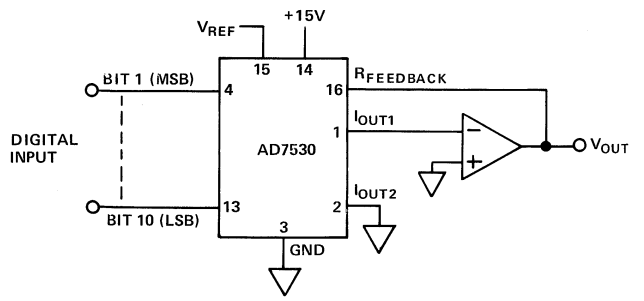


Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table 1. Code Table — Unipolar Binary Operation

BIPOLAR (OFFSET BINARY) OPERATION

Figure 2 illustrates the AD7530 connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. Input coding is offset binary (modified 2's complement) as shown in Table 2.

When a switch's control input is a Logical "1", that switch's current is steered to I_{OUT1}, forcing the output of amplifier #1 to

$$V_{OUT} = -(I_{OUT1})\ (10k)$$

where 10k is the value of the feedback resistor.

A Logical "0" on the control input steers the switch's current to I_{OUT2}, which is terminated into the summing junction of amplifier #2. Resistors R1 and R2 need not track the internal R-2R circuitry; however, they should closely match each other to insure that the voltage at amplifer #2's output will force a current into R2 which is equal in magnitude but opposite in polarity to the current at I_{OUT2}. This creates a push-pull effect which halves the resolution but doubles the output range for changes in the digital input.

With the MSB a Logic "1" and all other bits a Logic "0", a 1/2 LSB difference current exists between I_{OUT1} and I_{OUT2}, creating an offset of 1/2 LSB. To shift the transfer curve to zero, resistor R-9 is used to sum 1/2 LSB of current into the I_{OUT2} terminal.

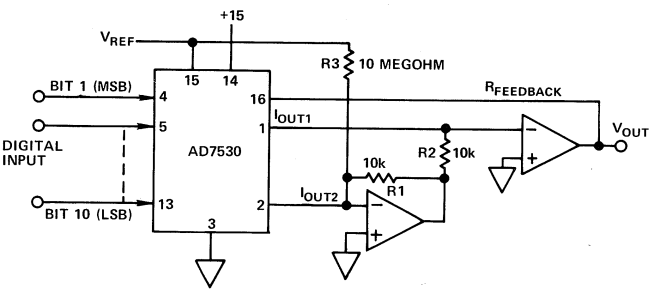


Figure 2. Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

Table 2. Code Table — Bipolar (Offset Binary) Operation

TERMINOLOGY

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DACs operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

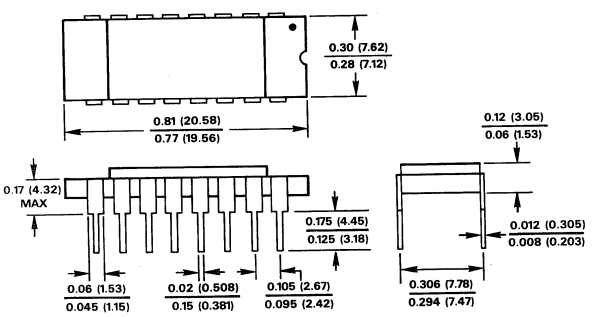
OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

OUTLINE DIMENSIONS

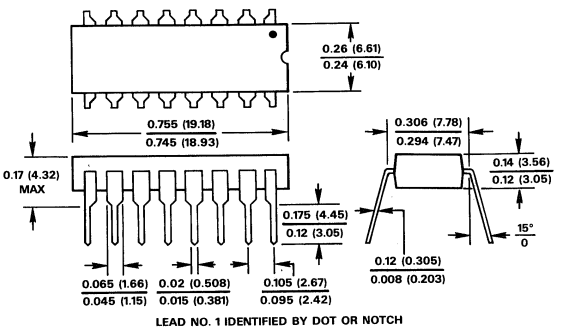
Dimensions shown in inches and (mm).

AD7530

16 PIN CERAMIC DIP

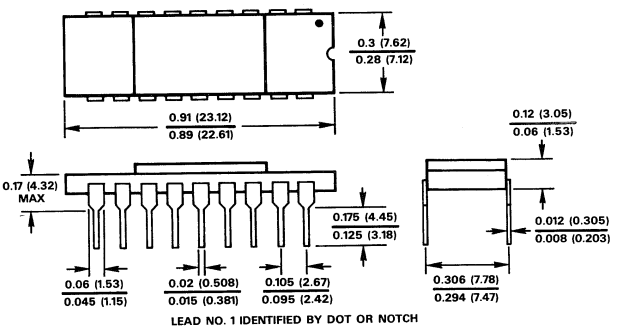


16 PIN PLASTIC DIP

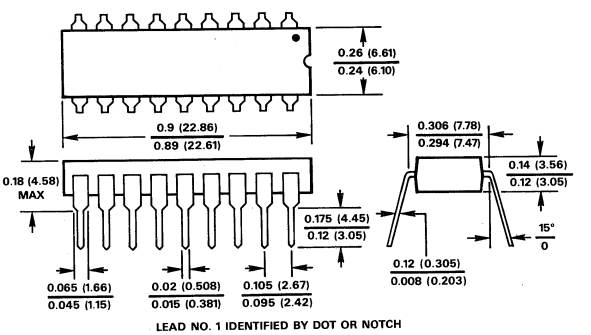


AD7531

18 PIN CERAMIC DIP



18 PIN PLASTIC DIP

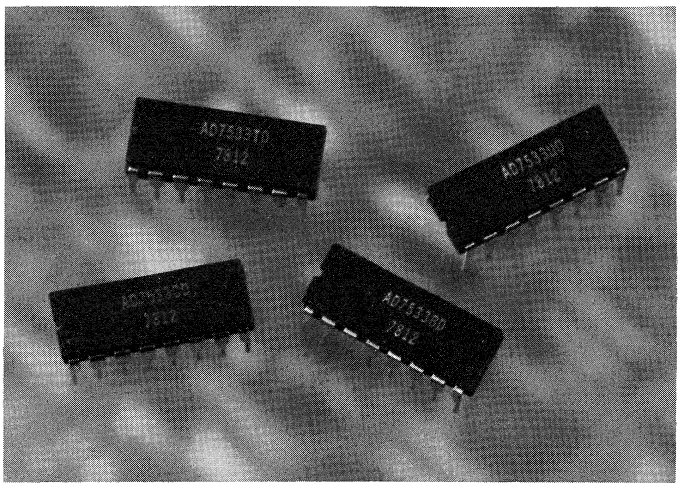


CMOS
Low Cost 10-Bit Multiplying DAC
AD7533

PRELIMINARY TECHNICAL DATA

FEATURES
- Lowest Cost 10-Bit DAC
- Direct AD7520 Equivalent
- Linearity: ½, 1 or 2LSB
- Low Power Dissipation
- Full Four-Quadrant Multiplying DAC
- CMOS/TTL Direct Interface

APPLICATIONS
- Digitally Controlled Attenuators
- Programmable Gain Amplifiers
- Function Generation
- Linear Automatic Gain Control



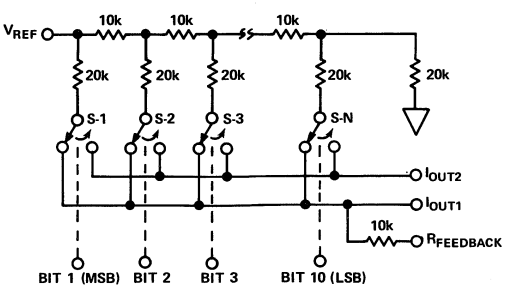
GENERAL DESCRIPTION

The AD7533 is a low cost 10-bit 4-quadrant multiplying DAC manufactured using an advanced thin-film-on-monolithic-CMOS wafer fabrication process.

Pin and function equivalent to the industry standard AD7520, the AD7533 is recommended as a lower cost alternative for old AD7520 sockets or new 10-bit DAC designs.

AD7533 application flexibility is demonstrated by its ability to interface to TTL or CMOS, operate on +5V to +15V power, and provide proper binary scaling for reference inputs of either positive or negative polarity.

FUNCTIONAL DIAGRAM



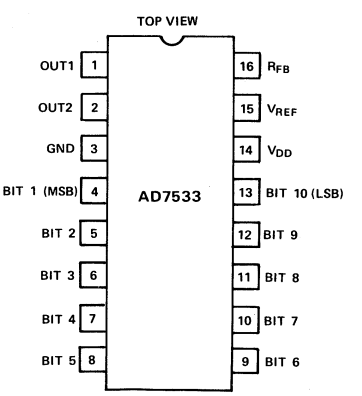
DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

Logic: A switch is closed to $I_{OUT\ 1}$ for its digital input in a "HIGH" state.

ORDERING INFORMATION

Nonlinearity	Temperature Range and Package		
	Commercial (Plastic) 0 to +70°C	Industrial (Ceramic) -25°C to +85°C	Military (Ceramic) -55°C to +125°C
±0.2%	AD7533JN	AD7533AD AD7533AD/883B	AD7533SD AD7533SD/883B
±0.1%	AD7533KN	AD7533BD AD7533BD/883B	AD7533TD AD7533TD/883B
±0.05%	AD7533LN	AD7533CD AD7533CD/883B	AD7533UD AD7533UD/883B

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +15V; V_{OUT1} = V_{OUT2} = 0V; V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = 25°C	T_A = Operating Range[1]	Test Conditions
STATIC ACCURACY			
Resolution	10 Bits	10 Bits	
Nonlinearity[2]			
AD7533JN, AD, SD	±0.2% FSR max	±0.2% FSR max	
AD7533KN, BD, TD	±0.1% FSR max	±0.1% FSR max	
AD7533LN, CD, UD	±0.05% FSR max	±0.05% FSR max	
Gain Error[3]	±1.4% FS max	±1.5% FS max	Digital Inputs = V_{INH}
Supply Rejection[4]			
$\Delta Gain/\Delta V_{DD}$	0.005%/%	0.008%/%	Digital Inputs = V_{INH}; V_{DD} = +14V to +17V
Output Leakage Current			
I_{OUT1} (pin 1)	±50nA max	±200nA max	Digital Inputs = V_{INL}; V_{REF} = ±10V
I_{OUT2} (pin 2)	±50nA max	±200nA max	Digital Inputs = V_{INH}; V_{REF} = ±10V
DYNAMIC ACCURACY			
Output Current Settling Time	600ns max[5]	800ns[4]	To 0.05% FSR; R_{LOAD} = 100Ω; Digital Inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error	±0.05% FSR max[4]	±0.1% FSR max[4]	Digital Inputs = V_{INL}; V_{REF} = ±10V, 100kHz sinewave.
REFERENCE INPUT			
Input Resistance (pin 15)	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max[6]	
ANALOG OUTPUTS			
Output Capacitance			
C_{OUT1} (pin 1)	100pF max[4]	100pF max[4]	Digital Inputs = V_{INH}
C_{OUT2} (pin 2)	35pF max[4]	35pF max[4]	Digital Inputs = V_{INH}
C_{OUT1} (pin 1)	35pF max[4]	35pF max[4]	Digital Inputs = V_{INL}
C_{OUT2} (pin 2)	100pF max[4]	100pF max[4]	Digital Inputs = V_{INL}
DIGITAL INPUTS			
Input High Voltage			
V_{INH}	2.4V min	2.4V min	
Input Low Voltage			
V_{INL}	0.8V max	0.8V max	
Input Leakage Current			
I_{IN}	±1μA max	±1μA max	V_{IN} = 0V and V_{DD}
Input Capacitance			
C_{IN}	5pF max[4]	5pF max[4]	
POWER REQUIREMENTS			
V_{DD}	+15V ±10%	+15V ±10%	Rated Accuracy
V_{DD} Range[4]	+5V to +16V	+5V to +16V	Functionality with degraded performance
I_{DD}	2mA max	2mA max	Digital Inputs = V_{INL} or V_{INH}
I_{DD}	100μA max	150μA max	Digital Inputs = OV or V_{DD}

NOTES:
[1] Plastic (JN, KN, LN versions): 0 to +70°C
Commercial Ceramic (AD, BD, CD versions): -25°C to +85°C
Military Ceramic (SD, TD, UD versions): -55°C to +125°C
[2] "FSR" is Full Scale Range.
[3] Full Scale (FS) = $-(V_{REF})\left(\frac{1023}{1024}\right)$
[4] Guaranteed, not tested.
[5] AC parameter, sample tested to ensure specification compliance.
[6] Absolute temperature coefficient is approximately -300ppm/°C.
[7] 100% screened to MIL-STD-883, method 5004, para. 3.1.1 through 3.1.12 for class B device. Final electrical tests are: Nonlinearity, Gain Error, Output Leakage Current, V_{INH}, V_{INL}, I_{IN} and I_{DD} at +25°C and +125°C (SD, TD, UD versions) or +25°C and +85°C (AD, BD, CD versions).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS
(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . -0.3V, +17V
R_{FB} to GND . . . . . ±25V
V_{REF} to GND. . . . . ±25V
Digital Input Voltage Range . . . . . -0.3V to V_{DD}
Output Voltage (pin 1, pin 2) . . . . . -0.3V to V_{DD}
Power Dissipation (Package)
Plastic (Suffix N)
To +70°C. 670mW
Derates above +70°C by . . . . . 8.3mW/°C
Ceramic (Suffix D)
To +75°C. 450mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature Range
Commercial (JN, KN, LN versions) . . . . . 0 to +70°C
Industrial (AD, BD, CD versions) . . . . . -25°C to +85°C
Military (SD, TD, UD versions) . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not apply voltages lower than ground or higher the V_{DD} to any pin except V_{REF} (pin 15) and R_{FB} (pin 16).
3. The inputs of some IC amplifiers (especially wide bandwidth types) present a low impedance to V^- during power-up or power-down sequencing. To prevent the AD7533 OUT1 or OUT2 terminals from exceeding -300mV (which causes catastrophic substrate current) a Schottky diode (HP5082-2811 or equivalent) is recommended. The diode should be connected between OUT1 (OUT2) and ground as shown in Figures 5 and 6.

TERMINOLOGY

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7533, a 10-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

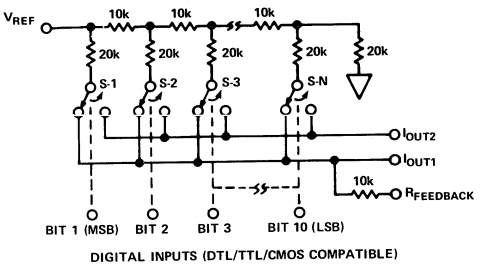


Figure 1. AD7533 Functional Diagram

One of the CMOS current switches is shown in Figure 2. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the switches are binarily sealed so the voltage drop across each switch is the same. For example, switch 1 of Figure 2 was designed for an "ON" resistance of 20 ohms, switch 2 or 40 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

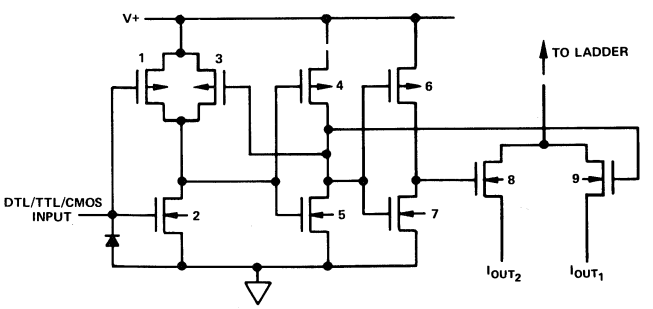


Figure 2. CMOS Switch

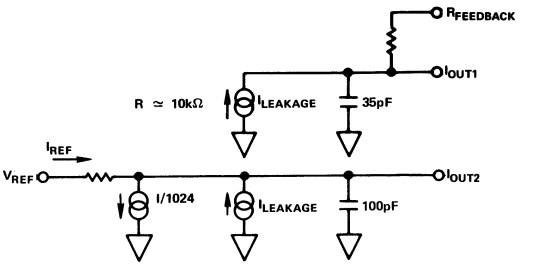


Figure 3. AD7533 Equivalent Circuit – All Digital Inputs Low

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 3 and 4. In Figure 3 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 120pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 30pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal I_{OUT1}, hence the 100pF at that terminal.

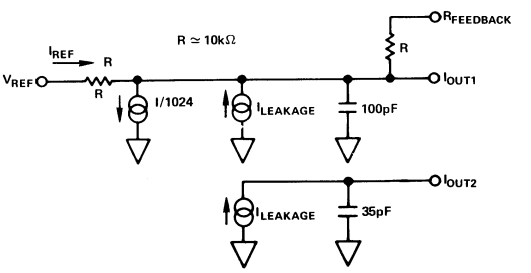
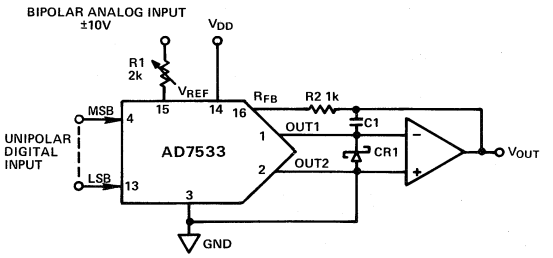


Figure 4. AD7533 Equivalent Circuit – All Digital Inputs High

OPERATION

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. SCHOTTKY DIODE CR1 (HP5082–2811 OR EQUIV) PROTECTS OUT1 TERMINAL AGAINST NEGATIVE TRANSIENTS. SEE "CAUTION" NOTE 3.
3. C1 PHASE COMPENSATION (5 – 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

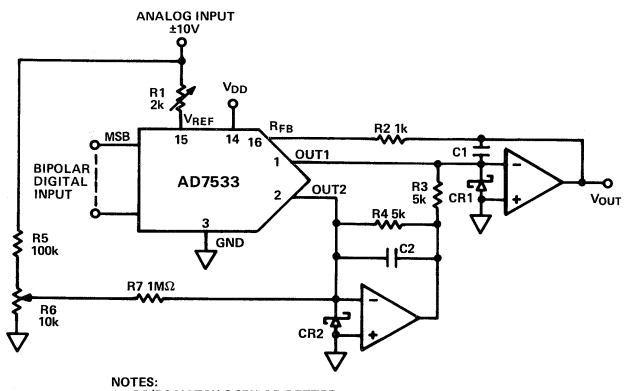
Figure 5. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB	LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 1)
1111111111		$-V_{REF}\left(\frac{1023}{1024}\right)$
1000000001		$-V_{REF}\left(\frac{513}{1024}\right)$
1000000000		$-V_{REF}\left(\frac{512}{1024}\right)=-\frac{V_{REF}}{2}$
0111111111		$-V_{REF}\left(\frac{511}{1024}\right)$
0000000001		$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000		$-V_{REF}\left(\frac{0}{1024}\right)=0$

NOTES:
1. Nominal Full Scale for the circuit of Figure 5 is given by $FS = -V_{REF}\left(\frac{1023}{1024}\right)$
2. Nominal LSB magnitude for the circuit of Figure 5 is given by $LSB = V_{REF}\left(\frac{1}{1024}\right)$

Table 1. Unipolar Binary Code Table

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED
3. C1, C2 PHASE COMPENSATION (5 – 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIERS.
4. SCHOTTKY DIODES CR1 AND CR2 (HP5082–2811 OR EQUIV) PROTECT OUT1 AND OUT2 TERMINALS FROM NEGATIVE TRANSIENTS. SEE "CAUTION" NOTE 3.

Figure 6. Bipolar Operation (4-Quadrant Multiplication)

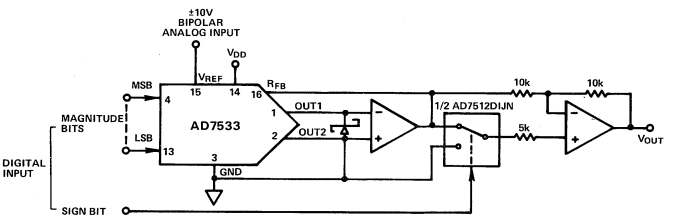
DIGITAL INPUT MSB	LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 2)
1111111111		$-V_{REF}\left(\frac{511}{512}\right)$
1000000001		$-V_{REF}\left(\frac{1}{512}\right)$
1000000000		0
0111111111		$+V_{REF}\left(\frac{1}{512}\right)$
0000000001		$+V_{REF}\left(\frac{511}{512}\right)$
0000000000		$+V_{REF}\left(\frac{512}{512}\right)$

NOTES:
1. Nominal Full Scale Range for the circuit of Figure 6 is given by $FSR = V_{REF}\left(\frac{1023}{512}\right)$
2. Nominal LSB magnitude for the circuit of Figure 6 is given by $LSB = V_{REF}\left(\frac{1}{512}\right)$

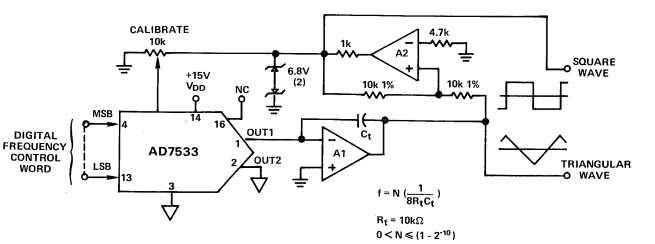
Table 2. Bipolar (Offset Binary) Code Table

APPLICATIONS

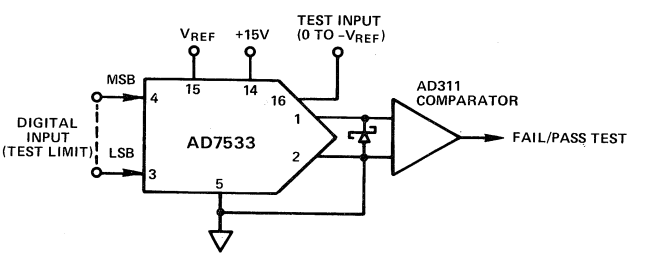
10-BIT AND SIGN MULTIPLYING DAC



PROGRAMMABLE FUNCTION GENERATOR

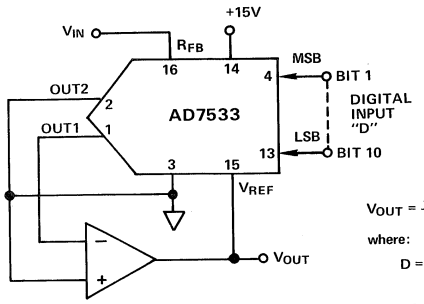


DIGITALLY PROGRAMMABLE LIMIT DETECTOR



APPLICATIONS (continued)

DIVIDER (DIGITALLY CONTROLLED GAIN)



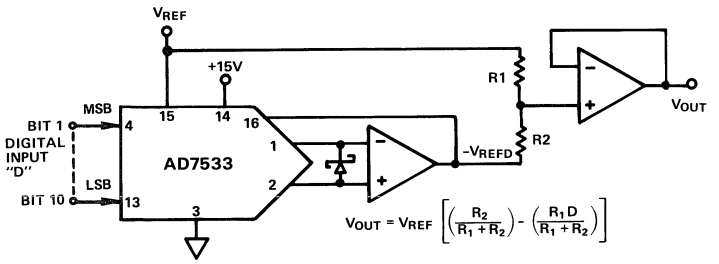
$$V_{OUT} = \frac{-V_{IN}}{D}$$

where:

$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ 10}{2^{10}}$$

$$0 < D \leq \frac{1023}{1024}$$

MODIFIED SCALE FACTOR AND OFFSET



$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1+R_2}\right) - \left(\frac{R_1 D}{R_1+R_2}\right)\right]$$

where:

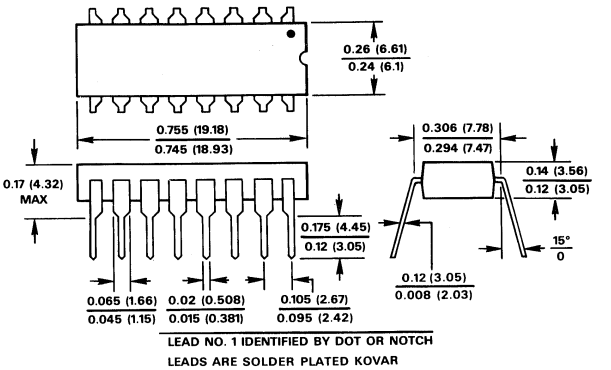
$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ 10}{2^{10}}$$

$$\left(0 \leqslant D \leqslant \frac{1023}{1024}\right)$$

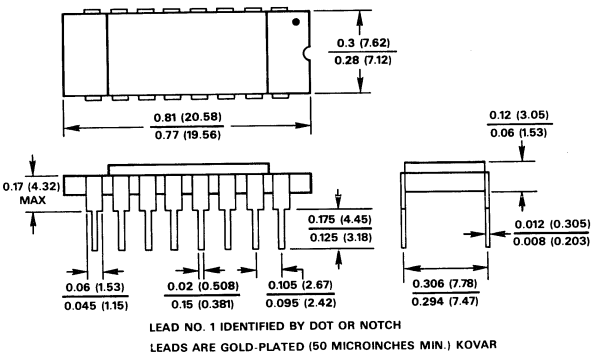
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16 PIN PLASTIC DIP

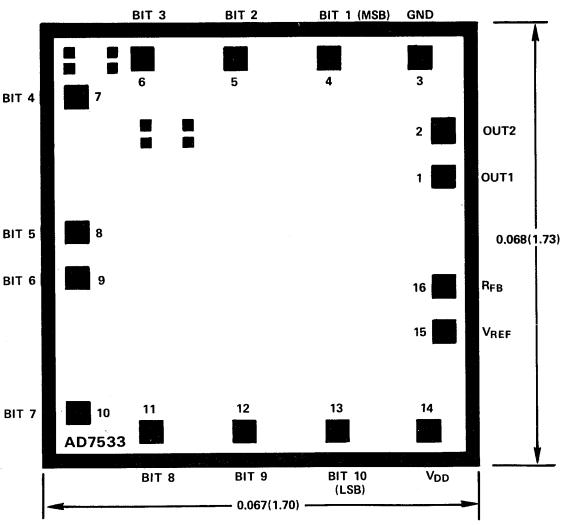


16 PIN CERAMIC DIP



BONDING DIAGRAM

Dimensions shown in inches and (mm).



CMOS 12-Bit Monolithic Multiplying DAC

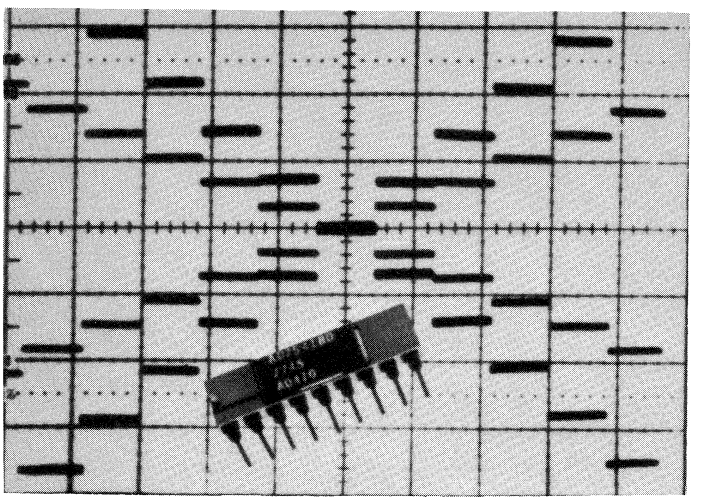
AD7541

FEATURES

Full Four Quadrant Multiplication
12-Bit Linearity (0.01%)
Pretrimmed Gain
TTL/CMOS Compatible
Low Power Comsumption
Low Feedthrough Error
Low Cost

APPLICATIONS

Digital/Synchro Conversion
Programmable Amplifiers
Ratiometric A/D Conversion
Function Generation



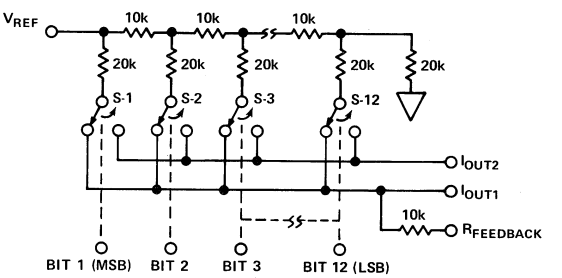
GENERAL DESCRIPTION

The Analog Devices AD7541 is a low cost, high performance 12-bit monolithic multiplying digital-to-analog converter fabricated using advanced double-layer-metal CMOS technology and packaged in a standard 18-pin DIP.

Pin compatible with the AD7521, this new device uses laser wafer trimming to provide full 12-bit linearity and excellent absolute accuracy.

The inherently low power dissipation, coupled with the current switching R-2R ladder, ensures that the performance is maintained over the full temperature range.

FUNCTIONAL DIAGRAM

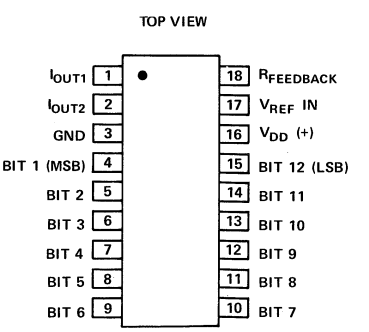


DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

ORDERING INFORMATION

	Temperature Range and Package		
Nonlinearity	Plastic 0 to +70°C	Ceramic -25°C to +85°C	Ceramic -55°C to +125°C
0.02%	AD7541JN	AD7541AD	AD7541SD
0.01%	AD7541KN	AD7541BD	AD7541TD

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = 15V, V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = +25°C	T_A = min-max	TEST CONDITION
STATIC ACCURACY			
Resolution	12 Bits min	12 Bits min	
Nonlinearity			V_{OUT1} =
AD7541JN, AD7541AD, AD7541SD	±0.02% FSR[1] max	±0.024% FSR max	V_{OUT2} = 0V
AD7541KN, AD7541BD, AD7541TD	±0.01% FSR max	±0.012% FSR max	
Gain Error[1,2]	±0.3% FSR max	±0.4% FSR max	
Power Supply Rejection	±01% per % max	±0.02% per % max	V_{DD} = 14.5V – 15.5V
Output Leakage Current	±50nA max	±200nA max	V_{REF} = ±10V
DYNAMIC PERFORMANCE			
Output Current Settling Time[3]	1μs max	1μs max	To 0.01% of FSR
Feedthrough Error[3]	1mV p-p max	1mV p-p max	V_{REF} = 20V p-p @ 10kHz
REFERENCE INPUT			
Input Resistance	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max	
DIGITAL INPUTS			
V_{INH}	2.4V max	2.4V max	
V_{INL}	0.8V min	0.8V min	
Input Leakage Current	±1μA max	±1μA min	V_{IN} = 0 or 15V
Input Capacitance[3]	8pF max	8pF max	
Input Coding	Binary or Offset Binary		
ANALOG OUTPUTS			
Output Capacitance[3]			
C_{OUT1}	200pF max	200pF max	Digital Inputs
C_{OUT2}	60pF max	60pF max	= V_{INH}
C_{OUT1}	60pF max	60pF max	Digital Inputs
C_{OUT2}	200pF max	200pF max	= V_{INL}
POWER REQUIREMENTS			
V_{DD} Range	+5V min, +16V max	+5V min, +16V max	Accuracy is not guaranteed over this range.
I_{DD}	2mA max	2mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES:
[1] FSR is Full Scale Range.
[2] Using internal feedback resistor.
[3] Guaranteed by design, not subject to test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to GND) . . . . . +17V
V_{REF} (to GND) . . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Output Voltage (Pin 1, Pin 2) . . . . . -100mV to V_{DD}
Power Dissipation (Package)
Up to +75°C 450mW
Derate above +75°C by . . . . . 6mW/°C
Operating Temperature
JN, KN Versions . . . . . 0 to +70°C
AD, BD Versions . . . . . -25°C to +85°C
SD, TD Versions . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused inputs in conductive foam at all times.

SPECIFICATION DEFINITIONS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

TYPICAL PERFORMANCE CHARACTERISTICS

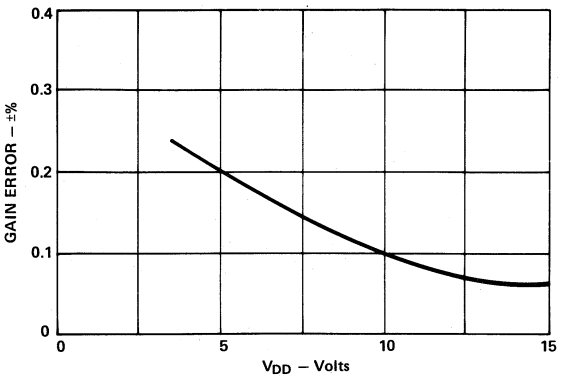


Figure 1. Gain Error vs. Supply Voltage

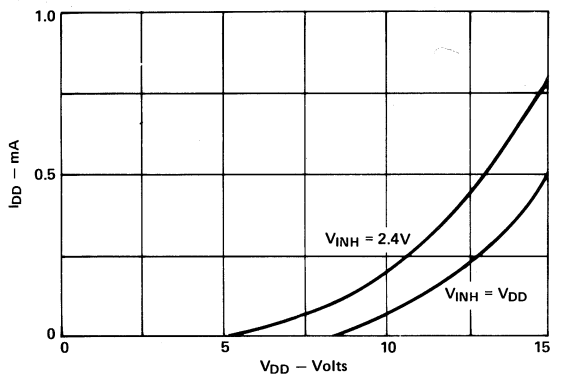


Figure 2. Supply Current vs. Supply Voltage

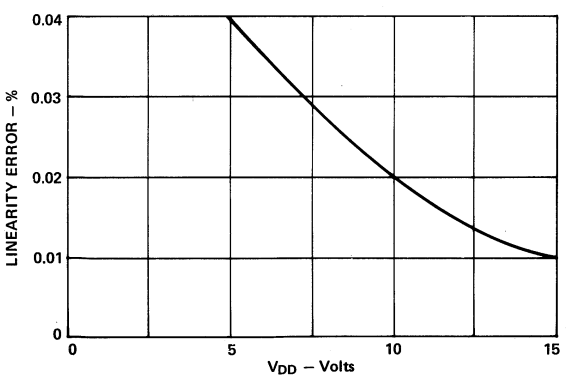


Figure 3. Linearity Error vs. Supply Voltage

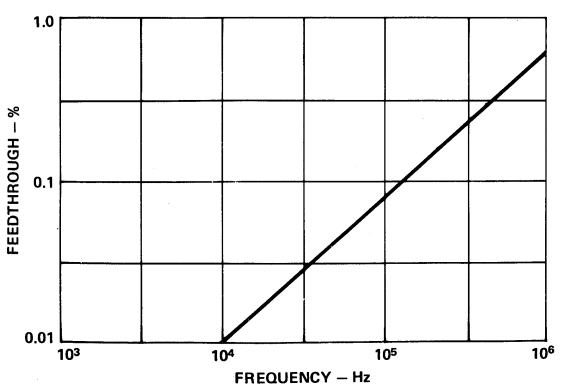


Figure 4. Feedthrough Error vs. Frequency

APPLICATION HINTS

Linearity depends upon the potential of I_{OUT1} and I_{OUT2} (pin 1 and pin 2) being exactly equal to GND (pin 3) and the output amplifiers non-inverting (+) input. Careful PC board layout and adjustment and selection of the amplifiers offset voltage and bias current is necessary.

The input structures of some high speed operational amplifiers can attempt to draw substantial current during switch-on. Schottky diodes should be used in these circumstances to prevent the absolute maximum rating for V_{OUT1} and V_{OUT2} being exceeded.

The power supply should be carefully checked for noise, which would affect performance, and overshoot which could damage the device.

Unused digital inputs must always be grounded or taken to V_{DD} to ensure correct operation. Particular care should be taken when digital inputs are routed to another PC card. It is recommended that inputs open-circuited when PC cards are disconnected be taken to V_{DD} or GND via high value (1MΩ) resistors to prevent the accumulation of static charges.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7541, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 5. An inverted R-2R ladder structure is used — that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

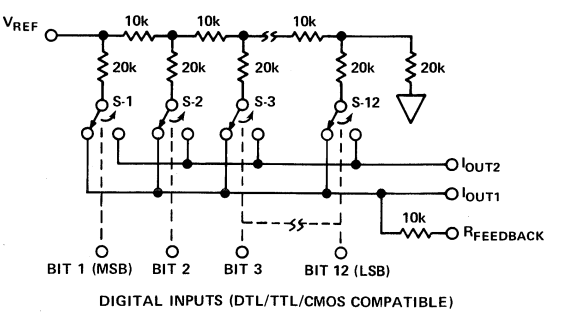


Figure 5. AD7541 Functional Diagram (Inputs "HIGH")

One of the CMOS current switches is shown in Figure 6. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the switches are binarily scaled so the voltage drop across each switch is the same. For example, switch 1 of Figure 6 was designed for an "ON" resistance of 10 ohms, switch 2 of 20 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on,

thus maintaining a constant 5mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

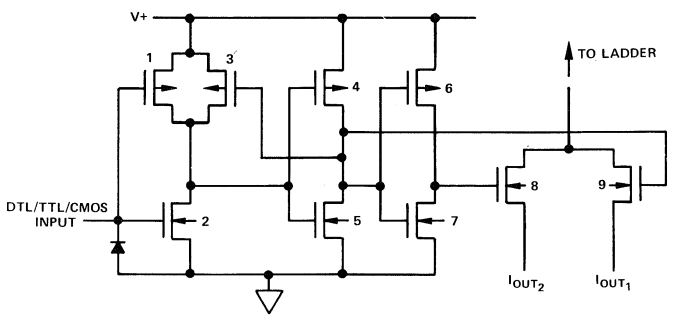


Figure 6. CMOS Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 7 and 8. In Figure 7 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the 1/4096 current source represents a constant 1-bit current drain through the

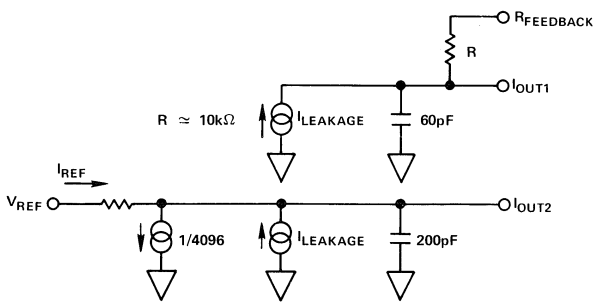


Figure 7. AD7541 Equivalent Circuit – All Digital Inputs Low

termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 200pF, as shown on the I_{OUT2} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 8, is similar to Figure 7; however, the "ON" switches are now on terminal I_{OUT1}, hence the 200pF at that terminal.

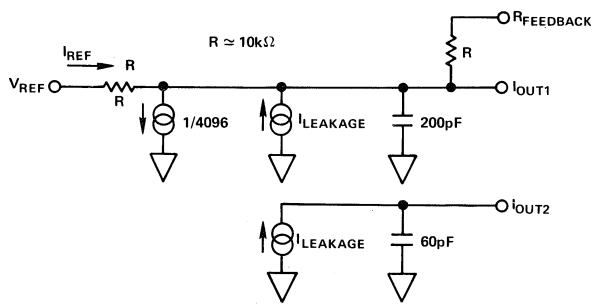


Figure 8. AD7541 Equivalent Circuit – All Digital Inputs High

DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The preceding circuit analysis shows that the output capacitance is dependent upon the digital code, as is the output resistance. Looking back into I_{OUT1} the resistance seen is anything between 10kΩ ($R_{FEEDBACK}$ alone) and 5kΩ (R_{FB} in parallel with the 10kΩ network resistance).

This variation affects both static accuracy and dynamic performance. The effect on static accuracy is further considered on the next two pages. The dynamic performance of the AD7541 will depend upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components.

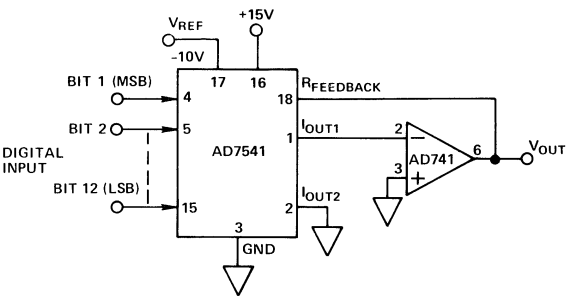


Figure 9. DAC Circuit Using AD741K

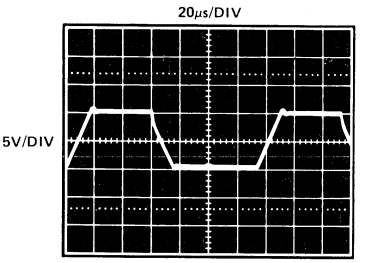


Figure 10. Output Waveform

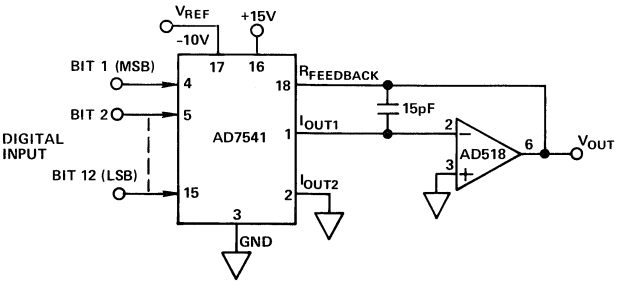


Figure 11. DAC Circuit Using AD518K

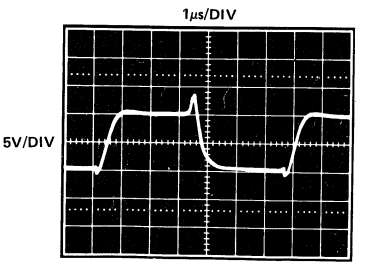


Figure 12. Output Waveform

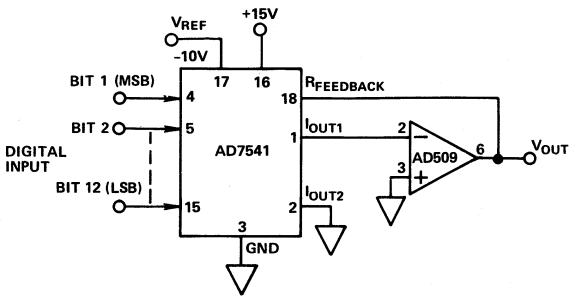


Figure 13. DAC Circuit Using AD509K

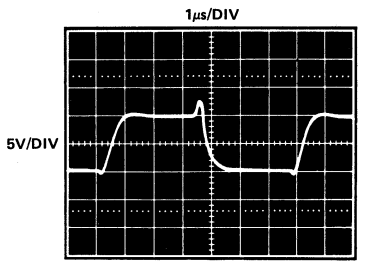


Figure 14. Output Waveform

The circuits and waveforms shown in Figures 9 to 14 are representative of the three principal types of output amplifiers. A general purpose low drift (AD741K), a high speed low cost (AD518), and a fast settling unit (AD509).

Points to remember when applying high speed amplifiers include:

1. Protection diodes as shown in Figures 15 and 16.
2. Phase compensation for the DAC's output capacitance.
3. Power supply decoupling and correct load earthing.

APPLICATIONS

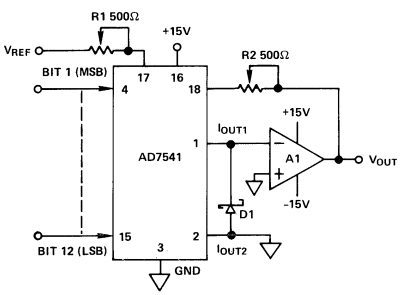


Figure 15. Unipolar Binary Operation

UNIPOLAR BINARY OPERATION

The connections required for unipolar digital binary operation are shown above. V_{REF} may be positive or negative so 2-quadrant multiplication may be performed. Schottky diode D1 (HP 5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

BIPOLAR (4-QUADRANT) BINARY OPERATION

The digital input is offset binary coded and multiplies V_{REF} according to Table 2. Resistors R1 and R2 should be equal within 0.1% at all temperatures, but need not track the resistors within the AD7541. D1 and D2 perform the same

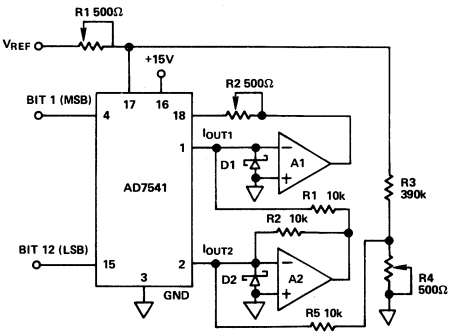


Figure 16. Bipolar (4-Quadrant) Binary Operation

function as in Figure 15. Network R3, R4, R5 sum ½LSB of current into I_{OUT2} to ensure correct coding at zero.

R1 or R2 can be adjusted to produce the outputs shown in Table 1. However, it is recommended that when the application permits it R1 and R2 be omitted. The maximum gain error in this condition is 0.3% of full scale. The offset voltage of amplifier A1 should be adjusted to less than 0.5mV over the temperature range.

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	-0.99975 V_{REF}
100000000000	-0.50000 V_{REF}
010000000000	-0.49975 V_{REF}
000000000000	0

Table 1. Code Table for Circuit of Figure 15.

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	-0.99951 V_{REF}
100000000001	-0.00049 V_{REF}
100000000000	0
010000000000	+0.50000 V_{REF}
000000000000	+1.00000 V_{REF}

Table 2. Code Table for Circuit of Figure 16.

Amplifiers A1 and A2 should be adjusted to an input offset of less than 0.1mV and should be better than 0.5mV over the temperature range. With V_{REF} set to approximately 10V, R4 should be adjusted so that with code 100000000000 V_{OUT} = 0V ±0.2mV. R1 or R2 should be adjusted so that with code 000000000000 $V_{OUT} = V_{REF}$.

As with the unipolar circuit R1 and R2 can be omitted, with a resulting maximum gain error of 0.3% of full scale. R4 may be replaced by a 100Ω fixed resistor. The maximum zero error if this is done is 0.015% of F.S.R.

OUTPUT AMPLIFIER CONSIDERATIONS

It has already been pointed out that the DAC output resistance varies with the digital code. The effect this has on static accuracy will now be considered.

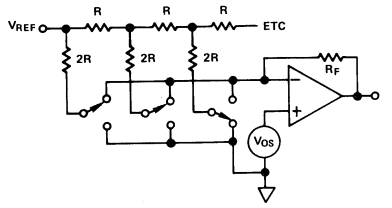


Figure 17.

The error voltage = $V_{OS}\left(1 + \frac{R_F}{R_O}\right)$

R_O is a function of the digital code.
$R_O \cong 10k\Omega$ for any more than 4-bits Logic 1.
$R_O \cong 30k\Omega$ for any single bit Logic 1.

The gain for offset, therefore, changes as follows:

At code 001111111111 $V_{ERROR1} = V_{OS}\left(1 + \frac{10k}{10k}\right) = 2\ V_{OS}$

At code 010000000000 $V_{ERROR2} = V_{OS}\left(1 + \frac{10k}{30k}\right) = \frac{4}{3}\ V_{OS}$

The error difference is therefore $\frac{2}{3}\ V_{OS}$

Since, for a 12-bit resolution DAC, one LSB has a weight (for V_{REF} = +10V) of 2.5mV, it is clearly important that V_{OS} be nulled, either using the amplifiers nulling facility or an external network.

It is important to realize that an offset can be caused by including the usual bias current compensation resistor in the amplifiers non-inverting input terminal. This should not be included. Instead the amplifier should have a bias current which is low over the temperature range of interest, and should certainly not exceed 75nA.

ANALOG/DIGITAL DIVISION

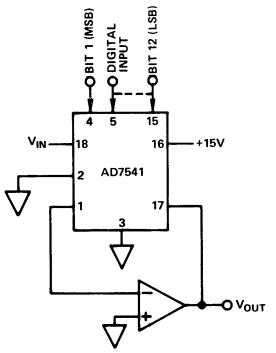


Figure 18. Analog/Digital Divider

With the AD7541 connected in its normal multiplying configuration as shown in Figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots\ldots \frac{A_{12}}{A^{12}}\right)$$

where the coefficients A_X assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 18, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots\ldots \frac{A_{12}}{A^{12}}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero is not defined. With the LSB (Bit 12) ON, the gain is 4096. With all bits ON, the gain is 1 (±1LSB).

DIGITAL/SYNCHRO CONVERTER

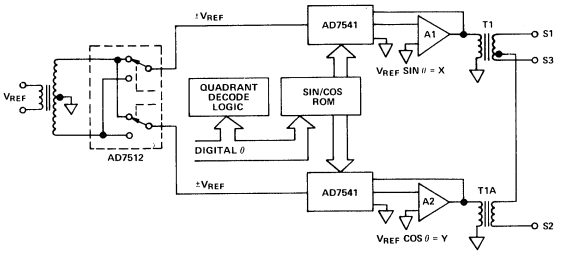


Figure 19. 14-Bit Digital to Synchro Converter

The low cost and high accuracy available from the AD7541, together with its bipolar multiplying capability is exploited fully in the circuit of Figure 19. V_{REF} is commonly 400Hz but by replacing the transformers with dc coupled circuits coordinate transformation may be performed.

The SIN/COS ROM is readily available at low cost and the AD7512 switch enables greater resolution to be obtained.

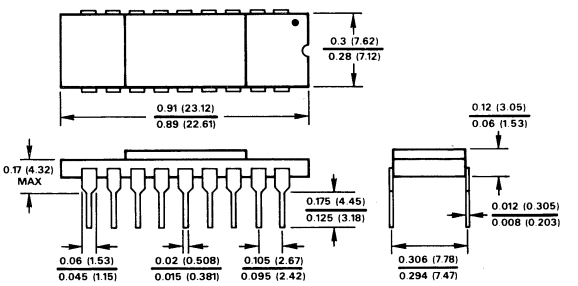
Resolver-to-synchro transformation is performed by the Scott connected pair T1 and T1A. The power available to the load connected to S1, S2 and S3 is determined by the amplifiers A1 and A2. A particular advantage of the circuit shown in Figure 19 is that it is invariant with respect to θ, and may be used to directly drive equipment such as CRT displays.

MECHANICAL INFORMATION

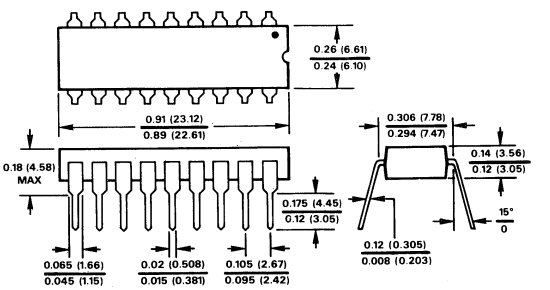
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

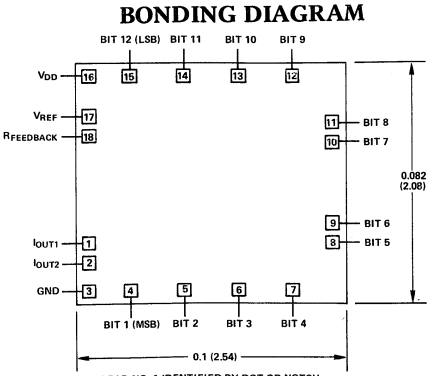
18 PIN CERAMIC DIP



18 PIN PLASTIC DIP



BONDING DIAGRAM



Low Cost Multipurpose Digital-to-Analog Converter

DAC1009

FEATURES
12 Bit Resolution
Positive True Logic Inputs
Fixed Reference or Multiplying Operation
TTL/DTL or CMOS Compatible
Current or Voltage Output
User Selected Output Ranges
Small Size – 2" x 2" x 0.4" (51 x 51 x 10mm)

GENERAL DESCRIPTION

The DAC1009 is a low cost, multipurpose digital-to-analog converter which can be readily adapted to a variety of applications. This versatile 12 bit device can be programmed for fixed reference or multiplying operation and for current or voltage output. It will interface with CMOS or DTL/TTL logic systems and it features convenient positive-true logic inputs. Performance specifications include ±½LSB linearity error, 4μsec settling time for a 10V output step, and a gain temperature coefficient of 11ppm/°C.

OUTPUT VERSATILITY

The DAC1009 can be used in either the voltage output or current output mode. When it is used as a voltage output device, any one of the five following output ranges are available:

Unipolar	0 to -5V, 0 to -10V
Bipolar	±2.5V, ±5V, ±10V

External jumpers at the module pins determine the output amplifier feedback resistance. Offset of exactly one-half full scale for bipolar applications is provided by connecting a jumper between an internal reference source and the summing junction of the output amplifier.

As a current output device the DAC1009 can be used to drive an external op amp. Internal feedback resistors can also be used with this external op amp to assure optimum temperature tracking of components.

DIGITAL INPUTS

The DAC1009 uses the positive-true logic convention preferred by many system designers (i.e., 111...1 digital input results in the maximum absolute value analog output). The logic levels of:

$+2.0V \leqslant \text{Logic "1"} \leqslant +15V$
$0V \leqslant \text{Logic "0"} \leqslant +0.8V$

are compatible with both DTL/TTL and CMOS systems. When used with CMOS logic, the driving gate for each input bit must be capable of sinking at least 1mA.

For unipolar outputs either Binary or BCD code may be used; for bipolar outputs Offset Binary code is available.

MULTIPLYING CAPABILITY

The DAC1009 can be readily configured as either a one or two-quadrant multiplying DAC. When used in this manner the one-quadrant analog input of 0 to -1mA is attenuated by an amount corresponding to the one-quadrant (unipolar) or two-quadrant (bipolar) digital input signal. By appropriate choice of the input resistor value, any input voltage range may be used. The following sections of this data sheet should be consulted to determine whether the multiplying characteristics of this device make it suitable for a given application.

SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

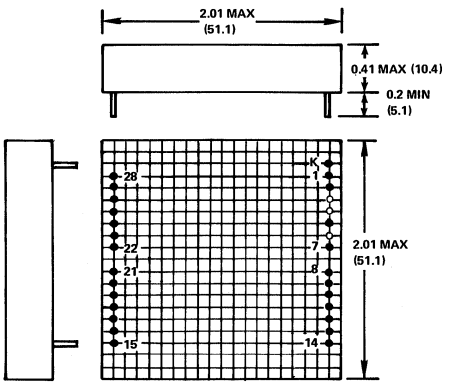
	Voltage Output	Current Output
RESOLUTION		
Binary	12 Bits	*
BCD	3 Digits	*
DIGITAL INPUTS[1]	TTL Compatible	*
0V ≤ Logic "0" ≤ +0.8V	@ -1mA	*
+2V ≤ Logic "1" ≤ +15V	@ +40μA	*
INPUT CODES		
Unipolar	Binary, BCD	*
Bipolar	Offset Binary	*
OUTPUT RANGES		
(User Programmable)	0 to -5V @ 10mA	0 to +2mA
	0 to -10V @ 5mA	
	±2.5V, ±5V @ 10mA	±1mA
	±10V @ 5mA	
Voltage Compliance	—	±400mV
OUTPUT IMPEDANCE	0.02Ω	6.9kΩ
SETTLING TIME[2]	4μs (7μs max)	700ns (1.5μs max)
LINEARITY ERROR	±½LSB max	*
TEMPERATURE COEFFICIENT		
Gain	±11ppm/°C (±40ppm/°C max)	*
Zero		
Unipolar	±12μV/°C (±50μV/°C max)[3]	±1nA/°C max[4]
Bipolar	±50μV/°C (±130μV/°C max)[5]	±7nA/°C (±60nA/°C max)
Differential Linearity Error	±4ppm/°C (±10ppm/°C max)	*
TEMPERATURE RANGE		
Operating	0 to +70°C	*
Storage	-25°C to +85°C	*
POWER REQUIREMENTS	+15V ±5% @ 17mA	*
	-15V ±5% @ 18mA	*
POWER SUPPLY SENSITIVITY[6]		
Gain	0.1ppm/%ΔV_S	*
Zero	1ppm/%ΔV_S	*
ADJUSTMENT RANGE		
Gain	±0.4% of F.S.	*
Zero	±14LSB	*

*Specification is same as for Voltage Output Mode.
[1] Open input equivalent to Logic "1".
[2] To ±0.01% accuracy for a full scale output step.
[3] For the 0 to -10V range.
[4] Doubles every 10°C.
[5] For the ±5V range.
[6] For the ±15V supplies only, with +15V and -15V supplies tracking.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

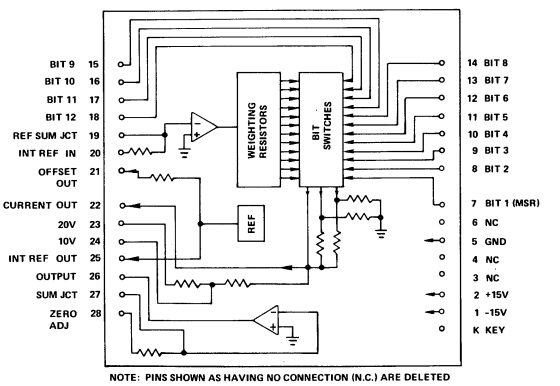
Dimensions shown in inches and (mm).



NOTE:

Terminal pins installed only in shaded hole locations.
Module weight: 1.6 ounces (45 grams)
All pins are gold plated half-hard brass (MIL-G-45204B), 0.019" ±0.001" (0.48 ±0.025mm) diameter.
For plug-in mounting card, order Board No. AC6160

BLOCK DIAGRAM AND PIN DESIGNATIONS



NOTE: PINS SHOWN AS HAVING NO CONNECTION (N.C.) ARE DELETED

ORDERING GUIDE:

DAC1009 /XXX

- BIN
- BCD

DIGITAL INPUT DATA

The DAC1009 is fully DTL/TTL compatible with each input bit representing one standard TTL load. The required logic levels of:

+2.0V ≤ Logic "1" ≤ +15V

0V ≤ Logic "0" ≤ +0.8V

are also compatible with CMOS logic systems. When driving the DAC1009 with a CMOS gate, standard CMOS/TTL interface rules must be observed to assure that the CMOS gate will adequately sink at least 1mA.

Binary or BCD code can be used for unipolar output; Offset Binary code is used for bipolar output. The following table illustrates the analog outputs associated with various digital input codes for fixed reference operation.

Digital Input	Nominal Analog Output	
	Voltage Output*	Current Output
Binary (12Bits)		
Unipolar		
111111111111	-9.9976V	+1.9995mA
000000000000	0	0
Bipolar		
111111111111	-9.9951V	+0.9995mA
100000000000	0	0
000000000000	+10V	-1.000mA
BCD (3 digits)		
Unipolar		
1001 1001 1001	-9.9900V	+1.2488mA
0000 0000 0000	0	0

*Voltages shown are for the 0 to -10V and ±10V ranges; outputs are proportionately smaller for other ranges.

VOLTAGE OUTPUT RANGE SELECTION

The following simplified schematic (Figure 1) represents the DAC1009 output circuit.

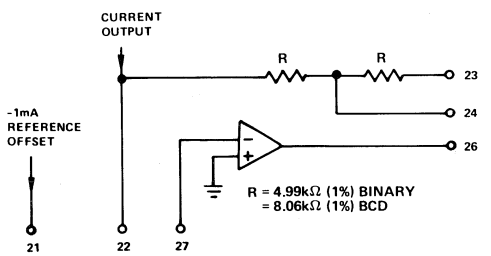


Figure 1. Simplified Output Circuit

The output voltage range is determined by the amount of feedback resistance used with the internal op amp. By connecting external jumpers between module pins, three feedback resistance values can be obtained.

A -1mA current must be applied to the internal op amp's summing junction to produce the half scale offset necessary for bipolar output. The OFFSET OUTPUT (pin 21), derived from the module's internal reference source, provides this current.

The following table shows the external connections used to program the various output ranges.

Output Range	Pins Jumpered Together		
±2.5V	27, 22, 21, 23	26, 24	
±5.0V	27, 22, 21	26, 24	
±10V	27, 22, 21	26, 23	
0 to -5V	27, 22, 23	26, 24	21, 5
0 to -10V	27, 22	26, 24	21, 5

CURRENT OUTPUT APPLICATIONS

The CURRENT OUTPUT terminal (pin 22) provides an output of 0 to +2mA for unipolar operation. When the OFFSET OUTPUT of pin 21 is connected to it, a ±1mA bipolar output results. Because of the ±400mV compliance of the CURRENT OUTPUT terminal, only an external inverting op amp should be used to transform the current output to a voltage output. The proper connection of such an op amp is shown below in Figure 2.

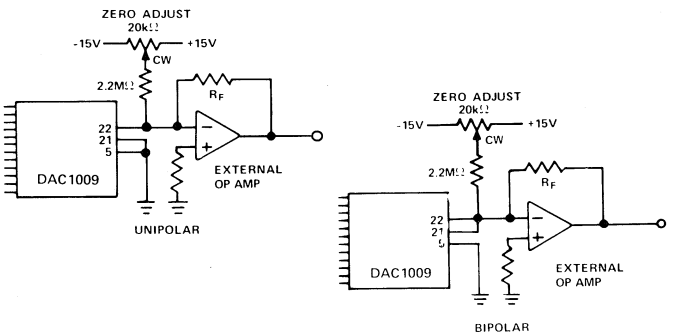


Figure 2. Connection of an External Op Amp (With External Feedback Resistor)

The feedback resistors which are normally used with the internal op amp can also be used with external op amps to provide optimum temperature tracking of the critical gain determining components. The arrangement of these resistors and their connections to the external op amp are shown below in Figure 3.

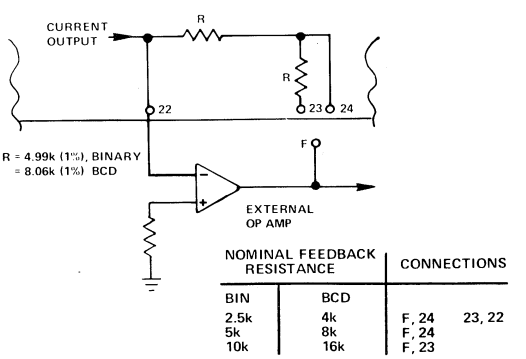


Figure 3. Connection of External Op Amp to Internal Feedback Resistors

In order to prevent the introduction of noise, the lead from the CURRENT OUTPUT terminal to the external op amp summing junction should be made with shielded cable and should be kept as short as possible.

FIXED REFERENCE OPERATION

Each module contains a precision -6.2V (nominal) reference source, the output of which is available at pin 25. When the

converter is used in the fixed reference mode, this output is connected via a 50Ω trim pot (supplied by the user) to the reference input terminal (pin 20) as shown in Figure 4.

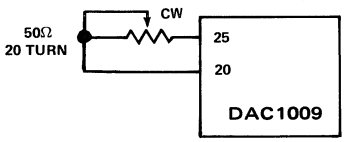


Figure 4. Reference Connection

Since the value of the reference input current ultimately determines the magnitude of the converter's analog output, this trim pot is used to make gain adjustments. An external reference source capable of supplying -6.2 volts at -1mA may be used in place of the internal reference.

MULTIPLYING OPERATION

When used as a multiplying DAC, the fixed reference input is replaced by a signal which can vary in amplitude from 0 to -1mA. The converter's output will then represent the product of the digital and analog inputs. The use of a unipolar input code produces one quadrant multiplication; a bipolar code produces two quadrant multiplication. As a multiplier, the DAC1009 has a small signal bandwidth of 950kHz, a full power bandwidth of 125kHz and a half power bandwidth of 750kHz. With proper external circuitry, maximum feedthrough is less than 1LSB at 50kHz.

The following simplified schematic (Figure 5) represents the analog input circuit configuration.

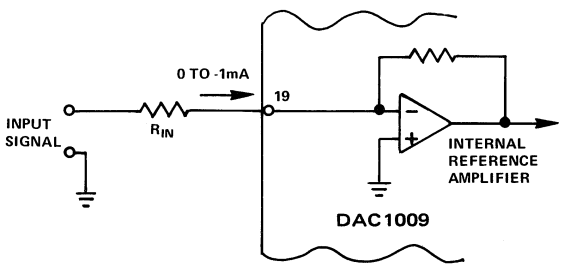


Figure 5. Analog Input Circuit

Pin 19 which is connected to the reference amplifier's summing junction is essentially at ground potential. The input resistance necessary to yield -1mA with the peak input voltage applied can, therefore, be readily calculated. Due to minor variations between units, an initial adjustment of up to ±2% in the value of the input resistor may be necessary to produce the proper overall gain.

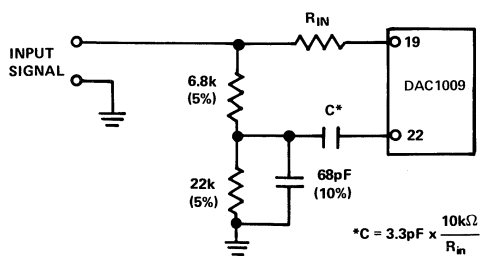


Figure 6. Feedthrough Reduction Circuit

The feedthrough characteristics of the DAC1009 can be greatly enhanced by the addition of the simple external circuit shown in Figure 6.

With this circuit, feedthrough is reduced by a factor of approximately 10:1. The following table lists typical values of feedthrough for a -1mA sine wave input and a digital input code of 000. . .00 for the 0 to -10V output range.

	Feedthrough (mV)	
Input Frequency	w/Circuit	w/o Circuit
10kHz	1.6	6
50kHz	2.0	24
100kHz	4.0	44

With full scale (-1mA) reference applied, each DAC1009 is carefully trimmed to eliminate minor errors in the weighting of individual bits. These errors tend to reappear when the reference level decreases as it does during multiplying operation. The overall effect of these errors is a function of reference input level as shown in Figure 7.

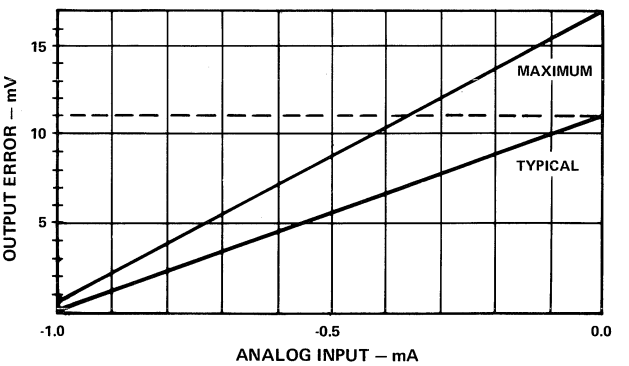


Figure 7. Output Error vs. Analog Input

Maximum linearity is achieved when the analog input signal remains close to full scale.

GAIN AND ZERO ADJUSTMENT

The proper connections of the user-supplied gain and zero adjustment potentiometers are shown below in Figure 8 for fixed reference voltage output operation. For current output operation, the wiper of the zero adjustment potentiometer should be connected via a 2.2MΩ resistor to pin 22 instead of directly to pin 28 as shown in Figure 2.

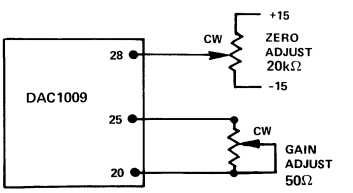


Figure 8. Gain and Zero Adjustments

With a digital code of 000. . .00 applied, adjust the zero pot until the analog output is zero ±1/10LSB for unipolar units or $+V_{FS}$ ±1/10LSB for bipolar units. With a full scale digital code of 111. . .11 (binary) or 1001 1001 1001 (BCD) applied, adjust the gain pot until the analog output is within ±1/10LSB of Full Scale less 1LSB.

High Speed Digital to Analog Converters

DAC1106/DAC1108

FEATURES

High Speed
- **8 Bits in 25ns**
- **10 Bits in 50ns**
- **12 Bits in 60ns**

Adjustment Free Operation
Gain TC: ±10ppm/°C
Linearity Error: ±½LSB max
Small Size: 2" x 2" x 0.4" Module

GENERAL DESCRIPTION

The DAC1108 is a high speed, current output digital-to-analog converter with 12-bit resolution and accuracy. The very fast settling times to 0.05% accuracy of 60ns and to 0.01% accuracy of 150ns make it ideal for use in high speed applications such as computer driven displays, automatic test equipment, and function generators. In addition to the ±½LSB maximum linearity error, the DAC1108 features temperature coefficients of 30ppm/°C for gain and 8ppm/°C for linearity.

The DAC1106 is also a high speed, current output digital-to-analog converter which is available in both eight and ten bit versions. The very fast settling times to ½LSB or 25ns (8 bit models) and 50ns (10 bit models). Accuracy specifications include ±½LSB linearity, 10ppm/°C temperature coefficient, and 0.002%/V power supply rejection.

Everything needed to perform high speed conversions is contained in the compact 2" x 2" x 0.4" package of the DAC1106/1108. Included are a precision temperature compensated reference source, high speed current switches and a carefully trimmed network of weighting resistors. Because of the inherent stability and careful factory adjustment of this device, no external zero or gain adjustment potentiometers are required.

The digital inputs of the DAC1106/1108 are fully DTL/TTL compatible. Binary code is used for unipolar operation and Offset Binary code is used for bipolar operation. The current output of this device can be applied directly to an external resistor to develop a voltage output or it can be applied to the input of a fast settling op amp if amplification or impedance transformation is desired.

INPUT CONSIDERATIONS

The binary weighted current sources which form the basis of the digital to analog conversion process are directly switched by their associated input bits. A change in the converter's current output will begin to occur approximately 10nsec after a new digital word is applied. Because of this extremely fast response, time skew in the digital input can result in momentary erroneous outputs or "glitches". Consider, for example, the case of a transition from 1000 . . . 0 to 0111 . . . 1, a step of only one LSB. If the MSB turns to a "0" before the rest of the bits have turned to "1"s, the input will momentarily be 0000 . . . 0 and the converter will start to respond accordingly as shown below in Figure 1.

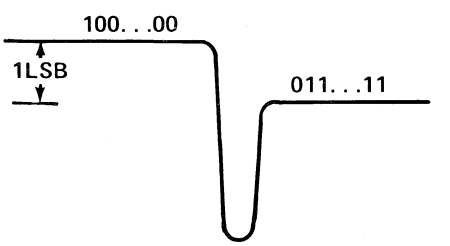


Figure 1. Switching Transient Caused by Time Skew

These switching transients will be minimized if the digital input data time skew is held to less than 5ns.

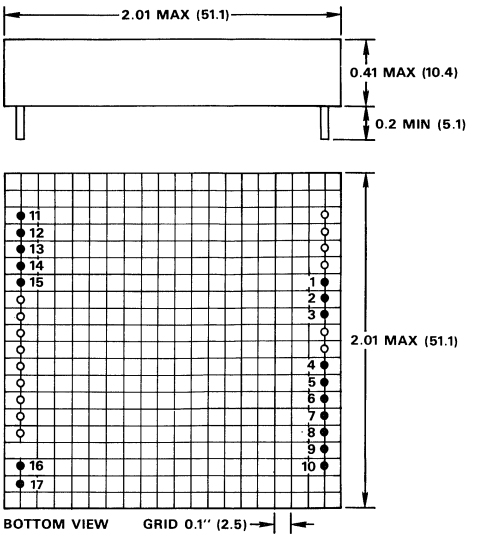
SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

MODELS	DAC1106	DAC1108
RESOLUTION	8/10 Bits	12 Bits
DIGITAL INPUTS	TTL Compatible	*
0V ≤ Logic "0" ≤ 0.8V	@ -3.2mA (max)	*
+2V ≤ Logic "1" ≤ 15V	@ 80μA (max)	*
INPUT CODES		
Unipolar	Binary	*
Bipolar	Offset Binary	*
OUTPUT RANGES	0 to +5mA	*
	-2.5 to +2.5mA	*
OUTPUT IMPEDANCE	600Ω ±1% (Unipolar)	510Ω ±2%
OUTPUT VOLTAGE COMPLIANCE	±1.2V	*[1]
ABSOLUTE ACCURACY		
Full Scale	±0.1%	*
Offset	±2mA	*
SETTLING TIME		
To 0.2%	25ns (30 max)	
To 0.1%	40ns (50 max)	
To 0.05%	50ns (60 max)	60ns
To 0.01%		150ns
LINEARITY ERROR	±½LSB max	*
TEMPERATURE COEFFICIENT		
Gain	±10ppm/°C	±30ppm/°C
Zero	±75μV/°C	*
Linearity	±8ppm/°C	*
TEMPERATURE RANGE		
Operating	0 to +70°C	*
Storage	-55°C to +85°C	-55°C to +125°C
POWER REQUIREMENTS		
+15V ±5%	47mA max	42mA max
-15V ±5%	37mA max	10mA max
POWER SUPPLY SENSITIVITY		
Gain	0.002%/V	0.01%/%ΔV
OUTLINE DIMENSIONS	2" x 2" x 0.4"	*

[1] ±1V for rated dynamic performance.
*Specifications same as DAC1106.
Specifications subject to change without notice.

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).



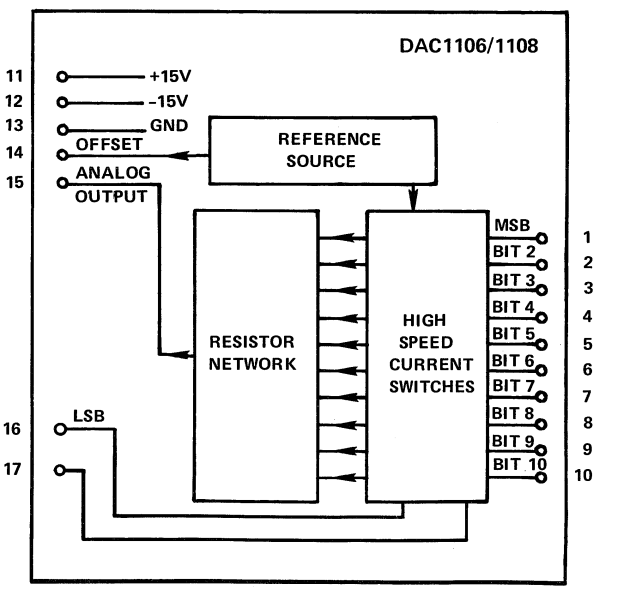
NOTE:
Terminal pins installed only in shaded hole locations.
Module weight: 2 ounces (57 grams).
All pins are gold plated half-hard brass, (MIL-G-45 204), 0.019 ±0.001 (0.48 ±0.03) dia.
Pins 9 and 10 included on 10 bit models only.
For plug-in mounting card order Board No. AC4102

ORDERING GUIDE:

Model DAC1106/XXX

- 001 (EIGHT BIT)
- 002 (TEN BIT)

BLOCK DIAGRAM AND PIN DESIGNATIONS



NOTE:
DAC1106 PIN 16 - N.C.
PIN 17 DELETED

DIGITAL INPUTS

The DAC1106/1108 is fully TTL/DTL compatible with each input bit representing two standard TTL Loads. The logic levels of

$$0V \leqslant \text{Logic "0"} \leqslant 0.8V$$
$$+2V \leqslant \text{Logic "1"} \leqslant 15V \text{ (Absolute Max)}$$

are also compatible with CMOS logic systems. When using this device in a CMOS system, standard CMOS/TTL interface rules must be observed to insure that the driving gate is capable of sinking at least 3.2mA.

The simple addition of an external inverter ahead of the MSB input terminal, as shown below in Figure 2, allows the bipolar Two's Complement code to be used.

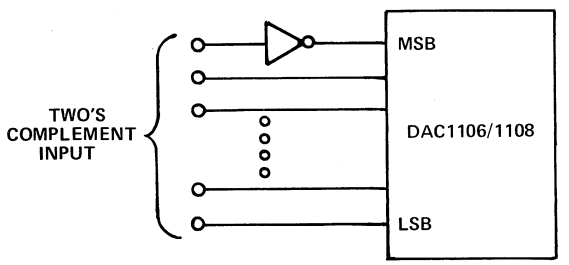


Figure 2. Two's Complement Input Connection

OUTPUT CHARACTERISTICS

The output of the DAC1106/1108 represents the sum of the currents produced by the individual binary-weighted current sources in response to the digital input word. This current varies from 0 to +5mA. In order to produce the half scale offset needed for bipolar outputs, a current of exactly -2.5mA must be added to the output. Such a current is generated internally and is available at pin 14. The analog outputs which are produced by various digital inputs are shown in the following tables.

UNIPOLAR

Digital Input	Analog Output		
	1106-001	1106-002	1108
111 111	+4.981mA	+4.995mA	+4.999mA
100 000	+2.500mA	*	*
000 001	+19.5μA	+4.88μA	+1.22μA
000 000	0mA	*	*

BIPOLAR

Digital Input	Analog Output		
	1106-001	1106-002	1108
111 111	+2.481mA	+2.495mA	+2.499mA
100 000	0mA	*	*
000 000	-2.500mA	*	*

Figures 3 and 4 illustrate the converter's output impedance characteristics for unipolar and bipolar operation.

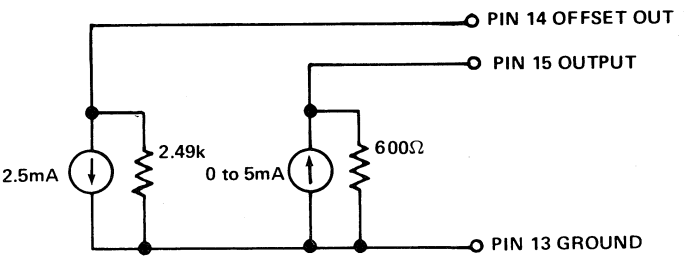


Figure 3. Equivalent Circuit DAC (Unipolar)

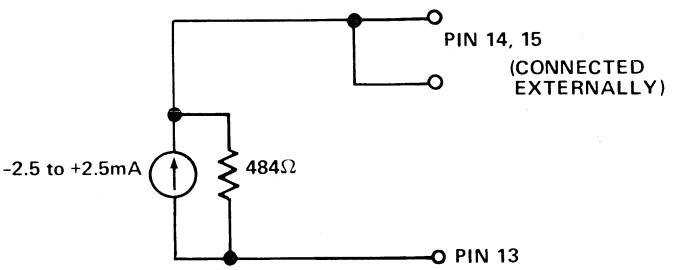


Figure 4. Equivalent Circuit DAC (Bipolar)

OUTPUT CONNECTIONS

The circuits used to develop an output voltage across a resistor are shown below in Figures 5 and 6 for unipolar and bipolar operation.

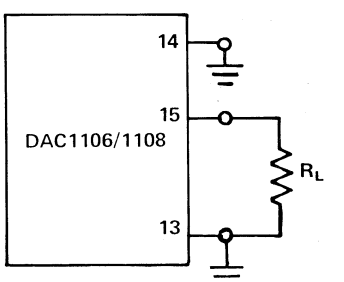


Figure 5. Voltage Output with Load Resistor (Unipolar)

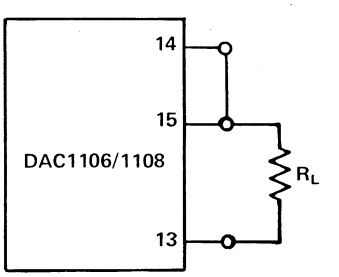


Figure 6. Voltage Output with Load Resistor (Bipolar)

In both cases, the output voltage is limited to ±1.2V max. By referring to Figures 3 and 4, the user can readily compute the value of R_L needed to produce the desired full scale voltage. For example, a 300Ω resistor will develop a 0 to +1V F.S. unipolar output and a 2.325kΩ resistor will develop a +1V F.S. bipolar output.

The DAC1106/1108 may be used in conjunction with a high speed external op amp when outputs greater than ±1.2V and 5mA are needed. Because current output converters such as the DAC1106/1108 are not ideal current sources, the op amp does not operate in a unity gain configuration. Figure 7 below shows, in simplified form, a unipolar DAC driving an op amp.

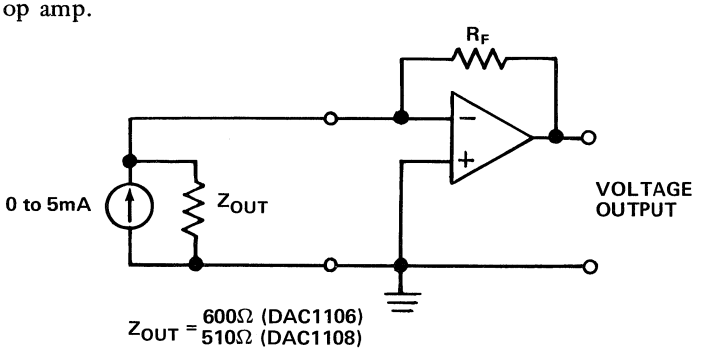


Figure 7. Voltage Output with an Op Amp Simplified Diagram

Because of the output impedance, the closed loop gain becomes $1 + R_F/Z_{OUT}$ instead of 1. For example with an R_F of 2kΩ the closed loop gain is 4.33 for DAC1106 and 4.92 for DAC1108.

This can complicate the job of selecting a suitable op amp since most manufacturers specify settling time at unity gain. One extremely fast op amp that performs as well at gains of 2 to 6 as it does at unity gain is the Analog Devices' model 50 differential input, FET amplifier. The model 50 will settle to ten-bit accuracy (0.05%) in a maximum of 200ns. The high current output of this device (100mA) also makes it ideal for use with the DAC1108 in CRT deflection applications.

Sometimes space or budgetary considerations dictate that an IC rather than a modular op amp be used. In these cases the AD509K fast settling IC op amp is recommended. The AD509K maintains its guaranteed maximum settling time specification (500ns to 0.1%) even at the closed loop gains encountered with the DAC1106/1108. Furthermore, when the closed loop gain is greater than 3, no external compensating components are required.

Figures 8 and 9 below show the proper means of connecting the converter to an op amp for unipolar and bipolar operation.

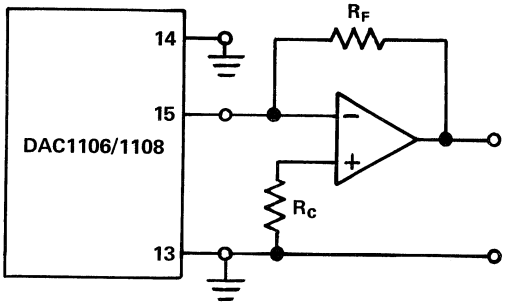


Figure 8. Connections to an External Op Amp (Unipolar)

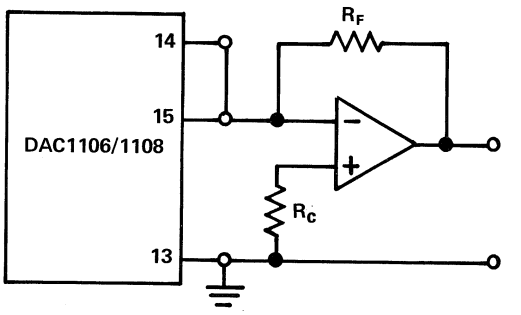


Figure 9. Connections to an External Op Amp (Bipolar)

The resistor R_C is used with the AD509K for bias current compensation. Because of the low bias currents inherent with the model 50, R_C is unnecessary and the noninverting input is connected directly to ground.

Great care must be taken in laying out the circuits of Figures 8 and 9 to assure true high speed performance. Several of the most important considerations are listed below:

1. Keep leads, especially those between the converter output and op amp summing junction, as short as possible to prevent the introduction of noise.
2. Orient components to minimize stray capacitance.
3. Carefully bypass power supplies to the op amp.
4. Select suitable components such as metal film resistors with their low capacitance and low stray inductance.
5. Design the signal and power supply ground circuits so as to prevent the introduction of extraneous voltages in ground signal path.
6. Use separate returns for analog and digital grounds. The DAC1106/1108 and op amp power supply returns go to analog ground; any logic circuits that precede the converter go to digital ground.

Low Cost General Purpose Digital-to-Analog Converter

DAC1118

FEATURES
12 Bit Resolution
Input Register Included
Choice of Codes
Programmable Output Ranges
Low Profile 2" x 4" x 0.4" Module

GENERAL DESCRIPTION

The DAC1118 is a 12 bit, general purpose digital-to-analog converter which comes complete with an input storage register and a versatile output amplifier. This low profile 2" x 4" x 0.4" module has been designed to provide economical solutions to a wide range of digital-to-analog conversion problems. Performance specifications include 5μs settling time to 0.01%, ±20ppm/°C gain temperature coefficient, and ±½LSB linearity error.

The design of the DAC1118 centers around the AD550 monolithic quad current switches and a hybrid resistor assembly consisting of matched precision resistors and a thick film network. The resistor assembly which contains all of the critical gain determining resistors and the quad switches with their inherent temperature tracking provide the DAC1118 with excellent performance over temperature.

The fully DTL/TTL compatible DAC1118 can be provided with a variety of input codes. In addition, any one of five voltage output ranges can be programmed by means of external jumpers connected to the module's terminal pins.

DIGITAL INPUT CHARACTERISTICS

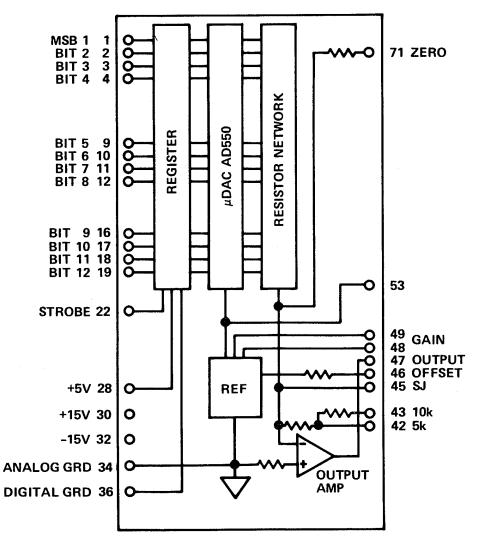
The TTL/DTL compatible storage register contained within the DAC1118 is configured during production to accept either Binary (including Offset Binary), Two's Complement, or BCD code. Digital data appearing at the converter's 12 input terminals will be strobed into the register whenever a positive-going transition is applied to the STROBE input (pin 22).

With the STROBE input held at either Logic "0" or Logic "1", the input data may be changed without affecting either the contents of the register or the output of the converter. The transfer characteristics of the DAC1118 are such that a full scale digital input (such as 1111..11 for Binary coded units) will result in a positive full scale voltage output.

OUTPUT CHARACTERISTICS

The 12 binary-weighted current sources which form the basis of the digital-to-analog conversion process are directly controlled by the digital data stored in the input register. The combined output of these sources is applied to the internal op amp summing junction to produce a voltage output signal. By connecting jumpers between the proper module pins, various values of op amp feedback resistance and thus, output voltage ranges can be selected.

In order to produce bipolar outputs, the current input to the internal op amp is offset by ½ Full Scale. This offset current is generated by the precision internal reference source and is applied to the op amp summing junction by means of jumpers connected to appropriate module terminals.



DAC1118 Block Diagram

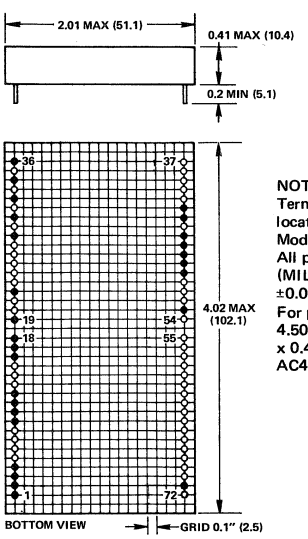
SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise specified)

RESOLUTION	12 Bits
DIGITAL INPUTS	
Logic Levels	0V ≤ Logic "0" ≤ 0.8V +2V ≤ Logic "1" ≤ +5V
Data Input Load	1 Standard TTL Load/Bit
Strobe Input Load	3 Standard TTL Loads
Strobe Pulse Width	20ns (min)
Data Set-Up Time	20ns (min)
Data Hold Time	5ns (min)
INPUT CODES	
Unipolar	Binary, BCD
Bipolar	Offset Binary, 2's Complement
OUTPUT RANGES	0 to +5V @ 10mA 0 to +10V @ 5mA ±2.5V @ 10mA ±5V @ 10mA ±10V @ 5mA
OUTPUT IMPEDANCE	0.02Ω
SETTLING TIME	5μs to 0.01%[1]
Slewing Rate	20V/μs
LINEARITY ERROR	±½LSB (Max)
TEMPERATURE COEFFICIENT	
Gain	±20ppm/°C (±30ppm/°C max)
Zero	
Unipolar	±30μV/°C (±50μV/°C max)
Bipolar	±100μV/°C (±130μV/°C max)
Differential Linearity	±2ppm/°C (±10ppm/°C max)
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +100°C
POWER REQUIREMENTS	+15V ±5% @ 20mA (25mA max) -15V ±5% @ 30mA (45mA max) +5V ±10% @ 125mA (171mA max)
POWER SUPPLY SENSITIVITY[2]	
Gain	±20ppm/%ΔV_S of Reading[3]
Zero	±5ppm/%ΔV_S of Range[4]
ADJUSTMENTS	
(User Provided)	
Gain (100Ω, 20 Turn Pot)	±0.2% of Range
Zero (20kΩ, 20 Turn Pot)	±0.3% of Range

[1] For 10V step.
[2] For ±15V supplies only with +15V and -15V supplies tracking.
[3] Reading for bipolar input is defined as | Actual Reading - (- F.S.) |.
[4] Range for unipolar operation ≡ + F.S.; Range for bipolar operation ≡ 2 (+ F.S.).
Specifications subject to change without notice.

OUTLINE DIMENSIONS

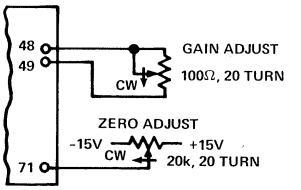
Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
Module weight: 3.5 ounces (99.3 grams)
All pins are gold plated half-hard brass, (MIL-G-45204), 0.019" ±0.001" (0.48 ±0.03mm) dia.
For plug-in mounting card and connector 4.500" (114.30mm) x 3.750" (95.25mm) x 0.410" (10.41mm) order Board No. AC4494

GAIN AND ZERO ADJUSTMENT

For units utilizing bipolar codes apply the digital input corresponding to the negative full scale analog output and adjust the zero pot until the value listed is obtained with ±1/10LSB. For Unipolar codes apply 00 . . . 0 and adjust for 0V out.



Gain and Zero Pot Connections

For all units, once the appropriate zero adjustment has been made apply the digital input corresponding to the positive full scale analog output. Adjust the gain pot until the value listed is obtained within ±1/10LSB.

OUTPUT CONNECTIONS

OUTPUT RANGE	PINS JUMPERED TOGETHER			
	Bipolar Offset		Feedback Resistance	
	Binary	BCD	Binary	BCD
±2.5V	45, 46		47, 42 43, 45	
±5.0V	45, 46		47, 42	
±10V	45, 46		47, 43	
0 to +5V	46, 34	46, 34	47, 42 43, 45	47, 42
0 to +10V	46, 34	46, 34	47, 42	47, 43

INPUT-OUTPUT RELATIONSHIPS

DIGITAL INPUT	NOMINAL VOLTAGE OUTPUT	
	0 to +5V Range	0 to +10V Range
Binary Code		
111111111111	+4.9988V	+9.9976V
000000000001	+0.0012V	+0.0024V
000000000000	0.0000V	0.0000V
BCD Code		
1001 1001 1001	+4.9950V	+9.9900V
0000 0000 0001	+0.0050V	+0.0100V
0000 0000 0000	0.0000V	0.0000V

Unipolar Output

DIGITAL INPUT	NOMINAL VOLTAGE OUTPUT		
	±2.5V Range	±5V Range	±10V Range
Two's Complement Code			
011111111111	+2.4988V	+4.9976V	+9.9951V
000000000001	+0.0012V	+0.0024V	+0.0048V
000000000000	0.0000V	0.0000V	0.0000V
100000000000	-2.5000V	-5.0000V	-10.0000V
Offset Binary Code			
111111111111	+2.4988V	+4.9976V	+9.9951V
100000000001	0.0012V	0.0024V	0.0048V
100000000000	0.0000V	0.0000V	0.0000V
000000000000	-2.5000V	-5.0000V	-10.0000V

Bipolar Output

ORDERING GUIDE:

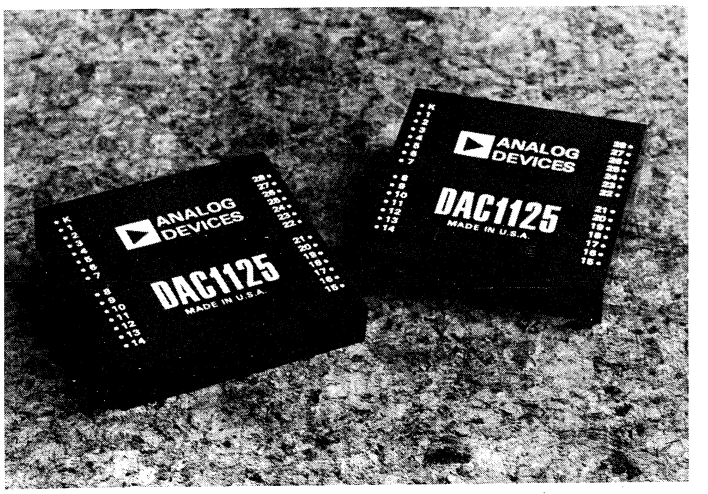
DAC1118 - XXX

- 023 (Binary, Offset Binary)
- 025 (BCD)
- 044 (2's Complement)

Low Feedthrough, 12 Bit, Multiplying D/A Converter

DAC1125

FEATURES
- **12 Bit Resolution and Accuracy**
- **Two Quadrant or Four Quadrant Operation**
- **Four Quadrant Feedthrough <½LSB to 40kHz**
- **3μs Settling Time**
- **3ppm/°C Gain TC**
- **Excellent Dynamics; <0.5° Input-Output Phase Shift @ 5kHz**



GENERAL DESCRIPTION

The DAC1125 is a 12-bit multiplying digital-to-analog converter. As shown in Figure 1, it functions essentially as a multiplier whose output voltage represents the product of a bipolar analog input voltage and a digitally programmed bipolar constant. This constant can be varied in 4,096 steps from -1 to 0 (Two Quadrant operation), or from -1 to +1 (Four Quadrant operation).

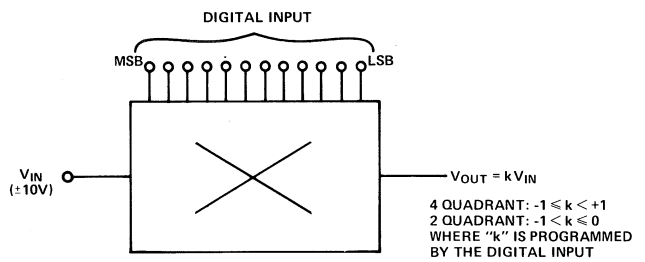


Figure 1. DAC1125 Functional Diagram

One of the primary features of the DAC1125 is its exceptionally low Four Quadrant Zero feedthrough. Analog input signals with frequencies of up to 40kHz produce a feedthrough which is guaranteed to be less than ±½LSB. The DAC1125 also features ±½LSB accuracy, 3μs settling time to ±0.01% of reading, and a ±10ppm/°C maximum gain temperature coefficient. The digital inputs are fully TTL/DTL compatible.

LOW FEEDTHROUGH

The ideal multiplying D/A converter would be one which had a feedthrough of zero. For such a device, the output voltage would be zero when "k" was programmed to be zero, regardless of the amplitude or frequency of the analog input signal. However, due to capacitive coupling, switch leakage, and other effects, practical multiplying D/A's do have a measurable feedthrough which increases with frequency. In 12 bit devices available prior to the DAC1125, Four Quadrant Zero feedthrough would generally exceed ½LSB for full scale input signals of 500Hz and above. The utility of these products was, therefore, greatly restricted.

The DAC1125 combines innovative design with advanced CMOS technology to achieve a new standard of converter performance. Figure 2 shows the typical zero feedthrough as a function of input signal frequency for the Two Quadrant and Four Quadrant modes of operation. Note that the Four Quadrant Zero feedthrough is under ½LSB even at 40kHz.

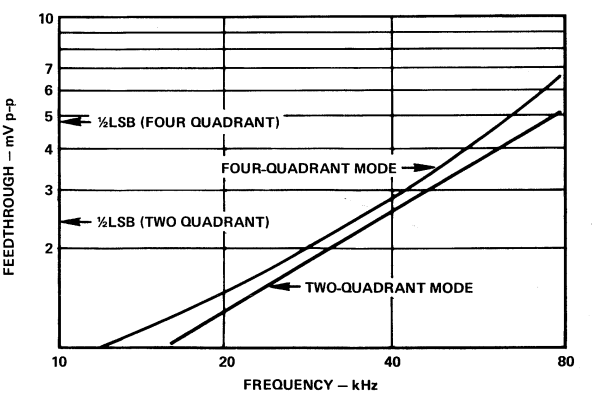


Figure 2. Typical Zero-Code Feedthrough vs. Input Frequency (For a 20V p-p Sinewave Input)

SPECIFICATIONS (typical @ +25°C and ±15V dc supplies unless otherwise noted)

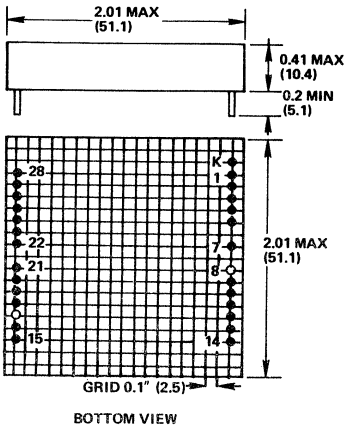
RESOLUTION	12 Bits
ACCURACY	
Relative to Input[1]	
Two Quadrant	±0.4LSB max
Four Quadrant	±0.5LSB max
Monotonicity	Guaranteed
	0 to +70°C (Two Quadrant)
	0 to +50°C (Four Quadrant)
ANALOG INPUT	
Voltage Range	
Nominal	±10V
Absolute Maximum	±15V
Input Impedance	5kΩ (±1%) Shunted by ≈10pF
DIGITAL INPUT	
Logic Levels	
0V ≤ Logic "0" ≤ 0.7V	-180μA max
2V ≤ Logic "1" ≤ 5.5V	+10μA max
Coding	
Two Quadrant	Complementary Binary
Four Quadrant	Positive True Offset Binary, or Two's Complement
OUTPUT	
Voltage	±11V max
Current	±5mA max
Impedance	<1 ohm
Capacitive Load	300pF max
DYNAMIC CHARACTERISTICS	
Feedthrough (4 Quad. Zero)	±0.5LSB max, 0 to 40kHz
Settling Time[2] (to 0.01% of FS)	3μs (10μs max)
Frequency Response[3]	-3dB @ 450kHz
Full Power Bandwidth	500kHz (300kHz min)
Slew Rate	20V/μs
Output Noise[4]	
Two Quadrant	5mV p-p
Four Quadrant	8mV p-p
Phase Shift[5]	-0.5° @ 5kHz
TEMPERATURE COEFFICIENTS	
Gain	3ppm/°C (10ppm/°C max)
Zero	
Two Quadrant	8μV/°C (20μV/°C max)
Four Quadrant	20μV/°C (50μV/°C max)
Differential Nonlinearity	3ppm/°C
POWER REQUIREMENT[6]	
Positive Supply	13V to 17V @ 17mA
Negative Supply	-12V to -18V @ -10mA
POWER SUPPLY REJECTION	>80dB
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +125°C

[1] For a ±10V sinewave, 0 to 10kHz.
[2] For a 20V output step of either polarity resulting from an analog or digital input change.
[3] For a ±10V sinewave input and output.
[4] White noise at output as measured over a 20MHz bandwidth.
[5] Input to output phase shift for a ±10V sinewave output.
[6] If input and output voltage ranges are restricted to ±5V, the positive supply may be reduced to 8.5V and the negative supply reduced to -7V.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

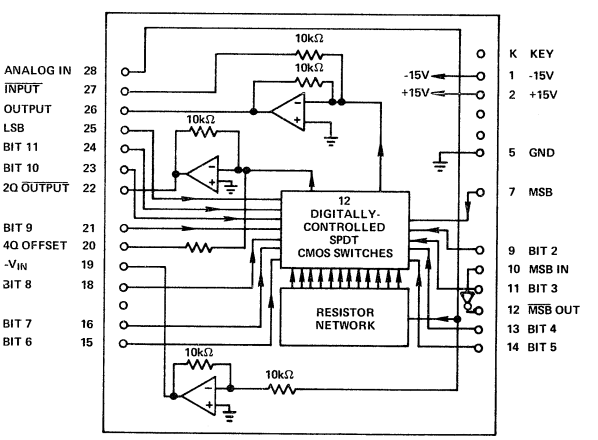
Dimensions shown in inches and (mm).



BOTTOM VIEW

NOTE:
Terminal pins installed only in shaded hole locations
Module weight: 1.6 ounces (45 grams)
All pins are gold plated half-hard brass, (MIL–G–45204), 0.019" ±0.001" (0.483 ±0.025mm) dia.
For plug-in mounting card order Board No. AC4102

DAC1125 BLOCK DIAGRAM



PRINCIPLE OF OPERATION

The DAC1125 consists of two identical current summing D/A's in one package. Figure 3 shows its circuitry in greatly simplified form.

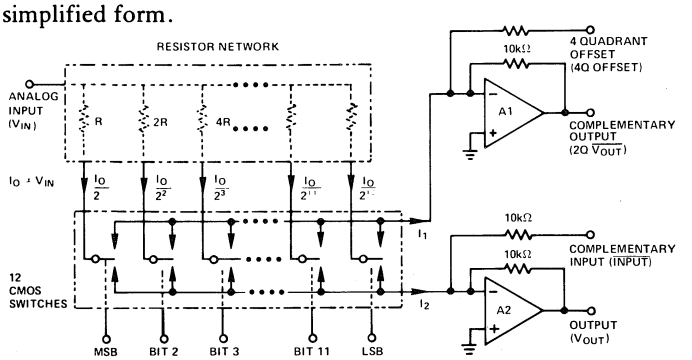


Figure 3. Simplified DAC1125 Circuit

An analog voltage which can vary from -10V to +10V is applied to the analog input. The resistor network develops a series of 12 binarily weighted currents which are proportional to the input voltage. These 12 currents are directed to either of two op amp summing junctions by a series of 12 digitally controlled SPDT CMOS switches. When a Logic "1" is applied to the switch control line, the corresponding bit current goes to the summing junction of A1 and when Logic "0" is applied it goes to A2. The maximum current going to A1 will occur when a digital input of 111111111111 is applied. Any other digital input will divert current to A2. Thus, for a fixed V_{IN}, the sum of I_1 and I_2 is a constant.

TWO QUADRANT OPERATION

In the Two Quadrant mode of operation, the COMPLEMENTARY INPUT and FOUR QUADRANT OFFSET inputs are grounded. The OUTPUT voltage is related to the INPUT voltage and the digitally programmed constant, k, by:

$$V_{OUT} = k\ V_{IN};\ -0.99976 \leqslant k \leqslant 0$$

Table I shows the relationship between the complementary binary coded digital input and the nominal value of k for this mode of operation. Note that a 1LSB step is represented by a fractional change of 0.00024.

DIGITAL INPUT	k
111111111111	0.00000
111111111110	-0.00024
101111111111	-0.25000
100000000000	-0.49976
011111111111	-0.50000
001111111111	-0.75000
000000000000	-0.99976

Table I. Values of k for the Two Quadrant Mode (Complementary Binary Code)

The COMPLEMENTARY OUTPUT voltage is related to the INPUT and OUTPUT voltages by the following two expressions:

$$V_{OUT} + 2QV_{OUT} = -0.99976\ V_{IN}$$

$$2QV_{OUT} = -(k + 0.99976)\ V_{IN}$$

The values of k as seen at the COMPLEMENTARY OUTPUT are not factory adjusted and may vary by ±1 percent from the ideal values.

FOUR QUADRANT OPERATION

To achieve Four Quadrant operation, the COMPLEMENTARY OUTPUT is connected to the COMPLEMENTARY INPUT. This subtracts the output of A1 from A2. To implement offset binary code, in which a digital input of 100000000000 gives an output of 0.0V, a small amount of current must be subtracted from I1. This current, proportional to V_{IN}, has to shift the OUTPUT voltage by ½LSB. This is done by using a third inverting op amp (not shown in Figure 3) to develop a voltage equal to $-V_{IN}$. A jumper connected between the output of this op amp and the 4Q OFFSET terminal provides the necessary ½LSB offset current. The OUTPUT voltage is thus related to the INPUT voltage and the digitally programmed constant, k, by:

$$V_{OUT} = k\ V_{IN};\ -1 \leqslant k \leqslant 0.99951$$

Table II shows the relationship between offset binary coded digital inputs and the nominal value of k. Note that a 1LSB step is represented by a fractional change of 0.00049.

DIGITAL INPUT	k
111111111111	+0.99951
110000000000	+0.50000
100000000001	+0.00049
100000000000	0.00000
011111111111	-0.00049
010000000000	-0.50000
000000000000	-1.00000

Table II. Values of k for the Four Quadrant Mode (Offset Binary Code)

A TTL inverter (input at pin 10, output at pin 12) is available for the purpose of inverting the MSB to obtain Two's Complement input coding in the Four Quadrant mode. Table III shows the relation between the nominal value of k and the digital input for this mode.

DIGITAL INPUT	k
011111111111	+0.99951
010000000000	+0.50000
000000000001	+0.00049
000000000000	0.00000
111111111111	-0.00049
110000000000	-0.50000
100000000000	-1.00000

Table III. Values of k for the Four Quadrant Mode (Two's Complement Code)

INPUT-OUTPUT RELATIONSHIPS

The input-output relationships are further illustrated below in Figure 4 which shows several two quadrant and four quadrant outputs for a 10V sinewave input and various digital codes.

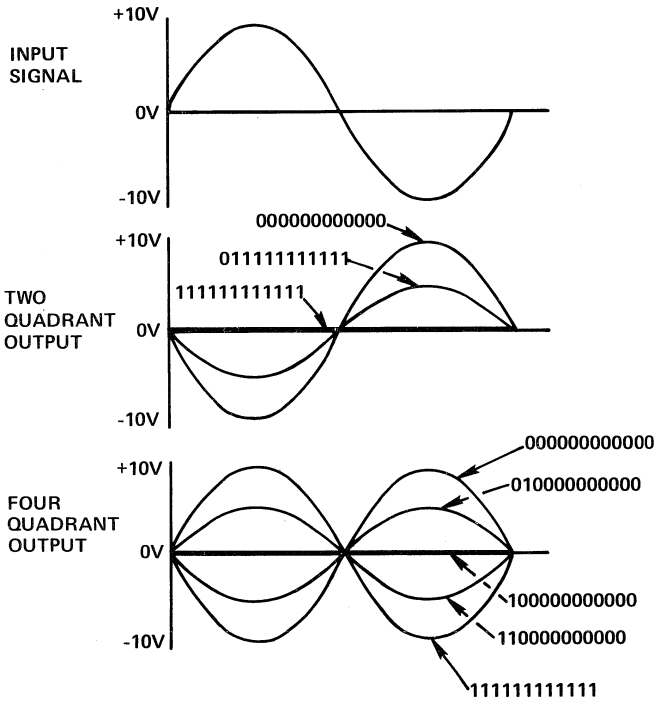


Figure 4. Response to Sinewave Input for Various Digital Inputs

MODULE CONNECTIONS

The DAC1125 is connected as shown in Figure 5 for two-quadrant, and Figure 6 for four-quadrant operation.

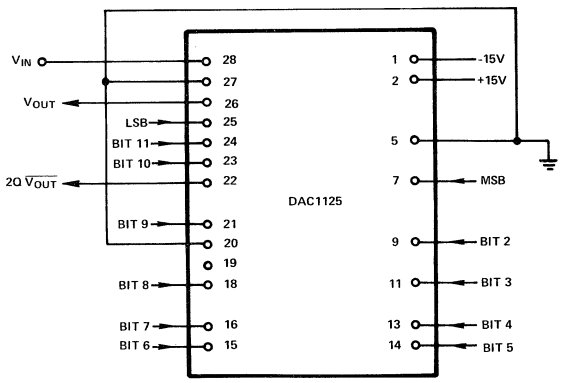


Figure 5. Connections for Two Quadrant Operation

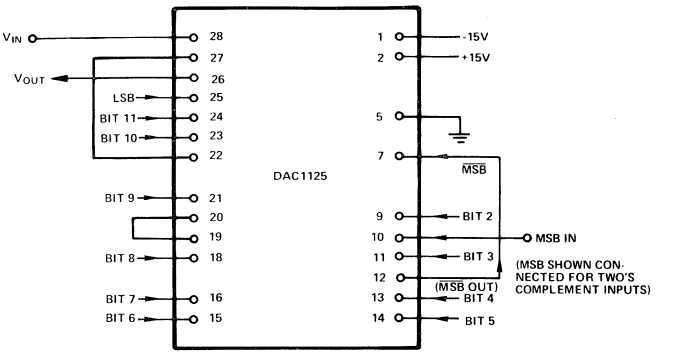


Figure 6. Connections for Four Quadrant Operation

All connections between module pins, especially where pins 20 and 27 are involved, should be made with short leads. The use of shielded cable is recommended for analog signal inputs and outputs if the lead length is greater than approximately one foot (300mm). The DAC1125 has internal 0.2μF capacitors which bypass the ±15V supplies and, therefore, external bypass capacitors will only be required in exceptionally noisy environments.

HANDLING CONSIDERATIONS

Care must be taken in the handling of the DAC1125 to prevent electrostatic damage to its internal CMOS switches. The unit should be transported on conductive foam or other suitable material and should only be handled by properly grounded personnel. The ground pin must be connected before power is applied. Electrostatic damage, should it occur, can result in excessive power supply current, degraded performance, or total failure.

THE AC4102 MOUNTING CARD

The AC4102 mounting card is available to assist in evaluation of the DAC1125. This 3" x 3" (76 x 76mm) printed circuit card has sockets which allow a DAC1125 to be plugged directly onto it. Each of the 28 active pin sockets is connected to a turret terminal so that connections can be easily made to the module without soldering directly to its pins.

High Performance Digital-to-Analog Converter

DAC1132

FEATURES
- 12 Bit Resolution
- Input Register Included
- Small Module Package
- Programmable Output Ranges
- 0 to +70°C Monotonicity
- Low 8ppm/°C Gain TC
- 2μs Settling Time

GENERAL DESCRIPTION

The DAC1132 is a 12 bit, high performance digital-to-analog converter packaged in a very compact 2" x 2" x 0.4" module. It comes complete with an input storage register and a fast settling output amplifier which can be jumper programmed to produce either of five output voltage ranges. Performance specifications include 2μs settling time to 0.01%, 8ppm/°C gain temperature coefficient, ±½LSB linearity error, and monotonicity from 0 to +70°C.

The DAC1132 combines the AD562 integrated circuit D/A with a TTL input register, an output amplifier, and a precision reference source to form a complete converter package. The laser trimmed AD562 which consists of precision current switches, and a very stable thin film resistor network provides the DAC1132 with excellent performance over temperature and makes possible its small module size.

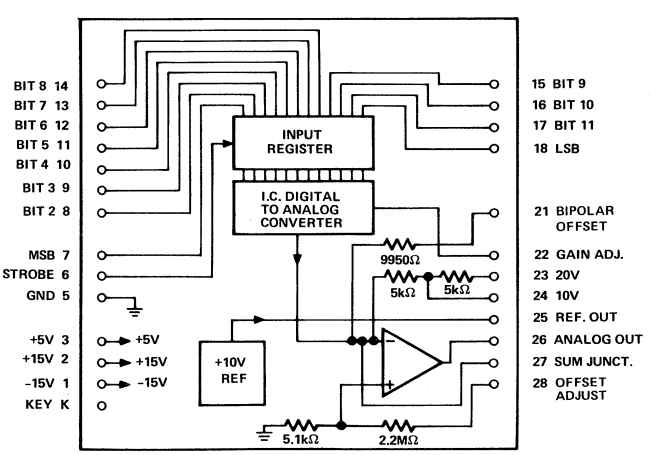
DIGITAL INPUT CHARACTERISTICS

The TTL/DTL compatible storage register contained within the DAC1132 accepts either Binary or Offset Binary coded inputs. Digital data appearing at the converter's 12 input terminals will be strobed into the register whenever a positive going transition is applied to the STROBE input (pin 6). With the STROBE input held at either Logic "0" or Logic "1", the input data may be changed without affecting either the contents of the register or the output of the converter. The transfer characteristics of the DAC1132 are such that a full scale digital input (111111111111) results in a positive full scale voltage output.

OUTPUT CHARACTERISTICS

The 12 binary-weighted current sources which form the basis of the digital-to-analog conversion process are directly controlled by the digital data stored in the input register. The combined output of these sources is applied to the internal op amp summing junction to produce a voltage output signal. By connecting jumpers between the proper module pins, various values of op amp feedback resistance and thus, output voltage ranges can be selected.

In order to produce bipolar outputs, the current input to the internal op amp is offset by ½ Full Scale. This offset current is generated by the precision internal reference source and is applied to the op amp summing junction by means of a jumper connected between appropriate module terminals.



Block Diagram

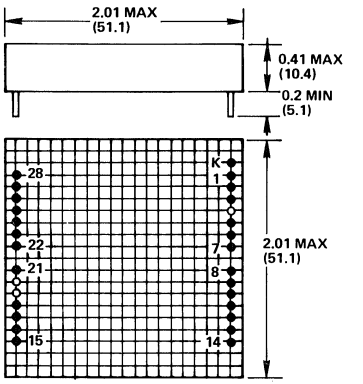
SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise specified)

RESOLUTION	12 Bits
DIGITAL INPUTS	
Logic Levels	0V ≤ Logic "0" ≤ 0.8V +2V ≤ Logic "1" ≤ +5V
Data Input Load	1 Standard TTL Load/bit
Strobe Input Load	2 Standard TTL Loads
Strobe Pulse Width	20ns (min)
Data Setup Time	20ns (min)
Data Hold Time	5ns (min)
INPUT CODES	
Unipolar	Binary
Bipolar	Offset Binary
OUTPUT RANGES	0 to +5V @ 10mA 0 to +10V @ 10mA ±2.5V @ 10mA ±5V @ 10mA ±10V @ 10mA
OUTPUT IMPEDANCE	0.02Ω
SETTLING TIME	2.0μs (3.0μs max) to 0.01%[1]
LINEARITY ERROR	±½LSB max
TEMPERATURE COEFFICIENT	
Gain[2]	±8.0ppm/°C (±15ppm/°C max) of Reading
Unipolar Offset	±5ppmV/°C (±20ppm/°C max)
Bipolar Offset[2]	±8ppm/°C (±25ppm/°C max)
Differential Nonlinearity	±2.8ppm/°C (±3.0ppm/°C max) of Full Scale
Reference Voltage	±5ppm/°C (±12ppm/°C max)
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +100°C
POWER REQUIREMENTS	+15V ±3% @ 32mA (37mA max) -15V ±3% @ 27mA (30mA max) +5V ±3% @ 140mA (150mA max)
POWER SUPPLY SENSITIVITY[3]	
Gain	4mV/V (7mV/V max)
Offset (unipolar)	4mV/V (7mV/V max)
Offset (bipolar)	4mV/V (7mV/V max)
Reference	2μV/V (5μV/V max)
ADJUSTMENTS (User Provided)	
Gain	±8LSB (min)
Offset	±10LSB (min)

[1] For a 10V step.
[2] These figures include the effects of Reference Voltage Temperature Drift.
[3] For ±15V supplies only with +15V and -15V supplies tracking.
Specifications subject to change without notice.

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
Module weight: 1.6 ounces (45 grams)
All pins are gold plated half-hard brass, (MIL-G-45204), 0.019" ±0.001" (0.483 ±0.025mm) dia.
For plug-in mounting card order Board No. AC1506

DIGITAL INPUT DATA

All digital inputs to the DAC1132 are fully DTL/TTL compatible. The 12 data inputs (pins 7–18) each represent one standard TTL load and the STROBE (pin 6) represents two TTL loads. The converter uses Binary input code to produce unipolar outputs and Offset Binary code to produce bipolar outputs.

Provided that certain timing requirements are met, data appearing at the converter's input terminals is loaded into the register by the positive-going edge of the strobe pulse. Figure 1 illustrates the required strobe timing.

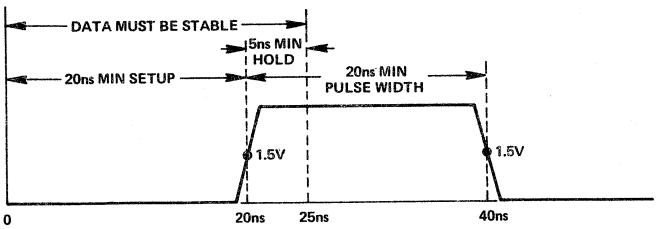


Figure 1. Strobe Timing Diagram

Note that the input data must be stable for at least 20ns before and 5ns after the pulse's leading edge. Note also that the strobe pulse must be a minimum of 20ns wide. In order to allow adequate time for the converter's analog output to settle between conversions, the strobe frequency should be limited to 500kHz.

OUTPUT CONNECTIONS

Figure 2, below, shows the output configuration of the DAC1132 in simplified form.

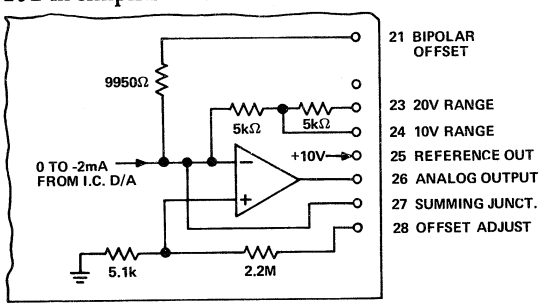


Figure 2. Output Circuit Block Diagram

External jumper connections determine whether the DAC1132 will be a unipolar or a bipolar device. Figures 3a and 3b below show the proper connections for both configurations.

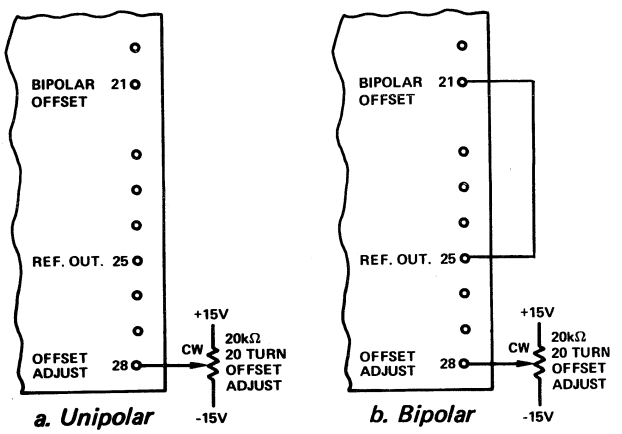


Figure 3. Unipolar/Bipolar Output Connection

The two 5kΩ feedback resistors associated with the op amp of Figure 2 are used to determine the output voltage range. Serial and parallel combinations of these resistors yield three different resistance values. Table 1 shows the feedback connections used to obtain the various output voltage ranges.

Output Range		Pins Jumpered Together	
Bipolar Units	**Unipolar Units**	**Pin 26 To:**	**Pin 23 To:**
±2.5V	0 to +5V	24	27
±5.0V	0 to +10V	24	--
±10V		23	--

Table 1. Range Programming Table

INPUT-OUTPUT RELATIONSHIPS

Table 2 and Table 3 list the analog outputs associated with various digital inputs for unipolar and bipolar units respectively.

DIGITAL INPUT	NOMINAL VOLTAGE OUTPUT	
	0 to +5V Range	**0 to +10V Range**
Binary Code		
111111111111	+4.9988V	+9.9976V
000000000001	+0.0012V	+0.0024V
000000000000	0.0000V	0.0000V

Table 2. Unipolar Input-Output Relationships

DIGITAL INPUT	NOMINAL VOLTAGE OUTPUT		
	±2.5V Range	**±5V Range**	**±10V Range**
Offset Binary Code			
111111111111	+2.4988V	+4.9976V	+9.9951V
100000000001	0.0012V	0.0024V	0.0048V
100000000000	0.0000V	0.0000V	0.0000V
000000000000	-2.5000V	-5.0000V	-10.0000V

Table 3. Bipolar Input-Output Relationships

GAIN, AND OFFSET ADJUSTMENTS

The gain and offset adjustments are made with two external potentiometers which the user supplies. With certain digital inputs applied, these potentiometers are adjusted until the desired output voltage is obtained. The voltmeter used to measure the output must be capable of clear and stable resolution of 1/10LSB in the region of zero and full scale. The adjustment procedure, described below, should be carefully followed to assure optimum converter performance.

The proper connection for the offset potentiometer was shown in Figures 3a and 3b. The gain potentiometer should be connected as shown below in Figure 4.

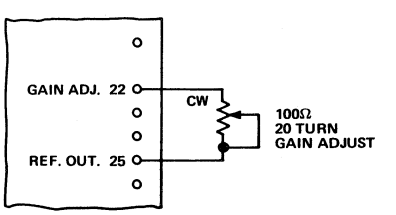


Figure 4. Gain Adjustment Connection

For unipolar units apply a digital input of 000000000000 and adjust the offset potentiometer until an output of 0V ±1/10LSB is obtained.

For bipolar units apply a digital input of 000000000000 and adjust the offset potentiometer until the negative full scale output shown in Table 3 is obtained within ±1/10LSB.

Once the appropriate offset adjustment has been made, apply a digital input of 111111111111. Adjust the gain potentiometer until the positive full scale output shown in Table 2 or Table 3 is obtained within ±1/10LSB.

POWER SUPPLY AND GROUNDING CONNECTIONS

The proper power supply and grounding connections are shown below in Figure 5.

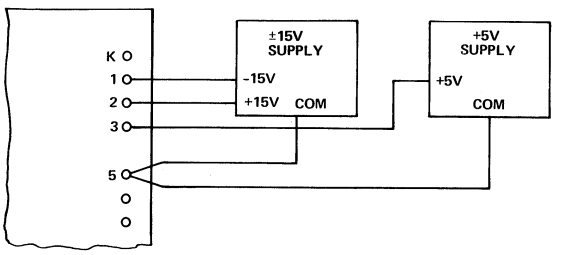


Figure 5. Power Supply and Grounding Connections

Capacitors have been added within the DAC1132 to bypass the ±15V and +5V power inputs. Under normal circumstances, no external bypass capacitors are needed.

REFERENCE OUTPUT

The +10V reference output (pin 25) is used to set the converter's gain as shown in Figure 4 and to provide the offset for bipolar devices as shown in Figure 3. It may also be used to provide a reference voltage for other circuits in the user's system provided that the output current is limited. No more than 1.5mA should be drawn from bipolar devices and no more than 2.5mA should be drawn from unipolar devices. Excessive current drain will degrade the converter's analog output and could damage the internal reference source.

THE AC1506 MOUNTING CARD

The AC1506 mounting card is available to assist in the application of the DAC1132. This 4.5" x 3.0" printed circuit card, shown below in Figure 6, has sockets which allow a DAC1132 to be plugged directly onto it. It includes the necessary gain, and offset adjustment potentiometers and it mates with a Cinch 250-22-30-170 (or equivalent) edge connector which is supplied with every card.

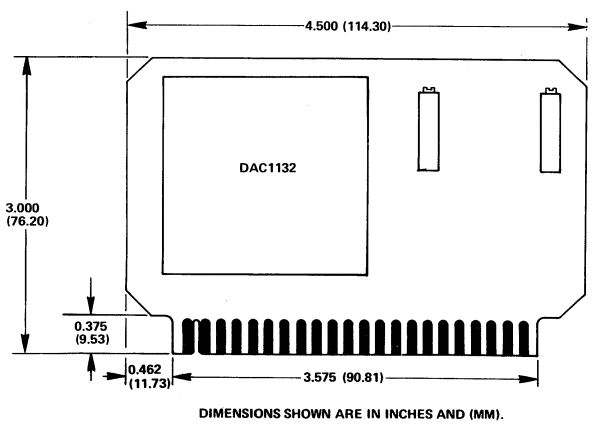
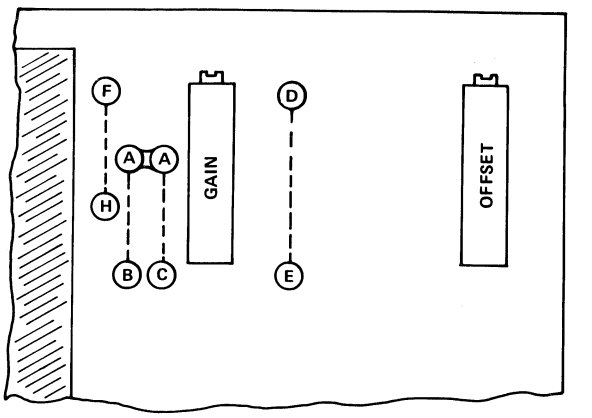


Figure 6. AC1506 Outline Drawing

The output voltage range is programmed by means of jumpers which the user installs as shown in Figure 7.



OUTPUT VOLTAGE RANGE	JUMPER CONNECTION
0 to +10V	A – C
0 to +5V	A – C, F – H
±2.5V	D – E, A – C, F – H
±5V	D – E, A – C
±10V	A – B, D – E

Figure 7. AC1506 Range Programming

The pin connections are as shown below in Table 4.

Pin	Designation	Pin	Designation
A	MSB	N	Bit 12
B	Bit 2	P	N.C.
C	Bit 3	R	N.C.
D	Bit 4	S	Ground
E	Bit 5	T	Ref. Out.
F	Bit 6	U	Analog Out.
H	Bit 7	V	Strobe
J	Bit 8	W	+5V
K	Bit 9	X	+15V
L	Bit 10	Y	-15V
M	Bit 11	Z	Ground

Table 4. AC1506 Pin Designations

High Resolution, 16 and 18 Bit Digital to Analog Converters

DAC1136/1138

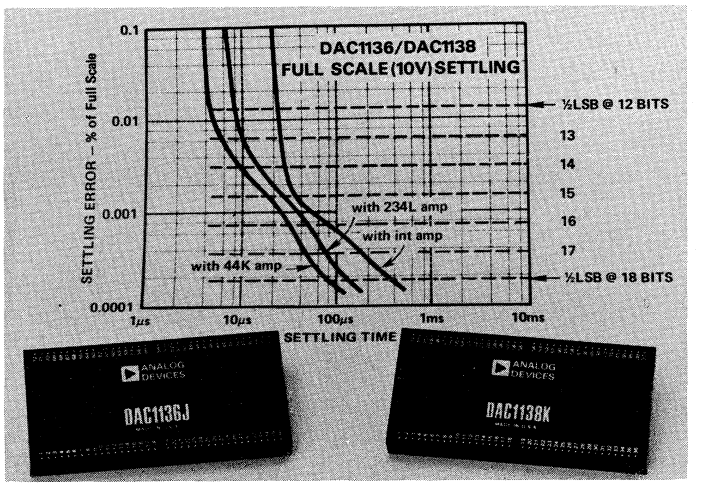
FEATURES

DAC1138

High Resolution 18 Bits (38μV, 1 Part in 262,144)
Integral Nonlinearity <½LSB
Differential Nonlinearity <½LSB
Settling to ½LSB (0.0002%) in 10μs
Programmable Output Ranges
Hermetically-Sealed Semiconductors
Low Profile 2″ x 4″ x 0.4″ Module

DAC1136

16 Bit Resolution and Accuracy
Low Cost
Linearity <½LSB
Settling to ½LSB (0.0008%) in 6μs



WHERE TO USE THE DAC1138

The DAC1138 delivers superior accuracy for a broad range of display, test, and instrumentation applications. With a resolution of 18 bits or 1 part in 262,144, the DAC1138 is ideally suited for applications requiring wide dynamic range measurement and control. Applications include data distribution systems, high resolution CRT displays, automatic semiconductor testing, typesetting, frequency synthesis and nuclear reactor control.

GENERAL DESCRIPTION

The DAC1136/1138 are complete self-contained modular converters with resolution and accuracy of 16 and 18 bits respectively. These modules are constructed in a compact 2″ x 4″ x 0.4″ package and are pin compatible with the popular DAC-14QM and DAC-16QM in most applications. The DAC1136/1138 combines precision current sources along with state-of-the-art steering switches to produce stable conversions. Inputs to the DAC1136/1138 are compatible with TTL levels. The converters have a current output of 2mA full scale. A voltage output can be obtained by connecting the internal amplifier to the current output by means of jumpers. By using additional jumpers, the user can select any one of the following output ranges: 0 to +5V, 0 to +10V, ±5V, and ±10V.

The DAC1136/1138 are available as a card mounted assembly. In this configuration, the user can select from a library of input codes and output amplifiers.

CERTIFICATE OF CALIBRATION

Each DAC1138 has been rigorously calibrated with equipment and methods that are traceable to the National Bureau of Standards (NBS). A certificate of performance is sent with each unit. This includes 1000 hour stability data for the reference zener and a test record.

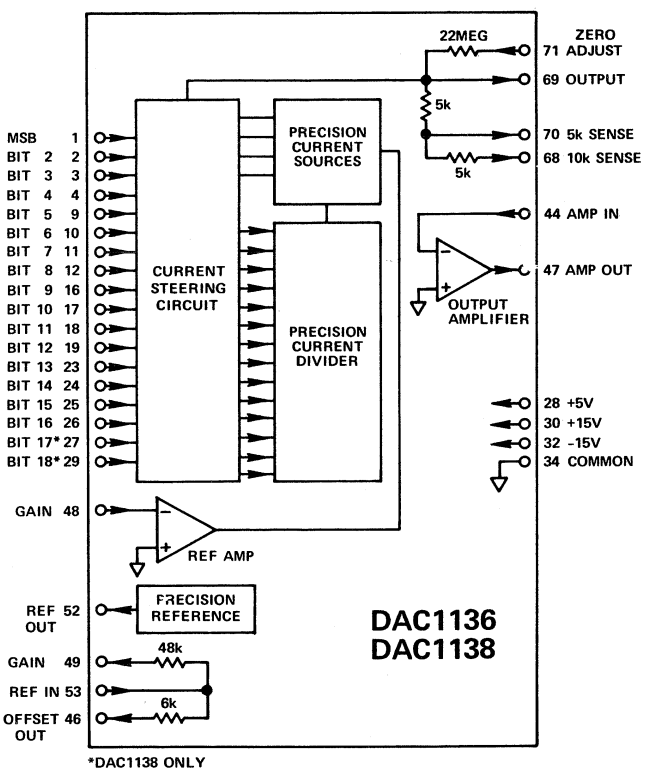


Figure 1. Block Diagram and Pin Designations

SPECIFICATIONS (typical @ +25°C, and rated supply voltages, unless otherwise noted)

MODEL	DAC1136J	DAC1136K	DAC1136 Card Mounted Assy W/IC AMP	W/44K	W/234L
RESOLUTION	16 Bits	16 Bits	*	*	*
Magnitude of 1LSB (10V range)	152μV	*	*	*	*
DIGITAL INPUTS	TTL/See Fig. 2	*	TTL	**	**
Input Codes					
Unipolar	Complementary Binary	*	See Ordering Guide		
Bipolar	Complementary Offset Binary	*	See Ordering Guide		
Strobe	N.A.	*	⌐ See Note 1		
ANALOG OUTPUTS					
Current Mode					
Source Resistance					
Unipolar	>33kΩ	*			
Bipolar	>5kΩ	*			
Source Capacitance	150pF	*			
Output Range					
Unipolar	-2mA to 0mA	*			
Bipolar	-1mA to +1mA	*			
Voltage Compliance					
Rated Accuracy	±2mV	*			
Clamp Limits[2]	±500mV	*			
Noise (rms, 10Hz-100kHz)	1nA	*			
Settling Time to ½LSB					
Full Scale Step	8μs	*			
LSB Step	6μs	*			
Voltage Mode					
Output Range	0 to +5V, 0 to +10V, ±5V, ±10V	*	See Ordering Guide		
Output Impedance	0.08Ω	*	*	0.01Ω	0.01Ω
Rated Output Load Current	4mA max	*	±4mA	±20mA	±5mA
Noise (rms, 10Hz-100kHz)					
0 to +10V, ±5V	19μV	*	22μV	30μV	35μV
0 to +5V	13μV	*	25μV	30μV	35μV
±10V	38μV	*	40μV	45μV	60μV
Settling to ½LSB					
LSB Step	6μs	*	6μs	5μs	7μs
Full Scale Step					
Unipolar	30μs	*	30μs	15μs	25μs
Bipolar	40μs	*	40μs	25μs	35μs
LINEARITY	±1LSB max	±½LSB max	See Linearity Spec. For Module		
TEMPERATURE COEFFICIENT (ppm/°C)					
Gain[9]	5	*	8	**	**
Offset	0.5	*	0.5	2	0.9
TEMPERATURE RANGE					
Operating Temp.[3]	0 to +70°C	*	*	*	*
Storage Temperature	-55°C to +85°C	*	*	*	*
POWER SUPPLY REQUIREMENTS[4]					
+5V dc ±5%	9mA	*	9[8]mA	**	**
±15V dc ±5%	30mA	*	30mA	40mA	37mA
POWER SUPPLY REJ. (VOLTAGE MODE)					
Gain Error	80dB	*	*	*	*
Offset[5]	75dB	*	75dB	80dB	100dB
STABILITY, LONG TERM (ppm/10³ hr) (Exclusive of Reference)					
Gain	5	*	*	**	**
Offset	6	*	6	30	6
REFERENCE VOLTAGE[6]	6.00V ±0.02%	*	*	*	*
Reference Stability (ppm/°C)	5	*	*	*	*
Ref. Long Term Stability (ppm/10³ hr)	10	*	5	**	**
OUTLINE DIMENSIONS	2" x 4" x 0.4"	*	See Figure 6		
Adjustments					
Internal	Linearity[7]	*	Gain, Offset, and Linearity		
External	Gain & Offset	*	None		

Specifications subject to change without notice.

*Specifications same as DAC1136J.

**Specifications same as DAC1136 with I.C. Amplifier.

NOTES:

[1] Positive going transition (Logic "0" to Logic "1") will clock data into series 74LS logic network.

[2] Clamp limits are set by Schottky diodes.

[3] 5% to 95% relative humidity non-condensing.

[4] Recommended power supply: Analog Devices models 904 and 903.

[5] Unipolar and bipolar.

[6] The reference output is high impedance, maximum load 1μA, ($Z_{out} \approx 200\Omega$)

[7] The module has 5 linearity adjustments: MSB, bit 2, bit 3, bit 4, and the sum of bits 5 → 18.

[8] 95mA using mounting card with input latching registers, see ordering guide.

[9] Exclusive of reference.

SPECIFICATIONS (typical @ +25°C, and rated supply voltages, unless otherwise noted)

MODEL	DAC1138J	DAC1138K	DAC1138 Card Mounted Assy W/IC AMP	W/44K	W/234L
RESOLUTION	18 Bits	18 Bits	*	*	*
Magnitude of 1LSB (10V range)	38μV	*	*	*	*
DIGITAL INPUTS	TTL/See Fig. 2	*	TTL	**	**
Input Codes					
Unipolar	Complementary	*			
	Binary		See Ordering Guide		
Bipolar	Complementary	*			
	Offset Binary		See Ordering Guide		
Strobe	N.A.	*	⎍ See Note 1		
ANALOG OUTPUTS					
Current Mode					
Source Resistance					
Unipolar	>33kΩ	*			
Bipolar	>5kΩ	*			
Source Capacitance	180pF	*			
Output Range					
Unipolar	-2mA to 0mA	*	Voltage Output Only		
Bipolar	-1mA to +1mA	*			
Voltage Compliance					
Rated Accuracy	±200μV	*			
Clamp Limits[2]	±500mV	*			
Noise (rms, 10Hz-100kHz)	1nA	*			
Settling Time to ½LSB					
Full Scale Step	10μs	*			
LSB Step	8μs	*			
Voltage Mode					
Output Range	0 to +5V, 0 to +10V, ±5V, ±10V	*	See Ordering Guide		
Output Impedance	See Characteristic Curves		See Characteristic Curves		
Rated Output Load Current	4mA max	*	4mA	20mA	5mA
Noise (rms, 10Hz-100kHz)					
0 to +10V, ±5V	19μV	*	22μV	30μV	35μV
0 to +5V	13μV	*	25μV	30μV	35μV
±10V	38μV	*	40μV	45μV	60μV
Settling to ½LSB					
LSB Step	18μs	*	18μs	16μs	20μs
Full Scale Step					
Unipolar	250μs	*	250μs	75μs	130μs
Bipolar	3ms	*	3ms	100μs	200μs
ACCURACY, (After Calibration)					
Differential Linearity Error (LSB)	±0.3 (±1 max)	±0.2 (±0.5 max)	See Accuracy Spec. For Module		
Integral Linearity Error (LSB)	±0.5 (±1 max)	±0.3 (±0.5 max)			
TEMPERATURE COEFFICIENT[3] (ppm/°C)					
Diff. Linearity	0.4	*	0.4	**	**
Integral Linearity	0.3	*	0.3	**	**
Gain[4]	1.0	*	1.5	**	**
Offset[5]	0.5	*	0.5	1.5	0.4
TEMPERATURE RANGE					
Operating Temp.[6]	0 to +70°C	*	*	*	*
Storage Temperature	-55°C to +85°C	*	*	*	*
POWER SUPPLY REQUIREMENTS[7,10]					
+5V dc ±5%	9mA	*	9mA[12]	**	**
±15V dc ±5%	30mA	*	30mA	40mA	37mA
POWER SUPPLY REJ. (VOLTAGE MODE)					
Gain	80dB	*	*	*	*
Offset[8]	75dB	*	75dB	80dB	100dB
STABILITY LONG TERM (ppm/10³ Hr) (Exclusive of Reference)					
Gain	2	*	*	**	**
Offset	2	*	2	30	2
REFERENCE VOLTAGE[9]	6.00V ±0.02%	*	*	*	*
Reference Stability (ppm/°C)	3	*	*	*	*
Ref. Long Term Stability (ppm/10³ Hr)	5	*	5	**	**
OUTLINE DIMENSIONS	2" x 4" x 0.4"	*	See Figure 6		
Adjustments					
Internal	Linearity[11]	*	Gain, Offset, and Linearity		
External	Gain & Offset	*	None		

Specifications subject to change without notice.

*Specifications same as DAC1138J.

**Specifications same as DAC1138 with I.C. Amplifier.

NOTES:

[1] Positive going transition (Logic "0" to Logic "1") will clock data into logic series 74LS network.

[2] Clamp limits are set by Schottky diodes.

[3] See characteristic curves for performance over temperature.

[4] Exclusive of reference for $+5°C \leq T_A \leq +50°C$.

[5] $+5°C \leq T_A \leq +50°C$, both unipolar and bipolar.

[6] 5% to 95% relative humidity non-condensing.

[7] Recommended power supply: Analog Devices models 904 and 903.

[8] Unipolar and bipolar.

[9] The reference output is high impedance, maximum load 1μA, Zout ≈ 200Ω.

[10] Change in differential limearity from factory setting due to power supply voltage variation from nominal is ≃ 3.5ppm/VΔV_S.

[11] Module has 5 linearity adjustments; MSB, bit 2, bit 3, bit 4, and the sum of bits 5→18.

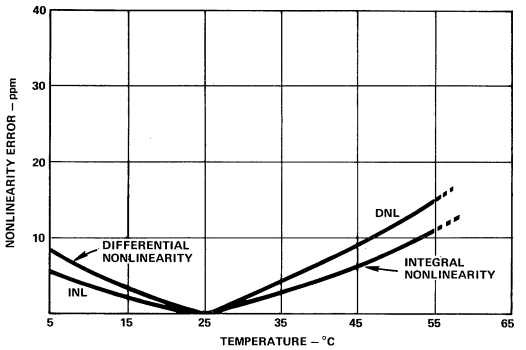
[12] 95mA using mounting card with input latching registers, see ordering guide.

DEFINITIONS:

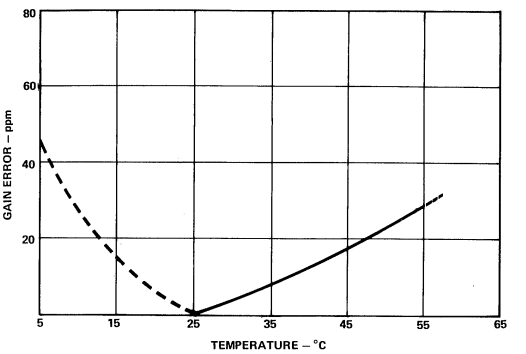
Differential Error: The difference between any 1 bit step and the ideal value of 1LSB.

Integral Error: The difference between the actual output transfer characteristic and the best straight-line equivalent through zero.

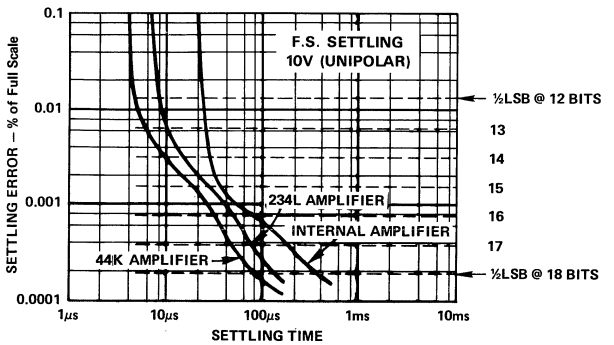
Characteristic Curves*



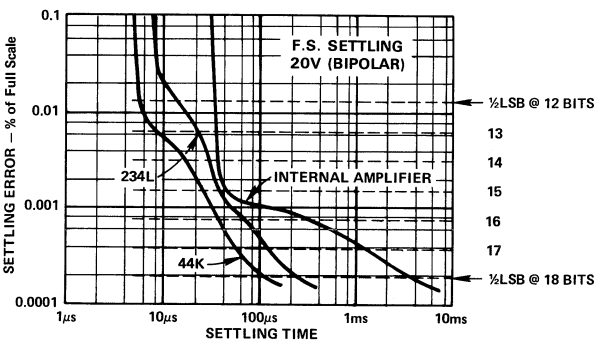
DAC1138 Nonlinearity vs. Temperature



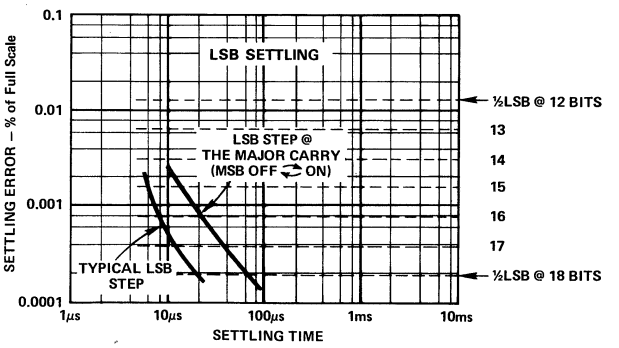
DAC1138 Gain Error vs. Temperature



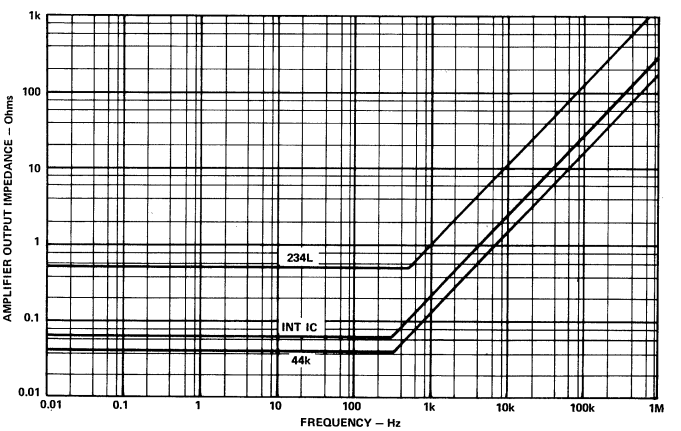
Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for 10V Output Step (0V ⇄ +10V)



Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for 20V Output Step (+10V ⇄ -10V)



Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for LSB Steps (Essentially Independent of Amplifier Used)

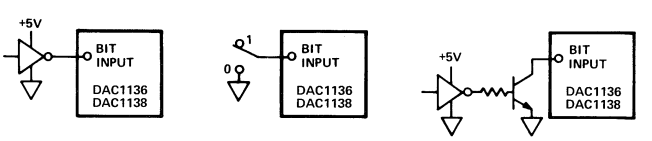


Amplifier Output Impedance vs. Frequency

*NOTE: All curves typical at rated supply voltage.
F.S. = Full Scale

INPUT CONSIDERATIONS

The DAC1136/1138 may be driven by TTL or CMOS as shown in Figure 2. Note that the TTL input is shown with inputs for both a direct "totem pole" TTL gate and open collector (or "pull-up") configurations.



2a. TTL Totem Pole | *2b. Switch or Relay Input*[2] | *2c. CMOS Input*

1. FOR TTL WITH OPEN COLLECTOR, DO NOT USE EXTERNAL PULLUP. CONVERTERS HAVE INTERNAL 10kΩ PULLUP ON EACH INPUT TO 3.8V.
2. USE SPST SWITCH OR RELAY TO GROUND. WHEN SWITCH IS OPEN, INTERNAL 10kΩ WILL PULL INPUT UP TO 3.8V.

Figure 2. Input Connections

OUTPUT GUARDING

The output connections of the DAC1136/1138 must be carefully planned.

Since an LSB is only 38μV (at 10 volts full scale for the DAC1138), care must be exercised to properly guard the outoutput of the converter. Suggested printed circuit board guarding to minimize leakage is shown in Figure 3, for operation in each mode; other suggestions may be obtained by referring to the DAC-16QM data sheet.

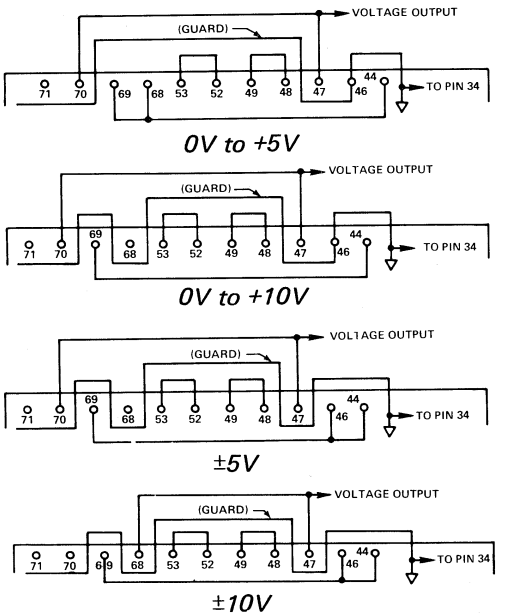


Figure 3. Suggested PCB Guarding (Unipolar and Bipolar Connections) to Minimize Leakage

GAIN AND OFFSET ADJUSTMENTS

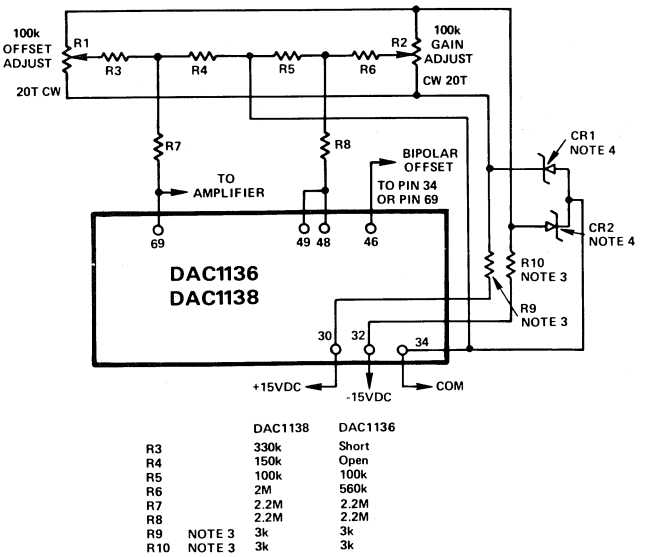
The gain and offset adjustments are made with external potentiometers which the user supplies. With certain digital inputs applied, these potentiometers are adjusted until the desired output voltage is obtained. The voltmeter used to measure the output should be capable of stable resolution of ¼LSB in the region of zero and full scale. The adjustment procedure, described below, should be carefully followed to assure optimum converter performance.

The proper connections for offset and gain are shown in Figure 4. For unipolar units, apply a digital input of all "1's" (equivalent in complementary binary to zero) and adjust the offset potentiometer until a 0.00000V output is obtained. (See Table 1). Once the appropriate offset adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the positive full scale output shown below is obtained.

RANGE	IDEAL OUTPUT		
		DAC1138	DAC1136
Unipolar:	All 11...1	All 00...0	
0V→+10V	0.00000V	+9.999962V	+9.999848V
0V→+5V	0.00000V	+4.999981V	+4.999924V
Bipolar:			
-10V→+10V	-10.00000V	+9.999934V	+9.999695V
-5V →+5V	-5.00000V	+4.999962V	+9.999848V
To adjust:	Adjust ZERO pot	Adjust GAIN pot	

Table 1. Full Scale Output

Note that there is some interaction between these two adjustments; this procedure should be repeated. Offset adjustment will affect gain; however, gain will not affect offset.



		DAC1138	DAC1136
R3		330k	Short
R4		150k	Open
R5		100k	100k
R6		2M	560k
R7		2.2M	2.2M
R8		2.2M	2.2M
R9	NOTE 3	3k	3k
R10	NOTE 3	3k	3k

1. ALL FIXED RESISTORS ARE 5% CARBON COMP. UNLESS OTHERWISE NOTED.
2. ALL POTS ARE INFINITE RESOLUTION TYPES.
3. R9 AND R10 ARE TYPE RN55D 1%.
4. CR1 AND CR2 ARE TYPE 1N753A.

Figure 4. Gain and Offset Connection

DIFFERENTIAL LINEARITY ADJUSTMENT

Each DAC1136/1138 has been rigorously factory calibrated and tested to achieve the performance indicated in the electrical specifications. Should it be necessary to readjust the linearity of these units, the user can do so. Before attempting this recalibration, it is imperative that the circuit application be rechecked to confirm that all precautions have been taken to insure proper application at the 16 bit or 18 bit levels. Field recalibration of differential linearity can be done to achieve optimum operation. The top 4 major carries, i.e., MSB vs. bits 2 through the LSB; down through bit 4 vs. bits 5 through the LSB can be trimmed using the procedure outlined below. Basically, the DAC is trimmed by comparing a bit to the sum of all lower bits, and adjusting if necessary for a one LSB positive difference. The setup for this adjustment is shown in Figure 5. In this procedure, an LSB is referred to as 38μV, implying that the DAC1138 is being used on the 10V range. For the DAC1136 an LSB is 152μV on the 10V range.

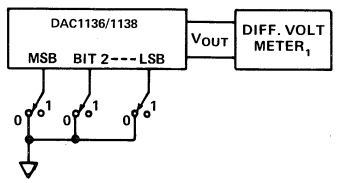
1. Bit 4 Trim
   a. Set bit switches to 11110 . . . . 0.
   b. Read the output voltage by nulling the voltmeter.
   c. Set bit switches to 11101 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 1b plus 1LSB. Adjust bit 4 if required.

2. Bit 3 Trim
   a. Set bit switches to 1110 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set switches to 1101 . . . . 1.
   d. Read voltage by nulling the voltmeter. This reading should be equal to that of step 2b plus 1LSB. Adjust bit 3 if required.

3. Bit 2 Trim
   a. Set bit switches to 110 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set bit switches to 101 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 3b plus 1LSB. Adjust bit 2 if required.

4. Bit 1 (MSB) Trim
   a. Set bit switches to 100 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set bit switches to 011 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 4b plus 1LSB. Adjust bit 1 (MSB) if required. If maximum available MSB weight is insufficient, then reduce weight of bits 5-n (and bits 4, 3, 2). If minimum available MSB weight is excessive, then increase weight of bits 5-n (and bits 4, 3, 2).

If insufficient range exists on any adjustment, then a separate adjustment for the weight of bits 5 through the LSB should be performed. This condition will probably not occur on bit 2, 3 and 4 but might occur on the MSB. If adjustment of the lower bits is made, the trim procedure for all bits should be repeated. Obviously, since the procedure affects the weight of individual bits, it affects the overall gain of the D to A converter. The final step should be adjustment of gain (user supplied adjustment external to module or pot at edge of mounting card).



1. A DIFFERENTIAL VOLTMETER CAPABLE OF 100μV FULL SCALE SHOULD BE USED. THIS WILL RESOLVE AN LSB, WHICH AT 18 BITS IS 38μV (10V RANGE). A FLUKE 895A, OR EQUIVALENT IS RECOMMENDED.

Figure 5. Differential Linearity Adjustment

DAC1136/1138 CARD MOUNTED ASSEMBLY

A card assembly has been designed to provide the user with a compatible range of input and output options to suit most applications. As shown in Figure 6, the card assembly has been designed with a separate dedicated Analog and Digital connector for optimum 18 bit performance.

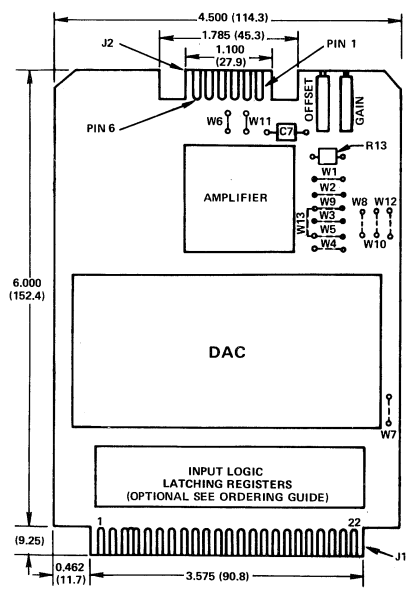


Figure 6. Mounting Card Assembly

Mounting Card Connector Designations

CONNECTOR J1

PIN	FUNCTION	PIN	FUNCTION
A	BIT 1	U	STROBE
B	BIT 2	V	BIT 18[1]
C	BIT 3	W	+5V
D	BIT 4	X	+15V
E	BIT 5	Y	-15V
F	BIT 6	Z	DIGITAL GND
H	BIT 7	1-4	NC
J	BIT 8	5	INTERLOCK
K	BIT 9	6	INTERLOCK
L	BIT 10	7-16	NC
M	BIT 11	17	BIT 17[1]
N	BIT 12	18	SEE NOTE 3
P	BIT 13	19	
R	BIT 14	20	
S	BIT 15	21	
T	BIT 16	22	

CONNECTOR J2

PIN	FUNCTION
1	ANALOG SENSE LOW
2	ANALOG SOURCE LOW
3	NC
4	ANALOG SOURCE HIGH
5	ANALOG SENSE HIGH
6	ANALOG REF. IN/OUT
A	ANALOG REF. IN/OUT
B	ANALOG SENSE HIGH
C	ANALOG SOURCE HIGH
D	NC
E	ANALOG SOURCE LOW
F	ANALOG SENSE LOW

J1 MATES WITH CINCH PIN 251-22-30-160. J2 MATES WITH CINCH PIN 251-06-30-160.
[1]DAC1138 ONLY

The output voltage range, amplifier, and reference configuration can be programmed by means of jumpers and resistors which the user installs, as shown below.

OUTPUT RANGE	INSTALL JUMPERS
±10V	W10, W5
±5V	W12, W5
+10V	W12, W3

REFERENCE	INSTALL JUMPERS
Internal	W2
External	W1

AMPLIFIER	INSTALL JUMPERS
Internal	W4, W9
External	W8*

*With 234L amplifier install C7, 0.01μF 10% ceramic capacitor. With 44K amplifier, install variable resistor in the R13 position and adjust the resistor for a ±100μV reading between pins 69 and 34 on the converter (typ valve ≈ 500Ω) to optimize voltage compliance.

NOTE:
1. To isolate analog and digital grounds, W7 is omitted.
2. W6 and W11 are not installed on standard units. This allows 4-wire connection to J2 when either a 44K or 234L amplifier is used.
3. To use this assembly with a DAC16QG mounting socket, connect jumpers from J1 to J2 at equivalent symbols to bring the output signal to the J1 connector. J2 is then not required.

INPUT OPTIONS

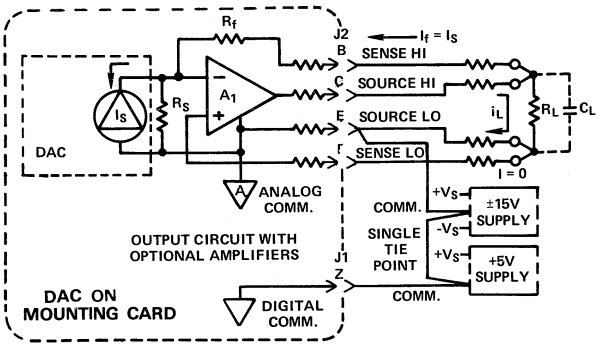
The DAC1136/1138 card assembly has been designed to accept standard TTL logic levels in any one of the following codes: binary, complementary binary, 2's complement, complementary 2's complement, sign plus magnitude binary, and complementary sign plus magnitude binary. In addition to the above logic codes, it is possible to bring the digital input "Direct" into the DAC1136/1138.

OUTPUT OPTIONS

The card assembly for the DAC1136/1138 allows for several output configurations:

1. Internal Monolithic Output Amplifier built into the DAC1138.
2. Analog Devices model 234L; for low noise, low drift applications (2μV, ±0.1μV/°C).
3. Analog Devices model 44K; recommended only for high speed or high current applications (75μs settling to 0.0002%, 20mA).

When using an external amplifier, a four terminal output connection can be utilized on the card assembly in order to allow for compensation of connector contact resistance. See Figure 7.



NOTE:
1. VOLTAGE DROP BETWEEN SOURCE LO AND SENSE LO MUST OBSERVE CURRENT MODE COMPLIANCE LIMITS FOR RATED ACCURACY.
2. THIS CONNECTION SCHEME CANNOT BE USED WITH INTERNAL MONOLITHIC AMPLIFIER.

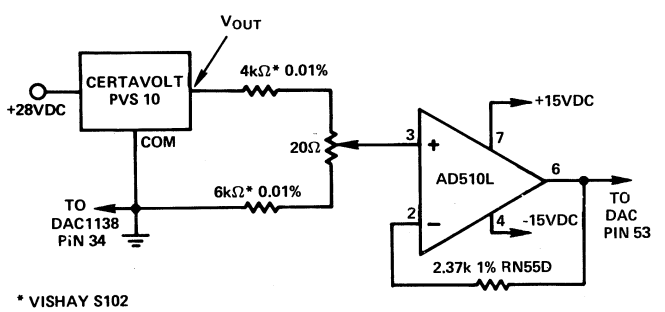
Figure 7. Output Circuit with Optional Amplifiers

IMPROVING LONG TERM STABILITY AND REFERENCE TEMPERATURE COEFFICIENT

The DAC1136/1138 can be operated with an external reference connected to pin 53 of the module. The current drain on the external reference will be 1.125mA. When an external reference is used, pin 52, the output of the internal reference is left open.

Codi Semiconductor manufactures a reference module called Certavolt [1] with a 10 volt output to within 10ppm (0.001%). This output is temperature compensated to within 1ppm/°C from +15°C to +55°C. The Certavolt requires a power supply of +28V dc @ 20mA. To convert the +10 volt output of the Certavolt to the +6 volts required by the DAC, the circuit shown in Figure 8 is recommended.

[1] Certavolt is a registered trade name by Computer Diode Corporation.

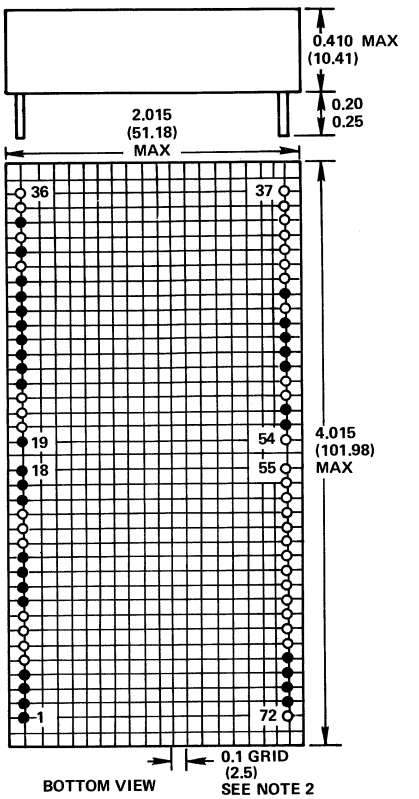


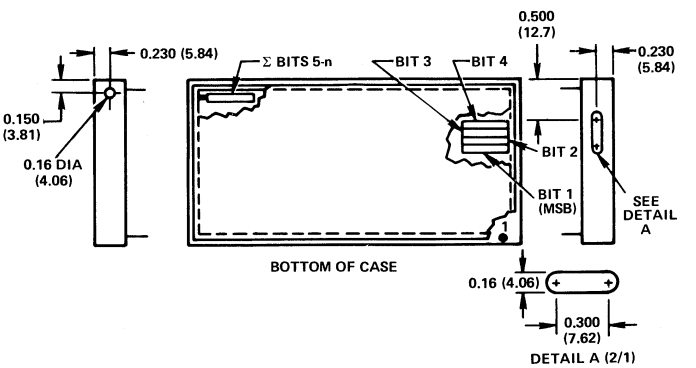
* VISHAY S102

Figure 8. DAC1138 with External Precision Reference

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

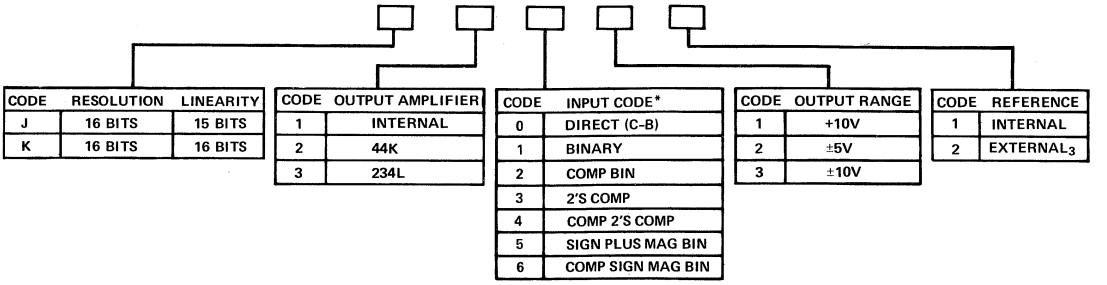
Dimensions shown in inches and (mm).





NOTES:
1. PINS: 0.019 ±0.001 DIA HALF HARD BRASS, GOLD PLATED PER MIL-G-45204B CLASS I, TYPE II.
2. GRID AND MARKINGS NEXT TO PINS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON UNIT.
3. PINS SHOWN FOR DAC1138

DAC1136 ORDERING GUIDE



CODE	RESOLUTION	LINEARITY
J	16 BITS	15 BITS
K	16 BITS	16 BITS

CODE	OUTPUT AMPLIFIER
1	INTERNAL
2	44K
3	234L

CODE	INPUT CODE*
0	DIRECT (C-B)
1	BINARY
2	COMP BIN
3	2'S COMP
4	COMP 2'S COMP
5	SIGN PLUS MAG BIN
6	COMP SIGN MAG BIN

CODE	OUTPUT RANGE
1	+10V
2	±5V
3	±10V

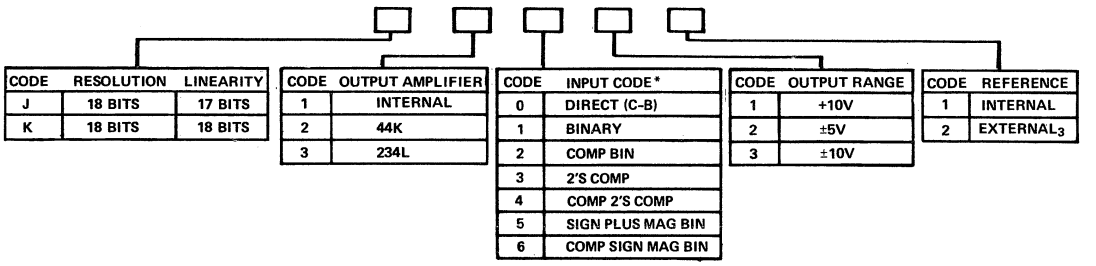
CODE	REFERENCE
1	INTERNAL
2	EXTERNAL$_3$

NOTES:

1. WHEN ORDERING THE DAC1136 WITHOUT THE CARD ASSEMBLY, ORDER EITHER DAC1136J OR DAC1136K.
2. WHEN ORDERING THE DAC1136 AS A CARD MOUNTED ASSEMBLY, THE PART MUST BE DESCRIBED WITH 5 SUFFIXES AS SHOWN ABOVE.
3. USER SUPPLIED THROUGH PIN ON EDGE CONNECTOR.

* TWO MOUNTING CARDS ARE AVAILABLE; A DIRECT INPUT VERSION (OPTION CODE Ø) WITHOUT INPUT REGISTER LATCHES, AND A REGISTER VERSION CONTAINING INPUT LATCHES WHICH IS SUPPLIED WHEN INPUT CODES 1 THRU 6 ARE ORDERED.

DAC1138 ORDERING GUIDE



CODE	RESOLUTION	LINEARITY
J	18 BITS	17 BITS
K	18 BITS	18 BITS

CODE	OUTPUT AMPLIFIER
1	INTERNAL
2	44K
3	234L

CODE	INPUT CODE*
0	DIRECT (C-B)
1	BINARY
2	COMP BIN
3	2'S COMP
4	COMP 2'S COMP
5	SIGN PLUS MAG BIN
6	COMP SIGN MAG BIN

CODE	OUTPUT RANGE
1	+10V
2	±5V
3	±10V

CODE	REFERENCE
1	INTERNAL
2	EXTERNAL$_3$

NOTES:

1. WHEN ORDERING THE DAC1138 WITHOUT THE CARD ASSEMBLY, ORDER EITHER DAC1138J OR DAC1138K.
2. WHEN ORDERING THE DAC1138 AS A CARD MOUNTED ASSEMBLY, THE PART MUST BE DESCRIBED WITH 5 SUFFIXES AS SHOWN ABOVE.
3. USER SUPPLIED THROUGH PIN ON EDGE CONNECTOR.

* TWO MOUNTING CARDS ARE AVAILABLE; A DIRECT INPUT VERSION (OPTION CODE Ø) WITHOUT INPUT REGISTER LATCHES, AND A REGISTER VERSION CONTAINING INPUT LATCHES WHICH IS SUPPLIED WHEN INPUT CODES 1 THRU 6 ARE ORDERED.

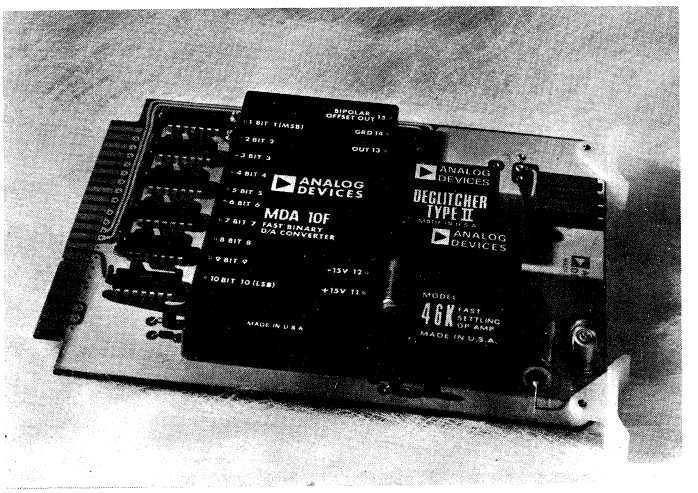
ANALOG DEVICES

Fast Display D/A Converter

DAC-10DF

FEATURES
Deglitcher
10-Bit Resolution & Accuracy
Monotonic
High Speed Settling to ±½LSB
40ns — 1LSB Step
200ns — Full Scale Step
Linearity ±½LSB
Coaxial Cable Connector Output
Schottky TTL Register Included

APPLICATIONS
Graphic Displays
Deflection Systems
Character Generators
High Speed D/A Systems

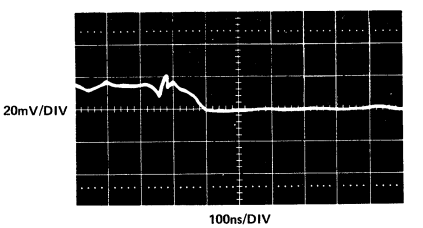


DESCRIPTION
The DAC-10DF is a 10-bit D/A converter that has a very fast settling, virtually glitch free, voltage output. These features make it a particularly good choice for use in CRT display systems. It is also well suited for other applications requiring high speed, glitchless operation, such as character generators, high speed test equipment, and very high speed A/D converters. A coaxial cable output is used to ensure that the DAC-10DF's high speed output signal is received exactly as transmitted. With a model 50 output amplifier, the output will settle to within ±½LSB in 40ns for 1LSB input change. Monotonicity is assured from +5°C to +45°C. Schottky TTL is used for the input register to increase speed and decrease time skew. Decreased register skew and a new deglitching circuit combine to practically eliminate the undesirable glitches which would otherwise occur at the major carry and other major transitions of the converter.

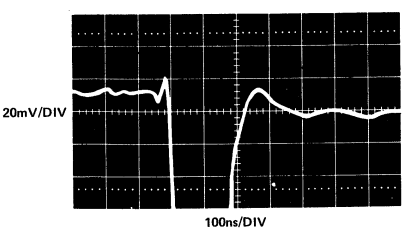
OUTPUT OPTIONS
The DAC-10DF is available with either a model 48K or a model 50K output amplifier. Both offer the same selection of output ranges, ±2.5V, ±5.0V, or ±10.0V. In either case, the amplifier's output is wired to a board mounted Microdot RF connector. The fast, high current output of the model 50 makes it suitable for driving a terminated 50 to 100Ω coaxial cable. Its 100mA output capability permits the high slew rates needed for good pulse transmission over a coaxial cable. The model 48K is a lower power amplifier, offering lower power supply current requirements. It may be used for driving higher impedance cables that don't require a high current source.

TIMING
The strobe pulse must have rise and fall times ⩽12ns, and a width of at least 50ns. The data inputs must remain constant from 10ns prior to until 10ns after the strobe pulse's leading edge. The digital input data is transferred from the input register to the D/A conversion circuitry approximately 20ns after the strobe pulse's leading edge.

GLITCH SUPPRESSION — DAC-10DF



WITH DEGLITCHER



WITHOUT DEGLITCHER

The two views above show the DAC-10DF during a major carry transition. Note that without the deglitcher, not only does the large glitch fly down way offscale, but also that the settling time is much longer.

SPECIFICATIONS (typical @ +25°C and nominal supply voltages, unless otherwise noted)

MODEL	DAC-10DF (With 48K Output Amplifier)	DAC-10DF (With 50K Output Amplifier)
RESOLUTION	10 Bits	*
Differential Linearity	±½LSB max	*
Monotonic	+5°C to +45°C Guaranteed	*
Linearity[1]	±½LSB max	*
LOGIC LEVELS	0 ≤ "0" ≤ +0.8V @ -2mA max	*
	+2.0 ≤ "1" ≤ +5.0V @ 80μA max	*
DIGITAL INPUTS	1 Schottky TTL Load/Bit	*
STROBE INPUT	Positive Pulse, 50 to 500ns, 1 Schottky TTL Load	*
CODING OPTIONS[2]	Offset Binary, Two's Complement	*
REFERENCE	Internal High Stability Reference Included	*
OPERATING TEMP. RANGE	0 to +70°C	*
OUTPUT OPTIONS	±2.5V, ±5.0V, ±10.0V @ 15mA max	±2.5V, ±5.0V, ±10.0V @ 100mA max
SETTLING TIME[3]		
For FS Step	500ns max	200ns max
For 1LSB Step	100ns max	40ns max
GLITCH	5mV Peak (max) 50ns Width (typ)	20mV Peak (max) 50ns Width (typ)
GAIN TEMPERATURE COEFFICIENT	±50ppm/°C of Reading (max)	*
ZERO TEMPERATURE COEFFICIENT	±20ppm/°C of FS (max)	±30ppm/°C of FS (max)
POWER REQUIREMENTS	+15V dc ±3% @ 80mA max	+15V dc ±3% @ 200mA max
	-15V dc ±3% @ 80mA max	-15V dc ±3% @ 200mA max
	+5V dc ±5% @ 400mA max*	*
SIZE & CONSTRUCTION	4.5" x 6.0" x 0.67" (114.3 x 152.4 x 17.02mm) PC Plug-In Card	*
MATING EDGE CONNECTOR	Cinch #250-22-30-170 (supplied)	*
MATING COAXIAL CONNECTOR	Microdot #132-0300-0003 (supplied)	*
ADJUSTMENTS	Gain	*
	Dynamic Zero (Glitch Suppression)	*
	Offset	*
GAIN ADJ. RANGE	±5% of Range	*

*Specifications same as for DAC-10DF with 48K amplifier.
[1] Deviation measured from the straight line through +Full Scale and -Full Scale.
[2] The unit is shipped connected for Offset Binary. The coding is determined by a jumper associated with 3 adjacent terminals on the PC board, lettered A, C, and B. B is jumpered to C for Offset Binary coding. A is jumpered to C for Two's Complement Coding.
[3] As measured with ±2.5 volt output, from trailing edge of clock pulse to point where output is within ±½LSB of final value.

Specifications subject to change without notice.

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
A	BIT 1 (MSB)	N	INTERLOCK
B	BIT 2	P	CONNECTIONS
C	BIT 3	R	+5V dc
D	BIT 4	S	
E	BIT 5	T	DIGITAL GROUND
F	BIT 6	U	
H	BIT 7	V	ANALOG GROUND
J	BIT 8	W	
K	BIT 9	X	+15V dc
L	BIT 10 (LSB)	Y	-15V dc
M	STROBE	Z	ANALOG GROUND

CIRCUIT CONNECTIONS

The DAC-10DF's output is connected to a coaxial cable via a Microdot RF connector. A 93Ω RG 195 cable or its equivalent is recommended. For optimum received signal shape, the receiving end of the cable must be terminated into a purely resistive load that has a resistance equal to the characteristic impedance of the cable. Because of this requirement, the ±10V output option cannot be used with a cable that has a characteristic impedance of <93Ω. In such an instance, the current required would exceed that available from the DAC-10DF. In order to prevent the possibility of a ground loop through the coaxial cable's shield, the DAC-10DF and the circuitry it drives should be powered by separate power supplies having no common connection. It is recommended that the ±15V dc power supply feeding the DAC-10DF have no other loads connected to it. The power supply should have an ac output impedance at 10kHz of <1Ω.

Normally, the digital and analog grounds of a D/A converter would be brought out separately, run to a common point, and then joined together. However, because of the DAC-10DF's exceptionally high speed, the inductance of the ground leads is likely to cause noise in the converter's output. Therefore, the digital and analog grounds are tied together on the DAC-10DF's PC board. The IR drop along common digital and analog ground leads that may cause problems with higher resolution (e.g., 14 or 16 bit) DAC's is not likely to be troublesome to a 10 bit DAC.

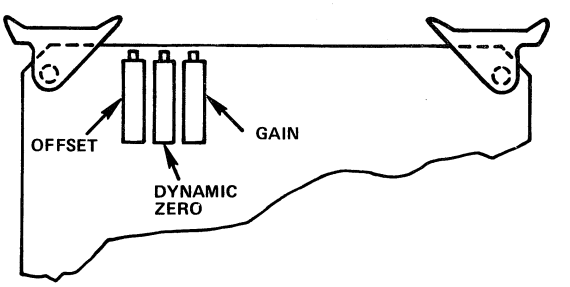
Because of the very high speed of the Schottky TTL input registers, it is possible that the digital input signals could be reflected back and forth between the DAC-10DF's inputs and their driving sources. This might result in a wavefront that builds up sufficient voltage to damage some of the logic. Driving the logic inputs with transmission lines, and terminating each cable at the DAC-10DF's socket with a resistor (equal to the characteristic impedance of the cable) in series with a 220pF capacitor between each input and ground will prevent these reflections.

ORDERING INFORMATION

DAC-10DF/XX/XX

Output Range	±2.5 Volts:	2.5
	±5.0 Volts:	5.0
	±10.0 Volts:	10
Output Amplifier	Model 48K:	48
	Model 50K:	50

POTENTIOMETER ADJUSTMENTS



High Resolution, Digital to Analog Converter

DAC-14/16QM, DAC-QG

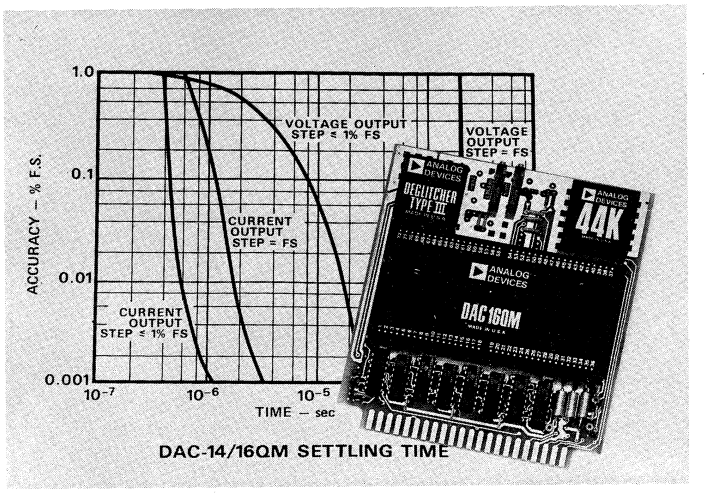
FEATURES

DAC-14/16QM

- **16 Bit Resolution**
- **Linearity Error Less Than: ±0.0015% (16 Bit Model)**
  ±0.003% (14 Bit Model)
- **Monotonic**
- **Compact 2" x 4" x 0.4" Module**
- **DTL/TTL Compatible**

DAC-QG

- **Versatile Input Register**
- **Many Code Options**
- **Optional Amplifiers for Fastest Settling or Highest Stability**
- **Optional Transient Suppressor**
- **4 Terminal Output Connection**



DAC-14/16QM SETTLING TIME

GENERAL DESCRIPTION OF THE DAC-14/16QM

The DAC-14/16QM high resolution digital to analog converters are compact 2" x 4" x 0.4" modules that offer true state-of-the-art performance in applications demanding the utmost in resolution and accuracy. Both units feature 16 bit resolution. The DAC-14QM has a maximum linearity error of 0.003% (at +25°C) while the DAC-16QM has a maximum linearity error of only 0.0015% (at +25°C).

DESCRIPTION OF THE DAC-QG

The DAC-QG is a manifold board which accepts any DAC-QM from 8 to 16 bits and offers several optional circuit supplements. The library of options includes: a "deglitcher" for limiting switching transients to 2 millivolts; a versatile input register with provisions for one of five input codes; and a choice of high-performance discrete output amplifiers to attain either optimum settling time, optimum stability, or lowest cost by using the IC amplifier contained in the DAC-QM. The DAC-QG also contains the offset and gain adjust potentiometers required by the DAC-QM.

DESIGN CONSIDERATIONS

Extreme care is required in the design, production, and application of converters such as the DAC-14/16QM/QG in order to insure that the fine resolution, broad dynamic range, and the high degree of accuracy and linearity expected of these precision devices is actually achieved. Factors of only secondary concern in the design of 12 bit converters can have an overwhelmingly adverse impact on the operation of a 16 bit unit. Consider the fact that a 16 bit converter with a 10VFS output range has an LSB of only 153μV! Problems such as thermocouple effects, voltage drops in connectors, low level noise, radio frequency interference and output amplifier temperature drift simply cannot be ignored. Several practical installation guidelines are offered in the following sections to help the user avoid these problems. Reprints of a two part series written for Electronics magazine by the staff of Analog Devices, Inc. discussing the details of high resolution data conversion are also available to aid in the application of these devices.

PERFORMANCE

Analog Devices, Inc. is committed to an extensive testing program which assures the customer that every unit received is truly the precision device described in this data sheet. Some very visible results of this program are the three documents shipped with every converter. The first certifies calibration with methods and equipment traceable to the National Bureau of Standards. The second certifies the performance of the converter's internal reference zener over temperature and over 1000 hours of burn-in. The third shows the actual linearity deviation of the converter by means of a recording which plots the difference between the converter's output and the output of a super-precision DAC at each of the 65,536 possible input words.

Ten-thousand hours of testing were also performed in order to actually measure the long-term stability of these devices. The impressive result was a linearity shift of less than 8ppm/10,000 hours!

SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

MODEL	QM	QG (THE QM ON A CARD MOUNTED ASS'Y) WITH IC AMP	WITH 184L	WITH 44K
RESOLUTION	16 Bits	*	*	*
LINEARITY				
(Straight Line – Zero to FS)	Monotonic	*	*	*
DAC-16 XX	±<0.0015%	*	*	*
DAC-14 XX	±<0.003%	*	*	*
DIGITAL INPUTS				
(DTL/TTL Compatible)				
Logic "0"	0V <E_0 <+0.8V @ –3mA	0V <E_0 <+0.8V @ –1.6mA	**	**
Logic "1"	+2.0V <E_1 <+5.0V @ 10μA	+2.0V <E_1 <+5V @ 20μA	**	**
CODE OPTIONS	Compl. Binary (CB)	Binary, BCD, 2's Compl. BIN,	**	**
	Compl. BCD (CBD)	Sign Plus Mag. BIN/BCD	**	**
OUTPUT				
Current Mode	0 to –2mA (CB) (CBD)	Voltage Mode Output Only		
	±1mA (CB)			
Source Impedance	15,000Ω ±0.01% (CB)			
	9,000Ω ±0.01% (CBD)			
Voltage Mode	0 to +10V (CB) (CBD)	0 to +10V (Unipolar Codes)	*	*
	±5V, ±10V (CB)	±5V, ±10V (Bipolar Codes)	*	*
Output Impedance	<1Ω	*	<0.001Ω	<0.05Ω
Output Current	±1mA (Int. Amp)	*	±2mA	±10mA
DYNAMIC RESPONSE				
Current Mode		Voltage Mode Output Only		
Settling Time	(See Figure 1)			
Peak Noise (worst case)	50% FS, 300ns			
rms Noise (10Hz to 1MHz)	±50μV			
Voltage Mode				
Settling Time	(See Figure 1)	(see Figure 2a, 2b)	*	*
Peak Noise (worst case)	2% FS, 5μs	(see Figure 3)	*	*
rms Noise (10Hz to 1MHz)	<0.0001% FS	*	<0.0002% FS	
REFERENCE				
Internal	+6.00V ±0.01% (±5ppm/°C)	*	*	*
ADJUSTMENTS				
Gain	(User Supplied)	(Provided)	**	**
Unipolar Offset	50Ω Pot	≈0.1% FS Range	**	**
Bipolar Offset	100kΩ Pot	≈0.07% FS Range	**	**
Dynamic Zero	20Ω Pot	≈0.15% FS Range	**	**
POWER REQUIREMENTS				
+5V dc ±10%	@ 40mA	@ 220mA	*	*
+15V dc ±2%	@ 20mA	@ 35mA	*	*
–15V dc ±2%	@ 50mA	@ 65mA	*	*
POWER SUPPLY SENSITIVITY[2]				
Current Mode		Voltage Mode Output Only		
Gain	±7ppm			
Unipolar Offset	±<1ppm			
Bipolar Offset	±<7ppm			
Voltage Mode				
Gain	±7ppm	±<10ppm	±<15ppm	±<30ppm
Unipolar Offset	±<2.5ppm	±<4ppm	±<1ppm	±<10ppm
Bipolar Offset	±5ppm	±<10ppm	±<7ppm	±<15ppm
TEMPERATURE COEFFICIENT				
(Expressed in ppm of FS/°C)				
Gain	±<1ppm (exclusive of reference)	±15ppm[3]	±7ppm[3]	±30ppm[3]
Unipolar Offset	±<1ppm	±9ppm	±0.5ppm	±25ppm
Bipolar Offset	±<3ppm	±15ppm	±7ppm	±7ppm
RECOMMENDED RECALIBRATION				
Interval		30 Days	*	*
TEMPERATURE RANGE				
Operating Within Specs	+20°C to +30°C	*	*	*
Operating	0 to +70°C	*	*	*
Storage	–55°C to +125°C	*	*	*
DIMENSIONS	Module: 2" x 4" x 0.4"	CARD: 4½" x 4¾"	**	**

[1] 16 Bit BCD (4 decimal digits) priced same as 14 Bit Binary.
[2] Expressed in ppm of FS/% change in ±15V supplies.
[3] Includes ±5ppm for reference.

*Specifications same as QM.
**Specifications same as QG with IC Amp.
Specifications subject to change without notice.

INSTALLATION

The following installation guidelines are offered to help minimize the potential causes of error discussed previously:

1. Locate the unit and the wiring to its connector so as to provide optimum isolation from sources of RFI and EMI.
2. Attempt to locate the unit and its connector in a plane of thermal equipotential. It must be appreciated that popular electronic wiring materials usually involve different metals, and the junctions will act as thermocouples if they are located in regions of differing temperature.
3. It is important to connect the +5V logic supply common (usually a carrier of pulse noise) to the analog supply common at a point that minimizes system noise.
4. When using the DAC-QG, the user must properly connect the four-terminal output amplifier to allow inherent circuit compensation for contact resistance.

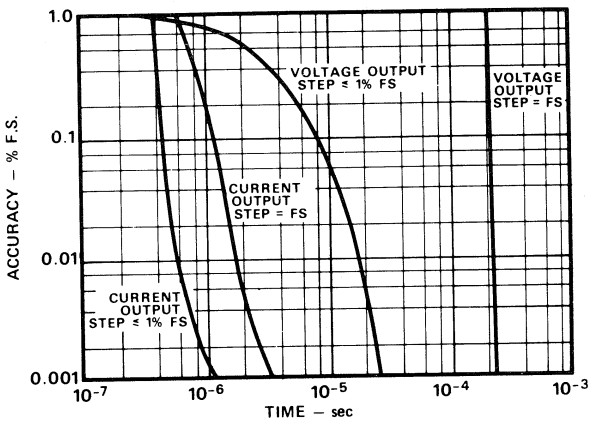


Figure 1. DAC-14/16QM Settling Time

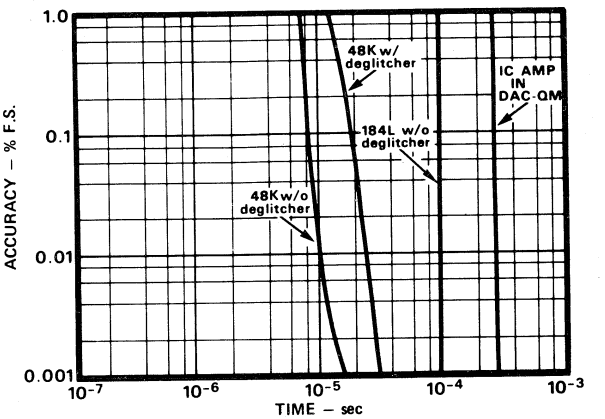


Figure 2a. Settling Time DAC-16QG, Step ∓FS to ±FS

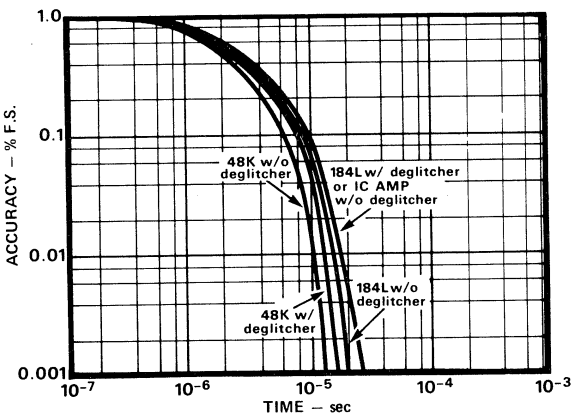


Figure 2b. Settling Time DAC-16QG, Step ≤1% FS

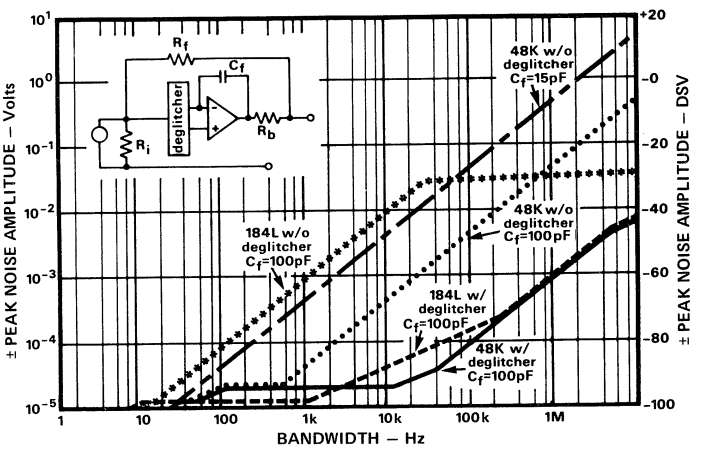


Figure 3. DAC-16QG, ±Peak Noise vs. Bandwidth

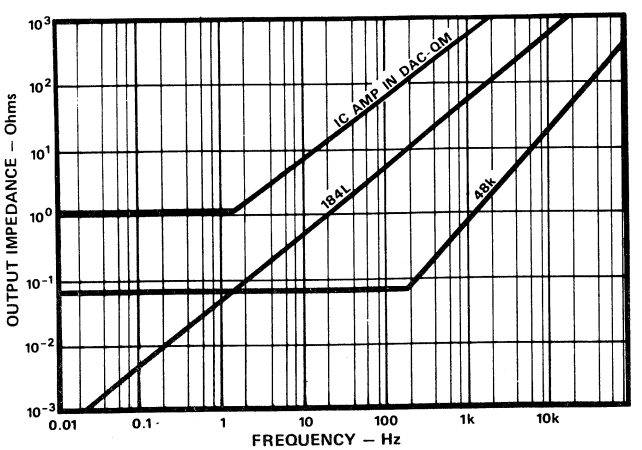


Figure 4. Output Impedance vs. Frequency

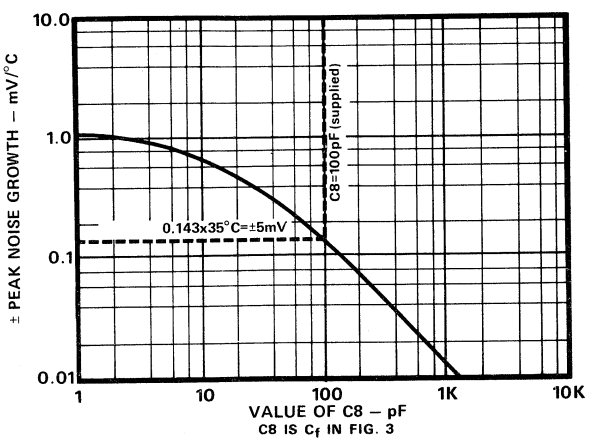


Figure 5. ±Peak Noise Growth per °C vs. Value of C8 (cf) when using Deglitcher

INPUT CODING

The DAC-14/16QM accepts data directly at its μDAC switch inputs and is available with either complementary binary (used as complementary offset binary for bipolar operation) and complementary BCD codes.

OUTPUT PROGRAMMING

The output amplifier circuit of the DAC-14/16QM is jumper programmed at the module terminals, allowing the user to determine which of the three possible output ranges will be used. Feedback resistance value is determined according to the following table by jumpers at pins 68 and 70 which provide 10k (8k for BCD units) and 5k ohms respectively.

OUTPUT RANGE	FEEDBACK RESISTOR	OFFSET ADJUST	ZERO ADJUST
0 to +10V	Complementary Binary: Connect 47 to 70 Complementary BCD: Connect 47 to 68	Ground 46	Connect 71 to Zero Adjust Pot
±10V	Complementary Offset Binary: Connect 47 to 68	Connect 44, 46 to Offset Adjust Pot	Not Connected
±5V	Complementary Offset Binary: Connect 47 to 70	Connect 44, 46 to Offset Adjust Pot	Not Connected

RANGE PROGRAMMING TABLE

ADJUSTMENT PROCEDURE

A voltmeter capable of 1/10LSB resolution and accuracy (e.g., 15μV for a 16 bit DAC) at both ends of the DAC-QM's output range is required. The accuracy of the converter subsequent to calibration is directly dependent upon the accuracy of the voltmeter.

The user must supply a 50Ω gain adjust pot (connected as shown in Figures 6, 7). This is used to adjust the output range to desired full scale values after the zero point has been set.

For unipolar (0 to +10V) operation, the user must supply a 100kΩ zero adjust pot (connected as shown in Figure 6) in addition to the gain adjust pot. To adjust the zero point apply the input code that should result in an output of zero. Adjust the zero pot until an output of 0V ±1/10LSB is obtained.

For bipolar operation (±5V, ±10V) the user must supply a 20Ω offset adjust pot (connected as shown in Figure 7) in addition to the gain adjust pot. To adjust the zero point, apply the input code that should result in an output of zero. Adjust the offset pot until an output of 0V ±1/10LSB is obtained.

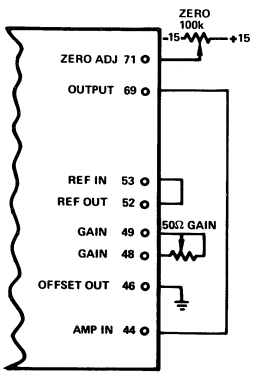


Figure 6. Connections for Unipolar Operation

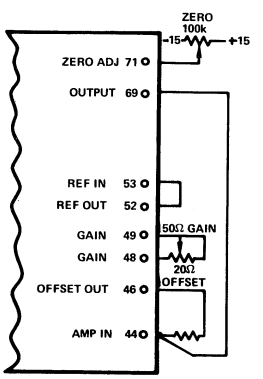
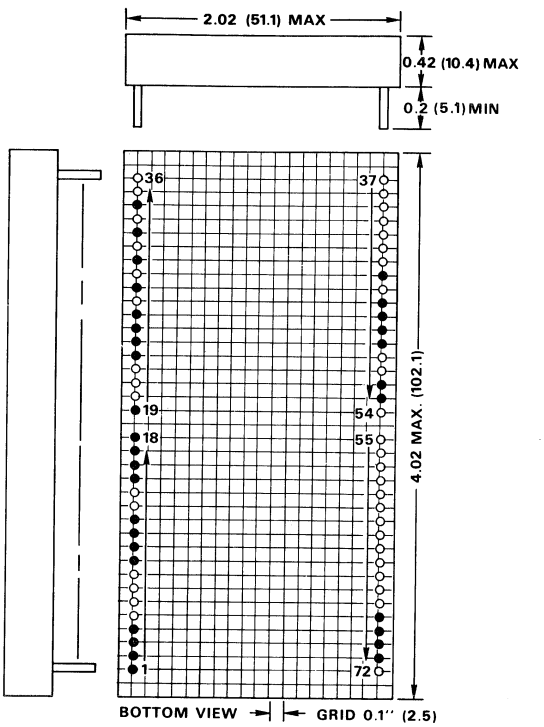


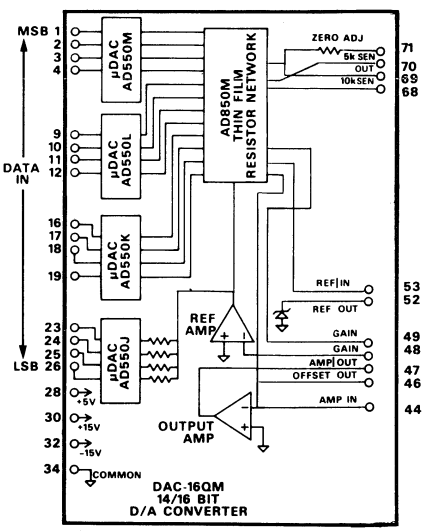
Figure 7. Connections for Bipolar Operation

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).



BLOCK DIAGRAM AND PIN DESIGNATIONS



ORDERING GUIDE:

DAC-	XX Linearity	QM	/XXX
	14 Bits 16 Bits		C-B (Complementary Binary) CBD[1] (Complementary BCD)

Note:
[1] CBD available only in 16-bit resolution

INPUT OPTIONS

The DAC-QG can be ordered with direct input, or in the case of the 14/16 bit models with the optional input register. When direct input is chosen, the user may only select one of the codes which is standard for the particular DAC-QM which is mounted. When the optional input register is chosen, the user may select any one of the following codes: Binary, 2's Complement, Sign plus Magnitude Binary, BCD, Sign plus Magnitude BCD. The code ordered by the user is set at the factory by means of various jumpers in the logic circuitry.

STROBE CHARACTERISTICS OF OPTIONAL REGISTER

Figure 8 shows the idealized strobe characteristics of the optional input register. The system utilizes a dynamic strobe circuit, transferring input data to the register essentially at the time of the leading edge of the strobe pulse. Due to the extremely wide dynamic range of operation of the DAC-16QG, it is an important consideration to operate all circuits in optimum noise modes. For instance, the DAC-16QG will operate when its strobe rise time is faster than indicated, but the larger high frequency content on the fast leading edge is liable to leak through the circuit, and cause detectable noise at the output. In the same way, noise caused by the strobe trailing edge is inherently minimized by the circuit unless the trailing edge occurs much longer than 500ns after the leading edge. Here again, the circuit will work properly with the long strobe, but it is likely that detectable noise will appear at the output.

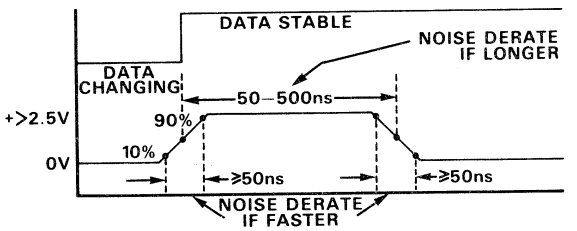


Figure 8. DAC-14/16QG Strobe with Optional Input Register

CONVERTER OPTIONS

The DAC-QG is normally ordered with the DAC-14/16QM. However, any converter in the DAC-QM line, such as the DAC-12QM, could be used, thereby providing it with transient suppression and a high performance output amplifier.

OUTPUT OPTIONS

The user can choose one of three standard output amplifier options. The first is the economical IC amplifier internal to the DAC-QM module; the second is the ultra-low drift model 184L chopperless amplifier, and the third is the fast settling model 44K amplifier.

Regardless of the amplifier chosen, the user may select any one of three output ranges by installing jumpers between terminals on the circuit board. Figure 9 shows the location of these terminals. The range programming table shows the proper connections to make to obtain the desired output range.

When the 2's complement or the Sign plus magnitude binary codes have been chosen, the ±5V or ±10V range may be used. When the Binary or BCD codes have been chosen, the +10V range may be used. When the Sign plus magnitude BCD code is used, the ±10V connections are made. However, the output range for the 16 bit converter will actually be ±8V which corresponds to the maximum code of ±7.999 for the 15 bits plus sign.

The Deglitcher Type II is also available as an option to limit converter switching transients to 0.2 millivolts. Since these switching transients are seen in all digital to analog converters due to the fact that switch turn-off time is not exactly the same as switch turn on time, the Deglitcher Type II is a key contributor to true state-of-the-art performance in the DAC-QG.

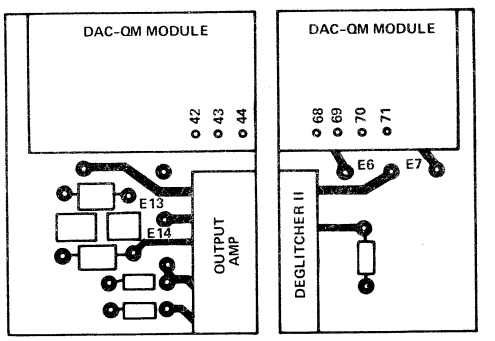


Figure 9. Top View of Portions of Circuit Board Showing Locations of Range Program Jumpers

JUMPER	E6	E7	E13	E14
0 to +10V	Not Connected	Connected	Not Connected	Connected
±5V	Not Connected	Connected	Connected	Not Connected
±10V	Connected	Not Connected	Connected	Not Connected

RANGE PROGRAMMING TABLE

OUTPUT CONNECTIONS

A four terminal output connection is utilized on the DAC-QG in order to allow inherent circuit compensation of connector contact resistance. To take advantage of this feature, the user must make connection of the "sense" lines (terminals 18 and 21) as close as possible to the actual loads.

It is important to connect the +5V logic supply common (usually a carrier of pulse noise) to the analog supply common at a point that minimizes system noise. The commons are kept isolated in the DAC-QG.

Figure 10 illustrates the proper output and grounding connections.

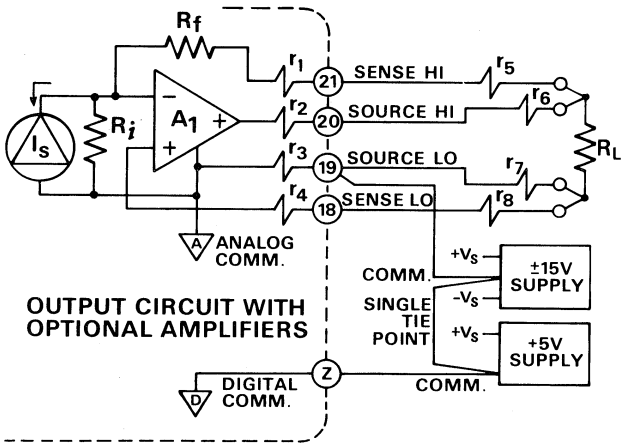


Figure 10. Output and Grounding Connections

ADJUSTMENT PROCEDURE

A voltmeter capable of 1/10LSB resolution and accuracy (e.g., 15μV for a 0 to +10V, 16 bit DAC) at both ends of the DAC-QG's output range and an oscilloscope are required. The accuracy of the converter subsequent to calibration is directly dependent upon the accuracy of the voltmeter.

The zero adjustment should be made first, followed by the offset adjustment, and then the gain adjustment.

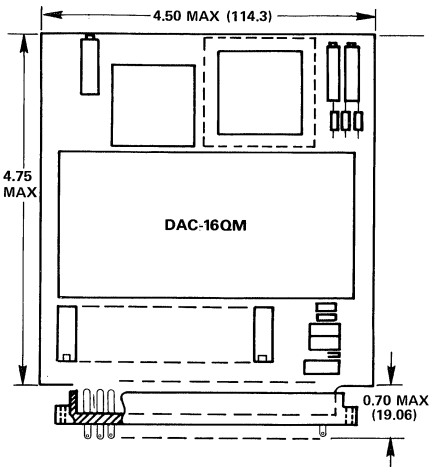
Zero adjustment (R3): with an oscilloscope connected to the DAC-QG's output, and any input code, apply a repetitive strobe pulse to the strobe input. Adjust R3 to minimize the height of glitches that occur with each strobe pulse.

Offset adjustment (R2): connect the voltmeter to the DAC-QG's output. For unipolar units, strobe the input code that should result in an output of zero. Adjust R2 until the converter's output is within ±1/10LSB of zero. For bipolar units, strobe in the code that should give minus full scale. Adjust R2 until the output reads minus full scale within ±10LSB. If the offset adjustment potentiometer's range is not sufficient to complete the adjustment, back it off one revolution and use the zero adjustment potentiometer (R3) to finish the adjustment.

Gain adjustment (R4): strobe in the input code that should give a positive full scale output. Adjust R4 until the DAC-QG's output reads plus nominal full scale minus 1LSB within ±1/10LSB.

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (cm).



CINCH CONNECTOR 251-22-30-160 (SUPPLIED)

PIN	FUNCTION	PIN	FUNCTION
1-17	N.C.	K	BIT 9
18	ANALOG SENSE LOW	L	BIT 10
19	ANALOG SOURCE LOW	M	BIT 11
20	ANALOG SOURCE HIGH	N	BIT 12
21	ANALOG SENSE HIGH	P	BIT 13
22	ANALOG REF. IN/OUT	R	BIT 14
A	BIT 1 (MSB)	S	BIT 15
B	BIT 2	T	BIT 16 (LSB)
C	BIT 3	U	STROBE
D	BIT 4	V	N.C.
E	BIT 5	W	+5V
F	BIT 6	X	+15V
H	BIT 7	Y	-15V
J	BIT 8	Z	GRD

ORDERING GUIDE

DAC-XX QG / XXX / XXX / XXXX / XXX / XXXX

INPUT		OUTPUT AMPLIFIER	
REG	REGISTER	STND	INTERNAL AMP
DIR	DIRECT	FAST	44K
		STAB	184L

LOGIC CODE	
BIN	BINARY
2SC	TWO'S COMPLEMENT
SMB	SIGN PLUS MAGNITUDE BINARY
BCD	BINARY CODED DECIMAL
SMD	SIGN PLUS MAGNITUDE BCD

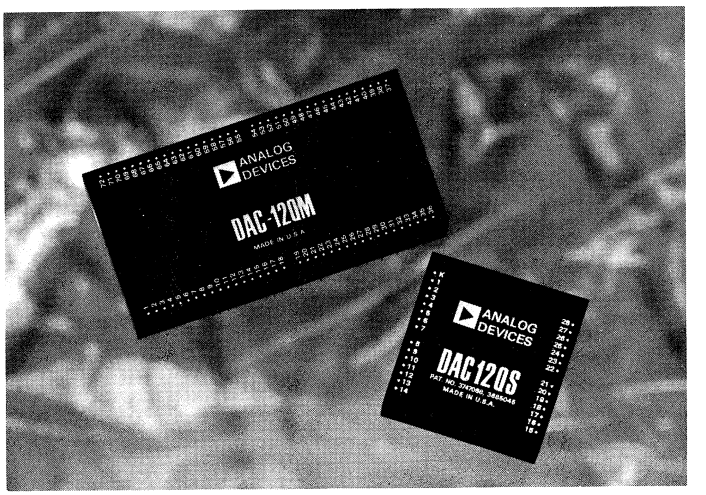
RESOLUTION	REFERENCE	
08	INT	INTERNAL
10	EXT	EXTERNAL
12		
14		
16		

DEGLITCHER	
DEGL	DEGLITCHER II (USE WITH FAST OR STAB AMP)
NONE	NO DEGLITCHER (USE WITH ANY AMP)

High Performance Digital to Analog Converters

DAC-QM, -QS

FEATURES
- 8-, 10-, 12-Bit Resolutions and Accuracies
- Low TC (±7ppm/°C)
- Complete with Register (DAC-QM)
- Binary or BCD Coding
- Output Range Customer Programmed
- Output Ranges Available: +5V, +10V, ±2.5V, ±5V, ±10V
- Excellent Power Supply Rejection (0.002%/% V_S)
- Low-Profile Modules



The DAC-QM

The DAC-QM is a complete self-contained digital-to-analog converter module, available in 8-, 10-, and 12-bit versions. Complete with strobed data entry to the input register, the module is offered wired for a variety of binary codes as well as BCD. Logic levels are compatible with DTL and TTL. The output amplifier circuit is exceptionally versatile, utilizing jumper programming at the module terminals to allow the user to determine the output range and offset. The DAC-QM module also contains monolithic μDAC current switches, a thin film resistor network, and a reference supply with amplifier.

THE DAC-QS

The DAC-QS is a much smaller module without input register, but is nonetheless a complete digital-to-analog converter in all respects, and is also available in 8-, 10-, and 12-bit versions. The internal μDAC AD550 converter switches are driven directly by complementary binary and complementary BCD input logic, without need for a strobe. In all other respects, the DAC-QS is electrically identical to the DAC-QM.

GENERAL DESCRIPTION

The DAC-QM and DAC-QS are module versions of the popular DAC-Q card mounted D/A converter. Each is a complete converter, containing the IC μDAC AD550 quad current switches, precision thin film resistor networks, reference, supply with amplifier, and the versatile output operational amplifier. The units are electrically identical, except for omission of the input register from the DAC-QS, in order to allow a package with appreciably reduced dimensions. For operation, they require only input data, DC power, and trimmer potentiometers for zero and gain.

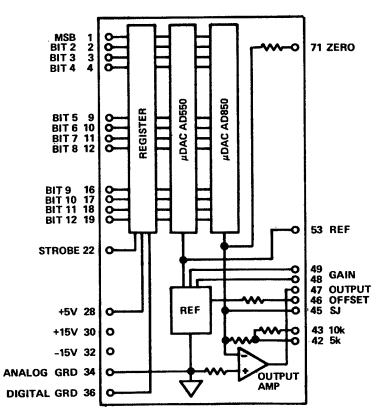
INPUT OPTIONS

The input storage register built into the DAC-QM can be provided for a variety of codes. Binary, 2's complement and Binary-Coded-Decimal are all offered. Special input coding is not required for Offset codes, such as Offset Binary. The DAC-QS, having no input register, accepts complementary binary code and complementary BCD.

OUTPUT PROGRAMMING

Provisions for variations in output characteristics are exceptionally versatile. By means of jumpers between terminals of the module, the user can select any one of five combinations of range and offset, to comply with the needs of the application. The choices are:

Unipolar: 0 to +5V, 0 to +10V
Bipolar: ±2.5V, ±5V, ±10V



DAC-QM Block Diagram and Pin Designations

SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

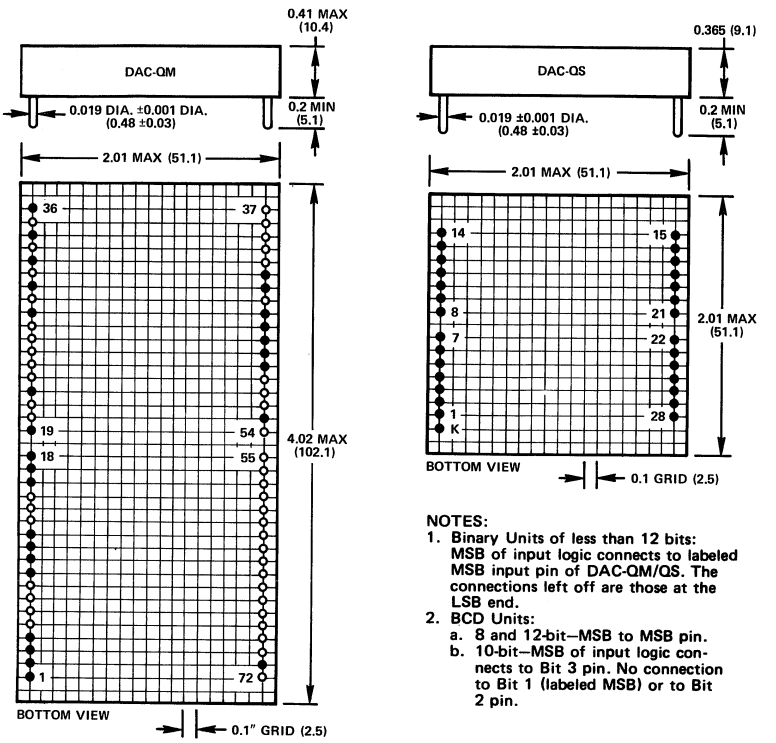
MODEL	DAC-QM	DAC-QS
RESOLUTION	-8QM 8-bits -10QM 10-bits -12QM 12-bits	-8QS 8-bits -10QS 10-bits -12QS 12-bits
DIGITAL INPUTS "0" E<+0.8V "1" +2<E<+6V	@ -3.2mA @ +80μA TTL Compatible	@ -1.6mA @ +100μA max *
STROBE	Data Transfers from Inputs to Register on "0" to "1" Change. Width at Least 50ns, "0–1" Transition at Least 100ns After Data Change.	No Strobe
INPUT CODES	Binary, 2's Complement, BCD	Compl. Binary & Compl. BCD
OUTPUT RANGES (User Programs With Jumpers) 0 to 5V ±2.5V, ±5V 0 to +10V ±10V	@ 10mA @ 5mA	* *
OUTPUT IMPEDANCE	0.02Ω	*
CONVERSION SPEED Slewing Rate	5μs to 0.01% 20V/μs	* *
LINEARITY	±½LSB	*
TEMP. COEFFICIENT Linearity Gain Zero	±3ppm/°C of Reading max ±7ppm/°C max ±15μV/°C max	* * *
TEMP. RANGE Standard Optional	0 to +70°C -55°C to +125°C	* *
POWER REQUIRED	+15V dc @ +25mA -15V dc @ -30mA +5V dc @ +150mA	* * +5V dc @ +35mA
POWER SUPPLY SENSITIVITY	0.002%/% supply ΔE (±15V dc Supplies Only)	*
ADJUSTMENTS (User Provides) Gain Adj. Zero Adj	100Ω Pot 20kΩ Pot	20kΩ Pot *

*Specifications same as model DAC-QM

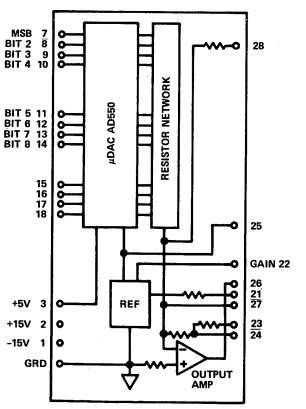
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES:
1. Binary Units of less than 12 bits: MSB of input logic connects to labeled MSB input pin of DAC-QM/QS. The connections left off are those at the LSB end.
2. BCD Units:
   a. 8 and 12-bit—MSB to MSB pin.
   b. 10-bit—MSB of input logic connects to Bit 3 pin. No connection to Bit 1 (labeled MSB) or to Bit 2 pin.

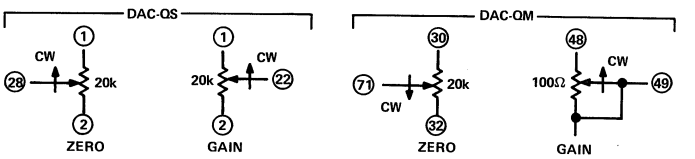


DAC-QS Block Diagram and Pin Designations

GAIN AND ZERO ADJUSTMENT

For units utilizing bipolar codes apply the digital input corresponding to the negative full scale analog output and adjust the zero pot until the proper value is obtained with ±1/10LSB. For unipolar codes apply 00 . . 0 and adjust for 0V out.

For all units, once the appropriate zero adjustment has been made apply the digital input corresponding to the positive full scale analog output. Adjust the gain pot until the proper value is obtained within ±1/10LSB.



Potentiometer Connections for Zero and Gain Adj.

ORDERING GUIDE: DAC-QM AND DAC-QS

Model No. DAC XX XX / XXX / XX

	No. of Bits	Series	Input Code	Temp Range
Conv. Type	8 10 12	QM QS[1]	BIN (binary) C-B (comp. binary)[1] 2SC (2's comp.) BCD CBD (comp. BCD)[1]	SN (Standard) ET (Extended)[2]

[1] DAC-QS available ONLY with Complementary Binary or Complementary BCD. These codes not available in DAC-QM.
[2] Use model number suffix ET (for extended temperature).

OUTPUT CONNECTIONS

Output Range	Pins Jumpered Together Bipolar Offset		Feedback Res.	
	QM	QS	QM	QS
±10V	45, 46	27, 21	47, 43	26, 23
±5V	45, 46	27, 21	47, 42	26, 24
±2.5	45, 46	27, 21	45, 43 42, 47	27, 23 24, 26
+10V	46, 34	21, 5	42, 47 45, 43	24, 26 27, 23
+5V	46, 34	21, 5	42, 47	24, 26

MOUNTING BOARDS[1]

DAC-QM	DAC-QS
P/N 4494-1	4516

[1] Mates with Cinch P/N 250-22-30-170 (Supplied)

Low Cost General Purpose Digital to Analog Converter

DAC-12QZ

FEATURES
- Low Cost
- 12 Bit Resolution
- ½LSB Linearity
- ±30ppm/°C TC
- 20ppm/% Power Supply Rejection
- Programmable Output Ranges
- Small Size – 2" x 2" x 0.4"

GENERAL DESCRIPTION

The DAC-12QZ is a low-cost/high performance 12-bit digital-to-analog converter designed for general purpose OEM applications. The completely self-contained module includes weighted resistor networks, monolithic μDAC current switches, temperature compensated reference and an externally programmable output amplifier. Performance specifications include ½LSB linearity error, 5μs settling time for full scale conversion, 30ppm/°C temperature coefficient and 20ppm/% power supply rejection.

μDAC DESIGN

This outstanding cost/performance ratio has been achieved by utilizing the popular AD550 μDAC current switches. The use of monolithic quad current switches offers close inherent matching of switch characteristics and excellent temperature tracking as well as reasonably fast conversion speed. A hybrid resistor assembly of matched precision resistors and a thick film network is used in conjunction with the μDAC switches. Resistors provided include not only the weighting resistors but also the inter-quad attenuators, amplifier feedback resistors, etc. to assure close temperature tracking.

INPUT CODING

The internal μDAC switches of the binary and BCD models are driven directly by complementary input codes without need of a strobe. The complementary codes for each model are:

MODEL	-F.S.	Zero	+F.S.
DAC-12QZ/BIN		1111 1111 1111	0000 0000 0000
	1111 1111 1111	0111 1111 1111	0000 0000 0000
DAC-12QZ/BCD		1111 1111 1111	0110 0110 0110
	1111 1111 1111	1010 1111 1111	0110 0110 0110

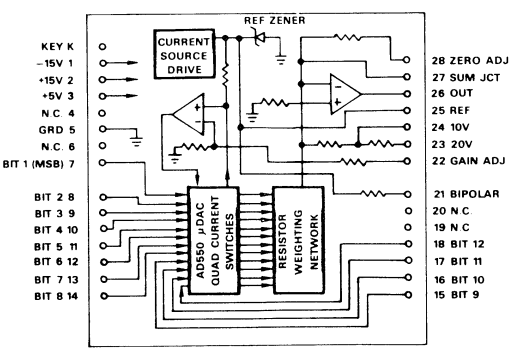
OUTPUT PROGRAMMING

The scale factor is programmed by connecting external jumpers between module pins. With either model, the user can select any one of five output ranges, including bipolar outputs. The choices are:

Unipolar	0 to +5V, 0 to +10V
Bipolar	±2.5V, ±5V, ±10V

The external jumpers at the module pins determine the output amplifier feedback resistance, allowing use of one 5k resistor, or both, either in series to provide 10k, or parallel to provide 2.5k. Offset of exactly one-half full scale for bipolar applications is provided by connecting another jumper to the summing junction of the output amplifier. To maintain constant load on the reference zener, the bipolar offset output should be grounded when using the module in a unipolar mode.

BLOCK DIAGRAM
DAC-12QZ



NOTE: PINS SHOWN AS HAVING NO CONNECTIONS (N.C.) ARE DELETED.

SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

RESOLUTION	12 Bits
DIGITAL INPUTS	TTL Compatible
'O' E <+0.8V	@ -1.6mA
'1' +2V<E<+6V	@ +0.1mA (open input equivalent to digital "1")
INPUT CODES	
Unipolar	Complementary Binary Complementary BCD
Bipolar	Complementary Offset Binary Complementary Offset BCD
OUTPUT RANGES	0 to +5V @ 10mA 0 to +10V @ 5mA
(User Programmable)	±2.5V, ±5V @ 10mA ±10V @ 5mA
OUTPUT IMPEDANCE	0.02Ω
CONVERSION SPEED	5μs to 0.01% (for 10V step)
Slewing Rate	20V/μs
LINEARITY ERROR	±½LSB
TEMPERATURE COEFFICIENT	
Gain	±30ppm/°C of Reading, max
Zero	±50μV/°C (Unipolar), max ±100μV/°C (Bipolar), max
Differential Linearity	±10ppm/°C F.S., max
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +125°C
POWER REQUIREMENTS[1]	+15V ±5% @ 25mA -15V ±5% @ 30mA +5V ±10% @ 35mA
POWER SUPPLY SENSITIVITY	
Gain	±20ppm/% } ±15V only;
Zero	±5ppm/% } tracking supplies
ADJUSTMENTS (USER PROVIDED)[2]	
Gain (20k, 20 turn pot)	±0.3% F.S.
Zero (20k, 20 turn pot)	±30mV
OUTLINE DIMENSIONS	2" x 2" x 0.400"

[1] Recommended Power Supply: Analog Devices models 904 and 906.
[2] A mounting board complete with trim pots and supplied with mating connector is available at extra cost. Order Part No. AC4516,
Pin Socket – 2-330808-8, 25 required

Specifications subject to change without notice.

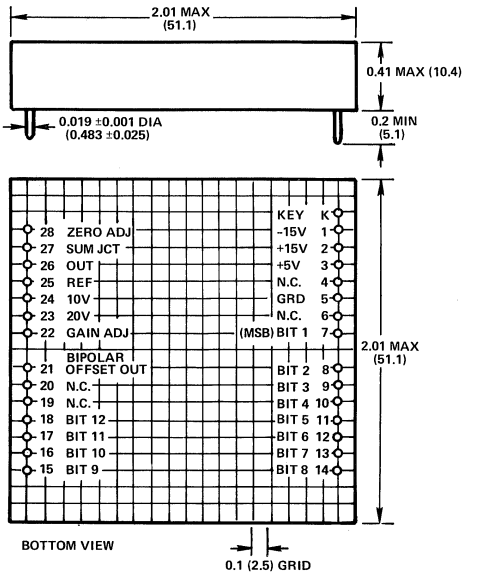
ORDERING GUIDE:

Model DAC-12QZ/XXX

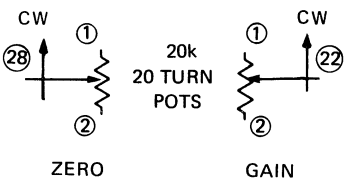
—BIN
—BCD

OUTLINE DIMENSIONS AND PIN CONNECTIONS

Dimensions shown in inches and (mm).



POTENTIOMETER CONNECTIONS



OUTPUT PROGRAMMING

Output Range	External Pin Connections		
±2.5V	21, 23, & 27	24 & 26	
±5V	21 & 27	24 & 26	
±10V	21 & 27	23 & 26	
+5V	23 & 27	24 & 26	21 & 5
+10V	24 & 26	21 & 5	

Connect pins as indicated for selected output.

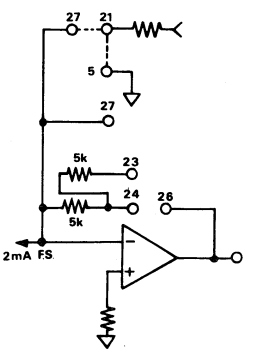
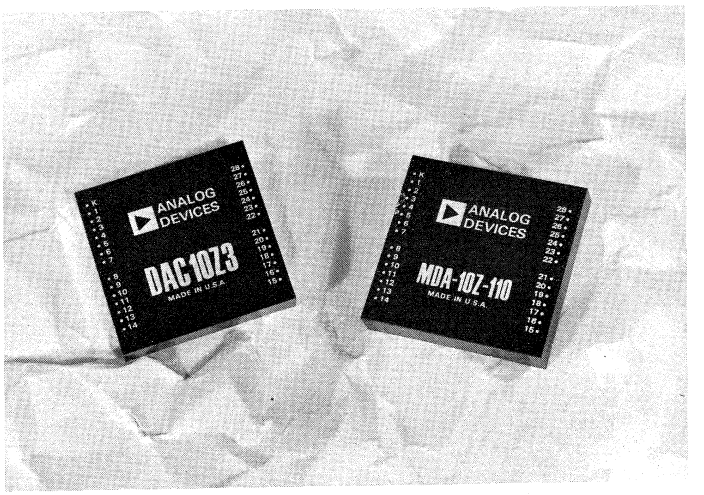


Figure 1. Output Amplifier

Low Cost General Purpose Digital to Analog Converter

DAC-10Z/MDA-10Z

FEATURES
Low Cost
10 Bit Resolution
±½LSB Linearity Error
Unipolar or Bipolar Outputs
Small Size (2" x 2" x 0.4")



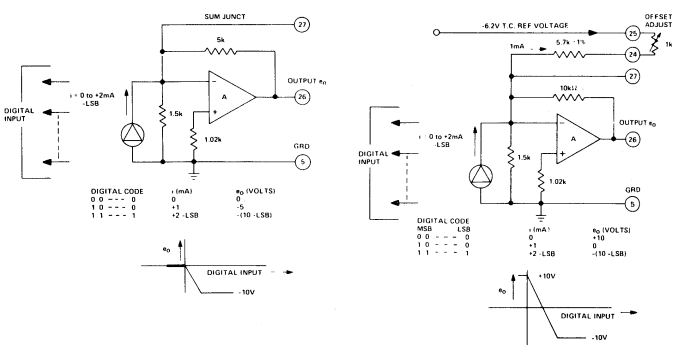
GENERAL DESCRIPTION

The MDA-10Z and DAC-10Z are low cost, 10-bit digital-to-analog converters packaged in compact 2" x 2" x 0.4" modules. The MDA-10Z is a current output device intended for use with external output amplifiers. It features a settling time to ±½LSB of 300ns. The DAC-10Z which comes complete with an IC op amp produces voltage outputs with 5μs settling times.

Both the DAC-10Z and MDA-10Z can be ordered with either unipolar or bipolar outputs. Unipolar units utilize Binary coded inputs and bipolar units use Offset Binary code. All digital inputs are fully TTL/DTL compatible.

DAC-10Z OUTPUT CHARACTERISTICS

The output circuit configuration as well as the input-output relationships of the DAC-10Z are shown below in Figure 1 for both the unipolar and bipolar output versions.



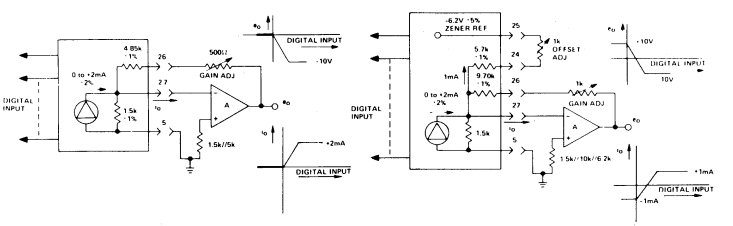
a) Unipolar – DAC-10Z-1 *b) Bipolar – DAC-10Z-3*

Figure 1. DAC-10Z Output Configuration

Note that the DAC-10Z-1 requires no external gain or zero adjustment. The DAC-10Z-3 requires a 1kΩ offset adjustment pot, which the user must supply. With a digital input of 0000000000 applied, this pot is adjusted until an output of +10.000V is obtained within ±2mV.

MDA-10Z WITH EXTERNAL AMPLIFIER

Figure 2, below, shows unipolar and bipolar versions of the MDA-10Z used with an external inverting op amp and also shows the resulting input-output relationships.



a) Unipolar – MDA-10Z-25 *b) Bipolar – MDA-10Z-110*

Figure 2. MDA-10Z With External Amplifier (Inverting Mode)

The gain of the MDA-10Z-25 is adjusted by means of a 500Ω trim pot which the user supplies. With a digital input of 1111111111 applied, this pot is adjusted until an output of -9.990V is obtained within ±1mV.

In addition to the gain adjustment, the MDA-10Z-110 requires a zero adjustment. With a digital input of 0000000000 applied, the 1kΩ offset pot is adjusted until a +10.000V output is obtained within ±2mV. Next, a digital input of 1111111111 is applied and the 1kΩ gain pot is adjusted until an output of -9.980V results within ±2mV.

SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

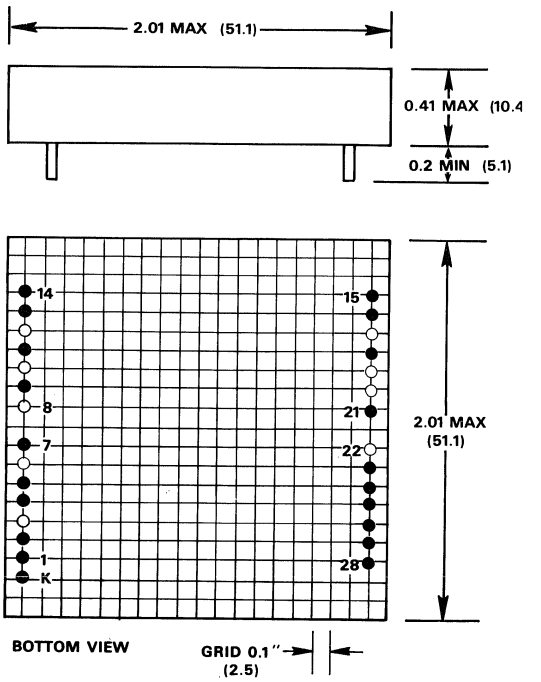
MODELS	DAC-10Z	MDA-10Z
RESOLUTION	10 Bits Binary	*
DATA INPUTS		
0V ≤ "0" ≤ +0.8V[1]	-1.2mA	*
2.4V ≤ "1" ≤ +5V (For Open Circuit)	+25nA	*
CODING		
Unipolar Output	Natural Binary	*
Bipolar Output	Offset Binary	*
OUTPUT		
UNIPOLAR		
Voltage	0V to -10V	See Terminal Limits
Current	See Terminal Limits	0mA to +2mA
Zero Offset	¼LSB (2.5mV) max	1/40LSB (50nA) max
BIPOLAR		
Voltage	±10V	See Terminal Limits
Current	See Terminal Limits	-1mA to +1mA
Zero Offset	½LSB, max	*
TERMINAL LIMITS	±5mA	-10V to +1.5V
IMPEDANCE	0.3 ohm, max	1.5k ohm, ±1%
FULL-SCALE CALIBRATION	10V -LSB, ±0.05%	2mA, ±2%
ACCURACY	±½LSB	±½LSB Rel. to F.S.
LINEARITY	±½LSB (±0.05% of Full Scale)	*
SETTLING TIME		
To 0.05% of F.S.	5μs for 10V Step	300ns for 2mA Step
OUTPUT CIRCUIT PROTECTION	Can be Opened or Shorted Indefinitely to Ground or ± Supply Voltage Without Damage.	Can be Opened or Shorted Indefinitely to Ground Without Damage.
POWER REQUIREMENT	±15V dc, ±2% @ ±15mA	*
POWER SUPPLY SENSITIVITY		
UNIPOLAR		
Zero	3ppm of F.S./%ΔV_S	*
Gain	150ppm of Reading/%ΔV_S	*
BIPOLAR		
Zero	10ppm of F.S./%ΔV_S	200ppm of F.S./%ΔV_S
Gain	300ppm of Reading/%ΔV_S	*
TEMPERATURE RANGE		
OPERATING	0 to +70°C	*
STORAGE	-55°C to +125°C	*
TEMPERATURE COEFFICIENT		
UNIPOLAR		
Zero	10ppm of F.S./°C	5ppm of F.S./°C
Gain	30ppm of Reading/°C	*
BIPOLAR		
Zero	30ppm of F.S./°C	*
Gain	30ppm of Reading Ref. to +F.S./°C	40ppm of Reading Ref. to -F.S./°C

[1] Maximum V input +15V allowable.
*Specifications same as model DAC-10Z.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

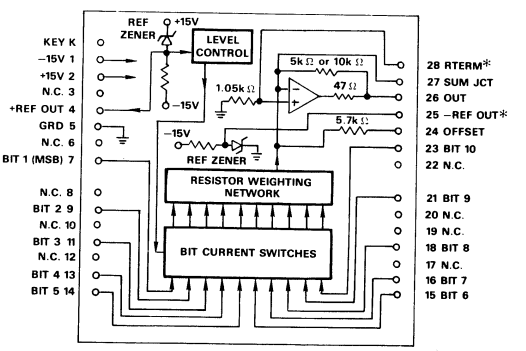
Dimensions shown in inches and (mm).



NOTE:

Terminal pins installed only in shaded hole locations.
See table below for deleted pins.
Module weight: 2 ounces (57 grams).
All pins are gold plated half-hard brass (MIL-G-45 204), 0.019" ±0.001" (0.48 ±0.03) dia.
For mounting card, order AC4102

BLOCK DIAGRAM
DAC-10Z & MDA-10Z



PINS SHOWN AS HAVING NO CONNECTIONS (N.C.) ARE DELETED. THE OUTPUT OP AMP ONLY APPEARS IN THE DAC-10Z's.

*NOTE: NOT ALL OF THE PINS SHOWN WITH CONNECTIONS TO THEM APPEAR ON EACH MODEL. THE PINS DELETED ON EACH MODEL ARE SHOWN BELOW:

MODEL	DELETED PINS
DAC-10Z-1	PINS 25, 28
DAC-10Z-3	PIN 28
MDA-10Z-25	PIN 25
MDA-10Z-110	NONE

ORDERING GUIDE:

DAC-10Z-1	10-bit binary with amplifier, 0V to -10V output voltage.
DAC-10Z-3	10-bit binary with amplifier, 10V to -10V output voltage.
MDA-10Z-25	10-bit binary without amplifier, with 0mA to +2mA output current and 5kΩ nominal (4.85kΩ ±1%) gain resistor.
MDA-10Z-110	10-bit binary without amplifier, -1mA to +1mA output current and 10kΩ nominal (9.70kΩ ±1%) gain resistor.

A/D Converters

Orientation
A/D Converters

FACTORS IN CHOOSING AN A/D CONVERTER

In the current issue of this catalog, there are listed some 15 different families of analog-to-digital converters (ADCs). If one were to consider all the variations, there would be more than 40 different types to choose among (excluding digital panel meters, which are catalogued elsewhere). The reason for so many different types is the number of degrees of freedom in selection—technological, functional, and performance. A selection guide follows these introductory notes. Complete information on converters may be found in the 246-page book, *Analog-Digital Conversion Notes,* published by Analog Devices and available for $5.95 from P.O. Box 796, Norwood MA 02062.

TECHNOLOGICAL FACTORS

The technologies represented here include modules (cards and potted circuits) and integrated circuits—monolithic and hybrid. Modules generally can provide the extremes of performance (resolution—14-bit ADC1131—and speed), as well as arbitrary levels of functional completeness. ICs are small and high in performance-per-dollar. They often require external components for performance of the complete function, but if they otherwise meet the required specifications, they will tend to supplant modules in new designs, because IC prices start low and tend to decrease further with time.

The three most important IC technologies in current use at Analog Devices are hybrid, thin-film-on-CMOS, and thin-film-on-bipolar. *Hybrid* provides the most-complete high-performance devices; for example, the AD572 is a completely self-contained 12-bit successive-approximations ADC, with versatile functional capability. *CMOS* provides high-density logic, low dissipation, and good voltage switches, but relatively poor linear circuitry. The AD7570 is a 10-bit successive-approximation converter that utilizes thin-film-on-CMOS in a configuration similar to that of the AD7522 DAC to obtain a monolithic device that needs only an external comparator for ratiometric A/D conversion. Another example of CMOS is the 13-bit "quad-slope" AD7550, a ratiometric integrating type that utilizes a patented digital error-correction scheme to obtain 1ppm/°C performance, despite the use of on-chip CMOS for both comparator and integrating amplifier. While there are no bipolar monolithic integrated-circuit A/D converters in this catalog, Analog Devices monolithic bipolar technology is the key to the performance and versatility of the hybrid AD572. In addition, the use of Integrated Injection Logic (I^2L) is a promising technique for soon-to-come products, combining the logic density of I^2L with the ability of bipolar to provide high-accuracy analog circuitry, including buried-Zener references and laser-wafer-trimmed thin-film resistors, all on a single monolithic chip. The A/D converter in the low-cost AD2026 Panel Meter is an example of the application of I^2L to monolithic bipolar ICs.

FUNCTIONAL CHARACTERISTICS

The converters described in this catalog employ two fundamental techniques—*successive-approximations*, for moderate-to-high resolution at moderate-to-high speed, and *integration,* for high resolution at modest speeds. The AD572 and ADC1131 are examples of the former, the AD7550 and ADC1105, the latter.

Like a chemist's balance with binary weights (1/2, 1/4, 1/8, etc.), the *successive-approximations* converter compares the unknown input with sums of accurately-known binary fractions of full scale, starting with the largest (2^{-1}), and rejecting any that change the comparator's state ("tip the scale"). At the end of conversion (EOC), the output of the converter is a digital word, representing the ratio of the input to full scale by a fractional-binary code.

Integrating types count pulses for a period proportional to the input. Most-frequently used are *dual slope* types, which count off the period required for the integral of the reference to become equal to the average value of the input (over a fixed period). Integrating types can be made insensitive to drift by storing errors during an error-correcting cycle and subtracting them during the input-measuring cycle. This correction can be performed in analog fashion, using capacitance for storage (ADC-1100 or ADC-17I), or digitally—using the information stored in a counter for correction (AD7550).

Block diagrams illustrating the various techniques appear on individual data sheets. Whatever the technique, these A/D converters comprise several essential functions: an analog section, a digital data-generating section, data outputs, and digital controls.

Analog Section

This section requires a reference, a high-gain comparator, and either a D/A converter (successive approximations) or a controllable integrator. The reference may be internal or external, fixed or variable, and of a specified polarity/sense in relation to the analog input. In ratiometric conversion, the reference is usually external and variable. For conversion with the AD7570, the comparator is connected externally.

In successive-approximation converters, the comparator is generally used in the *current-summing* mode; that is, the current output of the DAC is summed with the current developed in the DACs "feedback resistor" by the input voltage (of opposite polarity), and the balancing action of the converter tends to bring the summing junction towards a voltage null

(much like that of an op amp) at the end of conversion. The typical DAC feedback options, when applied in an ADC, provide input-scaling choices. When the bipolar-offset connection is jumpered to the summing point, input signals of both polarities can be handled. The current-switching action of the DAC, at the typically fast clock-rates used in successive-approximation converters, can disturb the output of the analog signal source, especially if it is a slow high-precision op amp. In such cases, buffering may be necessary; many of the modules, *and the AD572 IC,* have on-board analog buffer-followers.

In integrating types, absolute-value and polarity-sensing circuitry may be required at the front end to handle both polarities of input. Outputs are usually sign-magnitude BCD. However, the AD7550, which uses an offset-reference scheme, requires none of the above; and it has a two's-complement binary output.

Digital Data-Generating Section

In successive-approximation types, this section consists of a discrete or integrated successive-approximations register (SAR), its controls, and inputs from the comparator and clock (which is on-board, but in many cases permits external clock pulses, frequency adjustment, and/or control). In integrating types, this section consists of the clock-pulse generator, the counter(s), the input from the comparator, and the associated controls. Often, provisions are made for the pulse-train to be jumpered to the counter externally, so that the pulse train can be operated on externally, or can transmit its train of pulses to a remote counter. In a few types (the ADC1105 family), there are no on-board counters or registers; the pulse train, magnitude, overrange, and control terminals are intended to communicate with external counters and registers.

Data Outputs

Factors to consider here include coding, resolution, overrange information, levels, format, validity, and timing. *Coding* is usually binary, including jumper-connected offset-binary and/or two's complement for bipolar input signals. For some types, BCD is available, with sign-magnitude for bipolar inputs. Output coding specs should always be checked for digital polarity (positive- or negative-true) of both magnitude and sign information. The *resolution* (number of output bits) must be sufficient for the application; in addition, the specifications must be checked to ascertain that not only will all 2^n (binary) output codes be present (no missing codes), but they must all be present at any temperature in the operating range and related to the input with sufficient accuracy. Integrating types generally have no problems with missing codes (except sometimes at zero, with sign-magnitude coding). Nevertheless, nonlinear integration can cause the conversion relationship to become nonlinear. Successive-approximation types have no way of determining *overrange;* they simply fill up. However, counter types roll over and put out a carry flag to signal overrange.

The *data levels* available at the converter output must be checked (TTL, low-voltage CMOS, high-voltage CMOS), as must the load-driving capability and fanout, and the supply conditions under which appropriate output levels will be furnished. The available choice of output *formats* must also be as desired—parallel, serial, byte-serial, and/or pulse-train. If the converter is intended to communicate directly with a microprocessor data bus, the output should have three-state capability, and parallel outputs must be enabled in bytes of 8 or fewer lines (AD7570, AD7550). If the output is serial, it is usually NRZ (non-return-to-zero) and should be accompanied by a set of synchronized clock-pulses.

A *status* (or *busy* or *EOC*) output changes state to indicate when the data becomes *valid.* The exact nature of this transition should be specified—polarity, timing, levels, etc. For serial data, the exact relationship between the data and the synchronizing clock should be specified, to indicate when each bit becomes valid, and for how long. In general, the *timing* of the whole conversion process must be clearly understood, especially if high speeds are necessary, either for conversion, or for communication with a processor (or both). The timing diagrams on specification sheets are usually accompanied by adequate descriptions of the conversion process and specifications of the critical interface parameters.

Controls

The functions, action (levels or edges), polarity, and timing of all control inputs and outputs should be clearly understood, as well as their loading characteristics and dependence on the supply. In addition to the essential *start-conversion-command* input and a *status* output, various control commands may be available, such as *clock inhibit, high (low)-byte enable, status enable,* and—for speeding up conversion at the cost of resolution—*short-cycle.*

Power Supplies

Appropriate power supplies should be made available, considering the logic levels and analog input signals to be employed in the system. The appropriate degree of power-supply stability to meet the accuracy specifications should be employed. Any recommended external protection circuitry (e.g., Schottky diodes to ensure that V_{CC} is never more than 0.4V above V_{DD} in the AD7570) should be planned for. In almost all cases, separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals, while ensuring that a connection between grounds can always exist at one point, even if the "mecca" point is inadvertently unplugged from the system.

Application Checklist

The designer will generally require specific information in the following categories, before proceeding to the selection process:

- Accurate description of input and output
  1. analog signal range and source or load impedance
  2. digital code needed — binary, offset binary, 2's complement, BCD, etc.
  3. logic level system, i.e., TTL/DTL compatible
- What is the needed data throughput rate?

- What are the control interface details?
- What does the system error budget allow for the converter?
- What are environmental conditions – temperature range, time, supply voltage – over which the converter should operate to the desired accuracy?

For A/D converters, the following considerations are typical.

- What is the analog input voltage range, and to what resolution must the signal be measured?
- What is the requirement for linearity error (or relative accuracy error)?
- To what extent must the various sources of error be minimized as environmental temperature changes?
- How much time can be allowed in the system for each complete conversion?
- How stable is the system power supply? What errors will result from power supply terminal voltage variations of this order?
- Is monotonicity important to this application, or can the system tolerate a few missed codes (out of 4096 total true codes in a 12 bit ADC, for instance). Please note the discussion of monotonicity in the Specifications.
- What is the character of the input signal? Is it noisy, sampled, filtered, rapidly-varying, slowly-varying? What kind of pre-processing is to be (or can be) done that will affect the choice (and cost) of the converter?

SPECIFICATIONS

Definitions of performance specifications, and related information, are to be found on the following pages, in alphabetical order.

Accuracy, Absolute

The error of an A/D converter at a given output code is the difference between the theoretical and the actual analog input voltages required to produce that code. Since the code can be produced by any analog voltage in a finite band (see Quantizing Uncertainty), the "input required to produce that code" is defined as the midpoint of the band of inputs that will produce the code. For example, if 5 volts (±1.2mV) will theoretically produce a 12-bit half-scale code of 100000000000, then a converter for which any voltage from 4.997V to 4.999V will produce that code will have absolute error of 1/2(4.997 + 4.999) – 5 volts = –2mV.

Absolute error comprises gain error, zero error, and nonlinearity, together with noise, Absolute-accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

Accuracy, Relative

Relative accuracy error, expressed in %, ppm, or fractions of an LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated.

Since the discrete points on the theoretical transfer characteristic lie on a straight line, this deviation can also be interpreted as a measure of nonlinearity (see Linearity).

The "discrete points" of an A/D transfer characteristic are the midpoints of the quantization bands at each code (see Accuracy, Absolute).

Aperture Time

This is the time required in a sample-and-hold circuit, for the switch to open after the "hold" command has been given. In a good SHA, this usually does not exceed 50ns delay, including 5-10ns uncertainty due to jitter.

Common Mode Rejection (CMR)

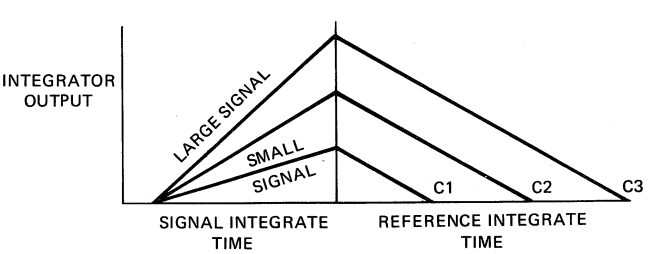
The ability of a device to reject the effect of voltage applied to both input terminals simultaneously. Usually expressed as the log of a "common-mode rejection ratio," e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 1,000,000 to 1 means that a 1V common-mode voltage passes through the amplifier as through it were a differential signal of one microvolt at the input.

Conversion Time

The time required for a complete measurement by an analog-to-digital converter is called conversion time. In successive-approximations converters, conversion times are available between 1.0μs for the 8 bit version of the ADC1103 and 400μs (for the ADC-16Q). The most popular general-purpose A/D converters, like the AD572, have conversion time of about 25μs. Conversion times for integrating types are usually in the tens of milliseconds.

Dual-Slop Converter

An integrating analog-to-digital converter in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time. Then a reference input is switched to the integrator, and integrates "down" from the level determined by the unknown until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period. A digital time-interval meter (i.e., counter) is generally used as the output indicator.



Feedthrough

Undesirable signal-coupling around switches or other devices that are supposed to be turned off or provide isolation, e.g.,

feedthrough error in a multiplexer. It is variously specified in %, ppm, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.

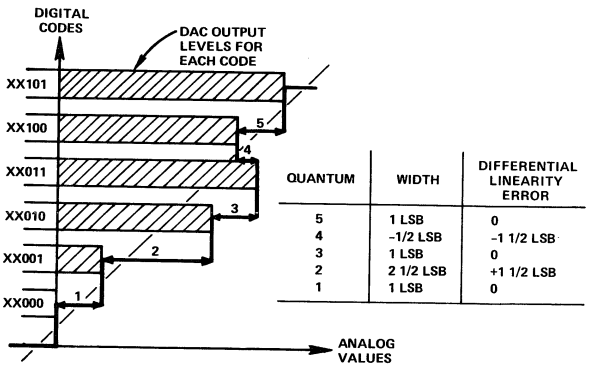
Gain Adjustment
The "gain" of a converter is that analog scale factor setting that provides the nominal conversion relationship, e.g., 10V full scale, in a fixed-reference converter. Gain- and zero-adjustment principles are discussed under *zero*.

Least Significant Bit (LSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the "least significant bit" is that digit (or "bit") that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost "1" is the LSB. Its analog weight, relative to full scale, is 2^{-n}, where n is the number of binary digits. It represents the smallest change that can be resolved by an n-bit converter.

Linearity
Linearity error of a converter, expressed in percent or parts-per-million of full-scale range, or fractions of a least-significant bit, is the deviation of the analog values from a straight line, in a plot of the measured conversion relationship. The straight line can be either a "best straight line," determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristic from this straight line; or, it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated. Sometimes referred to as "end-point" nonlinearity, the latter is both a more conservative measure and is much easier to verify in actual practice. "End-point" nonlinearity is similar to relative accuracy error (see Accuracy, Relative).

Linearity, Differential
A digital output code should correspond to a quantum of analog input values exactly 1 LSB in width (2^{-n} of full scale, for an n-bit converter). Any deviation of the measured "step" from the ideal width is called Differential Nonlinearity. It is an important specification, because a differential nonlinearity error greater than 1 LSB can lead to nonmonotonic behavior of of a D/A converter, and missed codes in an A/D converter employing such a DAC. A flagrant example of differential nonlinearity is shown here.

In the illustration, the horizontal bars represent the measured DAC output values corresponding to 6 adjacent digital codes. The DAC is nonlinear, in that the next-least-significant bit (XX010) is 1½ LSB too large. Thus, instead of the five quanta, or steps, being all equal (= 1 LSB), quantum 2 is 2½ LSB and quantum 4 is -½ LSB. The differential linearity error, the difference between the actual quantum width and the ideal 1 LSB, is +1½ LSB for quantum 2 and -1½ LSB for quantum 4.



QUANTUM	WIDTH	DIFFERENTIAL LINEARITY ERROR
5	1 LSB	0
4	-1/2 LSB	-1 1/2 LSB
3	1 LSB	0
2	2 1/2 LSB	+1 1/2 LSB
1	1 LSB	0

When this DAC is used in successive-approximations conversion, it will lead to a missed code. Analog inputs slightly larger than the value of XX100 will be converted to XX100, and analog inputs slightly less than the value of XX100 will be converted to XX010. The code XX011 will not exist; it will be a *missed code*.

Often, instead of a maximum differential nonlinearity specification, there will be a simple specification of "no missed codes", which implies a differential nonlinearity less than 1 LSB.

Power-Supply Sensitivity
The sensitivity of a converter to dc changes in power-supply voltages is normally expressed in terms of percentage change in analog input value (or fractions of the analog equivalent of 1 LSB), corresponding to a given code, for a 1% dc change in the power supply, e.g., $0.05\%/\%\Delta V_S$). Power-supply sensitivity may also be expressed in relation to a specified dc shift of the supply voltage. High-accuracy DACs intended for battery operation require excellent rejection of large supply-variations.

Quad-Slope Converter
This is an integrating analog-to-digital converter that goes through two cycles of *dual-slope* conversion, once with zero input and once with the analog input being measured. The errors determined during the first cycle are subtracted digitally from the result in the second cycle. The scheme results in an extremely accurate converter. For example, the 13-bit single-chip AD7550 is a CMOS quad-slope A/D converter with tempco (gain and zero temperature coefficients) less than 1ppm/°C.

Quantizing Uncertainty (or "Error")
The analog continuum is partitioned into 2^n discrete ranges for n-bit conversion. All analog values within a given range are represented by the same digital code, usually assigned to the nominal midrange value. There is, therefore, an inherent quantization uncertainty of ±½ LSB, in addition to the actual conversion errors. In integrating converters, this "error" is often expressed as "±1 count."

Ratiometric Converter
The output of an A/D converter is a digital number proportional to the ratio of (some measure of) the input to a reference. Most requirements for conversions call for an absolute measurement, i.e., against a fixed reference. In some cases, where the measurement is affected by a changing reference voltage (e.g., the voltage applied to a bridge), it is advantageous to use that same reference as the reference for the conversion, to eliminate the effect of variation. Ratiometric conversion can also serve as a substitute for analog signal division (where the denominator changes but little during the conversion).

Stability
Stability of a converter, usually applies to the insensitivity of its characteristics with time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion in tables of specifications (see "Temperature Coefficients").

Successive Approximations
Successive approximations is a high speed method of comparing an unknown against a group of weighted references. The operation of a successive approximations A/D converter is generally similar to the orderly weighing of an unknown quantity on a precision chemical balance, using a set of weights such as: 1 gram, 1/2 gram, 1/4 gram, 1/8 gram, 1/16 gram, etc. The weights are tried in order, starting with the largest. Any weight that tips the scale is removed. At the end of the process, the sum of the weights remaining on the scale will be within one LSB of the actual weight (±½ LSB, if the scale is properly biased – see *zero*).

Temperature Coefficients
In general, temperature instabilities are expressed in %/°C, ppm/°C, as fractions of 1 LSB/°C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include *gain, linearity, offset* (bipolar), and *zero*. The last three are expressed in % or ppm of full-scale range per Celsius degree.

Gain Tempco: Two factors principally affect converter gain instability with temperature

a) In fixed-reference converters, the reference source will vary with temperature. For example, the tempco of a good Zener diode is generally less than 5ppm/°C.
b) The reference circuitry and switches may add another 3ppm/°C in good 12-bit converters.

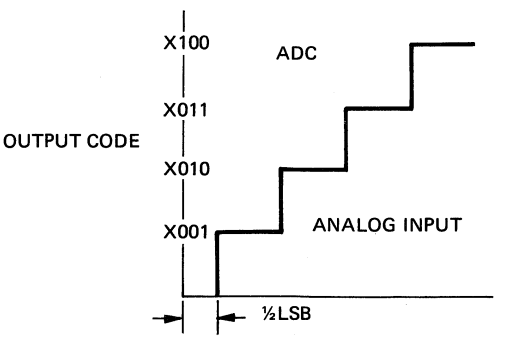
Linearity Tempco: Sensitivity of linearity to temperature over the specified range. To avoid missed codes, it is necessary that the differential nonlinearity error be less than 1 LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a specified temperature range, and/or implied by a statement that there are no missed codes when operating within a specified temperature range.

Offset Tempco The temperature coefficient of the all-DAC-switches-off (minus full-scale) point, of a bipolar successive-approximations converter, is dependent on three variables

1) The tempco of the reference source
2) The voltage stability of the input buffer and the comparator
3) The tracking capability of the bipolar-offset resistors and the gain resistors.

Unipolar Zero The zero tempco of an ADC is dependent only on the zero stability of the integrator and/or the input buffer and the comparator. It may be expressed in μV/°C, or in percent or ppm of full-scale per degree C.

Zero- and Gain-Adjustment Principles
The zero adjustment of a unipolar ADC is set so that the transition from all-bits-off to LSB-on occurs at $\frac{1}{2} \times 2^{-n}$ of nominal full-scale. The gain is set for the final transition



to all-bits-on to occur at F.S. $(1 - \frac{3}{2} \times 2^{-n})$. The "zero" of an offset-binary bipolar ADC is set so that the first transition occurs at –F.S. $(1 - 2^{-n})$ and the last transition at +F.S. $(1 - 3 \times 2^{-n})$. The data sheet instructions should be followed.

Selection Guide
A/D Converters

Description		Model §	Resolution (Bits)	Other	See Page
General Purpose		AD7570	10, 8	CMOS IC, no missing codes, ratiometric, μP-compatible	419
	•	AD571	10	Monolithic IC, I^2L, complete including reference, pretrimmed, μP-compatible	387
		ADC-12QZ	12, 10	Module, 40μs max conversion time, BCD optional	467
High Performance		AD572	12	Hybrid IC, 25μs max conversion time, no missing codes over temperature	395
		ADC1133	12	Module, 25μs max conversion time	457
		ADC1131	14	Module, 12μs max conversion time	453
		ADC1130	14	Module, 25μs max conversion time	453
		ADC1100	11, 3½BCD	Module	431
Integrating		AD7550	13	CMOS IC, 1ppm/°C gain and offset TC, quad slope	411
		ADC14I	14	Module, 5ppm/°C gain TC	459
		ADC-17I	4½BCD	Module, 5ppm/°C gain TC	459
		ADC1105	4½, 3½BCD	Module, gated pulse-train output	441
Display	•	AD2020	3 Digit	IC, I^2L dual-slope DPM chip	403
	•	AD2023	3 Digit	DPM module for separate display	407
High Speed		ADC1109	10	Module, 4μs max conversion time	447
		ADC1103	12, 10, 8	Module, 3.5/1.5/1.0μs max conversion time	437
		ADC1102	12	Module, 8μs max conversion time	435
		ADC1131	14	Module, 25μs max conversion time	453
High Resolution		ADC1130/31	14	Module, 25/12μs conversion time	453
		ADC-16Q	16	Module	463
Low Power		AD7570	10	CMOS IC, no missing codes, ratiometric, μP-compatible	419
		ADC1121	12	Module, CMOS logic, low power drain: 6μJ/conversion, 300μW standby	449
		AD7550	13	CMOS IC, 1ppm/°C gain and offset TC, quad-slope	411

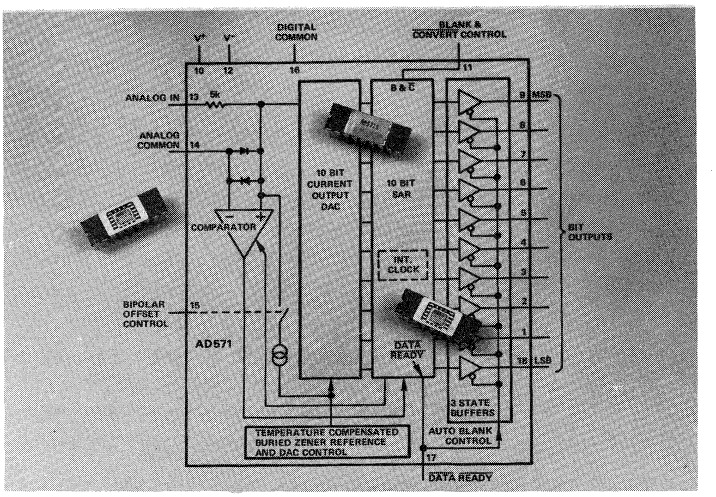
• These devices have been added since publication of the 1977 CONVERSION PRODUCTS CATALOG.
§ The products cataloged in this volume are those considered to be the most cost-effective for new designs. A number of popular older products are still available; they are listed on page 599. Data sheets are available upon request.

Integrated Circuit 10-Bit Analog to Digital Converter

AD571*

FEATURES

Complete A/D Converter with Reference and Clock
Fast Successive Approximation Conversion — 25μs
No Missing Codes Over Temperature
0 to +70°C — AD571K
-55°C to +125°C — AD571S
Digital Multiplexing — 3 State Outputs
18 Pin Ceramic DIP
Low Cost Monolithic Construction



PRODUCT DESCRIPTION

The AD571 is a 10-bit successive approximation A/D converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers — all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 25μs.

The AD571 incorporates the most advanced integrated circuit design and processing technology available today. It is the first complete converter to employ I^2L (integrated injection logic) processing in the fabrication of the SAR function. Laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) insures high accuracy, which is maintained with a temperature compensated, subsurface Zener reference.

Operating on supplies of +5V to +15V and -15V, the AD571 will accept analog inputs of 0 to +10V, unipolar or ±5V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven low, the three state outputs will be open and a conversion will commence. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go low and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ input high blanks the outputs and readies the device for the next conversion. The AD571 executes a true 10-bit conversion with no missing codes in approximately 25μs.

The AD571 is available in two versions for the 0 to +70°C temperature range, the AD571J and K. The AD571S guarantees 10-bit accuracy and no missing codes from -55°C to +125°C. All three grades are packaged in an 18-pin hermetically-sealed ceramic DIP.

***Covered by Patent No. 3,940,760, other patents pending.**

PRODUCT HIGHLIGHTS

1. The AD571 is a complete 10-bit A/D converter. No external components are required to perform a conversion. Full scale calibration accuracy of ±0.3% is achieved without external trims.
2. The AD571 is a single chip device employing the most advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction.
3. The AD571 accepts either unipolar (0 to +10V) or bipolar (-5V to +5V) analog inputs by simply grounding or opening a single pin.
4. The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.
5. Operation is guaranteed with -15V and +5V to +15V supplies. The device will also operate with a -12V supply.
6. The AD571S is also available with full processing to MIL-STD-883A, Class B. The single chip construction and functional completeness make the AD571 especially attractive for high reliability applications.
7. Every AD571 is subjected to long-term stabilization bakes, given a powered burn-in at +125°C, and temperature cycled ten times from -65°C to +150°C prior to final test to insure reliability and long-term stability. In addition, all units are tested 100% at the extremes of their respective temperature ranges for all parameters to guarantee full performance.

SPECIFICATIONS

(typical @ +25°C with V+ = +5V, V– = –15V, all voltages measured with respect to digital common, unless otherwise indicated)

MODEL	AD571JD	AD571KD	AD571SD/AD571SD-883B[5]
RESOLUTION	10 Bits	*	*
RELATIVE ACCURACY @ 25°C[1]	±1LSB max	±1/2LSB max	±1LSB max
T_{min} to T_{max}	±1LSB max	±1/2LSB max	±1LSB max
FULL SCALE CALIBRATION[2] (With 15Ω Resistor In Series With Analog Input	±2LSB (typ)	*	*
UNIPOLAR OFFSET (max)	±1LSB	±1/2LSB	*
BIPOLAR OFFSET (max)	±1LSB	±1/2LSB	*
DIFFERENTIAL NONLINEARITY (Resolution for Which no Missing Codes are Guaranteed)			
+25°C	10 Bits	*	*
T_{min} to T_{max}	9 Bits	10 Bits	10 Bits
TEMPERATURE RANGE	0 to +70°C	*	–55°C to +125°C
TEMPERATURE COEFFICIENTS			
Guaranteed max Change			
T_{min} to T_{max}			
Unipolar Offset	±2LSB (44ppm/°C)	±1LSB (22ppm/°C)	±2LSB (20ppm/°C)
Bipolar Offset	±2LSB (44ppm/°C)	±1LSB (22ppm/°C)	±2LSB (20ppm/°C)
Full Scale Calibration (With 15Ω Fixed Resistor or 50Ω Trimmer)	±4LSB (88ppm/°C)	±2LSB (44ppm/°C)	±5LSB (50ppm/°C)
POWER SUPPLY REJECTION			
Max Change In Full Scale Calibration			
CMOS Positive Supply (K only)			
+13.5V≤V+≤+16.5V	N.A.	±1LSB max	N.A.
TTL Positive Supply			
+4.5V≤V+≤+5.5V	±2LSB max	±1LSB max	*
Negative Supply			
–16.5V≤V+≤–13.5V	±2LSB max	±1LSB max	*
ANALOG INPUT RESISTANCE	3kΩ min	*	*
	5kΩ typ	*	*
	7kΩ max	*	*
ANALOG INPUT RANGES			
(Analog Input to Analog Common)			
Unipolar	0 to +10V	*	*
Bipolar	–5V to +5V	*	*
OUTPUT CODING			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary	*	*
LOGIC OUTPUT[3]			
Bit Outputs and $\overline{\text{Data Ready}}$			
Output Sink Current	3.2mA min	*	*
(V_{OUT} = 0.4V max, T_{min} to T_{max})	(2TTL Loads)	*	*
Output Source Current (Bit Outputs)[4]			
(V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5mA min	*	*
Output Leakage When Blanked	±40μA max	*	*
LOGIC INPUT			
Blank and Convert Input			
0≤V_{in}≤V+	±40μA max	*	*
Blank – Logic "1"	2.0V min	*	*
Convert – Logic "0"	0.8V max	*	*
CONVERSION TIME	15μs min	*	*
	25μs typ	*	*
	30μs max	*	*

MODEL	AD571JD	AD571KD	AD571SD/AD571SD-883B[5]
POWER SUPPLY			
Absolute Maximum			
V+	+7V	+16.5V	*
V-	-16.5V	*	*
Specified Operating — Rated Performance			
V+	+5V	+5V to +15V	*
V-	-15V	*	*
Operating Range			
V+	+4.5V to +5.5V	+4.5V to +16.5V	*
V-	-12V to -16.5V	*	*
Operating Current			
Blank Mode			
V+ = +5V	2mA typ (10mA max)	*	*
V+ = +15V	5mA typ (10mA max)	*	*
V- = -15V	9mA typ (15mA max)	*	*
Convert Mode			
V+ = +5V	5mA	*	*
V+ = +15V	10mA	*	*
V- = -15V	10mA	*	*

*Specifications same as AD571J
**Specifications same as AD571K
Specifications subject to change without notice.

NOTES:
[1] Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.
[2] Full scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.
[3] Logic Input and Output Thresholds and Levels are a function of V+. They are guaranteed TTL compatible at V+ = +5V, CMOS compatible at V+ = 15V for the AD571K.
[4] The Data output lines have active pull-ups to source 0.5mA. The DATA READY line is open collector with a nominal 6kΩ internal pull-up resistor.
[5] The AD571S is available fully processed and screened to the requirements of MIL-STD-883A, Class B. A complete list of tests is given further. When ordering, specify the AD571SD-883B.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common AD571J, S . . . . . .0 to +7V
AD571K. . . . . 0 to +16.5V
V- to Digital Common . . . . . .0 to -16.5V
Analog Common to Digital Common. . . . . .±1V
Analog Input to Analog Common. . . . . ±15V
Control Inputs . . . . . 0 to V+
Digital Outputs (Blank Mode). . . . . .0 to V+
Power Dissipation. 800mW

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

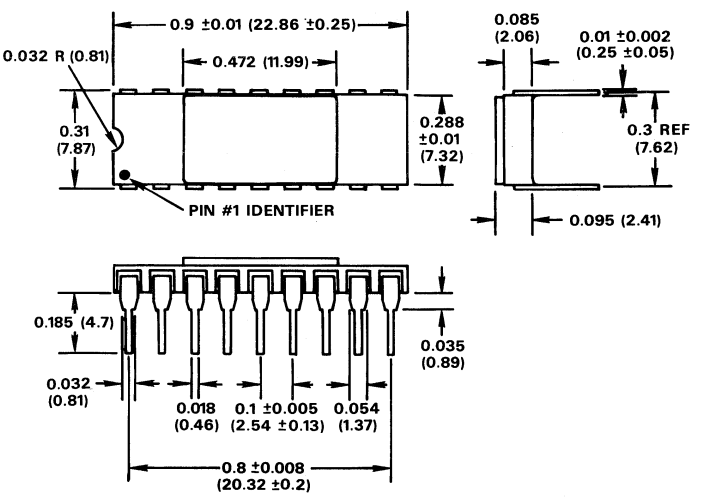


Figure 1. 18-Lead Ceramic Dual-In-Line Package

CIRCUIT DESCRIPTION

The AD571 is a complete 10-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD571 is shown in Figure 2. Upon receipt of the CONVERT command, the internal 10-bit current output DAC is sequenced by the I^2L successive-approximation register (SAR) from its most-significant bit (MSB) to least-significant bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less the bit is left on, if more, the bit is turned off. After testing all the bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within ±½LSB (0.05%).

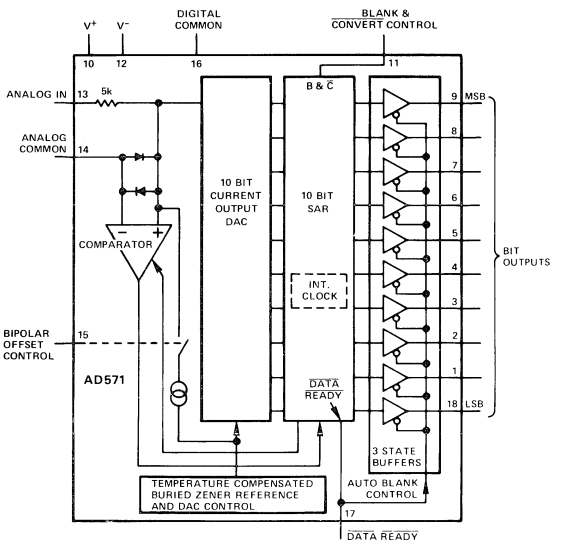
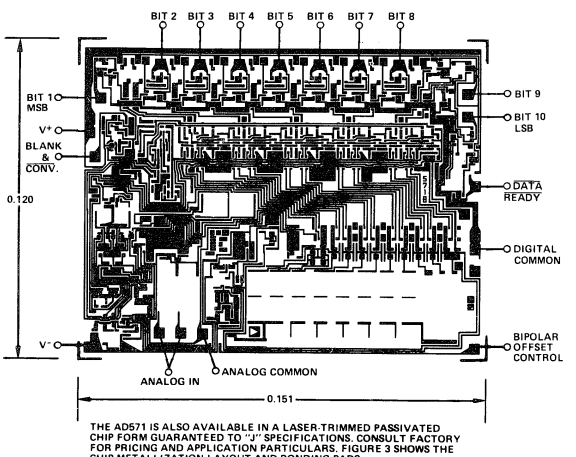


Figure 2. AD571 Functional Block Diagram

Upon completion of the sequence, the SAR sends out a DATA READY signal (active low), which also brings the three-state buffers out of their "open" state, making the bit output lines become active high or low, depending on the code in the SAR. When the BLANK and CONVERT line is brought high, the output buffers again go "open", and the SAR is prepared for another conversion cycle. Details of the timing are given further.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less ½LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a −5V to +5V range. The 5kΩ thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on. (The input resistor is trimmed slightly low to facilitate user trimming, as discussed on the next page.)



THE AD571 IS ALSO AVAILABLE IN A LASER-TRIMMED PASSIVATED CHIP FORM GUARANTEED TO "J" SPECIFICATIONS. CONSULT FACTORY FOR PRICING AND APPLICATION PARTICULARS. FIGURE 3 SHOWS THE CHIP METALLIZATION LAYOUT AND BONDING PADS.

Figure 3. Chip Bonding Diagram

POWER SUPPLY SELECTION

The AD571 is designed for optimum performance using a +5V and −15V supply, for which the AD571J and AD571S are specified. AD571K will also operate with up to a +15V supply, which allows direct interface to CMOS logic. The input logic threshold is a function of V+ as shown in Figure 4. The supply current drawn by the device is a function of both V+ and the operating mode (BLANK or CONVERT). These supply current variations are shown in Figure 5. The supply currents change only moderately over temperature as shown in Figure 9.

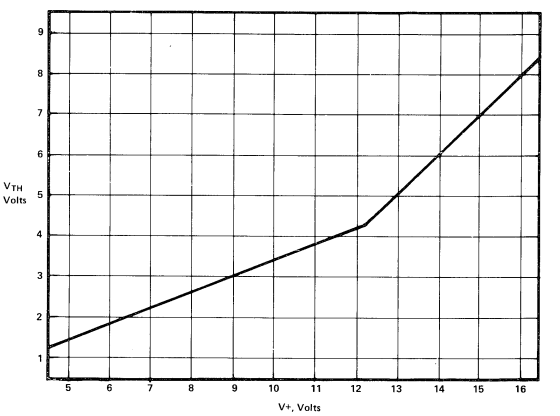


Figure 4. Logic Threshold (AD571K Only)

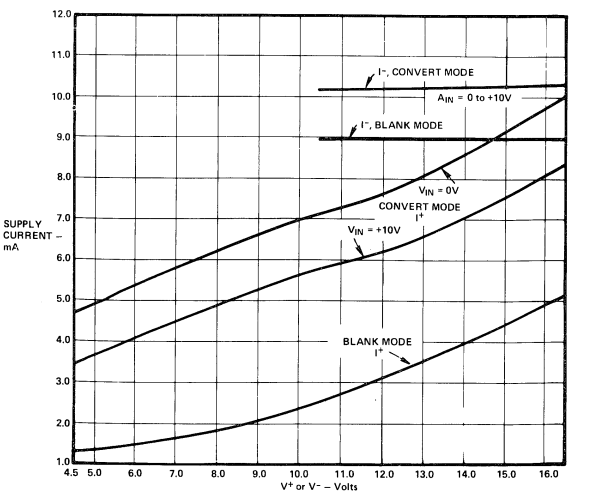


Figure 5. Supply Currents vs Supply Levels and Operating Modes

CONNECTING THE AD571 FOR STANDARD OPERATION

The AD571 contains all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is connection of the power supply (+5 and -15), the analog input, and the conversion start pulse. But, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 6.

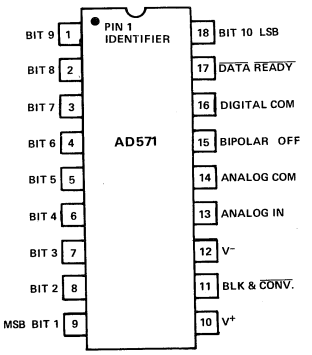


Figure 6. AD571 Pin Connections

FULL SCALE CALIBRATION

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC—plus about 0.3%—when a full scale analog input voltage of 9.990 volts (10 volts − 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.99 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 13. Typical full scale calibration error will then be about ±2LSB or ±0.2%. If the more precise calibration is desired, a 50Ω trimmer should be used instead. Set the analog input at 9.990 volts, and set the trimmer so that the output code is just at the transition between 1111111110 and 1111111111. Each LSB will then have a weight of 9.766mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have weight of exactly 10.00mV), a 100Ω resistor in series with a 100Ω trimmer (or a 200Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ.

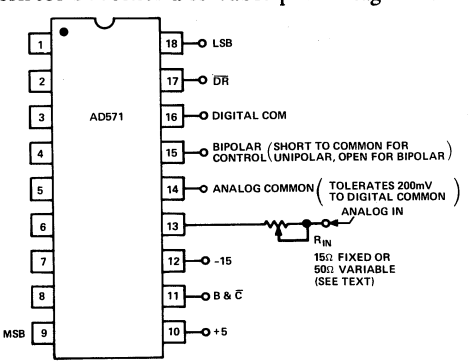


Figure 7. Standard AD571 Connections

BIPOLAR OPERATION

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a -5V to +5V range with an offset binary output code. (-5.00 volts in will give a 10-bit code of 0000000000; an input of 0.00 volts results in an output code of 1000000000 and 4.99 volts at the input yeilds the 1111111111 code). The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 8.

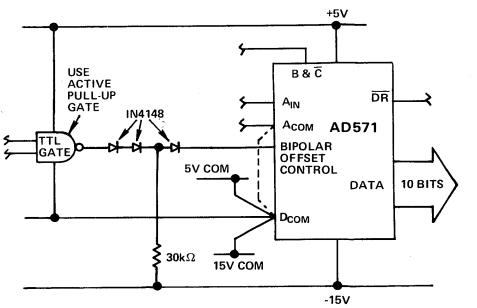


Figure 8. Bipolar Offset Controlled by Logic Gate

Gate Output = 1 Unipolar 0 - 10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

COMMON MODE RANGE

The AD571 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode range between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. An additional 1mA will flow in during a blank interval with zero analog input. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. We recommend the connection of a parallel pair of back-to-back protection diodes between the commons if they are not connected locally.

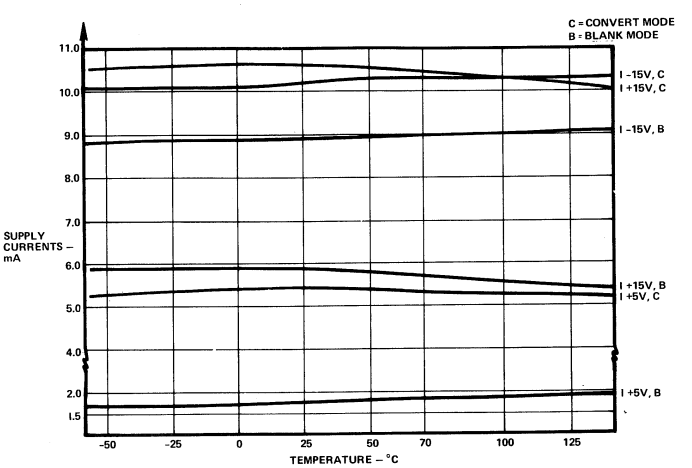


Figure 9. AD571 Power Supply Current vs Temperature

ZERO OFFSET

The apparent zero point of the AD571 can be adjusted by inserting an offset voltage between the Analog Common of the device and the actual signal return or signal common. Figure 10 illustrates two methods of providing this offset. Figure 10A shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

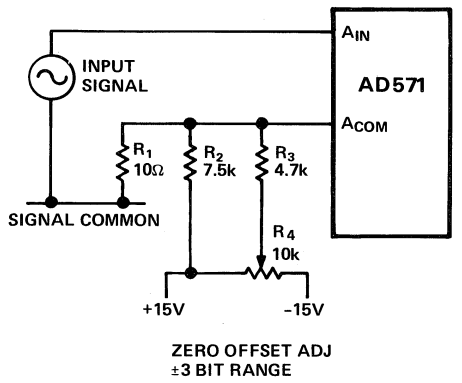


Figure 10.(A)

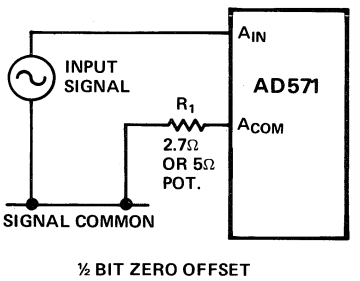


Figure 10.(B)

Figure 11 shows the nominal transfer curve near zero for an AD571 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in Figure 10B. At balance (after a conversion) approximately 2mA flows into the Analog Common terminal. A 2.7Ω resistor in series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 5Ω potentiometer (connected as a rheostat) can be used as R2. Additional negative offset range may be obtained by using larger values of R2. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½LSB is introduced, full scale trimming as described on previous page should be done with an analog input of 9.985 volts.

NOTE: During a conversion transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling which returns to analog signal common, should go to the signal input side of the resistive offset network.

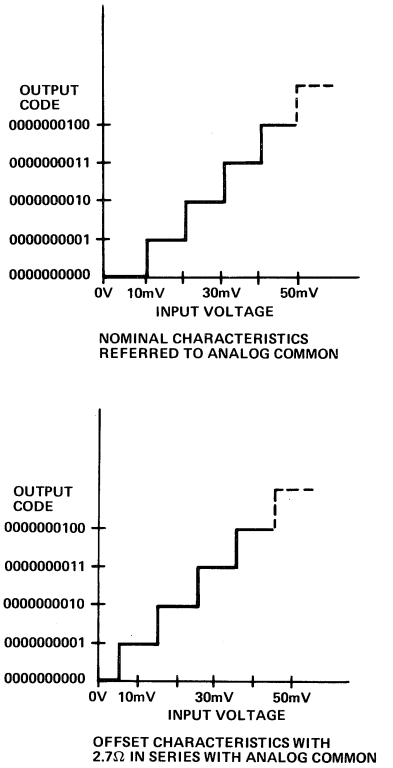


Figure 11. AD571 Transfer Curve - Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~ 9.766mV)

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD571, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further insure reliability, the AD571 is offered with 100% screening to MIL-STD-883B, method 5004.

Table I details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883B screening to these tests on a 100% basis.

TABLE I

TEST	METHOD
1) Internal Visual (Pre cap)	2010, Test Condition B
2) Stabilization Bake	Method 1008, 24 hours @ +150°C
3) Temperature Cycling	Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C
4) Constant Acceleration	Method 2001, Test Condition E, Y1 plane, 30kg
5) Seal, Fine and Gross	Method 1014, Test Condition A and C
6) Burn-in Test	Method 1015, Test Condition B, 168 hours @ +125°C
7) Final Electrical Tests	Performed 100% to all min and max specifications on data pages
8) External Visual	Method 2009

CONTROL AND TIMING OF THE AD571

There are several important timing and control features on the AD571 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 12.

The normal stand-by situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{\text{C}}$) line is held high, the output lines will be "open", and the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) line will be high. This mode is the lowest power state of the device (typically 150mW). When the (B & $\overline{\text{C}}$) line is brought low, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and Data lines do not change state. When the conversion cycle is complete (typically 25μs), the $\overline{\text{DR}}$ line goes low, and within 500ns, the Data lines become active with the new data.

About 1.5μs after the B & $\overline{\text{C}}$ line is again brought high, the $\overline{\text{DR}}$ line will go high and the Data lines will go open. When the B & $\overline{\text{C}}$ line is again brought low, a new conversion will begin. The minimum pulse width for the B & $\overline{\text{C}}$ line to blank previous data and start a new conversion is 2μs. If the B & $\overline{\text{C}}$ line is brought high during a conversion, the conversion will stop, and the $\overline{\text{DR}}$ and Data lines will not change. If a 2μs or longer pulse is applied to the B & $\overline{\text{C}}$ line during a conversion, the converter will clear and start a new conversion cycle.

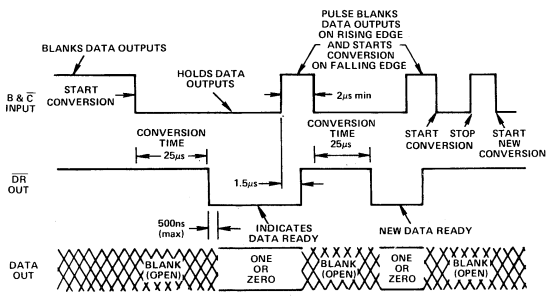


Figure 12. AD571 Timing and Control Sequence

CONTROL MODES WITH BLANK AND $\overline{\text{CONVERT}}$

The timing sequence of the AD571 discussed above allows the device to be easily operated in a variety of systems with differing control modes. The two most common control modes, the Convert Pulse Mode, and the Multiplex Mode, are illustrated here.

Convert Pulse Mode — In this mode, data is present at the output of the converter at all times except when conversion is taking place. Figure 13 illustrates the timing of this mode. The BLANK and $\overline{\text{CONVERT}}$ line is normally low and conversions are triggered by a positive pulse. A typical application for this timing mode is shown in Figure 16, in which μP bus interfacing is easily accomplished with three-state buffers.

Multiplex Mode — In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing shown in Figure 14. A typical AD571 multiplexing application is shown in Figure 17.

This operating mode allows multiple AD571 devices to drive common data lines. All BLANK and $\overline{\text{CONVERT}}$ lines are held high to keep the outputs blanked. A single AD571 is selected, its BLANK and $\overline{\text{CONVERT}}$ line is driven low and at the end of conversion, which is indicated by $\overline{\text{DATA READY}}$ going low, the conversion result will be present at the outputs. When this data has been read from the 10-bit bus, BLANK and $\overline{\text{CONVERT}}$ is restored to the blank mode to clear the data bus for other converters. When several AD571's are multiplexed in sequence, a new conversion may be started in one AD571 while data is being read from another. As long as the data is read and the first AD571 is cleared within 15μs after the start of conversion of the second AD571, no data overlap will occur.

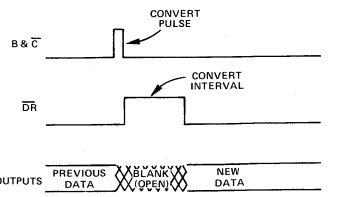


Figure 13. Convert Pulse Mode

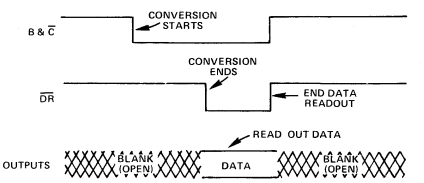


Figure 14. Multiplex Mode

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD571

Many situations in high-speed acquisition systems or digitizing of rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD571, a SHA can also serve as a high input impedance buffer.

Figure 15 shows the AD571 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10μs with a droop rate less than 100μV/ms. The control signals are arranged so that when the control line goes low, the AD582 is put into the "hold" mode, and the AD571 will begin its conversion cycle. (The AD582 settles to final value well in advance of the

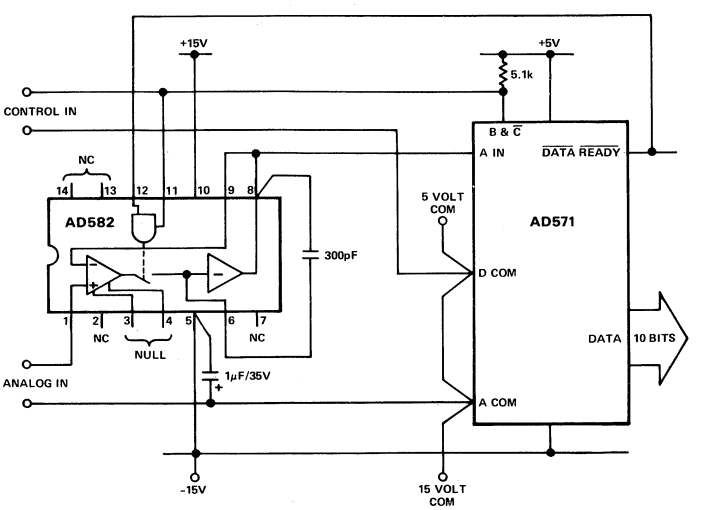


Figure 15. Sample-Hold Interface to the AD571

first comparator decision inside the AD571). The $\overline{\text{DATA READY}}$ line is fed back to the other side of the differential input control gate so that the AD582 cannot come out of the "hold" mode during the conversion cycle. At the end of the conversion cycle, the $\overline{\text{DATA READY}}$ line goes low, automatically placing the AD582 back into the sample mode. This feature allows simple control of both the SHA and the A-D converter with a single line. Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle to give the most accurate measurements.

INTERFACING THE AD571 TO A MICROPROCESSOR

The AD571 can easily be arranged to be driven from standard microprocessor control lines and to present data to any standard microprocessor bus (4-, 8-, 12-or 16-bit) with a minimum of additional control components. The configuration shown in Figure 16 is designed to operate with an 8-bit bus and standard 8080 control signals.

The input control circuitry shown is required to insure that the AD571 receives a sufficiently long B & $\overline{\text{C}}$ input pulse. When the converter is ready to start a new conversion, the B & $\overline{\text{C}}$ line is low, and $\overline{\text{DR}}$ is low. To command a conversion, the start address decode line goes low, followed by $\overline{\text{WR}}$. The B & $\overline{\text{C}}$ line will now go high, followed about 1.5μs later by $\overline{\text{DR}}$. This resets the external flip-flop and brings B & $\overline{\text{C}}$ back to low, which initiates the conversion cycle. At the end of the conversion cycle, the $\overline{\text{DR}}$ line goes low, the data outputs will become active with the new data and the control lines will return to the stand-by state. The new data will remain active until a new conversion is commanded. The self-pulsing nature of this circuit guarantees a sufficient convert pulse width.

This new data can now be presented to the data bus by enabling the three-state buffers when desired. A data word (8-bit or 2-bit) is loaded onto the bus when its decoded address goes low and the $\overline{\text{RD}}$ line goes low. This arrangement presents data to the bus "left-justified," with highest bits in the 8-bit word; a "right-justified" data arrangement can be set up by a simple re-wiring. Polling the converter to determine if conversion is complete can be done by addressing the gate which buffers the $\overline{\text{DR}}$ line, as shown. In this configuration, there is no need for additional buffer register storage since the data can be held indefinitely in the AD571, since the B & $\overline{\text{C}}$ line is continually held low.

BUS INTERFACING WITH A PERIPHERAL INTERFACE CIRCUIT

An improved technique for interfacing to a μP bus involves the use of special peripheral interfacing circuits (or I/O devices), such as the MC6820 Peripheral Interface Adapter (PIA). Shown in Figure 17 is a straightforward application of a PIA to multiplex up to 8 AD571 circuits. The AD571 has 3-state outputs, hence the data bit outputs can be paralleled, provided that only one converter at a time is permitted to be the active state. The $\overline{\text{DATA READY}}$ output of the AD571 is an open collector with resistor pull-up, thus several $\overline{\text{DR}}$ lines can be wire-ored to allow indication of the status of the selected device. One of the 8-bit ports of the PIA is combined with 2-bits from the other port and programmed as a 10-bit input port. The remaining 6-bits of the second port are programmed as outputs and along with the 2 control bits (which act as outputs), are used to control the 8 AD571's. When a control line is in the "1" or high state, the ADC will be automatically blanked. That is, its outputs will be in the inactive open state. If a single control line is switched low, its ADC will convert and the outputs will automatically go active when the conversion is complete. The result can be read from the two peripheral ports; when the next conversion is desired, a different control line can be switched to zero, blanking the previously active port at the same time. Subsequently, this second device can be read by the microprocessor, and so-forth. The status lines are wire-ored in 2 groups and connected to the two remaining control pins. This allows a conversion status check to be made after a convert command, if necessary. The ADC's are divided into two groups to minimize the loading effect of the internal pull-up resistors on the $\overline{\text{DATA READY}}$ buffers. See the MC6820 data sheet for more application detail.

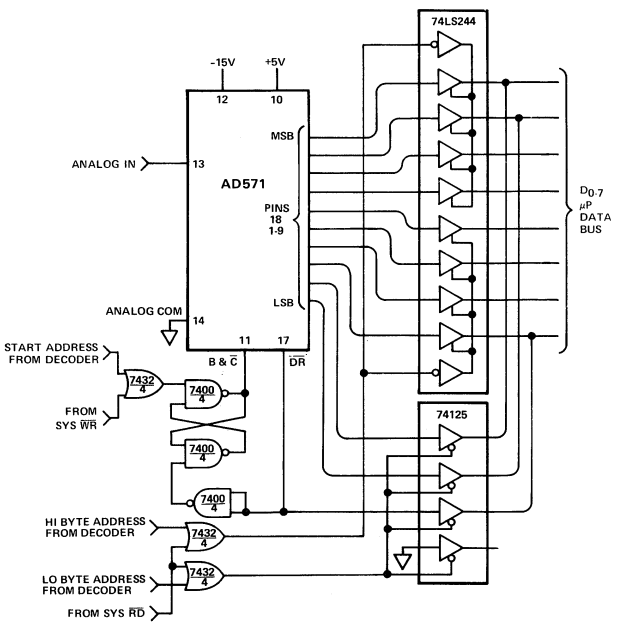


Figure 16. Interfacing AD571 to an 8-Bit Bus (8080 Control Structure)

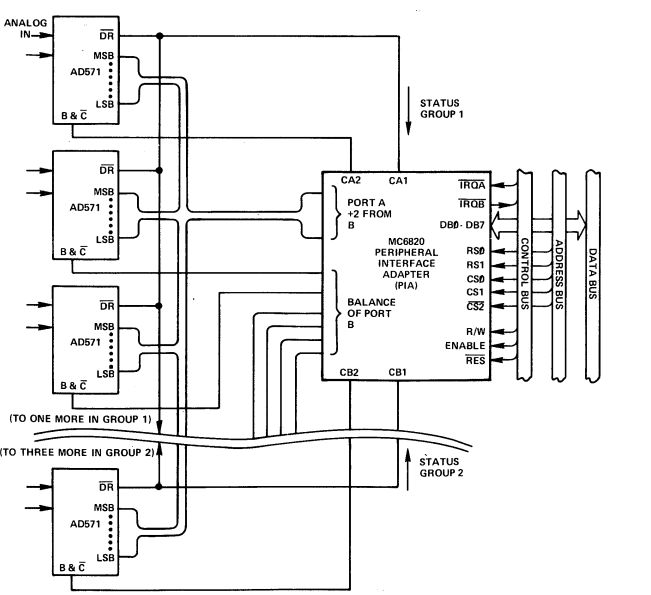


Figure 17. Multiplexing 8 AD571's Using Single PIA for µP Interface. No Other Logic Required (6800 Control Structure)

12-Bit Successive Approximation Integrated Circuit A/D Converter

AD572

FEATURES

Performance

- True 12-Bit Operation: Max Nonlinearity < ±0.012%
- Low Gain T.C.: < ±15ppm/°C (AD572B)
- Low Power: 900mW
- Fast Conversion Time: < 25μs
- Monotonic Feedback DAC Guarantees No Missing Codes
- Hermetically-Sealed, Electrostatically-Shielded DIP

Versatility

- Military/Aerospace Temperature Range: -55°C to +125°C (AD572S)
- MIL-STD-883B Processing Available
- Positive-True Serial or Parallel Logic Outputs
- Short-Cycle Capability

Value

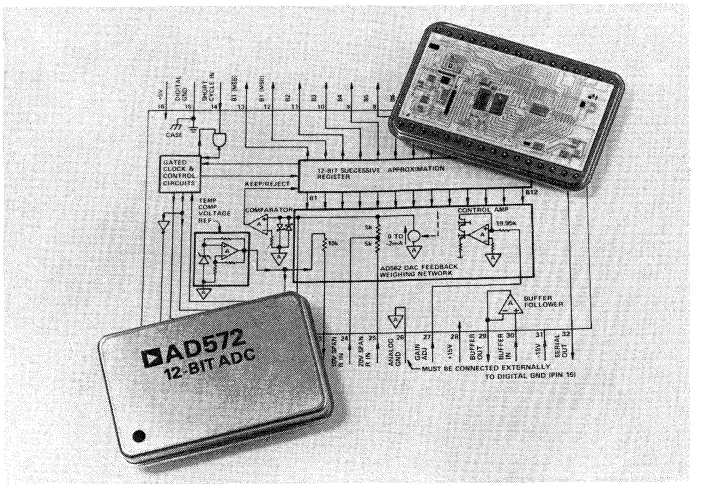
- Precision +10V Reference for External Application
- Internal Buffer Amplifier
- High Reliability Welded Metal Package
- Low Cost

GENERAL DESCRIPTION

The AD572 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference, comparator, and buffer amplifier. Its hybrid IC design utilizes MSI digital and linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide modular performance, flexibility, and ease of use, combined with IC size, price, and reliability.

Important performance characteristics of the AD572 include a maximum linearity error at 25°C of ±0.012%, gain T.C. below 15ppm/°C, typical power dissipation of 900mW, and conversion time of less than 25μs. Of considerable significance in military and aerospace applications is the guaranteed performance from -55°C to +125°C of the AD572S, and the availability of units processed to MIL-STD-883B. Monotonic operation of the feedback D/A converter guarantees no missing output codes over temperature ranges of 0 to +70°C, -25°C to +85°C, and -55°C to +125°C.

The design of the AD572 includes scaling resistors that provide analog input signal ranges of ±2.5, ±5.0, ±10, 0 to +5, or 0 to +10 volts. Adding flexibility and value are the +10V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is positive-true and available in either serial or parallel form.



The AD572 is packaged in a hermetically-sealed, all-metal DIP. Welding...rather than solder sealing...eliminates any possibility of contamination from flux and solder particles. The metal construction provides excellent shielding from random electrostatic and/or electromagnetic radiation which could cause incorrect output codes. To insure a level of reliability consistent with its performance, each AD572 receives a stringent pre-cap visual inspection, high temperature storage and temperature cycling, acceleration testing, fine and gross leak testing, and operating burn-in.

The AD572 is available in three versions with differing guaranteed performance characteristics and operating temperature ranges; the "A" and "B" are specified from -25°C to +85°C, and the "S" from -55°C to +125°C.

PRODUCT DESCRIPTION

The AD572 functional diagram and pin-out are shown in Figure 1. The device consists of the following monolithic bipolar transistor and thin-film resistor circuit elements:

1. 12-bit successive-approximation register
2. 12-bit feedback DAC weighing network
3. low-drift comparator
4. temperature-compensated precision +10V reference
5. high-impedance buffer follower
6. gated clock and digital control circuits

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD572AD	AD572BD	AD572SD
RESOLUTION	12 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5.0, ±10.0V	*	*
Unipolar	0 to +5, 0 to +10V	*	*
Impedance (Direct Input)			
0 to +5V, ±2.5V	2.5kΩ	*	*
0 to +10V, ±5V	5.0kΩ	*	*
±10V	10kΩ	*	*
Buffer Amplifier			
Impedance (min)	100MΩ	*	*
Bias Current	50nA	*	*
Settling Time			
to 0.01% of FSR for 20V step	2μs	*	*
DIGITAL INPUTS			
Convert Command	Note 1	*	*
Logic Loading	1 TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error (Note 2)	±0.05% FSR (Adj to Zero)	*	*
Unipolar Offset Error	±0.05% FSR (Adj to Zero)	*	*
Bipolar Offset Error	±0.1% FSR (Adj to Zero)	*	*
Linearity Error (max)	0.012% FSR	*	*
Inherent Quantization Error	±½ LSB	*	*
Differential Linearity Error	±½ LSB	*	*
No Missing Codes	Guaranteed: 0 to +70°C	Guaranteed: -25°C to +85°C	Guaranteed: -55°C to +125°C
Power Supply Sensitivity			
±15V	±0.002% FSR/%ΔV_S	*	*
±5V	±0.001% FSR/%ΔV_S	*	*
TEMPERATURE COEFFICIENTS			
Gain (max)	±30ppm/°C (-25°C to +85°C)	±15ppm/°C (-25°C to +85°C)	±15ppm/°C (-25°C to +85°C) ±25ppm/°C (-55°C to +125°C)
Unipolar Offset	±3ppm FSR/°C	±3ppm FSR/°C (max)	**
Bipolar Offset (max)	±15ppm FSR/°C	±7ppm FSR/°C	**
Linearity	±3ppm FSR/°C	±2ppm FSR/°C	**
CONVERSION TIME (max)	25μs	*	*
DIGITAL OUTPUTS (All Codes Positive-True)			
Parallel Data			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*
Output Drive	2 TTL Loads	*	*
Serial Data (NRZ format)			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary	*	*
Output Drive	2 TTL Loads	*	*
Status	Logic "1" during Conversion	*	*
$\overline{\text{Status}}$	Logic "0" during Conversion	*	*
Output Drive	2 TTL Loads	*	*
Internal Clock			
Output Drive	2 TTL Loads	*	*
Frequency	500kHz	*	*
INTERNAL REFERENCE VOLTAGE	+10.00V, ±5mV	*	*
Max External Current	±4mA	*	*
Voltage Temperature Coefficient (max)	±20ppm/°C	±10ppm/°C	**
POWER REQUIREMENTS			
Supply Voltages/Currents	+15V, ±5% @ +25mA	*	*
	-15V, ±5% @ -20mA	*	*
	+5V, ±5% @ +50mA	*	*
Total Power Dissipation	925mW	*	*
TEMPERATURE RANGE			
Specification	-25°C to +85°C	*	-55°C to +125°C
Operating	-55°C to +125°C	*	*
Storage	-55°C to +150°C	*	*

*Same specification as AD572AD

**Same specification as AD572BD

Specifications subject to change without notice.

Note 1 Positive pulse 200nsec wide (min). Leading edge ("0" to "1") resets registers. Trailing edge ("1" to "0") initiates conversion.

Note 2 With 50Ω, 1% fixed resistor in place of Gain Adjust pot; see Figures 4 and 5.

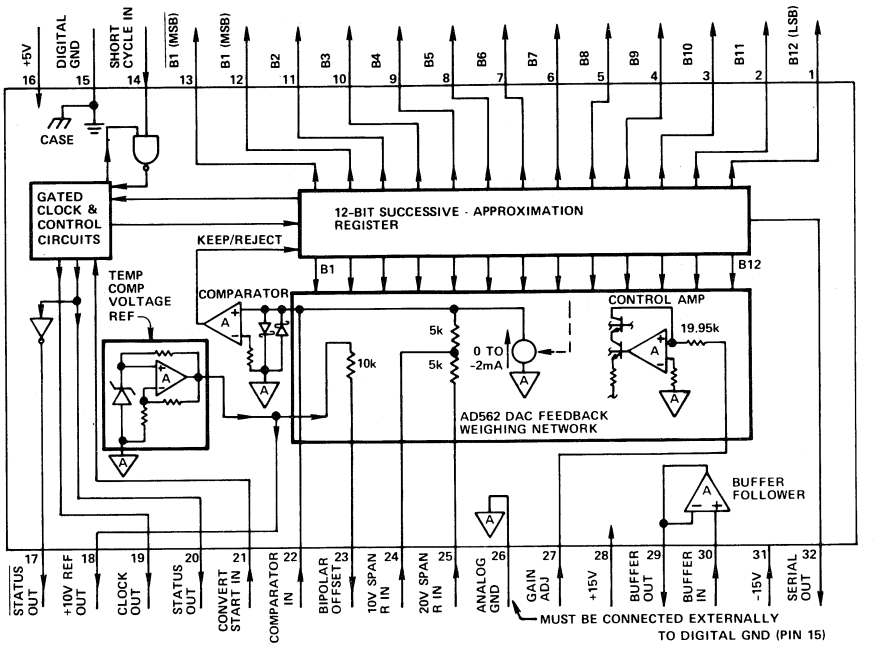


Figure 1. AD572 Functional Diagram & Pinout

The +10V reference is derived from a low T.C. zener reference diode which has its zener voltage amplified and buffered by an op amp. The reference voltage is calibrated to +10V, ±1mV by active laser trimming of the thin-film resistors which determine the closed-loop gain of this op amp.

The DAC feedback weighing network is comprised of a proprietary 12-bit analog current switch chip and silicon-chromium thin-film ladder network (separately packaged as the AD562 12-bit D/A converter). This ladder network is active laser-trimmed to calibrate all bit ratio scale factors to a precision of 0.0005% of FSR (full-scale range) to guarantee no missing codes over the appropriate temperature ranges specified for the AD572A, AD572B, and AD572S versions.

Different unipolar and bipolar analog input ranges can be selected by changing connections at the device terminal pins. The analog voltage input can be applied to either of the span (direct input) resistors. Alternatively, the unity buffer follower can be connected between the analog signal and either direct input terminal when a high impedance input is required.

THEORY OF OPERATION

On receipt of a CONVERT START command, the AD572 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows:

The 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the respective device bit output pins and to the corresponding bit inputs of the feedback DAC.

The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 2. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through

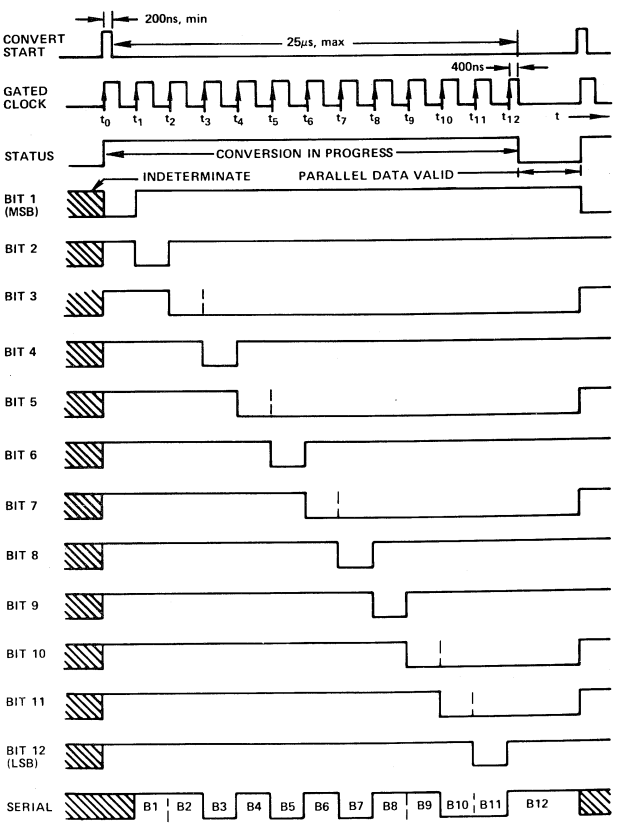


Figure 2. Timing Diagram (Binary Code 110101011001)

13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 -B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 400ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 8).

Incorporation of this 400ns delay period guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

BINARY CODING

The AD572 binary output number $N_o = B_1\ B_2\ B_3 \ldots B_{12}$ is related to the analog input voltage E_{in} for all unipolar ranges by the expression:

$$\frac{B_1\ 2^{11} + B_2\ 2^{10} + B_3\ 2^9 + \ldots + B_{12}\ 2^0}{2^{12}} = \frac{E_{in}}{FSR} \qquad (1)$$

. . .where B_1 = MSB, B_{12} = LSB, and FSR = full-scale range. For all bipolar ranges a fixed bipolar offset equal to $\frac{+FSR}{2}$ is internally summed with E_{in} so that the sum of E_{in} plus this offset will be positive over the rated operating range. For bipolar ranges, expression (1) becomes:

$$\frac{B_1\ 2^{11} + B_2\ 2^{10} + B_3 2^9 + \ldots + B_{12}\ 2^0}{2^{12}} = \frac{E_{in} + \frac{FSR}{2}}{FSR} \qquad (2)$$

Expressions (1) and (2) can be put in an alternate form:

$$\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \ldots + \frac{B_{12}}{4096}\right) FSR = E_{in} \qquad (3)$$

Unipolar (Binary Coding)

...and...

$$\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \ldots + \frac{B_{12}}{4096}\right) FSR - \frac{FSR}{2} = E_{in} \qquad (4)$$

Bipolar (Offset Binary Coding)

Several examples will illustrate how this binary coding works.

0 TO +10V INPUT RANGE

Assume FSR = 10V and $B_1\ B_2\ B_3\ \ldots B_{12}$ = 110001000001, then from (3), E_{in} = +5V +2.5V +0.1563V + 0.0024V = +7.6587V.

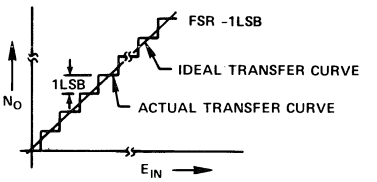
-5V TO +5V INPUT RANGE

Assume FSR = 10V as above, but that the bipolar offset is connected and $B_1\ B_2\ B_3\ \ldots B_{12}$ = 0110000000001. Then from (4), E_{in} = (+2.5V + 1.25V + 0.0024V) - 5V = -1.2476V.

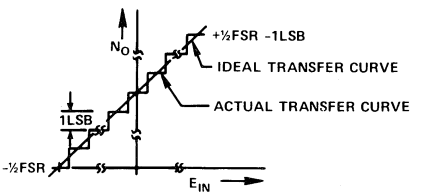
-10V TO +10V INPUT RANGE

Assume the bipolar offset is connected as above, but that the input span is now 20V. Assuming the same digital output code as in the -5V to +5V input range example, from (4), E_{in} = (+5V +2.5V +0.0049V) -10V = -2.4951V, or twice the value of the previous example (neglecting round-off errors).

The encoding process defined by the previous relations (1) and (2) or (3) and (4) determines that the analog input lies within one of the 2^{12} = 4096 quantization levels between 0 and FSR (or -FSR/2 and +FSR/2). Figures 3 (A) and 3 (B) show the actual device transfer curves for unipolar and bipolar ranges (offset binary coding). They also show the ideal straight-line transfer curves which pass through the center of each quantization level. As can be seen from these figures, the actual and ideal transfer curves differ by exactly ±½LSB at the end of each quantization interval, giving rise to the fundamental ±½LSB quantization error inherent in the digitizing process.



(A) Unipolar Range (Binary Coding)



(B) Bipolar Range (Offset Binary Coding)

Figure 3. Unipolar and Bipolar Range Transfer Curves

ANALOG INPUT AND POWER CONNECTIONS

Offset Adjust: Analog and power connections for 0 to +10V unipolar and -10V to +10V bipolar input ranges are shown in Figures 4 and 5, respectively. The Bipolar Offset pin 23 is open-circuited for all unipolar input ranges, and connected to Comparator Input pin 22 for all bipolar input ranges. The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 3.9MΩ resistor to Comparator Input pin 22 for all ranges. The tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of 8 x 244 x 10^{-6} x 1200ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

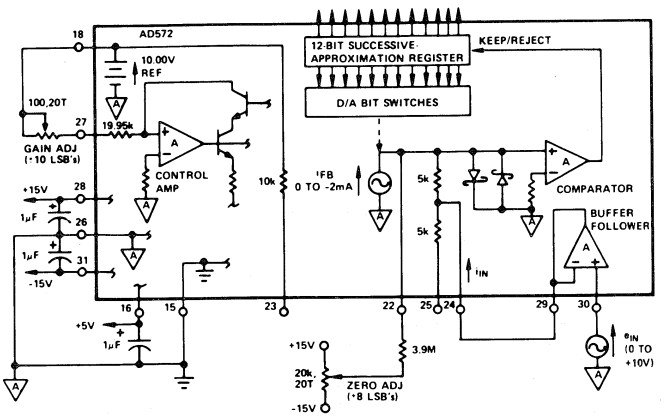


Figure 4. Analog and Power Connections for Unipolar 0 to +10V Input Range with Buffer Follower

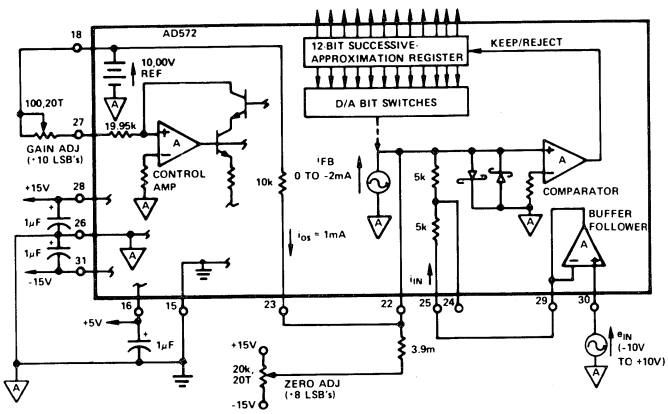


Figure 5. Analog and Power Connections for Bipolar -10V to +10V Input Range with Buffer Follower

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco < 100 ppm/°C) are used, is shown in Figure 6.

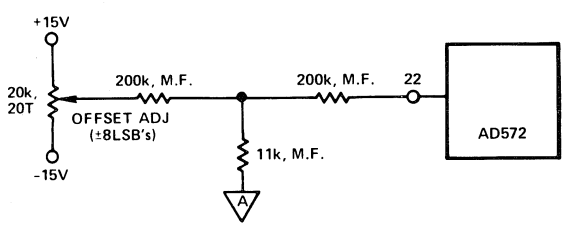


Figure 6. Low Tempco Zero Adj Circuit

In either zero adjust circuit, the fixed resistor connected to pin 22 should be located close to this pin to keep the pin 22 connection runs short, since the Comparator Input pin 22 is quite sensitive to external noise pick-up.

Gain Adjust: The gain adjust circuit consists of a 100Ω potentiometer connected between +10V Reference Output pin 18 and Gain Adjust Input pin 27 for all ranges. Both GAIN and ZERO ADJ potentiometers should be multi-turn, low tempco types; 20T cermet (tempco = 100ppm/°C max) types are recommended. If the 100Ω GAIN ADJ potentiometer is replaced by a fixed 50Ω resistor, absolute gain calibration to ±0.1% of FSR is guaranteed.

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground pin 26 and Digital Ground pin 15 are not connected internally; these two pins must be connected externally for the device to operate properly. Preferably, this connection is made at only one point, and as close to the device as possible. The case is connected internally to pin 15 to provide good electrostatic shielding.

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the device. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling (as is required with some competitive products), since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 3 and 4, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -½FSR for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 000000000001; Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 111111111110 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 100000000000.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 000000000001 digital output (offset binary) code. Set analog input to +9.9902V; adjust Gain for 111111111110 digital output (offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (offset binary) code should be 100000000000.

Other Ranges: Representative digital coding for 0 to +10V, -5V to +5V, and -10V to +10V ranges is shown in Table 1. Coding relationships and calibration points for 0 to +5V and -2.5V to +2.5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -5V to +5V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±¼LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 4.

Analog Input - Volts (Center of Quantization Interval)			Input Normalized to FSR		Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)	
0 to +10V Range	-5V to +5V Range	-10V to +10V Range	Unipolar Ranges	Bipolar Ranges	B1 (MSB)	B12 (LSB)
+9.9976	+4.9976	+9.9951	+FSR-1 LSB	+½FSR-1 LSB	1 1 1 1 1 1 1 1 1 1 1 1	
+9.9952	+4.9952	+9.9902	+FSR-2 LSB	+½FSR-2 LSB	1 1 1 1 1 1 1 1 1 1 1 0	
:	:	:	:	:	:	
+5.0024	+0.0024	+0.0049	+½FSR+1 LSB	+1 LSB	1 0 0 0 0 0 0 0 0 0 0 1	
+5.0000	+0.0000	+0.0000	+½FSR	ZERO	1 0 0 0 0 0 0 0 0 0 0 0	
:	:	:	:	:	:	
+0.0024	-4.9976	-9.9951	+1 LSB	-½FSR+1 LSB	0 0 0 0 0 0 0 0 0 0 0 1	
+0.0000	-5.0000	-10.0000	ZERO	-½FSR	0 0 0 0 0 0 0 0 0 0 0 0	

Table 1. Digital Output Codes vs Analog Input For Unipolar and Bipolar Ranges

RANGE AND BUFFER FOLLOWER PIN CONNECTIONS

Analog pin connections for each of the ranges, with and without the buffer follower being used, are shown in Table 2.

Range	Buffer Follower	Connect Analog Input To Pin:	Connect Span Pin:	Connect Bipolar Pin 23 To:
0 to +5V	Used	30, and 29 to 24	25 to 22	—
	Not Used	24		
0 to +10V	Used	30, and 29 to 24	—	
	Not Used	24		
-2.5 to +2.5V	Used	30, and 29 to 24	25 to 22	22
	Not Used	24		
-5 to +5V	Used	30, and 29 to 24	—	
	Not Used	24		
-10 to +10V	Used	30, and 29 to 25	—	
	Not Used	25		

Table 2. Range and Buffer Follower Pin Connections

When the analog signal source has a low impedance (as would be the case if it were the output of the sample-hold amplifier of Figure 9), it can be connected to either of the direct input pins 24 or 25. The buffer follower is used in the application as shown in Figure 6, in which the analog input to the converter comes directly from the output of a FET analog multiplexer. The selected channel has a typical r_{on} = 200Ω which has a 3000ppm/°C tempco. If the multiplexer output were connected to the 0 to +10V direct input pin 24 (5kΩ input impedance, nominal), this r_{on} would introduce a 4% gain scale-factor loading error, which is well beyond the normal ±0.25% FSR external gain adjustment range, and a tempco of approximately 3000ppm/°C x 4% = 120ppm/°C. By connecting the buffer between the multiplexer output and direct input, these errors are eliminated. The buffer amplifier input bias current (50nA typical) must flow through the analog signal source, however. This limits the upper practical source impedance to several kilohms so that the offset voltage I_{BIAS} R_{SOURCE} can be kept negligible, even though the buffer amplifier dynamic input impedance ⩾ 100MΩ. The buffer amplifier has a 2μs settling time to 0.01% FSR for a 20V input step. This must be added to the conversion time when the input voltage can change significantly between successive conversions (as could be the case in the circuit of Figure 7).

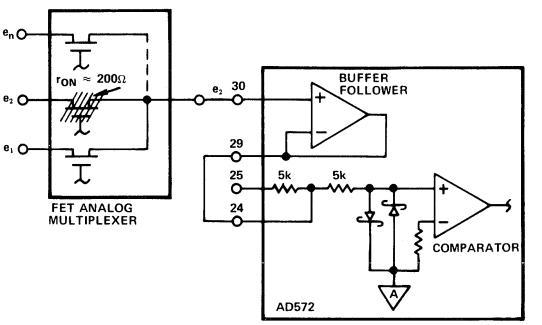


Figure 7. Using Buffer Follower With Multiplexed Analog Input

Short Cycle Input: A Short Cycle Input pin 14 permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 24 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +400ns in timing diagram of Figure 2). Short Cycle pin connections and associated maximum 12, 10, and 8-bit conversion times are summarized in Table 3.

Connect Short Cycle Pin 14 to Pin:	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset at: (Figure 2)
16	12	0.024	25	t_{12} + 400ns
2	10	0.10	21	t_{10} + 400ns
4	8	0.39	17	t_8 + 400ns

Table 3. Short Cycle Connections

(One should note that the calibration voltages listed in Table 1 are for 12-bit resolution only, and are not those corresponding to the center of each discrete quantization interval at reduced bit resolutions.)

DIGITAL OUTPUT DATA

Both parallel and serial data are in positive-true form and outputted from TTL storage registers. Parallel data output coding is binary for unipolar ranges and either offset binary

or two's complement binary, depending on whether Bit 1 (pin 12) or its logical inverse $\overline{\text{BIT 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 200ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is binary for unipolar input ranges and offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid on all negative-going clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 8. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 2. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

APPLICATIONS

Sample-Hold Amplifier: A sample-hold amplifier (SHA) is normally connected between the analog signal source and AD572 analog input when the analog signal can change by more than ½LSB during conversion. Typical SHA-AD572 interconnections are shown in Figure 9. The $\overline{\text{STATUS}}$ output drives the SHA SAMPLE/HOLD input directly. On receipt of a CONVERT START pulse, the $\overline{\text{STATUS}}$ flag changes from "1" to "0" causing SHA mode to change from SAMPLE to HOLD. The SHA output voltage $e_{o\ S\text{-}H}$ is then held constant at the value existing just prior to application of the HOLD command for the complete conversion period. At the end of conversion, the $\overline{\text{STATUS}}$ flag returns to "1", restoring the SHA mode to SAMPLE, and $e_{o\ S\text{-}H}$ again tracks the analog signal voltage $e_{in\ S\text{-}H}$ (after the signal acquisition transient has subsided).

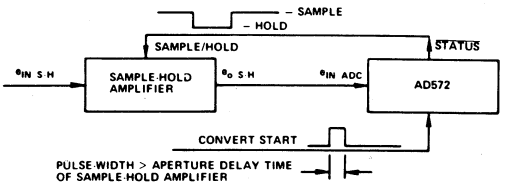


Figure 9. Sample-Hold Amplifier – AD572 Interconnections

Note that the internal (gated) clock is inhibited for the duration of the CONVERT START pulse and does not start running until the termination of this pulse (see timing). This can be used to simplify control signal timing requirements. In the circuit of Figure 9, for example, the CONVERT START signal pulse-width can be extended beyond the aperture delay time of the SHA to assure that $e_{o\ S\text{-}H}$ is in steady-state before conversion is initiated. This assures accurate conversion without requiring additional delay timing circuitry. The effect of varying the CONVERT START pulse-width on the conversion timing cycle is shown in Figure 10.

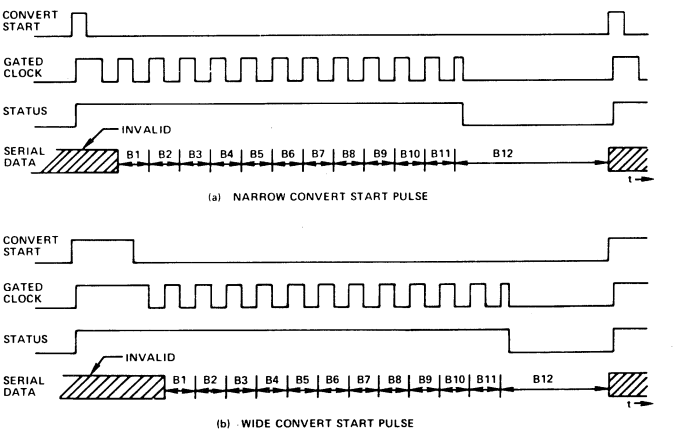


Figure 10. Effect of Convert Start Pulse-Width on Timing

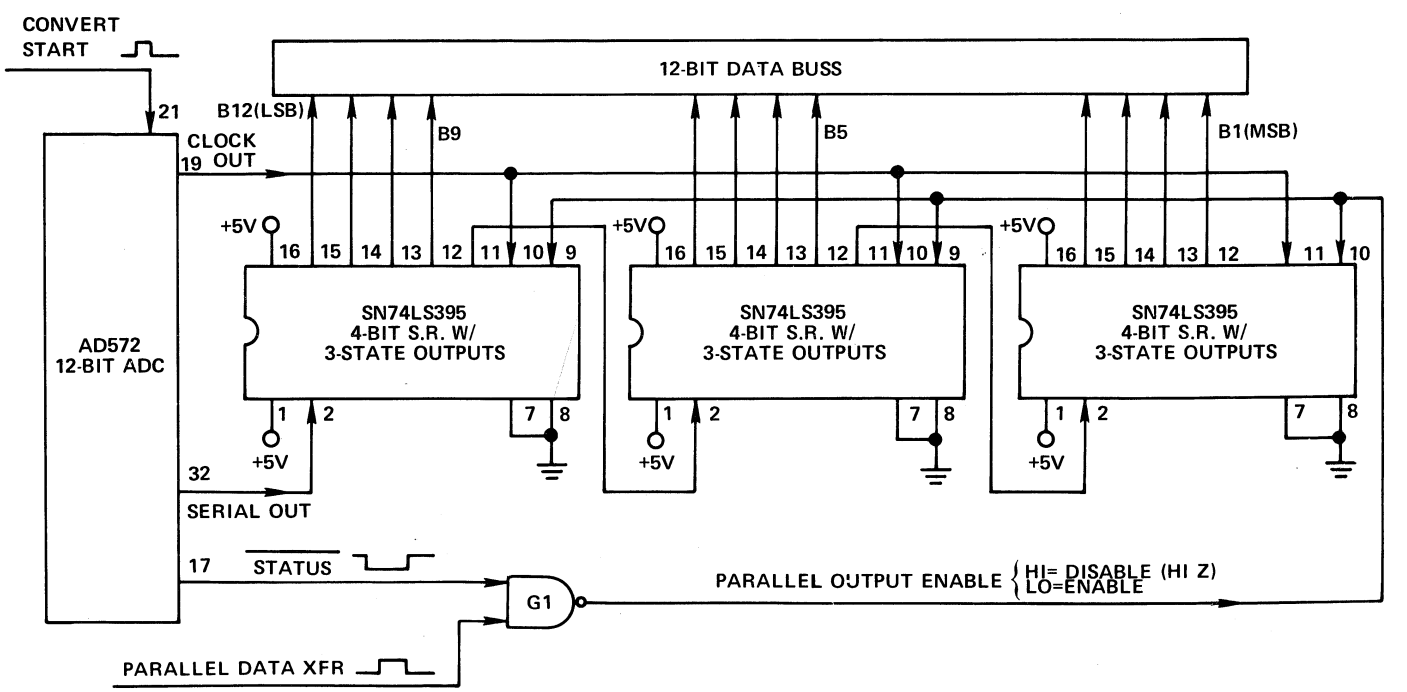


Figure 8. Serial Data Transfer Into Shift Register With Parallel Output to Data Buss

Digital Gain Control: Figure 11 shows a method of varying the AD572 gain digitally, using an 8-bit DAC. The 100Ω GAIN ADJ potentiometer is replaced by a 15Ω fixed resistor. This biases full-scale high by approximately 35Ω/20,000Ω = +0.18% of FSR. The AD559 has a large positive compliance voltage which permits its Current Output pin 4 to be connected directly to the AD572 Reference Input pin 27. The AD559 2.5mA output current is established by the AD580 +2.5V voltage reference connected through a 1kΩ resistor to Reference Current Input pin 14. The 2.5mA DAC full-scale output current removed from the AD572 pin 27 node changes the pin 27 input current -2.5mA x 15Ω/20kΩ = -1.88μA, or -1.88μA/500μA = -0.38% of FSR; this permits a digital gain adjustment range of approximately ±0.2% FSR from nominal.

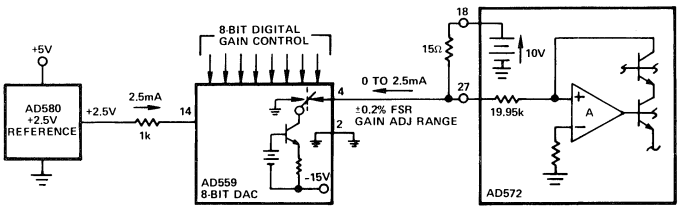
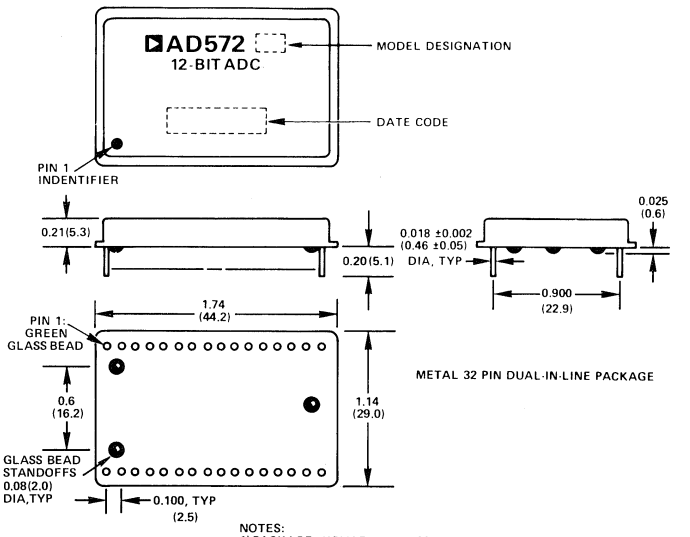


Figure 11. Digital Gain Control Using 8-Bit DAC

OUTLINE DIMENSIONS
PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).



NOTES:
1) PACKAGE: KOVAR WITH 100μIN. MIN., NICKEL PLATE
2) PINS: KOVAR WITH 50μIN. MIN 24K GOLD PLATE
3) PACKAGE AND PINS MEET ALL REQUIREMENTS OF MIL-STD-883
4) TOLERANCES, UNLESS OTHERWISE NOTED:
   a) .XX: ±.01 (.25)
   b) .XXX: ±.005 (.13)

MATING SOCKET: SET OF TWO 16 PIN SOCKET STRIPS (ORDER P/N AC1H72)

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all models of the AD572 receive the following processing:

PROCESS	CONDITIONS
1. Pre-Cap Visual Inspection	In-House Criteria
2. Stabilization Bake	24 hours @ +150°C
3. Temperature Cycling	10 cycles, -65°C to +150°C
4. Constant Acceleration	5000G
5. Seal, Test, Fine and Gross	In-House Criteria
6. Operating Burn-In	48 hours @ +125°C

PROCESSING TO MIL-STD-883

All models ordered to the requirements of MIL-STD-883, Method 5004, Class B are identified with a /883B suffix, and receive the following processing:

1. Pre-Cap Visual Inspection	2010, Test Condition B
2. Stabilization Bake	1008, 24 hours @ +150°C
3. Temperature Cycling	1010, Test Condition C, 10 cycles, -65°C to +150°C
4. Constant Acceleration	2001, Y_1 plane, 5000G
5. Seal Test, Fine and Gross	1014, Test Condition A and C
6. Operating Burn-In	1015, Test Condition B, 160 hours @ +125°C
7. Final Electrical Testing	Performed at max and min operating temperatures
8. External Visual Inspection	2009

AD572 ORDERING GUIDE

Model	Specification Temp Range	Max Gain T.C.	Max Reference T.C.	Guaranteed Temp Range No Missing Codes
AD572AD	-25°C to +85°C	±30ppm/°C	±20ppm/°C	0 to +70°C
AD572BD	-25°C to +85°C	±15ppm/°C	±10ppm/°C	-25°C to +85°C
AD572SD	-55°C to +125°C	±15ppm/°C (-25°C to +85°C) ±25ppm/°C (-55°C to +125°C)	±10ppm/°C	-55°C to +125°C
AD572BD/883B, AD572SD/883B	Meet all specifications after processing to the requirements of MIL-STD-883, Method 5004,			

NOTE: D suffix = Dual-In-Line package designator.

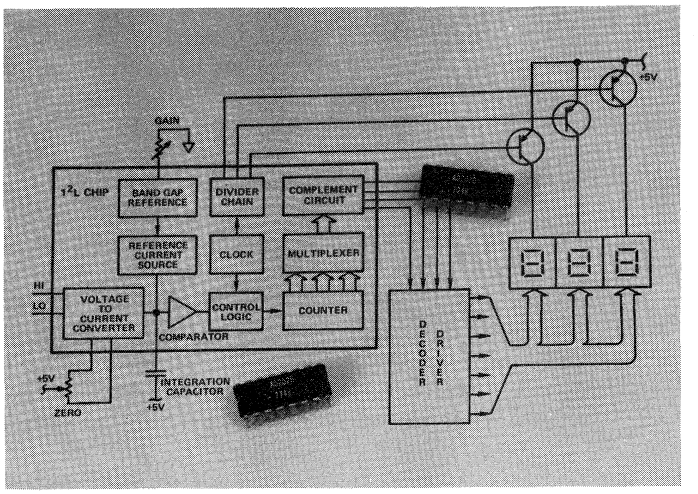
ANALOG DEVICES

I^2L 3 Digit A/D Converter

AD2020

FEATURES

- **Low Cost**
- **I^2L LSI Design**
- **Multiplexed Character Serial BCD Output**
- **Support Components Required — 10 (including displays)**
- **Single +5V Power Supply Required**
- **Balanced Differential Input**
- **Internal Reference**
- **Low Power Consumption (50mW typical)**
- **Small Size: 16 Pin Dual-in-Line**
- **Wide Temperature Range: Operating 0 to +75°C**
  Storage -55°C to +150°C
- **Extended Temperature Range Available Upon Special Request**



GENERAL DESCRIPTION

The AD2020 is a low cost 3 digit A/D Converter, needing only 10 additional support components to make a complete 3 digit DPM/DVM. The small total component count, the low cost, and high reliability allow for a wide variation in display applications, especially those previously utilizing APM's (Analog Panel Meters).

The technology utilized in the AD2020 is Integrated Injection Logic (I^2L), an extension of the long proven, high yield bipolar process. This technique offers a significantly higher circuit packing density. The input amplifier, comparator, band-gap reference, counters, clock, control logic, multiplexer and drivers needed to implement the dual slope conversion, are all included on a single die.

The AD2020, although it has an internal reference, consumes only 50mW of power and is operated from a single +5V supply, unlike most DPM chips requiring two (2) supplies.

The DPM chip is packaged in a standard size 16 pin-dual-in-line package. Utilizing a unique double passivation and noble-metal interconnect scheme, this plastic package offers essentially hermetic performance over a wide temperature range. The chip is available in two versions with differing guaranteed operating temperature ranges. The standard AD2020 is specified from 0 to +75°C and because of the special packaging technique, an extended temperature version is also available upon request.

EXCELLENT PERFORMANCE

The AD2020 measures inputs from -99mV to +999mV with an accuracy of 0.1% of reading ±1 digit. The balanced differential input rejects common mode voltages up to 200mV dc, enough to eliminate most ground loop problems. Polarity detection is automatic and "+" and "–" Overload conditions are indicated through BCD coding, i.e., BCD code for "+" Overload is 1011 and 1010 for "–" Overload. Zero shift is ±0.5mV over the full operating temperature range resulting in the same performance as a chip with Auto-Zero.

The benefits in manufacturing labor, inventory and reliability are self-evident. The only external components required for a complete digital display product are: 1 capacitor, 3 transistors, 1 decoder driver, 2 potentiometers and 3 displays, all operated from a single 5 volt supply.

WHAT IS I^2L?

MOS and bipolar are the two basic LSI semiconductor processes. MOS produces very dense — therefore low-cost — logic circuits, but has difficulty achieving precision analog circuitry. Before I^2L, bipolar could offer stable high-quality devices suitable for precision analog circuits, but logic consumed much expensive chip area.

Integrated Injection Logic (I^2L) now allows the design of single-chip devices containing both analog and digital functions, without calling for the compromises required in the past. I^2L has a logic density that equals or exceeds that of MOS, while employing a bipolar process suitable for precision analog circuitry.

I^2L eliminates the complexity of conventional bipolar logic by using inverted transistors (collectors and emitters are interchanged). Figure 1 shows a conventional transistor, with its wraparound P+ isolation region, which is needed to separate the collectors of adjacent transistors. When the transistors are inverted, the collectors are automatically isolated, and the emitters are grounded, at the same time.

SPECIFICATIONS (@ +25°C, V_{CC} = +5V)

PARAMETER	SPECIFICATIONS MIN	TYP	MAX	UNITS	CONDITIONS
ACCURACY					
Range	-99		+999	mV	
Accuracy		0.05	0.1	%RDG	±1 Digit
Unadjusted Gain	0.94	1.0	1.06		Gain Pot @ 2.4kΩ
Unadjusted Zero Offset	-12		+12	mV	Zero Pot Centered
Zero Width		1		Count	
Gain Temperature Coefficient		50		ppm/°C	Gain Adjusted[1]
Offset Temperature Coefficient		10.0		μv/°C	Offset Adjusted[1]
Intercode Noise		0.1		Counts	
ANALOG INPUT					
Input Impedance		100		mΩ	
Bias Current		110		nA	
Common Mode					
Voltage			±0.2	V dc	
Rejection Ratio		50		dB	
CONVERSION RATE					
Normal	2	3.5	7	Conv./sec	Hold Pin @ 0V
High Speed	48	72	168	Conv./sec	Hold Pin ⩾3.2V
CONTROL INPUT (PIN 6)					
Normal Rate			0.4V	V	Pin May Be Left Open
Hold	0.8		1.6V	V	
High Speed	3.2			V	
BCD OUTPUTS					
Logic Low Sink Current	0.4	3.2		mA	V_o = ⩽0.5V
Logic High Leakage Current		500		pA	V_o = 4.0V (open collector output)
DIGIT SELECT OUTPUTS					
Digit "On" Sink Current	1.6	3.2		mA	V_o = 4.0V
Digit "Off" Leakage Current		500		pA	V_o = 4.0V (open collector output)
POWER SUPPLY					
Operating Range	4.5	5.0	5.5	V	
Supply Current		10.0	17.0	mA	V_{CC} = 5.0V
Power Supply Rejection		60		dB	

ABSOLUTE MAXIMUM RATINGS @ +25°C[2]

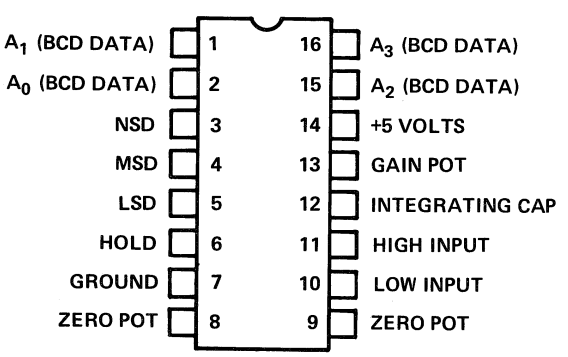
- Analog Input Voltage (pins 10 or 11 to pin 7) ..... ±15V
- V_{CC} to GND (pin 14 to pin 7) ..... +7V; -0V
- Operating Temperature Range ..... 0 to +75°C
- Storage Temperature Range ..... -55°C to +150°C
- Power Dissipation (package) up to T_A = +55°C 750mW
- Derates Above +55°C by ..... 6.7mW/°C
- Lead Temperature ..... +265°C for 10sec (max) at distance of 1/16" ±1/32" from case to solder

OVERLOAD DECODING

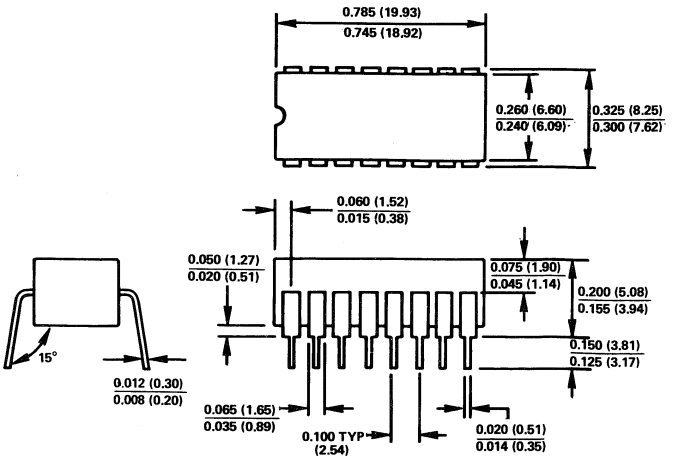
Positive Overload: 1011 (decodes as "EEE" on display via 9374 decoder driver).
Negative Overload: 1010 (decodes as "– – –" on display via 9374 decoder driver).
Negative Indication: 1010 during MSD (decodes as "–88" on display via 9374 decoder driver).

[1] Unadjusted gain and zero result in additional T.C. of 3.3μV/°C per unadjusted bit.
[2] Beyond which damage may occur.
Specifications subject to change without notice.

PIN CONFIGURATION
TOP VIEW



OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).



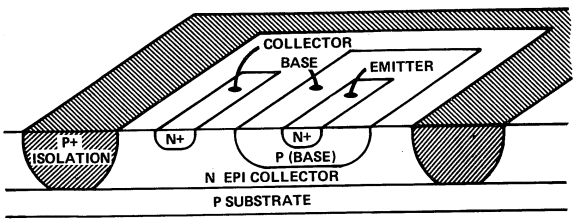


Figure 1. 3-Dimensional Section of Conventional NPN Transistor

Since I^2L logic gates can easily have multiple outputs, it is possible to use simple "wired-or logic", a means of implementing the logical "and" operation using only one conductor (wire).

A major contributor to I^2L's compactness is replacement of conventional "pullup" resistors or transistors by an injector bar. In Figure 2 the P injector acts as a combined power supply rail and pullup current source for the I^2L gates.

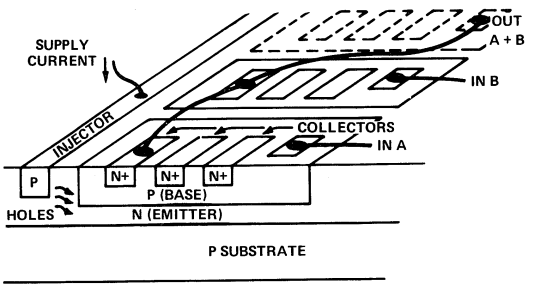


Figure 2. Sectional View of I^2L Circuit

Analog circuitry may be placed on the same chip by using conventional transistors like that of Figure 1. Thus, I^2L can be seen to combine the possibility of high-density logic functions with precision analog circuitry.

APPLYING THE AD2020

The Block Diagrams in Figure 3 and Figure 4 are two typical applications of the AD2020. In Figure 3 the AD2020 is shown in an application where LED's were the desired display. All of the A/D conversion takes place within the chip which feeds character serial data to a seven segment decoder driver. The appropriate digit is identified in three digit select lines. As shown, only 10 support components (including displays) are required. A return path for the bias current from each input (pins 11 and 10) to ground (pin 7) must be provided. Return impedance must not exceed 100kΩ.

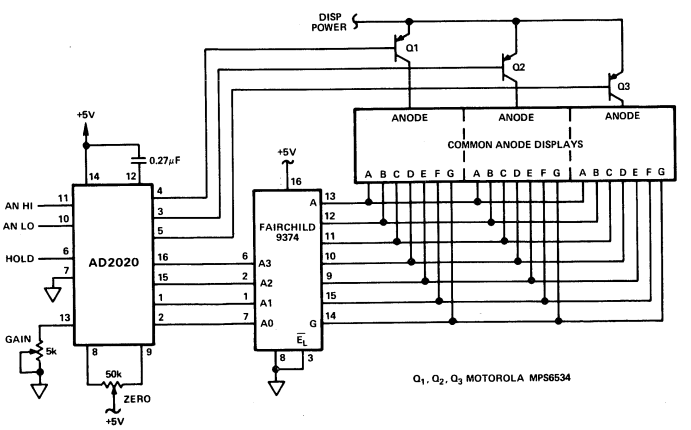


Figure 3.

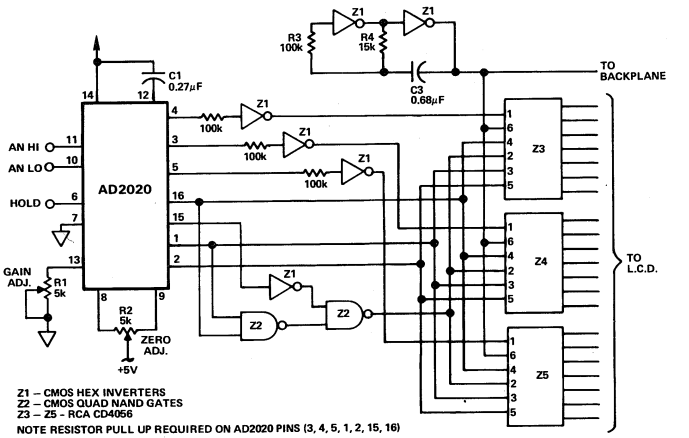
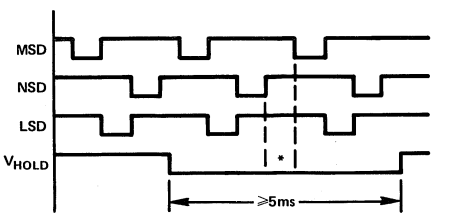


Figure 4.

The Block Diagram in Figure 4 shows an application where an LCD display was the choice. Digit selection is made via Z1, a HEX Inverter. The character serial BCD data feeds Z3, Z4, and Z5 LCD drivers by way of Z2, a CMOS quad nand gate. For CMOS compatibility, pullup resistors are required on the output pins (3, 4, 5, 1, 2, 15, 16).

TIMING DIAGRAM

The Timing Diagram, Figure 5, shows that the Hold input may be used as a psuedo-trigger provided the trigger pulse is ⩾5ms (insures at least 1 conversion). A conversion can only be initiated when all three digit lines are high and the Hold line is low. As shown, the sequence of digits is MSD, LSD, and NSD.



*CONVERSION TAKES PLACE HERE
NOTE: [1] OVERLAP MAY OCCUR BETWEEN DIGITS
[2] DATA IS VALID 2μsec. AFTER FALLING EDGE OF DIGIT SELECT LINE
[3] SWITCHING SPIKES MAY OCCUR ON DIGIT SELECT LINES

Figure 5.

A/D CONVERTER

The AD2020 can also be used as a low cost A/D Converter. The digit select signals are used to strobe the BCD data into latches. Since the AD2020 design was optimized for display applications, precautions should be taken in generating the strobe pulse. Figure 6 shows a typical configuration that provides filtering and delays necessary to ensure proper latching of data (4μs delay is sufficient).

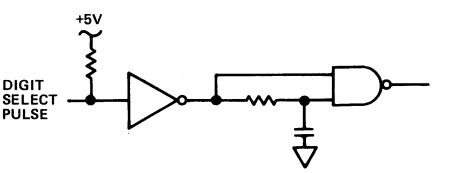


Figure 6.

HOLD, NORMAL, HIGH SPEED CONVERSIONS

Hold, normal and high speed conversion rates are controlled via voltage levels applied to the Hold pin (pin 6) of the AD2020. The circuit in Figure 7 shows how the three conditions are controlled by a single pin.

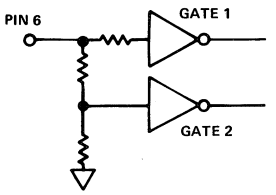


Figure 7.

- Normal Conversion
  A voltage less than 0.4V (or an open circuit) will keep both gate 1 and gate 2 off. The AD2020 in this state will convert at its normal rate.
- Hold
  A voltage greater than 0.8V but less than 1.6V will cause gate 1 to turn on but gate 2 will remain off. In this state the AD2020 will "hold" the last valid conversion.

  High Speed
  A voltage greater than 3.2V will cause both gates to turn on allowing the AD2020 to convert at its maximum rate.

Logic Compatibility

A typical circuit for making the AD2020 hold function logic compatible is shown in Figure 8. A Logic "1" applied to the base of the transistor will allow normal operation. A Logic "0" will cause the AD2020 to "hold".

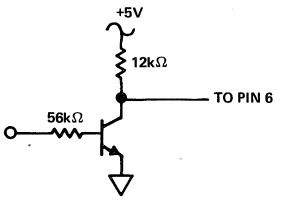
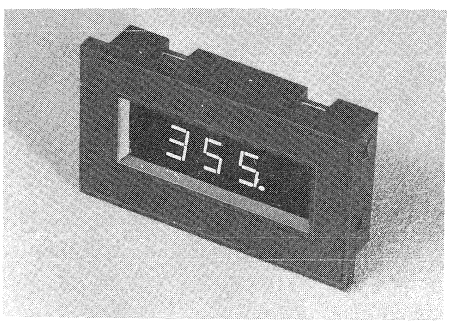
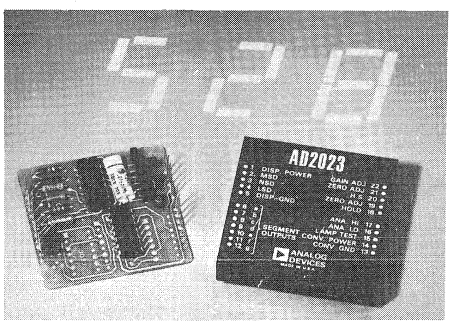
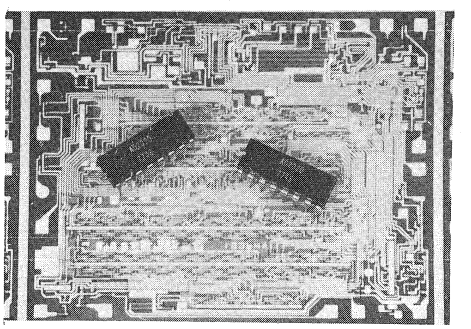


Figure 8.

"3RD GENERATION I^2L"







THE AD2026

The AD2026 was specifically designed to provide a digital alternative to analog panel meters. The complete DPM is mounted on a single 3″ by 1 5/8″ PCB. A unique case design utilizes molded-in fingers, both to capture the PCB and to provide snap-in mounting of the DPM in a standard panel cutout. No mounting hardware of any kind is used. The DPM occupies less than 1″ of space behind the panel. Only 13 components (including 3 decimal point resistors) in addition to the AD2020 make up the AD2026. Reliability is assured by the low component count, low internal heat rise (5°C), and extensive factory testing. MTBF is 260,000 hours at +25°C (for further information on the AD2026 consult factory).

THE AD2023

The AD2023 is a 3 digit DPM module containing all the circuitry, except gain adjust pot, to drive three external display digits. The AD2023 with 7-segment output and the AD2023/B, with character serial BCD output, enables the user to drive most any type of display. Like the AD2026, the AD2023 is based on the AD2020. Packaged in a small 2″ x 2″ x 0.4″ module and requiring only +5V power, the AD2023 and AD2023/B address DPM needs where available front panel space is limited. Optional operating temperature extremes of −40°C and +100°C and storage temperatures of −55°C and +125°C allow the user to apply the AD2023 in environments where conventional DPM's cannot be used.

AD2020

Completing the "Third Generation I^2L Family", Analog Devices now makes the AD2020 available to the market. Requiring only 10 support components, the AD2020 is the most complete DPM Chip available today. High reliability and performance are proven by success of the AD2026, introduced in November 1976.

3 Digit DPM Module

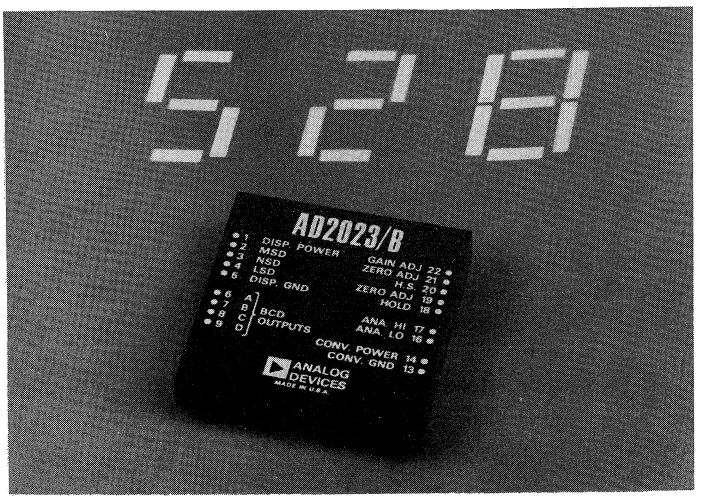
AD2023

FEATURES

- Third Generation I^2L LSI Design
- Multiplexed Seven Segment Output Version
- Character Serial BCD Output Version
- Balanced Differential Input
- Low Power: +5V @ 0.1 Watts (Converter Only)
- Small Size 2" x 2" x 0.4" (51x51x10.2mm)
- Wide Operating Temperature Range to Extremes of -40°C and +100°C Available Upon Special Request
- Low Cost

APPLICATIONS

- LED, LCD, Beckman, etc. Display, Digital Panel Meters (DPM's), Particularly Where Available Front Panel Meters Prohibits Use of Traditional DPM's.
- ADC Requirements



GENERAL DESCRIPTION

The AD2023 is a low cost, 3 digit DPM module containing all the circuitry, except gain adjust pot, to drive three external display digits. The AD2023, with seven segment output, and the AD2023/B, with character serial BCD output, enable the user to drive any type of digital display.

Packaged in a small 2" x 2" x 0.4" module and requiring only +5V power, the AD2023 and AD2023/B address DPM needs where available front panel space is limited.

The module, utilizing an I^2L LSI design, minimizes component count. Most of the analog and digital circuitry is implemented on a single proprietory chip. The design is similar to and is based on the same I^2L device as the highly successful AD2026 DPM. And all of the high AD2026 standards for quality and reliability are retained.

AD2023 (WITH SEVEN SEGMENT OUTPUT)

The AD2023 can drive a 3 digit LED (light emitting diode) display. Except for the display which is wired directly to the segment output pins of the module and a gain pot, all the circuitry is self contained (an optional offset pot can also be used if desired). The AD2023 drives any size and type of currently available LED display (for application assistance see Figure 3).

AD2023/B (WITH BCD OUTPUT)

With appropriate decoder driver, the AD2023/B character serial BCD output unit can drive a variety of different displays . . . ie., LED, LCD, Beckman, etc. . Only decoder driver, gain adjust pot, display and digit drivers when necessary are needed to complete the DPM.

EXCELLENT PERFORMANCE

The AD2023 measures inputs from -99mV to +999mV with an an accuracy of 0.1% of reading ±1 digit. Zero shift is ±0.5mV over the full operating temperature range, resulting in the same performance as a DPM with auto zero. The balanced differential input rejects common mode voltages up to 200mV, enough to eliminate most ground loop problems.

Automatic polarity indication is provided by using the MSD (most significant digit) to indicate negative inputs. With the AD2023, automatic overrange indication for inputs greater than +999mV is displayed as ⊐ ⊐ ⊐ and for inputs less than -99mV, as - - -. The AD2023/B overload indication is BCD output code 1011 for all digits for inputs greater than +999mV and 1010 for all digits for inputs less than -99mV.

WIDE TEMPERATURE RANGE

Wide temperature range modules, for extreme environment applications, are available upon special request. Operating temperature extremes of -40°C and +100°C and storage temperature of -55°C and +125°C allow the user to apply the AD2023 in environments where conventional DPM's cannot be used. Wide temperature range displays are also currently available from several vendors. (For further information consult factory.)

SPECIFICATIONS (typical @ +25°C and +5V dc unless otherwise noted)

ANALOG INPUT
- Configuration: Limited bipolar, balanced differential input.
- Full Scale Input Range: -99mV to +999mV
- Automatic Polarity
- Input Impedance: 100MΩ
- Bias Current: 110nA
- Over Voltage Protection: ±15V (Inputs to Ground)

AD2023 DISPLAY OUTPUTS
- Display Current: 46mA/segment multiplexed
- Positive Overload Indication: ⅃ ⅃ ⅃
- Negative Range Overload Indication: - - -
- Digit Select Outputs: Supply Voltage, 5.5V (max) I_{OUT}, 480mA (max pk)

AD2023/B DATA/DISPLAY OUTPUTS
- Negative Indication: BCD code 1010 during MSD
- Positive Overload Indication: BCD code 1011 for all digits
- Negative Overload Indication: BCD Code 1010 for all digits
- Output Loading: I_{OL} = 8mA @ $V_{OUT} \leq 0.5V$ I_{OL} = -400μA @ $V_{OUT} \geq 2.7V$
- Digit Select Outputs: Supply Voltage, 5.5V (max) I_{OUT}, 100mA (max pk)

ACCURACY
- 0.1% reading ±1 digit
- Resolution: 1mV
- Linearity: ±1 Bit
- Temperature Range[1]: -10°C to +70°C operating -55°C to +125°C storage
- Temperature Coefficient: Gain: 50ppm/°C Zero: 10μV/°C (essentially auto zero)
- Warm Up Time to Rated Accuracy: Instantaneous
- Settling Time to Rated Accuracy: 0.3 second for full input voltage swing
- Input Offset Voltage: ±0.3mV (max)

COMMON MODE REJECTION (1kΩ source imbalance, dc to 1kHz)
- 50dB

COMMON MODE VOLTAGE
- ±200mV

CONVERSION RATE
- Normal: 4 conversions per second
- High Speed (H.S.): 48 to 168 conversion per second

CONTROL INPUTS
- $\overline{\text{Hold}}$ (1LSTTL Load). Logic "0" or grounding disables internal or external trigger and last conversion is held. Logic "1" allows for normal operation.
- High Speed: Logic "0" on the $\overline{\text{Hold}}$ pin (18) and connecting the H.S. pin (20) to +5V, the module will convert 48 to 168 times per second.
- Lamp Test - Logic "0" on the Lamp Test pin (15) will turn all segments on in the positive range only.

GAIN ADJUST
- A 5k multiturn pot connected from the gain pin (22) to ground provides the full scale adjustment. This pot is user supplied.

EXTERNAL ZERO ADJUST (OPTIONAL)
- A 10kΩ pot across the zero terminals and the center arm to +5V the user can externally adjust zero offset.

POWER INPUT
- Converter: +5V ±5%, 0.1 watts typ.; 0.16 watts max
- Display: +4.75V to +5.5V @ 1.3 watts typ

SIZE
- Module 2" x 2" x 0.4" (51 x 51 x 10.2mm)

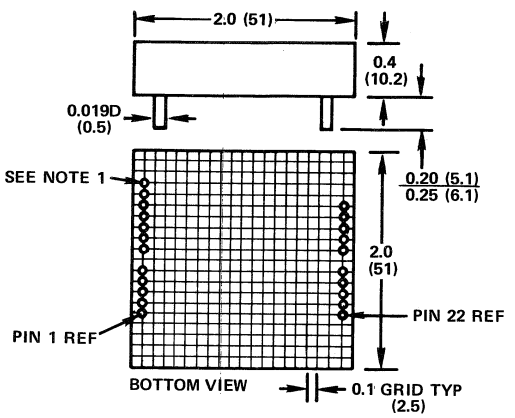
WEIGHT
- 1 ounce (28.4 grams)

ORDERING GUIDE
- AD2023: Multiplexed seven segment output
- AD2023/B: Character serial BCD output
- AC2623: Mounting card with gain and zero adjusts
- AC2625: Mounting card with gain and zero adjusts and three ½" high LED's

[1] Guaranteed

Specifications subject to change without notice.

NOTES:
1. PINS 10, 11, 12 AND 15 NOT ON MODEL AD2023/B



OUTLINE DIMENSIONS AND PIN CONFIGURATIONS

Dimensions shown in inches and (mm).

AD2023

1	DISP. POWER	22	GAIN ADJUST
2	MSD	21	ZERO ADJUST
3	NSD	20	H. S.
4	LSD	19	ZERO ADJUST
5	DISP. GND	18	HOLD
6	A	17	ANALOG HI
7	B	16	ANALOG LO
8	C (SEGMENT OUTPUTS)	15	LAMP TEST
9	D	14	CONV. POWER
10	E	13	CONV. GND
11	F		
12	G		

AD2023/B

1	DISP. POWER	22	GAIN ADJUST
2	MSD	21	ZERO ADJUST
3	NSD	20	H. S.
4	LSD	19	ZERO ADJUST
5	DISP. GND	18	HOLD
6	A	17	ANALOG HI
7	B (BCD OUTPUTS)	16	ANALOG LO
8	C	14	CONV. POWER
9	D	13	CONV. GND

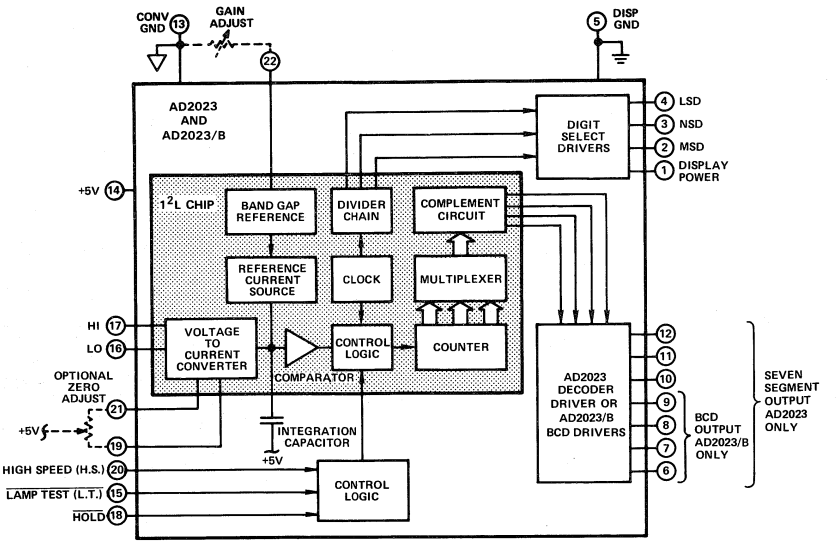


Figure 1. Block Diagram

MOUNTING CARDS

To make AD2023 evaluation easy, two accessory mounting cards are available. Both are 4½"x4" (114.3x101.6mm) printed circuit cards. One comes equipped with gain and zero adjust pots and is suitable for use with the AD2023 or AD2023/B. The other also includes ½" high LED display and is used with the AD2023. 3.4 square inches of breadboarding area is also provided on the two accessory cards. Interconnect is via standard 44 pin card edge connector.

APPLYING THE AD2023

Description of Operation

The AD2023 and AD2023/B Block Diagram is shown in Figure 1. The two versions are functionally identical except at the data output section. In the AD2023 the 4 BCD lines from the I^2L Chip are fed into a Decoder Driver and presented on pins 6 through 12 in seven segment output form for use with LED displays. The BCD lines in the AD2023/B model are processed through BCD Drivers and are presented on pins 6 through 9 in a Character Serial BCD format.

Signal input, user supplied Gain adjust and optional Zero adjust connections are applied directly to the chip. Hold, High Speed conversion and Lamp Test are implemented via Control Logic circuitry.

Most of the Analog to Digital conversion takes place within the chip which feeds Character Serial data to a seven segment decoder driver (AD2023) or BCD line drivers (AD2023/B). The appropriate digit is identified via three digit select lines.

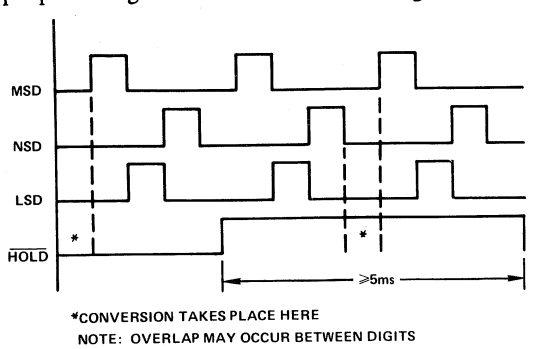


Figure 2. Timing Diagram

The Timing Diagram, Figure 2, shows that the Hold input may be used as a psuedo-trigger provided the trigger pulse is ≥5ms (insures at least 1 conversion). A conversion can only be initiated when all three digit lines are low and the Hold line is high. As shown, the sequence of digits is MSD, LSD, and NSD.

Led Dispaly DPM

The total requirement to construct a LED display DPM using the AD2023 is shown in Figure 3.

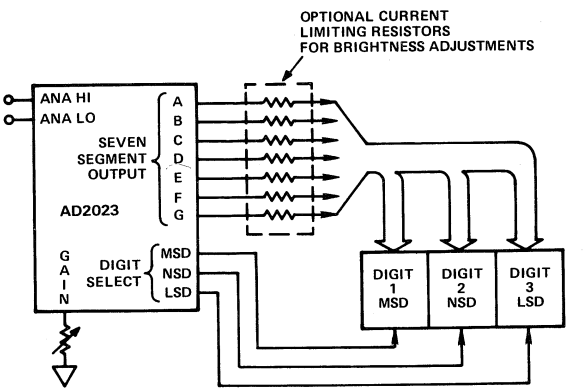


Figure 3. AD2023 with LED Interface

LCD Display DPM

Construction of LCD display DPM requires only an AD2023, LCD driver and the LCD's.

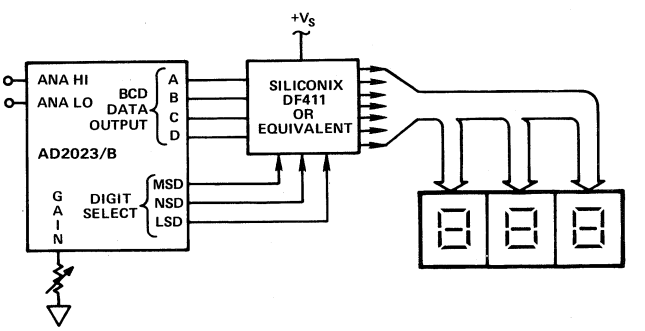


Figure 4. AD2023/B with LCD Interface

Beckman Display DPM

If a Beckman Gas Discharge Display is desired added components are: three displays, one DD700 Decoder Driver and three High Voltage Anode Drivers.

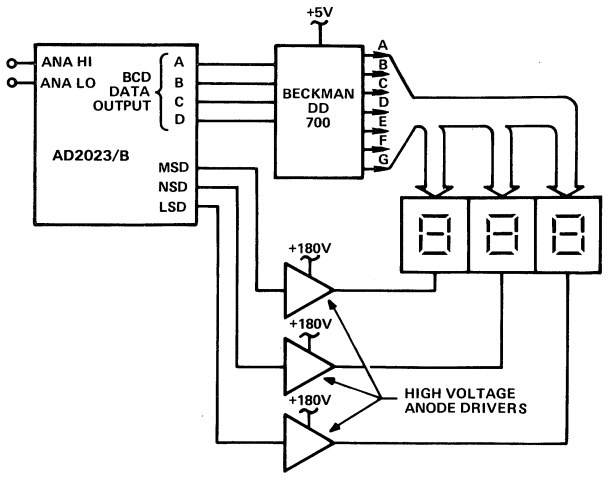


Figure 5. AD2023/B with Beckman Interface

BCD Output DPM

In some cases the AD2023/B may be the choice even when LED display is to be used. This permits the AD2023/B BCD output to drive other devices as well as the display and display can be used to show converted data directly and/or processed data. Figure 6 shows a BCD output DPM with LED displays. It is possible to obtain BCD outputs in this fashion when using other displays as well.

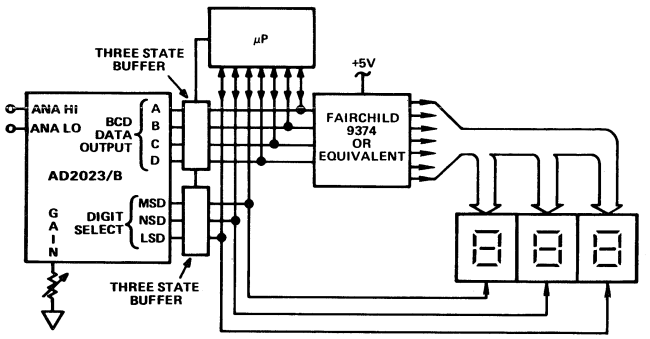


Figure 6. AD2023/B with LED/μP Interface

Input Wiring Connections

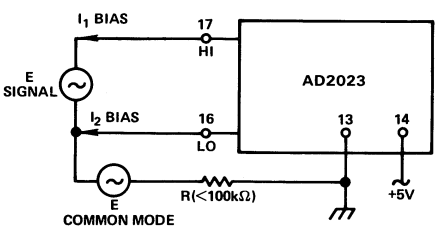


Figure 7.

Connect to AD2023 as per above for balanced differential input as shown. The common mode loop MUST provide a return path for Bias Currents (I_1 Bias, I_2 Bias) internal to the AD2023. The resistance (R) of this path must be less than 100kΩ. CAUTION: Total Common Mode Voltage between Pins 13 and 16 must not exceed 200mV.

For single ended input, connect Pin 13 to Pin 16.

Accessory Cards

As shown in Figures 8 and 9, two cards are available, the AC2623 with Gain and Zero Pots and the AC2625 with Gain Pot, Zero Pot and three seven segment LED displays. Both versions come complete with solder pads, power buss tracks and other features to allow for easy breadboarding. Right angle connectors for mounting LED's perpendicular to the P.C. board are available and accessory card is laid out to be able to receive these connectors. Connectors are availabe from Augat 6x51-73-161 and Aries Electronics 34-6823-90.

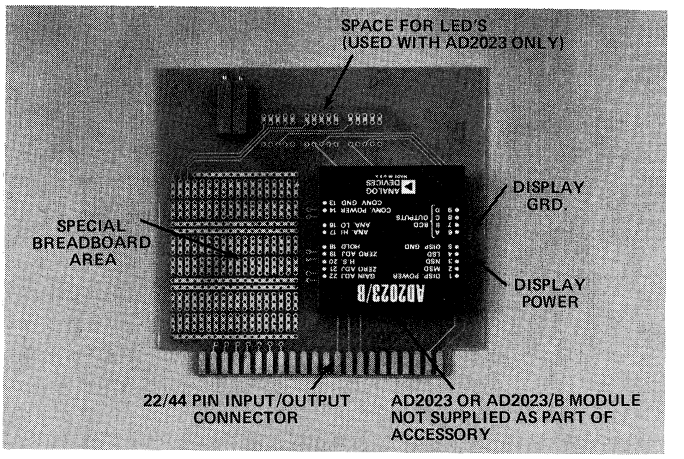


Figure 8. AC2623

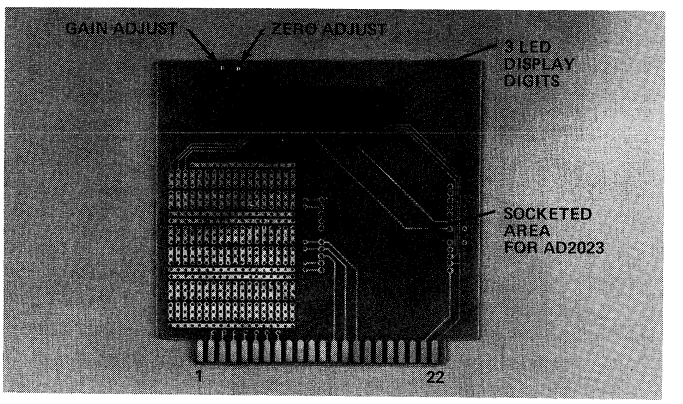


Figure 9. AC2625

1		A	
2		B	
3		C	
4		D	
5		E	
6		F	
7		H	
8		J	ANALOG HIGH
9		K	ANALOG LO
10		L	LAMP TEST
11	SPARE	M	CONV. POWER
12	SPARE	N	POWER GND.
13	HIGH SPEED	P	SEG G
14	ZERO ADJUST	R	F
15	HOLD	S	E
16		T	D (BCD D)
17		U	C (BCD C)
18		V	B (BCD B)
19		W	SEG A (BCD A)
20		X	DISPLAY GND.
21	MSD	Y	LSD
22	DISPLAY POWER	Z	NSD

Figure 10. Accessory Card Pin Connections

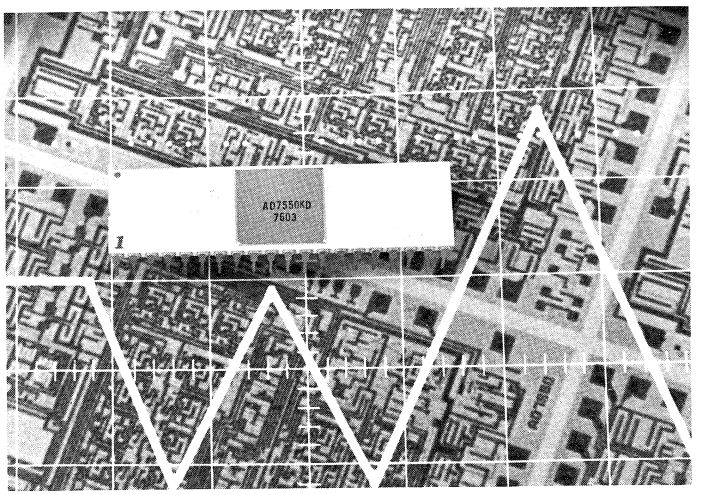
ANALOG DEVICES

CMOS 13-Bit Monolithic A/D Converter

AD7550

FEATURES

- Resolution: 13 Bits, 2's Complement
- Relative Accuracy: ±1/2 LSB
- "Quad Slope" Precision
  - Gain Drift: 1ppm/°C
  - Offset Drift: 1ppm/°C
- Microprocessor Compatible
- Ratiometric
- Overrange Flag
- Very Low Power Dissipation
- TTL/CMOS Compatible
- CMOS Monolithic Construction



GENERAL DESCRIPTION

The AD7550 is a 13-bit (2's complement) monolithic CMOS analog-to-digital converter on a 118 x 125 mil die packaged in a 40-pin ceramic DIP. Outstanding accuracy and stability (1ppm/°C) is obtained due to its revolutionary integrating technique, called "Quad Slope" (Analog Devices patent No. 3872466). This conversion consists of four slopes of integration as opposed to the traditional dual slope and provides much higher precision.

The AD7550 parallel output data lines have three-state logic and are microprocessor compatible through the use of two enable lines which control the lower eight LSB's (low byte enable) and the five MBS's (high byte enable). An overrange flag is also available which together with the BUSY and $\overline{\text{BUSY}}$ flags can be interrogated through the STATUS ENABLE providing easy microprocessor interface.

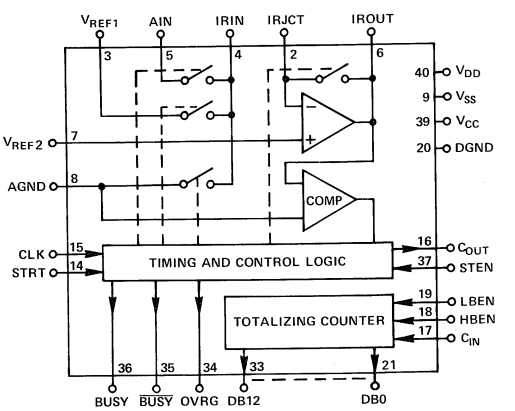
The AD7550 conversion time is about 40ms with a 1MHz clock. Clock can be externally controlled or internally generated by simply connecting a capacitor to the clock pin. A positive start pulse can be self-generated by having a capacitor on the start pin or can be externally applied.

For most applications, the AD7550 needs only three resistors, one capacitor, and a reference voltage since the integrating amplifier, comparator, switches and digital logic are all on the CMOS chip.

A wide range of power supply voltages (±5V to ±12V) with minuscule current requirements make the AD7550 ideal for low power and/or battery operated applications. Selection of the logic (V_{CC}) supply voltage (+5V to V_{DD}) provides direct TTL or CMOS interface on the digital input/output lines.

The AD7550 uses a high density CMOS process featuring double layer metal and silicon nitride passivation to ensure high reliability and long-term stability.

FUNCTIONAL DIAGRAM



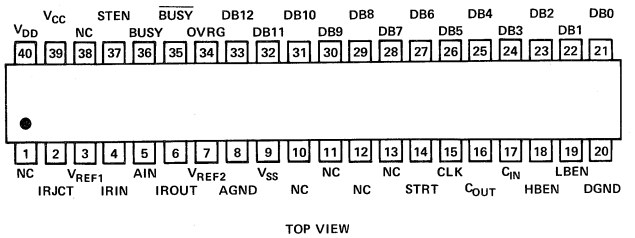
SPECIFICATIONS (V_{DD} = +12V, V_{SS} = -5V, V_{CC} = +5V, V_{REF1} = +4.25V unless otherwise noted)

PARAMETER	TA = +25°C	OVER SPECIFIED TEMPERATURE RANGE	TEST CONDITIONS
ACCURACY			
Resolution		13 Bits 2's Comp min	
Relative Accuracy	±0.5LSB max	±0.5LSB max	f_{CLK} = 100kHz, R1 = 1MΩ,
Gain Error	±0.5LSB max		C1 = 0.005μF, IRJCT Voltage
Gain Error Drift	1ppm/°C typ		Adjusted to $\frac{V_{REF1}}{2}$ ±0.6%
Offset Error	±0.5LSB max		
Offset Error Drift	1ppm/°C typ		
ANALOG INPUTS			
AIN Input Resistance[1]	R1MΩ min		
V_{REF1} Input Resistance[1]	R1MΩ min		
V_{REF2} Leakage Current	10pA typ		
DIGITAL INPUTS			
CIN, LBEN, HBEN, STEN			
V_{INL}	+0.8V max	+0.8V max	V_{CC} = +5V
V_{INH}	+2.4V min	+2.4V min	
V_{INL}	+1.2V max	+1.2V max	V_{CC} = +12V
V_{INH}	+10.8V min	+10.8V min	
I_{INL}, I_{INH}	5nA typ		
START			
V_{INL}	+0.8V max	+0.8V max	V_{CC} = +5V to V_{DD}
V_{INH}	+2.4V min	+2.4V min	
I_{INL}	-1μA typ		V_{CC} = +5V to V_{DD}, BUSY = Low
I_{INH}	+150μA typ		V_{CC} = +5V to V_{DD}, BUSY = High
CLOCK			
V_{INL}	+0.8V max	+0.8V max	V_{CC} = +5V
V_{INH}	+3V min	+3V min	
V_{INL}	+1.2V max	+1.2V max	V_{CC} = +12V
V_{INH}	+10.8V min	+10.8V min	
I_{INL}	-100μA typ		V_{IN}=V_{INL}; V_{CC} = +5V to +12V
I_{INH}	+100μA typ		V_{IN}=V_{INH}; V_{DD}= +5V to +12V
DIGITAL OUTPUTS			
V_{OUTL}	+0.5V max	+0.8V max	V_{CC} = +5V, I_{SINK} = 1.6mA
V_{OUTH}	+2.4V min	+2.4V min	V_{CC} = +5V, I_{SOURCE} = 40μA
V_{OUTL}	+1.2V max	+1.2V max	V_{CC} = +12V, I_{SINK} = 1.6mA
V_{OUTH}	+10.8V min	+10.8V min	V_{CC} = +12V, I_{SOURCE} = 0.6mA
Capacitance (Floating State) (OVRG, $\overline{BUSY}$, BUSY, and DB0–DB12)	5pF typ		
I_{LKG} (Floating State) (OVRG, $\overline{BUSY}$, BUSY, and DB0–DB12)	±5nA typ		V_{CC} = +5V to +12V V_{OUT} = 0V and V_{CC}
DYNAMIC PERFORMANCE			
Conversion Time	40ms typ		$V_{IN(CLK)}$ = 0 to +3V, f_{CLK} = 1MHz
STEN, HBEN, LBEN Propagation Delay t_{ON}, t_{OFF}	250ns typ, 500ns max		V_{IN}(STEN, HBEN, LBEN) 0 to +3V
External STRT Pulse Duration	800ns min		$V_{IN(STRT)}$ = 0 to +3V
POWER SUPPLIES			
V_{DD} Range	+10V min, +12V max		
V_{SS} Range	-5V min, -12V max		
V_{CC} Range	+5V min, V_{DD} max		
I_{DD}	0.6mA typ, 2mA max		
I_{SS}	0.3mA typ, 2mA max		f_{CLK} = 1MHz
I_{CC}	0.06mA typ, 2mA max		

[1] The equivalent input circuit is the integrator resistor R_1 (1MΩ min, 10MΩ max) in series with a voltage source $\frac{V_{REF1}}{2}$, (see Figure 1).

Specifications subject to change without notice.

PIN CONFIGURATION



TOP VIEW

ORDERING INFORMATION

Model	Temperature Range	Package
AD7550BD	−25°C to +85°C	Ceramic

ABSOLUTE MAXIMUM RATINGS

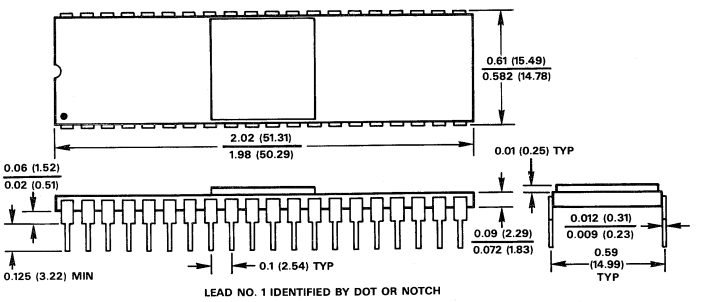
V_{DD} to AGND . . . . . 0V, +14V
V_{DD} to DGND . . . . . 0V, +14V
V_{SS} to AGND . . . . . 0V, −14V
V_{SS} to DGND . . . . . 0V, −14V
AGND to DGND . . . . . 0V, +14V
V_{CC} to DGND . . . . . .0V, V_{DD}
V_{REF1} . . . . . V_{SS}, V_{DD}
V_{REF2} . . . . . AGND, V_{DD}
AIN . . . . . V_{SS}, V_{DD}
IRIN . . . . . V_{SS}, V_{DD}
IRJCT . . . . . AGND, V_{DD}
IROUT . . . . . V_{SS}, V_{DD}
Digital Input Voltage
HBEN, LBEN, STEN, C_{IN} . . . . . DGND, (DGND +27V)
CLK, START . . . . . DGND, V_{DD}
Digital Output Voltage
DB0–DB12, OVRG, BUSY, $\overline{BUSY}$, C_{OUT} . . . DGND, V_{CC}
Power Dissipation (Package)
Up to +50°C 1000mW
Derates above +50°C by . . . . . 10mW/°C
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature . . . . . −25°C to +85°C

CAUTION:

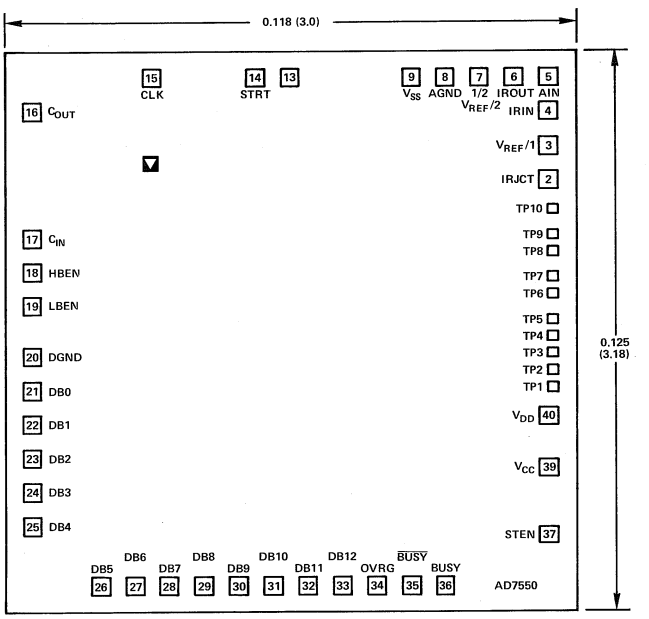
1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times. Prior to pulling the devices from the conductive foam, ground the foam to deplete any accumulated charge.
2. V_{CC} should never exceed V_{DD} by more than 0.4V, especially during power ON or OFF sequencing.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



40-Pin Ceramic Dip



Bonding Diagram

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	NC	No Connection
2	IRJCT	IntegratoR JunCTion. Summing junction (negative input) of integrating amplifier.
3	V_{REF1}	Voltage REFerence Input
4	IRIN	IntegratoR INput. External integrator input R is connected between IRJCT and IRIN.
5	AIN	Analog INput. Unknown analog input voltage to be measured. Fullscale AIN equals $V_{REF}/2.125$.
6	IROUT	IntegratoR OUTput. External integrating capacitor C_1 is connected between IROUT and IRJCT.
7	V_{REF2}	Voltage REFerence ÷ 2 Input
8	AGND	Analog GrouND
9	V_{SS}	Negative Supply (-5V to -12V)
10	NC	No Connection
11	NC	No Connection
12	NC	No Connection
13	NC	No Connection
14	STRT	STaRT Conversion. When STRT goes to a Logic "1," the AD7550's digital logic is set up and BUSY is latched "high." When STRT returns "low," conversion begins in synchronization with CLK. Reinitiating STRT during conversion causes a conversion restart. STRT can be driven from an external logic source or can be programmed for continuous conversion by connecting an external capacitor between STRT and DGND. An externally applied STRT command must be a positive pulse of at least 800 nanoseconds to ensure proper set-up of the AD7550 logic.
15	CLK	CLocK Input. The CLK can be driven from external logic, or can be programmed for internal oscillation by connecting an external capacitor between CLK and DGND.
16	C_{OUT}	Count OUT provides a number (N) of gated clock pulses given by: $N = \left[\frac{AIN}{V_{REF1}} \; 2.125 + 1\right] \; 4096$
17	C_{IN}	Count IN is the input to the output counter. 2's complement binary data appears on the DB0 through DB12 output lines (if the HBEN and LBEN enable lines are "high") if C_{OUT} is connected to C_{IN}.
18	HBEN	High Byte ENable is the three-state logic enable input for the DB8-DB12 data outputs. When HBEN is low, the DB8–DB12 outputs are floating. When HBEN is "high," digital data appears on the data lines.
19	LBEN	Low Byte ENable is the three-state logic enable for DB0–DB7. When LBEN is "low," DB0–DB7 are floating. When "high," digital data appears on the data lines.
20	DGND	Digital GrouND is the ground return for all digital logic and the comparator.
21	DB0	Data Bit 0 (least significant bit)
22	DB1	
23	DB2	
24	DB3	
25	DB4	
26	DB5	
27	DB6	CODE: 2's Complement
28	DB7	
29	DB8	
30	DB9	
31	DB10	
32	DB11	
33	DB12	Data Bit 12 (most significant bit)
34	OVRG	OVerRange indicates a Logic "1" if AIN exceeds plus or minus full scale by at least 1/2 LSB. OVRG is a three-state output and floats until STEN is addressed with a Logic "1".
35	$\overline{BUSY}$	Not BUSY. $\overline{BUSY}$ indicates whether conversion is complete or in progress. $\overline{BUSY}$ is a three-state output which floats until STEN is addressed with a Logic "1." When addressed, $\overline{BUSY}$ will indicate either a "1" (conversion complete) or a "0" (conversion in progress).
36	BUSY	BUSY indicates conversion status. BUSY is a three-state output which floats until STEN is addressed with a Logic "1." When addressed, BUSY indicates a "0" (conversion complete) or a "1" (conversion in progress).
37	STEN	STatus ENable is the three-state control input for BUSY, $\overline{BUSY}$, and OVRG.
38	NC	No Connection
39	V_{CC}	Logic Supply. Digital inputs and outputs are TTL compatible if V_{CC} = +5V, CMOS compatible for V_{CC} = +10V to V_{DD}.
40	V_{DD}	Positive Supply +10V to +12V.

PRINCIPLES OF OPERATION

BASIC OPERATION

The essence of the quad slope technique is best explained through Figures 1 and 2.

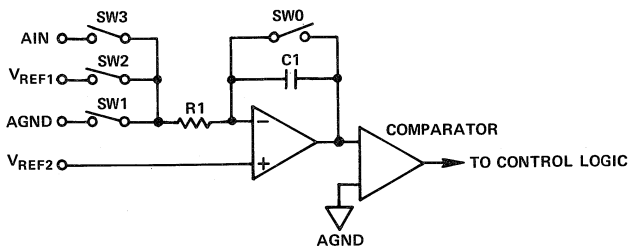


Figure 1. Quad Slope Integrator Circuit

The inputs AGND (analog ground), V_{REF1}, AIN (analog input) and V_{REF2} are applied in sequence to an integrator (Figure 1), creating four slopes (phases 1 through 4, Figure 2) at the integrator output. Voltage V_{REF2} is normally equal to $\frac{V_{REF1}}{2}$, but if not, will create an error count "n" that will be minimized by the "quad-slope" conversion process. V_{REF1} and V_{REF2} must be positive voltages.

The equivalent integrator input voltages and their integration times are shown in Table 1.

TABLE 1
INTEGRATOR EQUIVALENT INPUT VOLTAGES AND INTEGRATION TIMES

Phase	Input Voltage	Integration Time
1	$AGND-V_{REF2}$	$t_1 = K_1 t$
2	$V_{REF1}-V_{REF2}$	$t_2 = (K_1 + n)t$
3	$AIN-V_{REF2}$	$t_3 = (2K_1 - n)t$
4	$V_{REF1}-V_{REF2}$	$t_4 = (K_3 - 2K_1 + n - 2N)t$

where:
- t = The CLK period
- n = System error count
- K_1 = A fixed count equal to 4352 counts
- K_2 = A fixed count equal to 17408 counts ($K_2 = 4K_1$)
- K_3 = A fixed count equal to 25600 counts
- N = Digital output count corresponding to the analog input voltage, AIN

PHASE 0
After the start pulse is applied, switch SW2 is closed (all other switches open) and the integrator output is ramped to comparator zero crossing. Phase 0 can be considered the reset phase of the converter, and always has a duration $t_0 = R_1C_1$ (integrator time constant). Upon zero crossing, counters K_1 and K_2 are started, switch SW2 is opened and SW1 is closed.

PHASE 1
Phase 1 integrates ($AGND - V_{REF2}$) for a fixed period of time (by counter K_1) equal to $t_1 = K_1 t$. At the end of phase 1, switch SW1 is opened and SW2 is closed.

PHASE 2
The integrator input is switched to ($V_{REF1}-V_{REF2}$) and the output ramps down until zero crossing is achieved. The integration time $t_2 = (K_1 + n)t$ includes the error count "n" due to offsets, etc. At the end of phase 2, switch SW2 is opened, SW3 is closed, and a third counter (K_3) is started.

PHASE 3
Phase 3 integrates the analog input ($AIN - V_{REF2}$) until counter K_2 counts $4K_1t$. At this time SW3 is opened and SW2 is closed again.

PHASE 4
Phase 4 integrates ($V_{REF1}-V_{REF2}$) and the comparator output ramps down until zero crossing once again is achieved. Since the comparator always approaches zero crossing from the same slope, propagation delay is constant and hysteresis effect is eliminated.

Notes
1 $t = 1/f_{CLK}$
2 Time periods shown in BOLD are unaffected by n since they are determined by counters K_1, K_2, or K_3
3 STEN = LOGIC 1. If STEN = 0, BUSY and $\overline{BUSY}$ are in floating state

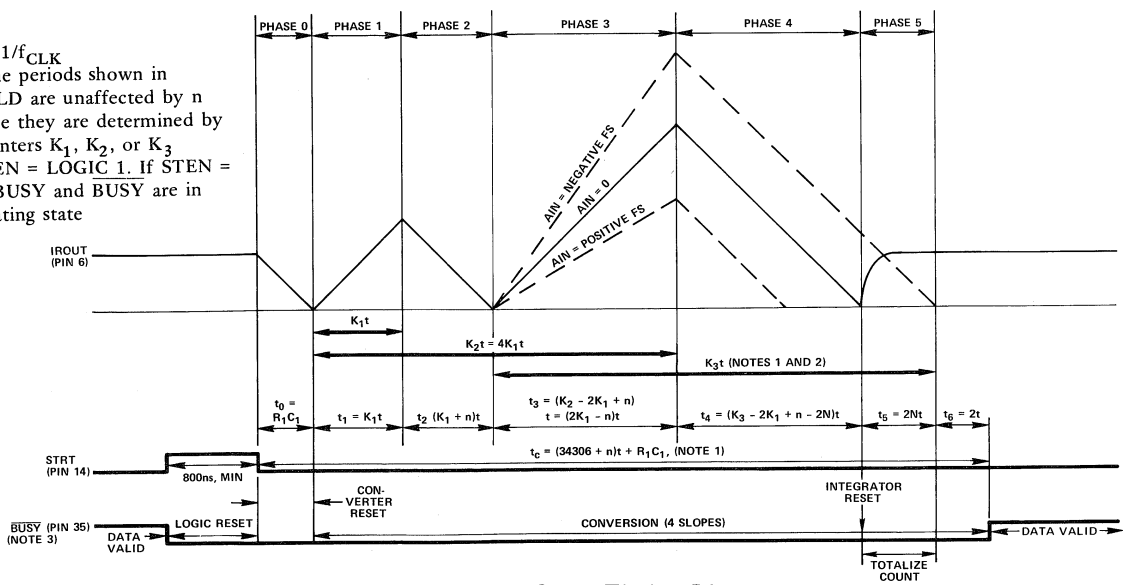


Figure 2. Quad Slope Timing Diagram

The time t_5 between the phase 4 zero crossing and the termination of counter K_3 is considered equal to 2N counts. N, the number of counts at the C_{OUT} terminal, is obtained by a divide-by-two counter stage. This reduces "jitter" effect. Barring third (and higher) order effects, it can be proven that:

(EQN 1)

$$N = \underbrace{\left(\frac{AIN}{V_{REF1}} - 1\right) \cdot 2K_1 + \frac{K_3}{2}}_{\text{ideal transfer function}} + \underbrace{\left(\frac{AIN}{V_{REF1}} - 1\right) \cdot \left[\frac{AGND}{V_{REF1}}(1 + 2\alpha) - \alpha^2\right] \cdot 2K_1}_{\text{error term}}$$

where:

$$\alpha = \frac{2V_{REF2} - V_{REF1}}{V_{REF1}}$$

The ideal case assumes:

AGND = 0V

$V_{REF2} = \frac{V_{REF1}}{2}$, therefore $\alpha = 0$

Then (EQN 1) simplifies to:

$$N = \frac{AIN}{V_{REF1}} \cdot 8704 + 4096 \qquad \text{(EQN 2)}$$

or

$$N = \frac{AIN}{V_{FS}} \cdot 4096 + 4096 \qquad \text{(EQN 3)}$$

where:

V_{FS} = full scale input voltage = $\frac{V_{REF1}}{2.125}$

The parallel output (DB0–DB12) of the AD7550 represents the number N in binary 2's complement coding when the C_{OUT} pin is connected to the C_{IN} pin (see Table II).

TABLE II
OUTPUT CODING (Bipolar 2's Complement)

Analog Input (Note 1)	N (Note 2)	Parallel Digital Output (Note 3)			
		OVRG	DB12		DB0
+Overrange	–	1	0	1 1 1 1	1 1 1 1
+VFS ($1-2^{-12}$)	8191	0	0	1 1 1 1	1 1 1 1
+VFS (2^{-12})	4097	0	0	0 0 0 0	0 0 0 1
0	4096	0	0	0 0 0 0	0 0 0 0
-VFS (2^{-12})	4095	0	1	1 1 1 1	1 1 1 1
-VFS	0	0	1	0 0 0 0	0 0 0 0
-Overrange	–	1	1	0 0 0 0	0 0 0 0

Notes
1 $V_{FS} = \frac{V_{REF1}}{2.125}$
2 N = number of counts at C_{OUT} pin
3 C_{OUT} strapped to C_{IN}; LBEN and HBEN = Logic 1

ERROR ANALYSIS

Equation 1 shows that only α and AGND generate error terms. Their impact can be analyzed as follows:

Case 1: AGND = 0, $\alpha \neq 0$

Error sources such as capacitor-leakage (I_L) and op amp offset (e) cause α to be different from zero.

Under this condition,

$$\alpha = \frac{2(e + I_L R_1)}{V_{REF1}}$$

where $I_L R_1$ is the equivalent error voltage generated by leakage I_L.

The evaluation of this error term is best demonstrated through the following example:

Assume:

e = 5mV, I_L = 5nA, R_1 = 1MΩ and V_{REF1} = 4.25V.

Then:

$\alpha = 4.7 \times 10^{-3}$

and:

$$N = \left[\frac{AIN}{V_{REF1}} - 1\right] \times 8704 + 12800 - \underbrace{\left[\frac{AIN}{V_{REF1}} - 1\right] \times 22.1 \times 10^{-6} \times 8704}_{\text{error term } N_\epsilon}$$

Therefore, the error count N_ϵ is as follows:

For AIN = $-V_{FS}$: N_ϵ = 0.28 counts = 0.28LSB
AIN = 0: N_ϵ = 0.19 counts = 0.19LSB
AIN = $+V_{FS}$: N_ϵ = 0.09 counts = 0.09LSB

The above example shows the strong reduction of the circuit errors because of the α^2 term in (EQN 1). Another consequence of this effect is that N_ϵ is always positive, regardless of the polarity of the circuit errors.

Case 2: AGND ≠ 0, $\alpha = 0$

When AGND is different from the signal ground, then this error will come through on a first-order basis. Indeed:

$$N = \left[\frac{AIN}{V_{REF1}} - 1\right] \cdot 8704 + 12800 + \underbrace{\left[\frac{AIN}{V_{REF1}} - 1\right] \cdot \frac{AGND}{V_{REF1}}}_{\text{error term } N_\epsilon}$$

The following example demonstrates the impact of AGND.

Let AGND = 1mV and V_{REF1} = 4.25V.

For AIN = $-V_{FS}$, then N_ϵ = 3.01 counts
AIN = 0, then N_ϵ = 2.05 counts
AIN = + V_{FS}, then N_ϵ = 1.08 counts

Therefore, ground loops should be minimized because a 330μV difference between AGND and signal ground will cause 1 count (1 LSB) of error when the analog input is at minus full scale. An optimized ground system is shown in Figure 7.

OPERATING GUIDELINES

The following steps, in conjunction with Figure 3, explain the calculations of the component values required for proper operation.

1. DETERMINATION OF V_{REF1}

When the full scale voltage requirement (VFS) has been ascertained, the reference voltage can be calculated by:

$V_{REF1} = 2.125\ (V_{FS})$

V_{REF1} must be positive for proper operation.

2. SELECTION OF C_3 (INTERNAL CLOCK OPERATION)

For internal clock operation, connect capacitor C_3 to the clock pin as shown in Figure 3. The clock frequency versus capacitor C_3 is shown in Figure 4.

The clock frequency must be limited to 1.3MHz for proper operation.

3. SELECTION OF INTEGRATOR COMPONENTS (R_1 AND C_1)

To ensure that the integrator's output doesn't saturate to its bound (V_{DD}) during the phase (3) integration cycle, the integrator time constant (R_1C_1) should be approximately equal to:

$$\pi = R_1C_1 = \frac{V_{REF}\ (9 \times 10^3)}{f_{CLK}\ (V_{DD} - 4V)}$$

The integrator components R_1 and C_1 can be selected by referring to Figure 5 and/or Figure 6. Figure 5 plots the time constant (R_1C_1) versus clock frequency for different reference voltages. Figure 6 is a direct plot of the required C_1 versus f_{CLK} for R_1 values of 1MΩ and 10MΩ.

R_1 can be a standard 10% resistor, but must be selected between 1MΩ to 10MΩ.

The integrating capacitor "C_1" must be a low leakage, low dielectric absorption type such as teflon, polystyrene or polypropylene. To minimize noise, the outside foil of C_1 must be connected to IR_{OUT}.

4. CONVERSION TIME

As shown in Figure 2, the conversion time is independent of the analog input voltage AIN, and is given by:

$$t_{convert} = t_{STRT} + \frac{34306}{f_{CLK}} + R_1C_1$$

where:

t_{STRT} = STRT pulse duration
R_1C_1 = Integrator Time Constant
f_{CLK} = CLK Frequency

For example, if V_{REF1} = 4.25V, R_1 = 1MΩ, C_1 = 400pF and CLK = 1MHz, the conversion time (not including t_{STRT}, which is normally only microseconds in duration) is approximately 40 milliseconds.

5. EXTERNAL OR AUTO STRT OPERATION

The STRT pin can be driven externally, or with the addition of C_2, made to self-start.

The size of C_2 determines the length of time from end of conversion until a new conversion is initiated. This is the "data valid" time and is given by:

$t_{DAV} \approx (1.7 \times 10^6\Omega)\ C_2 + 20\mu s$

When first applying power to the AD7550, a 0V to V_{DD} positive pulse (power up restart) is required at the STRT terminal to initiate auto STRT operation.

6. INITIAL CALIBRATION

Trim R_4 (Figure 3) so that pin 2 (IRJCT) equals 1/2 V_{REF1} ±0.6%. When measuring the voltage on IRJCT, apply a Logic "1" to the STRT terminal.

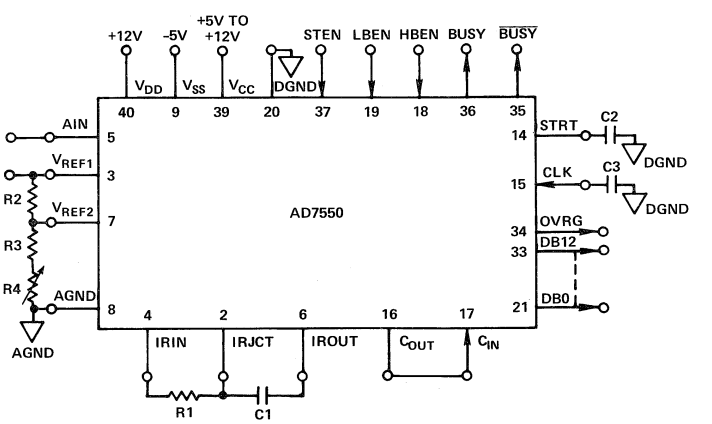


Figure 3. Operation Diagram

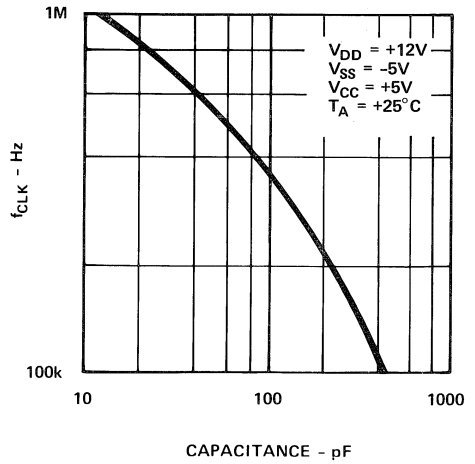


Figure 4. f_{CLK} vs. C_3

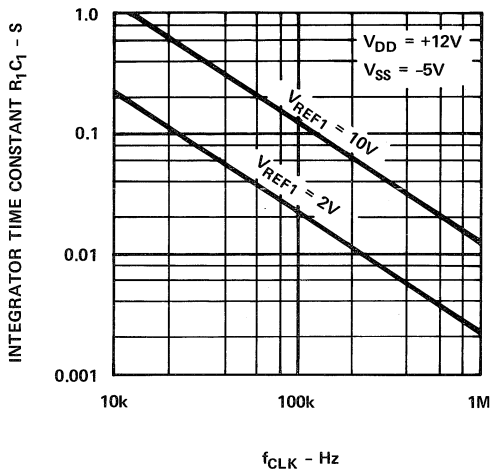


Figure 5. Integrator Time Constant (R_1C_1) vs. f_{CLK} for Different Reference Voltages

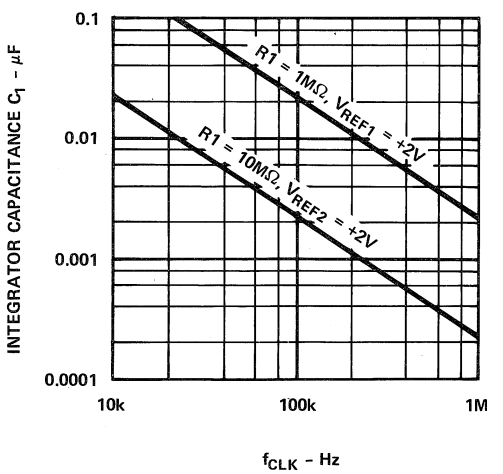


Figure 6. Integrator Capacitance (C_1) vs. f_{CLK} for Different Integrator Resistances (R_1)

APPLICATION HINTS

When operating at f_{CLK} greater than 500kHz, the following steps are recommended to minimize errors due to noise coupling (see Figure 7).

1. Decouple AIN (pin 5), V_{REF1} (pin 3) and V_{REF2} (pin 7) through 0.01µF to signal ground.
2. Signal ground must be located as close to pin 8 (AGND) as possible.
3. Keep the lead lengths of R_1 and C_1 toward pin 2 (IRJCT) as short as possible. In addition, both components should lie over the analog ground plane. If C_1 has an outside foil, connect it to pin 6 (IROUT), not pin 2.
4. Hold the data bit enables (HBEN, LBEN) in the 0 state during conversion. This is easily accomplished by tying STEN to the 1 state and driving HBEN and LBEN with BUSY. This prevents the DB0 through DB12 outputs from coupling noise into the integrator during the phase 1–4 active integration periods.

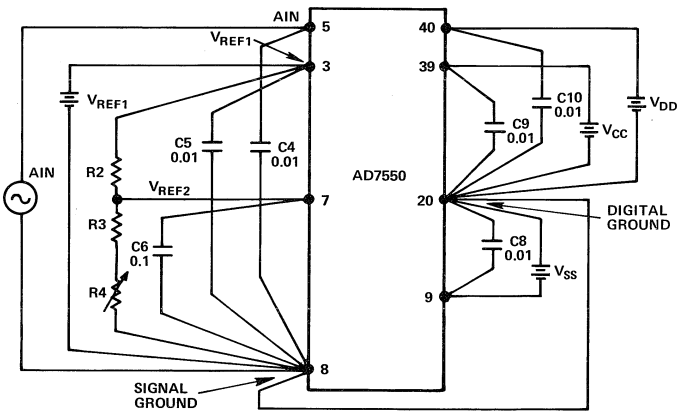
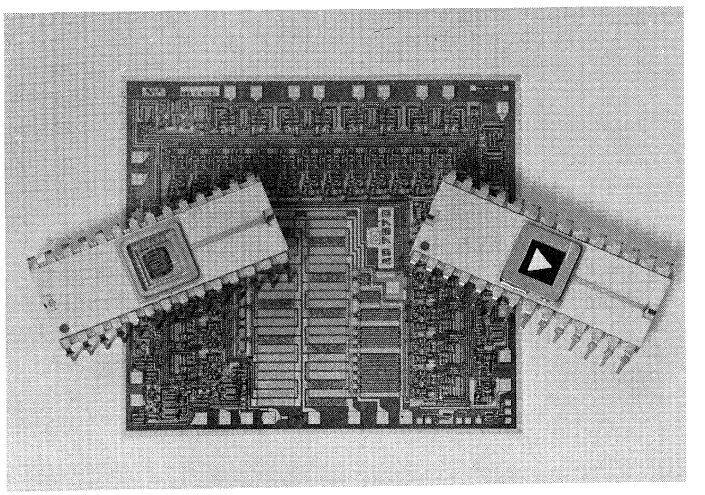


Figure 7. Ground System

CMOS 10-Bit Monolithic A/D Converter

AD7570

FEATURES
- 8 and 10-Bit Resolution
- 20μs Conversion Time
- Microprocessor Compatibility
- Very Low Power Dissipation
- Parallel and Serial Outputs
- Ratiometric Operation
- TTL/DTL/CMOS Logic Compatibility
- CMOS Monolithic Construction



GENERAL DESCRIPTION

The AD7570 is a monolithic CMOS 10-bit successive approximation A/D converter on a 120 by 135 mil chip, requiring only an external comparator, reference and passive clocking components. Ratiometric operation is inherent, since an extremely accurate multiplying DAC is used in the feedback loop.

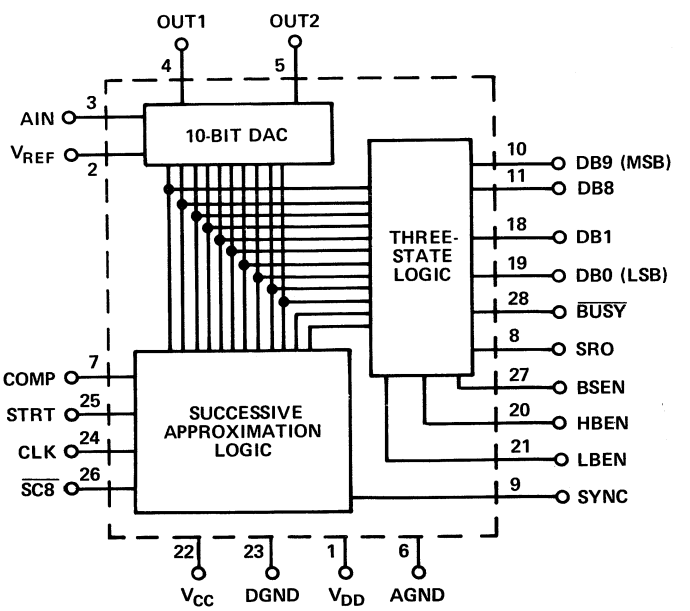
The AD7570 parallel output data lines and Busy line utilize three-state logic to permit bussing with other A/D output and control lines or with other I/O interface circuitry. Two enables are available: one controls the two MSBs; the second controls the remaining 8 LSBs. This feature provides the control interface for most microprocessors which can accept only an 8 bit byte.

The AD7570 also provides a serial data output line to be used in conjunction with the serial synchronization line. The clock can be driven externally or, with the addition of a resistor and a capacitor, can run internally as high as 0.6MHz allowing a total conversion time (8 bits) of typically 20μs. An 8 bit short cycle control pin stops the clock after exercising 8 bits, normally used for the "J" version (8 bit resolution).

The AD7570 requires two power supplies, a +15V main supply and a +5V (for TTL/DTL logic) to +15V (for CMOS logic) supply for digital circuitry. Both analog and digital grounds are available.

The AD7570 is a monolithic device using a proprietary CMOS process featuring a double layer metal interconnect, on-chip thin-film resistor network and silicon nitride passivation ensuring high reliability and excellent long term stability.

FUNCTIONAL DIAGRAM



SPECIFICATIONS (V_{DD} = +15V, V_{CC} = +5V, V_{REF} = ±10V unless otherwise noted)

PARAMETER[1]	VERSIONS	T_A = +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
ACCURACY				
Resolution	J	8 Bits min	8 Bits min	$\overline{SC8}$ = Logic "0"
	L	10 Bits min	10 Bits min	$\overline{SC8}$ = Logic "1"
Quantization Uncertainty	J, L	±1/2LSB max	±1/2LSB max	
Relative Accuracy	J, L	±1/2LSB max	±1/2LSB max	f_{CLK} = 100kHz
Differential Nonlinearity	J, L	1LSB max	1LSB max	See Figure 5
Gain Error	J, L	0.3% Reading typ		
Gain Temperature Coefficient	J, L	5ppm Reading per °C typ	10ppm Reading per °C max	
ANALOG INPUTS				
Analog Input Resistance	J, L	10kΩ typ	5kΩ min, 20kΩ max	
Analog Input Resistance Tempco	J, L	−150ppm/°C typ		
Reference Input Resistance	J, L	10kΩ typ	5kΩ min, 20kΩ max	
Reference Input Resistance Tempco	J, L	−150ppm/°C typ		
ANALOG OUTPUTS				
Output Leakage Current (OUT1, OUT2)	J, L	10nA typ	200nA max	$V_{OUT1, 2}$ = 0V DB0 through DB9 = Logic "1"
Output Capacitance OUT1	J, L	120pF typ		
OUT2	J, L	40pF typ		
OUT1	J, L	40pF typ		DB0 through DB9 = Logic "0"
OUT2	J, L	120pF typ		
DIGITAL INPUTS				
V_{INL}[2]	J, L	+1.4V typ, +0.8V max	+0.8V max	V_{CC} = +5V
V_{INH}[2]	J, L	+2.4V min, +1.4V typ	+2.4V min	
V_{INL}[2]	J, L	+1.5V max	+1.5V max	V_{CC} = +15V
V_{INH}[2]	J, L	+13.5V min	+13.5V min	
I_{INL}, I_{INH}[3]	J, L	±0.1μA typ, ±10μA max		V_{IN} = 0 to V_{CC}
CLK Input Current	J, L	+0.4mA typ, +1mA max		During Conversion V_{CC} = +5V; 2.4V ≤ V_{IN} ≤ V_{CC}
CLK Input Current	J, L	+1.7mA typ, +3mA max		During Conversion V_{CC} = +15V; 10V ≤ V_{IN} ≤ V_{CC}
CLK Input Current	J, L	±1μA typ		V_{CC} = +5V to +15V Conversion Complete or CLK IN ≤ V_{INL}
C_{IN}	J, L	2pF typ		
DIGITAL OUTPUTS				
V_{OUTL}	J, L	+0.5V max	+0.8V max	V_{CC} = +5V, I_{SINK} = 1.6mA
V_{OUTH}	J, L	+2.4V min	+2.4V min	V_{CC} = +5V, I_{SOURCE} = 40μA
V_{OUTL}	J, L	+1.5V max	+1.5V max	V_{CC} = +15V, I_{SINK} = 3mA
V_{OUTH}	J, L	+13.5V min	+13.5V min	V_{CC} = +15V, I_{SOURCE} = 1mA
C_{OUT} (Floating) (SYNC, SRO, $\overline{BUSY}$, and DB0 through DB9)	J, L	5pF typ		V_{CC} = +5V to +15V SRO and SYNC; Conversion Complete $\overline{BUSY}$; BSEN = Logic "0" DB0–DB9; HBEN, LBEN = Logic "0"
I_{LKG} (Floating) (SYNC, SRO, $\overline{BUSY}$ and DB0 through DB9)		±5nA typ		V_{CC} = +5V to +15V SRO and SYNC; Conversion Complete $\overline{BUSY}$; BSEN = Logic "0" DB0–DB9; HBEN, LBEN = Logic "0" V_{OUT} = 0V and V_{CC}
DYNAMIC PERFORMANCE				
Conversion Time	J	20μs typ, 40μs max	40μs max	See Figure 5
	L	40μs typ, 120μs max	120μs max	
Internal CLK Frequency (See Figure 2, and Section 6 of Pin Function Description)	J, L	100kHz typ		V_{CC} = +5V; CLK Duty Cycle = 50%, R = 33k, C = 760pF
	J, L	100kHz typ		V_{CC} = +15V, CLK Duty Cycle = 50%, R = 10k; C = 2500pF
LBEN, HBEN Propagation Delay				V_{CC} = +5V
t_{ON}	J, L	650ns typ		LBEN, HBEN = 0V to +3V
t_{OFF}	J, L	200ns typ		Data Bit Load = 5k, 16pF Measured from 50% of Enable Input to 50% Point of Data Bit Output
BSEN Propagation Delay				V_{CC} = +5V
t_{ON}	J, L	450ns typ		BSEN = 0V to +3V
t_{OFF}	J, L	200ns typ		$\overline{BUSY}$ Load = 5k, 16pF Measured from 50% Point of BSEN Input Waveform to 50% Point of $\overline{BUSY}$ Output Waveform
Convert Start (STRT)[4] Pulse Duration Requirement	J, L	0.5μs min		

PARAMETER[1]	VERSIONS	T_A = +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
POWER SUPPLIES				
V_{DD}	J, L	+5V to +15V typ		See Figures 3 and 4
V_{CC}	J, L	+5V to V_{DD} typ		
I_{DD}	J, L	0.2mA typ, 2mA max		V_{DD} = +15V, f_{CLK} = 0 to 100kHz Continuous Conversion (80% Duty Cycle)
I_{CC}	J, L	0.02mA typ, 2mA max		V_{CC} = +5V, f_{CLK} = 0 to 100kHz Continuous Conversion (80% Duty Cycle)
	J, L	0.1mA typ, 2mA max		V_{CC} = +15V, f_{CLK} = 0 to 100kHz Continuous Conversion (80% Duty Cycle)

[1] "J" version parameters specified for $\overline{SC8}$ = 0.
[2] V_{INL} and V_{INH} specifications applicable to all digital inputs except COMP. COMP terminal must be driven with CMOS levels (i.e., comparator output pullup must be tied to V_{CC}).
[3] I_{INL}, I_{INH} specifications not applicable to CLK terminal. See "CLK input current" in specifications table.
[4] $\overline{STRT}$ falling edge should not coincide with CLK in falling edge.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND . . . . . +17V
V_{CC} to GND. . . . . +17V
V_{CC} to V_{DD} . . . . . +0.4V
V_{REF} to GND. . . . . ±25V
Analog Input to GND. . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to GND

I_{OUT1}, I_{OUT2} . . . . . ±5mA
Power Dissipation (package)
up to +50°C. 1000mW
Derate above +50°C by. . . . . 10mW/°C
Operating Temperature. . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION:

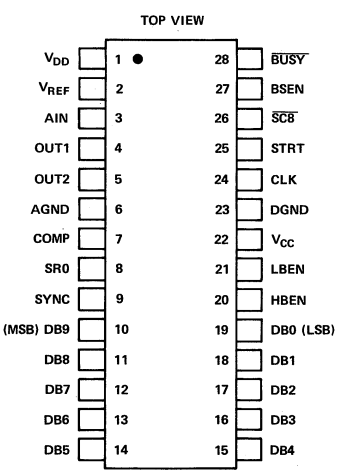
1. Do not apply voltages higher than V_{CC} or less than GND to any input/output terminal except V_{REF} or AIN.
2. The digital control inputs are zener protected; however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
3. V_{CC} should never exceed V_{DD} by more than 0.4V, especially during power ON or OFF sequencing.

ORDERING INFORMATION

Resolution	Temperature Range
	-25°C to +85°C
8-Bit	AD7570J
10-Bit	AD7570L

Suffix D: Ceramic Package

PIN CONFIGURATION



TYPICAL PERFORMANCE CHARACTERISTICS

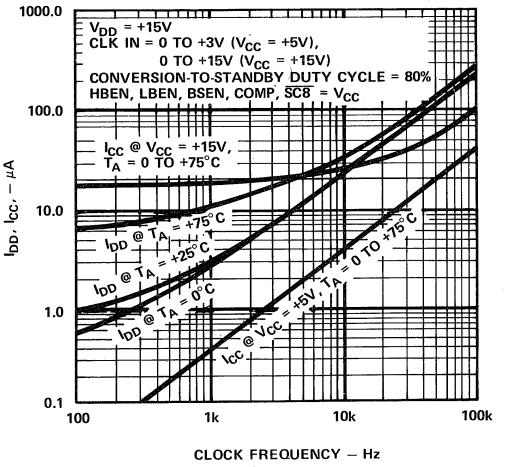


Figure 1. I_{DD}, I_{CC} vs. f_{CLK} at Different Temperatures

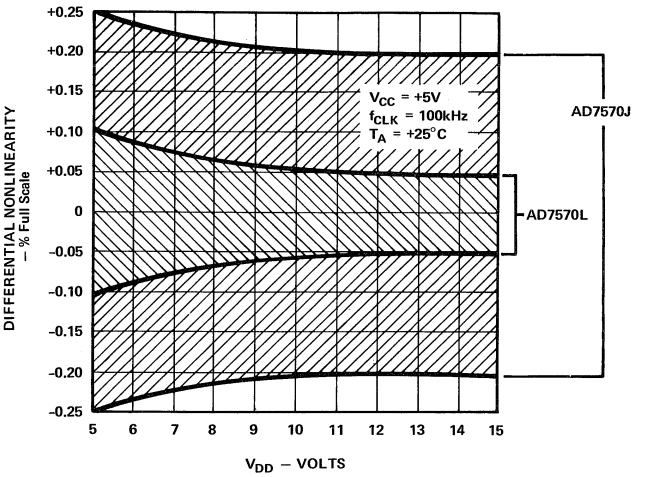


Figure 3. Differential Nonlinearity vs. V_{DD}

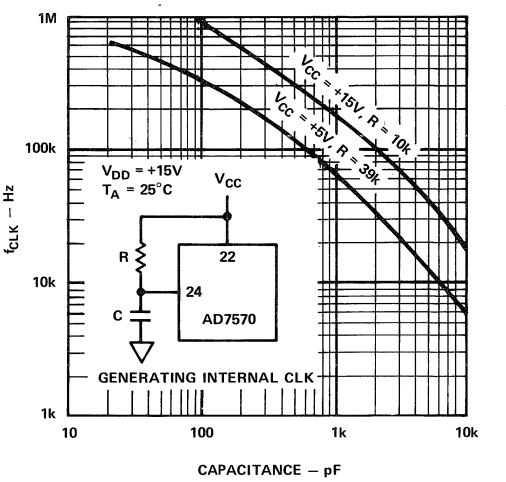


Figure 2. f_{CLK} vs. R and C at V_{CC} = +5V, +15V

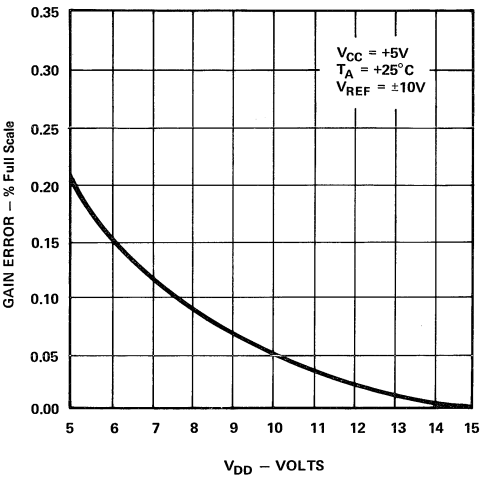


Figure 4. Gain Error vs. V_{DD} (Normalized for V_{DD} = 15V)

TEST CIRCUITS

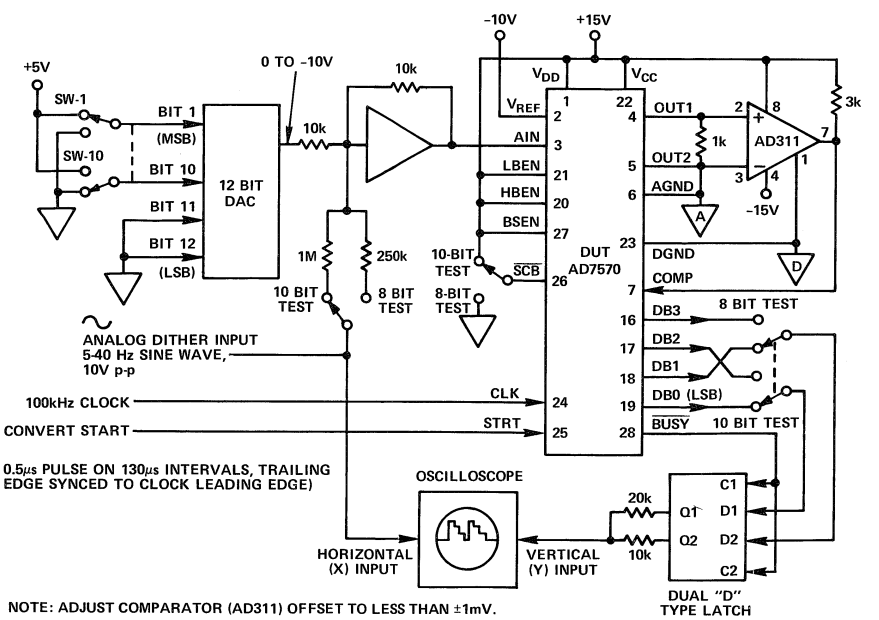
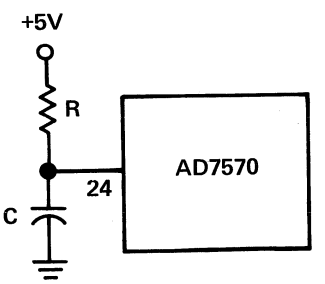


Figure 5. Dynamic Crossplot Accuracy Test

PIN FUNCTION DESCRIPTION

INPUT CONTROLS

1. Convert Start (pin 25 – STRT)
   When the start input goes to Logical "1", the MSB data latch is set to Logic "1" and all other data latches are set to Logic "0". When the start input returns low, the conversion sequence begins. The start command must remain high for at least 500 nanoseconds. If a start command is reinitiated *during* conversion, the conversion sequence starts over.
2. High Byte Enable (pin 20 – HBEN)
   This is a three-state enable for the bit 9 (MSB) and bit 8. When the control is low, the output data lines for bits 9 and 8 are floating. When the control is high, digital data from the latches appears on the data lines.
3. Low Byte Enable (pin 21 – LBEN)
   Same as High Byte Enable pin, but controls bits 0 (LSB) through 7.
4. Busy Enable (pin 27 – BSEN)
   This is an interrogation input which requests the status of the converter, i.e., conversion in process or convert complete. The converter status is addressed by applying a Logic "1" to the Busy Enable. (See Busy under Output Functions.)
5. Short Cycle 8 Bits (pin 26 – $\overline{SC8}$)
   With a Logic "0" input, the conversion stops after 8 bits reducing the conversion time by 2 clock periods. This control should be exercised for proper operation of the "J" version. When a Logic "1" is applied, a complete 10 bit conversion takes place ("L" version).
6. Clock (pin 24 – CLK)
   With an external RC connected, as shown in the figure below, clock activity begins upon receipt of a Convert-Start command to the A/D and ceases upon completion of conversion. An external clock (CMOS or TTL/DTL levels) can directly drive the clock terminals, if required. Figure 2 shows the internal CLK frequency versus R and C. If V_{CC} is <4.75V, the internal CLK will not operate.



Generating Internal Clock Frequency

7. V_{DD} (pin 1)
   V_{DD} is the positive supply for all analog circuitry plus some digital logic circuits that are not part of the TTL compatible input/output lines (back-gates to the P-channel devices). Nominal supply voltage is +15V.
8. V_{CC} (pin 22)
   V_{CC} is the logic power supply. If +5V is used, all control inputs/outputs (with the exception of comparator terminal) are DTL/TTL compatible. If +15V is applied, control inputs/outputs are CMOS compatible.

OUTPUT FUNCTIONS

1. Busy (pin 28 – $\overline{BUSY}$)
   The Busy line indicates whether conversion is complete or in process. Busy is a three-state output and floats until the Busy-Enable line is addressed with a Logic "1". When addressed, Busy will indicate either a "1" (conversion complete) or a "0" (conversion in process).
2. Serial Output (pin 8 – SRO)
   Provides output data in serial format. Data is available only during conversion. When the A/D is not converting, the Serial Output line "floats." The Serial Sync (see next function) *must* be used, along with the Serial Output terminal to avoid misinterpreting data.
3. Serial Synchronization (pin 9 – SYNC)
   Provides 10 positive edges, which are synchronized to the Serial Output pin. Serial Sync is floating if conversion is not taking place.

Note that all digital inputs/outputs are TTL/DTL compatible when V_{CC} is +5V, and CMOS compatible when V_{CC} is +15V.

PIN NO.	MNEMONIC	FUNCTION
1	V_{DD}	Positive Supply (+15V)
2	V_{REF}	Voltage **REF**erence (±10V)
3	AIN	Analog **IN**put
4	OUT1	DAC Current **OUT**put **1**
5	OUT2	DAC Current **OUT**put **2**
6	AGND	Analog Grou**ND**
7	COMP	**COMP**arator
8	SRO	**S**e**R**ial Output
9	SYNC	Serial **SYNC**hronization
10	DB9	**D**ata **B**it **9** (MSB)
11	DB8	**D**ata **B**it **8**
12	DB7	**D**ata **B**it **7**
13	DB6	**D**ata **B**it **6**
14	DB5	**D**ata **B**it **5**
15	DB4	**D**ata **B**it **4**
16	DB3	**D**ata **B**it **3**
17	DB2	**D**ata **B**it **2**
18	DB1	**D**ata **B**it **1**
19	DB0	**D**ata **B**it **0** (LSB)
20	HBEN	High Byte **EN**able
21	LBEN	Low Byte **EN**able
22	V_{CC}	Logic Supply (+5V to +15V)
23	DGND	Digital Grou**ND**
24	CLK	**CL**o**C**k
25	$\overline{STRT}$	**ST**a**RT**
26	$\overline{SC8}$	Short Cycle **8** Bits
27	$\overline{BSEN}$	**BU**S**y EN**able
28	$\overline{BUSY}$	**BUSY**

Table 1. Function Table

FUNCTIONAL ANALYSIS

BASIC DESCRIPTION

The AD7570 is a monolithic CMOS A/D converter which uses the successive approximations technique to provide up to 10 bits of digital data in a serial and parallel format. Most A/D applications require the addition of only a comparator and a voltage or current reference.

In the successive approximations technique, successive bits, starting with the most significant bit (DB9) are applied to the input of the D/A converter. The DAC output is then compared to the unknown analog input voltage (AIN) using a zero crossing detector (comparator). If the DAC output is greater than AIN, the data latch for the trial bit is reset to zero, and the next smaller data bit is tried. If the DAC output is less than AIN, the trial data bit stays in the "1" state, and the next smaller data bit is tried.

Each successive bit is tried, compared to AIN, and set or reset in this manner until the least significant bit (DB0) decision is made. At this time, the AD7570 output is a valid digital representation of the analog input, and will remain in the data latches until another convert start (STRT) is applied.

TIMING DESCRIPTION

Figure 6 is the AD7570 timing diagram, showing the successive trials and decisions for each data bit. When convert start (STRT) goes HIGH, the MSB(DB9) is set to the Logic "1" state, while DB0 through DB8 are reset to the "0" state.

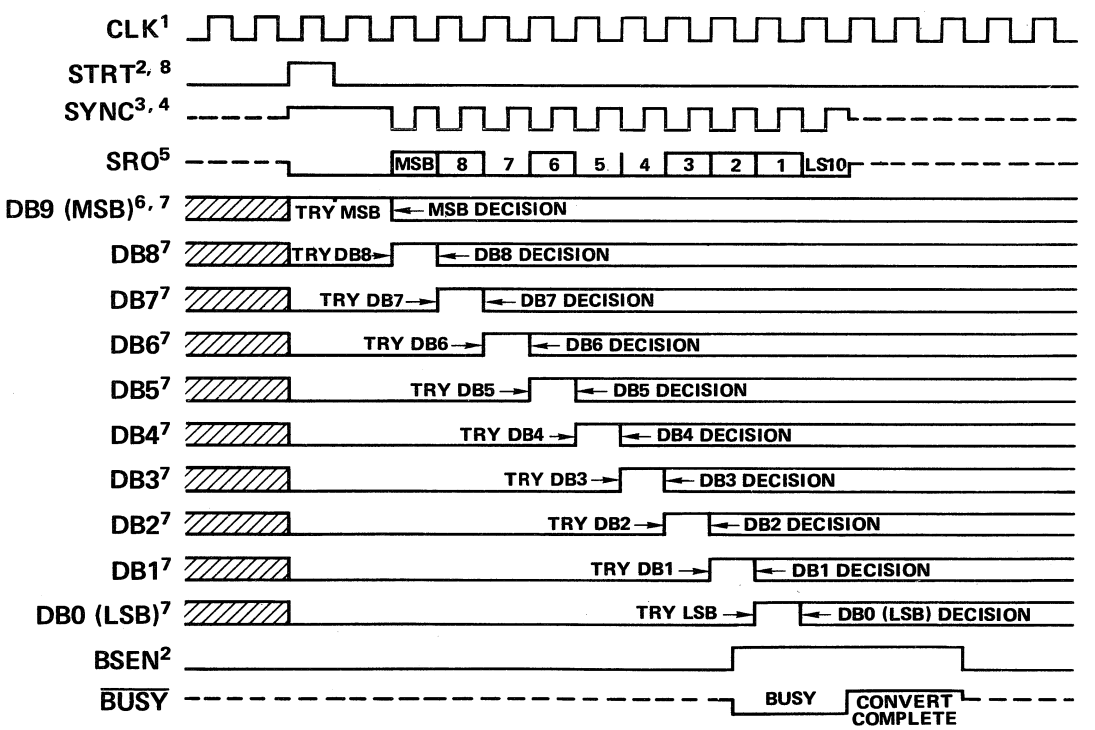
Two clock *pulses* plus 200ns after STRT returns LOW, the MSB decision is made, and DB8 is tried. Each succeeding trial and decision is made at t_{CLK} + 200ns.

Serial NRZ data is available during conversion at the SRO terminal. SYNC provides 10 positive edges which occur in the middle of each serial output bit. SYNC out must be used in conjunction with SRO to avoid misinterpretation of data. Both SYNC and SRO "float" when conversion is not taking place.

8-BIT SHORT CYCLE NOTES

If the AD7570 is short cycled to 8 bits ($\overline{SC8}$ = 0V), the following will occur:

1. The SYNC terminal will provide 8, instead of 10, positive output pulses.
2. DB1 goes "high" coincident with the LSB (DB2 is the LSB when short cycled to 8 bits) decision, and remains high until another STRT is initiated. DB0 remains in the "0" state.
3. $\overline{BUSY}$ goes "high" one clock period after the DB2 (DB2 is the LSB when short cycled) decision is made.



NOTES:
1. INTERNAL CLOCK RUNS ONLY DURING CONVERSION CYCLE (EXTERNAL CLOCK SHOWN).
2. EXTERNALLY INITIATED.
3. SERIAL SYNC LAGS $\overline{CLOCK}$ BY ≈ 200ns.
4. DOTTED LINES INDICATE "FLOATING" STATE.
5. FOR ILLUSTRATIVE PURPOSES, SERIAL OUT SHOWN AS 1101001110.
6. CROSS HATCHING INDICATES "DON'T CARE" STATE.
7. SET AND RESET OF OUTPUT DATA BITS LAGS CLOCK POSITIVE EDGE BY ≈ 200ns.
8. STRT FALLING EDGE SHOULD NOT COINCIDE WITH CLK IN FALLING EDGE.
9. SHOWN FOR $\overline{SC8}$ = 1.

Figure 6. AD7570 Conversion Timing Sequence

DYNAMIC PERFORMANCE

The upper clock frequency limitation (hence the conversion speed limitation) of the AD7570 is due to the output settling characteristics of the current weighting DAC in conjunction with the propagation delay of the comparator, not to speed limitations in the digital logic.

DAC EQUIVALENT CIRCUIT

The D/A converter section of the AD7570 is a precision 10-bit multiplying DAC. The simplified DAC circuit, shown in Figure 7, consists of ten single-pole-double-throw current steering switches and an "inverted" R-2R current weighting network. (For a complete description of the DAC, refer to the AD7520 data sheet.)

The output resistance and capacitance at OUT1 (and OUT2) are code dependent, exhibiting resistive variations from 0.5 "R" to 0.75 "R", and capacitive variations from 40pF to 120pF.

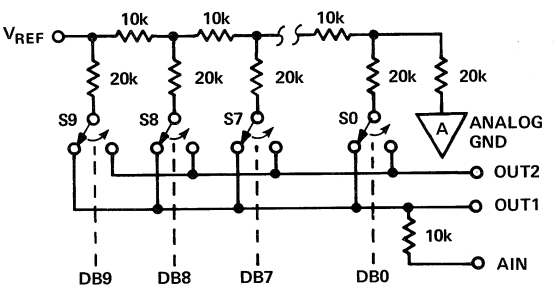


Figure 7. DAC Circuit

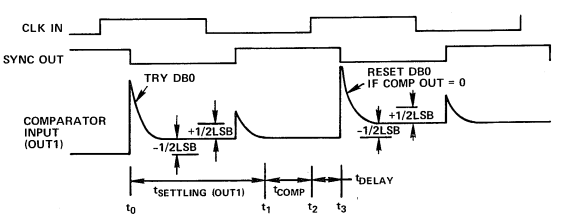
SETTLING TIME ANALYSIS

Due to the changing C_{OUT1} and R_{OUT1}, the time constant on OUT1 falls anywhere between 250 and 900ns, depending on the instantaneous state of the AD7570 digital output code.

Worst case settling requirements occur when a trial bit causes the OUT1 terminal to charge towards a final value which is precisely 1/2 LSB beyond zero crossing. When this occurs, the trial bit must settle and remain within 1/2 LSB of final value, or an incorrect decision will be made by the comparator.

For 10-bit accuracy, the first MSB must settle to within 0.1% of final value; the second MSB to within 0.2%. The LSB settling requirement is only 50% of the LSB value. Figure 8 illustrates the settling time available during a given clock period. The pulse shown on the OUT1 terminal falling mid-way between t_0 and t_3 is a feedthrough from internal clock mechanisms and is due primarily to bonding wire and header capacitance. Two methods may be used to reduce the OUT1 settling time:

1. Load OUT1 with a 1k resistor. This reduces the time constant by a factor of 10. Further reduction of the 1kΩ load reduces the amount of comparator overdrive, thus increasing the comparator propagation delay, resulting in a reduction of available settling time (t1 - t0 on Figure 8).
2. Use a zero input impedance comparator. Figure 9 illustrates a comparator circuit which has an input impedance of approximately 26Ω. Proper circuit layout will provide 10 bit accuracy for clock frequencies >500kHz.



NOTES:
1. "$t_{SETTLING}$" ($t_1 - t_0$) IS THE TIME REQUIRED FOR THE OUT1 TERMINAL TO SETTLE WITHIN ±1/2LSB OF THE FINAL VALUE.
2. "t_{COMP}" ($t_2 - t_1$) IS THE COMPARATOR SWITCHING TIME.
3. "t_{DELAY}" ($t_3 - t_2$) IS AN INTERNALLY GENERATED TIME DELAY EQUAL TO APPROXIMATELY 400 NANOSECONDS.
4. COMPARATOR OUTPUT IS LATCHES AT TIME t_2.

Figure 8. Expanded Timing Diagram

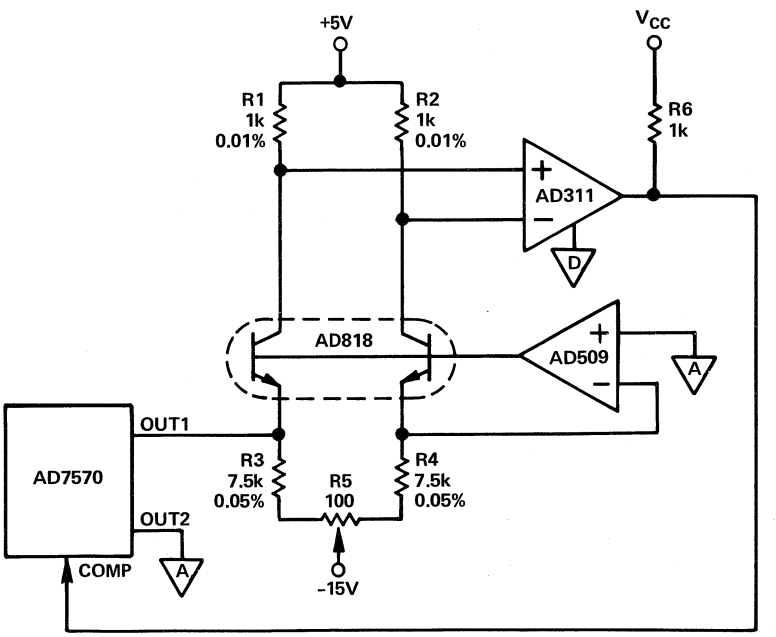


Figure 9. Current Comparator With Low Input Impedance

OPERATION GUIDELINES

UNIPOLAR BINARY OPERATION

Figure 10 shows the circuit connections required for unipolar analog inputs. If *positive* analog inputs are to be quantized, V_{REF} must be *negative*, and the OUT1 (pin 4) terminal of the AD7570 must be connected to the "+" comparator input. For *negative* analog inputs, V_{REF} must be *positive*, and the OUT1 terminal connected to the "–" input of the comparator.

For clarity, the digital control functions have been omitted from the diagram. For proper use of the digital input/output control functions, refer to the pin function description.

The input voltage/output code relationship for unipolar operation is shown in Table 2. Due to the inherent multiplying capability of the internal D/A converter, the AD7570 can accurately quantize full scale ranges of 10V to 1V. It should be noted, however, that for smaller full scale ranges, the resolution and speed limitations of the comparator impose a limitation on the maximum conversion rate.

BIPOLAR (OFFSET BINARY) OPERATION

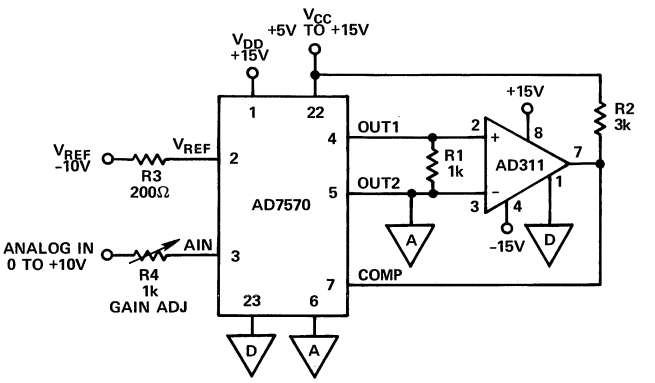
Figure 11 shows the AD7570 configured for offset binary (modified 2's complement) operation. Input voltage/output codes are shown in Table 3.

Amplifier A1, in conjunction with resistors R1, R2, and R3, offsets the bipolar analog input by full scale, and reduces its gain by a factor of 2. The analog signal applied to the AIN terminal is, therefore, a unipolar signal of 0 to +V or 0 to –V, depending on the polarity of V_{REF}.

ADJUSTMENT PROCEDURES UNIPOLAR OPERATION

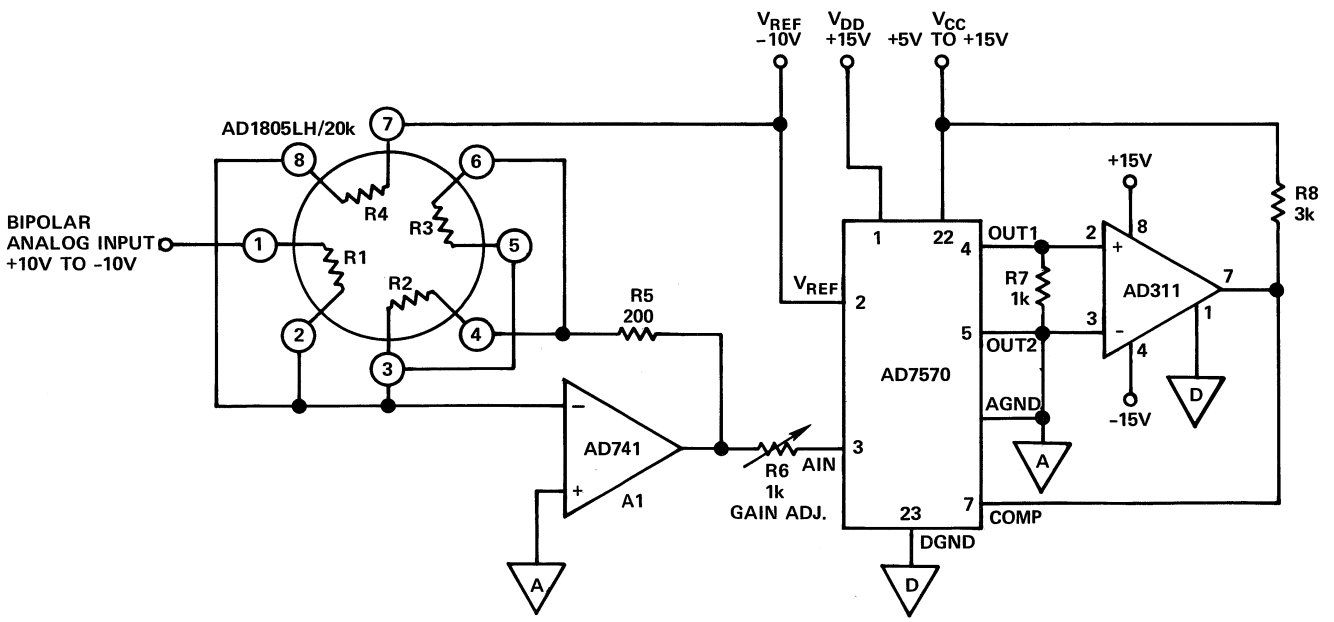
Gain Adjustment

1. Apply continuous start commands to the STRT input of the AD7570.
2. Apply full scale minus 1-1/2LSB to AIN.
3. Observe the SRO terminal as described under zero offset procedure above, and adjust the gain potentiometer (R4) until the LSB flickers between 0 and 1, and all other data bits equal "1". An alternate method is to adjust V_{REF} instead of using R4.



NOTE:
IF POSITIVE V_{REF} IS USED, THE ANALOG INPUT RANGE IS 0 TO $-V_{REF}$, AND THE COMPARATOR'S (–) INPUT SHOULD BE CONNECTED TO OUT1 (PIN 4) OF THE AD7570.

Figure 10. Unipolar Operation



NOTE: IF POSITIVE V_{REF} IS USED, CONNECT MINUS INPUT OF COMPARATOR TO OUT1 (PIN 4) OF THE AD7570.

Figure 11. Bipolar Operation

Table 2. Unipolar Operation

Analog Input (AIN) Notes 1, 2, 3	Digital Output Code MSB LSB
FS – 1LSB	1 1 1 1 1 1 1 1 1 1
FS – 2LSB	1 1 1 1 1 1 1 1 1 0
3/4 FS	1 1 0 0 0 0 0 0 0 0
1/2 FS + 1LSB	1 0 0 0 0 0 0 0 0 1
1/2 FS	1 0 0 0 0 0 0 0 0 0
1/2 FS – 1LSB	0 1 1 1 1 1 1 1 1 1
1/4 FS	0 1 0 0 0 0 0 0 0 0
1LSB	0 0 0 0 0 0 0 0 0 1
0	0 0 0 0 0 0 0 0 0 0

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full scale, i.e., ($-V_{REF}$).
3. For 8-bit operation, 1LSB equals ($-V_{REF}$) (2^{-8}); for 10-bit operation, 1LSB equals ($-V_{REF}$) (2^{-10}).

Table 3. Bipolar Operation

Analog Input (AIN) Notes 1, 2, 3	Digital Output Code MSB LSB
+(FS – 1LSB)	1 1 1 1 1 1 1 1 1 1
+(FS – 2LSB)	1 1 1 1 1 1 1 1 1 0
+(1/2 FS)	1 1 0 0 0 0 0 0 0 0
+(1LSB)	1 0 0 0 0 0 0 0 0 1
0	1 0 0 0 0 0 0 0 0 0
–(1LSB)	0 1 1 1 1 1 1 1 1 1
–(1/2 FS)	0 1 0 0 0 0 0 0 0 0
–(FS – 1LSB)	0 0 0 0 0 0 0 0 0 1
–FS	0 0 0 0 0 0 0 0 0 0

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full scale; i.e., (V_{REF}).
3. For 8-bit operation, 1LSB equals ($-V_{REF}$) (2^{-7}); for 10-bit operation, 1LSB equals ($-V_{REF}$) (2^{-9}).

ADJUSTMENT PROCEDURES BIPOLAR OPERATION

Gain Adjustment

1. Apply continuous start commands to the STRT input of the AD7570.
2. Apply 1-1/2LSB less than positive full scale (FS = V_{REF}) to the bipolar analog input of Figure 11.
3. Trim the gain potentiometer R6 for a flickering LSB, and all other data bits equal to Logic "1." Observe the SRO terminal, as described in zero offset procedure above.

APPLICATION HINTS

1. Unused CMOS digital inputs should be tied to their appropriate logic level and not left floating. Open digital inputs may cause undesired digital activity in the presence of noise.
2. Analog and digital grounds should have separate returns.
3. Load the OUT1 terminal with a 1k resistor to reduce the time constant when operating at clock frequencies >50kHz.
4. For 10 bit operation, the comparator offset should be adjusted to less than 1mV. Each millivolt of comparator offset will cause approximately 0.015% of differential nonlinearity when a 10V reference is used.
5. The comparator input and output should be isolated to prevent oscillations due to stray capacitance (see layout on next page).
6. If an external clock is used, the negative transition of STRT should not coincide with the trailing edge of the clock input.

OPERATING PRECAUTIONS

1. Do not allow V_{CC} to exceed V_{DD}. In cases where V_{CC} could exceed V_{DD}, the diode protection scheme in Figure 12 is recommended.
2. Do not apply voltages greater than V_{CC} or lower than ground to any digital *output* from sources which can supply >20mA.
3. Do not apply voltages (from a source which can supply more than 5mA) lower than ground to the OUT1 or OUT2 terminal (see Figure 12).

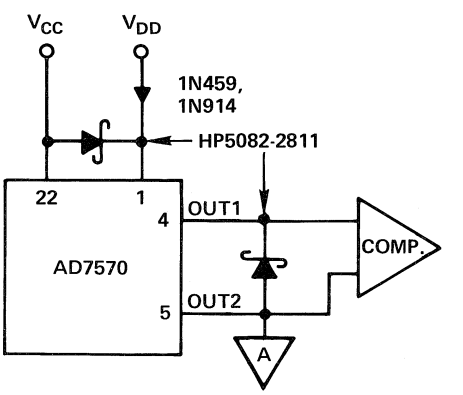
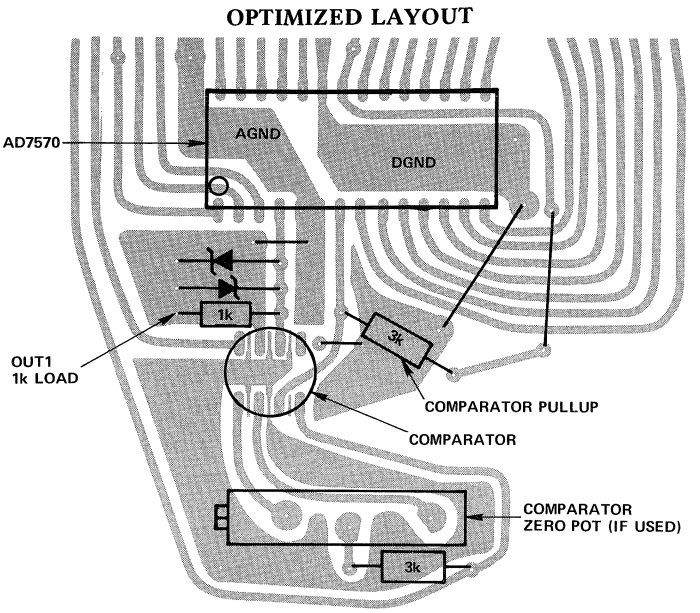


Figure 12. Diode Protection Scheme



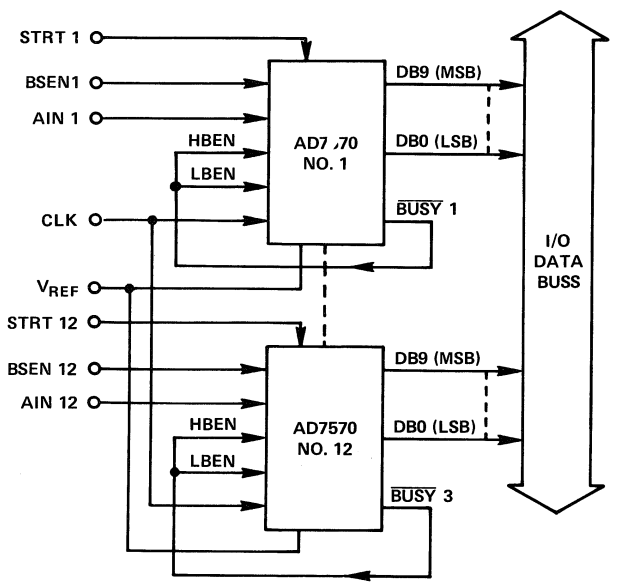
NOTES:
1. ALL PC TRACES ON BOTTOM OF BOARD.
2. LAYOUT SHOWN TERMINATES OUT1 INTO + INPUT OF AD311 TYPE COMPARATOR. (V_{REF} = -10V, AIN = 0 TO +10V).

Figure 13. PC Layout (Top View)

BUSING MULTIPLE AD7570 OUTPUTS

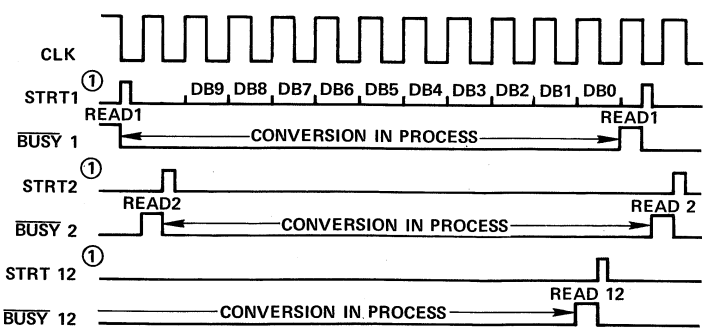
Several AD7570's may be paralleled to a data bus to provide an A/D converter per analog channel, this providing increased system throughput rate. For example, Figure 14 shows such a system for 12 AD7570's in parallel.

The three-state output logic enables of each AD7570 is controlled by its own BUSY (status) outputs. Thus, data is available at the A/D output only after conversion is complete, and until another "convert start" is initiated. The timing diagram of Figure 15 illustrates how the STRT signals of the twelve AD7570's might be staggered to provide a total system throughput twelve times as great as the classic method of data acquisition (an analog multiplexer feeding multichannel analog data to a single A/D converter).



NOTE: BSEN ON EACH AD7570 IS "ENABLED" (LOGIC 1).

Figure 14. Busing Multiple AD7570's



NOTE: STRT SIGNAL 0.5μs PULSE WIDTH, LEADING EDGE SYNCHRONIZED TO CLK TRAILING EDGE.

Figure 15. Timing Diagram

MICROPROCESSOR INTERFACE

Since most 8-bit microprocessors utilize a bidirectional data bus, each input peripheral (such as the AD7570) must be capable of isolating itself from the data bus when other I/O devices, memory, or the CPU takes control of the bus. The AD7570 output data and status (BUSY) lines all utilize three-state logic to provide this requirement.

Figure 16 illustrates a method of interfacing a TTY keyboard and printer to the AD7570, using an 8080 microprocessor as the interface controller.

The program (stored in Read Only Memory) waits for a keystroke on the TTY keyboard. When a keystroke is detected, an A/D conversion is started. When conversion is complete, the 8080 reads in the binary data from the AD7570, converts it to ASCII, and prints out the decimal number (preceded by a carriage return and line feed) on the teletype printer.

More specifically, the main sequence of events would be as follows:

1. When a TTY keystroke is detected by the CPU (via the UAR/T Receiver), a "convert start" (STRT) is applied to the AD7570.
2. BSEN is enabled, placing $\overline{\text{BUSY}}$ (conversion status) on the data bus. When the 8080 detects $\overline{\text{BUSY}}$ = 1, conversion is complete, and BSEN is disabled, causing $\overline{\text{BUSY}}$ to return to its floating state.
3. LBEN is enabled, and the eight least significant data bits (DB0-DB7) are applied to the data bus for subsequent transfer to the 8080. When the data transfer is complete, LBEN is disabled, and DB0-DB7 return to their floating state.
4. HBEN is enabled, and the two most significant AD7570 data bits (DB8 and DB9) are applied to the data bus for subsequent transfer to the 8080. When the data transfer is complete, HBEN is disabled, and DB8 and DB9 return to their floating state.
5. The 8080 (in conjunction with the programmed Read Only Memory) performs a binary to decimal conversion.
6. $\overline{\text{SWE}}$ (Status Word Enable) on the UAR/T transmitter is enabled, applying XBMT (Transmitter Buffer Empty) to the data bus. When a Logic "1" is detected by the 8080, $\overline{\text{SWE}}$ is disabled, and XBMT returns to a floating state.
7. TDS (Transmitter Data Strobe) strobes the converted decimal number into the UAR/T transmitter for subsequent serial clocking into the keyboard.

The interface scheme shown below is only one example of a myriad of possible data acquisition/control systems which could conveniently use the AD7570 to provide digital data to a microprocessor or minicomputer bus.

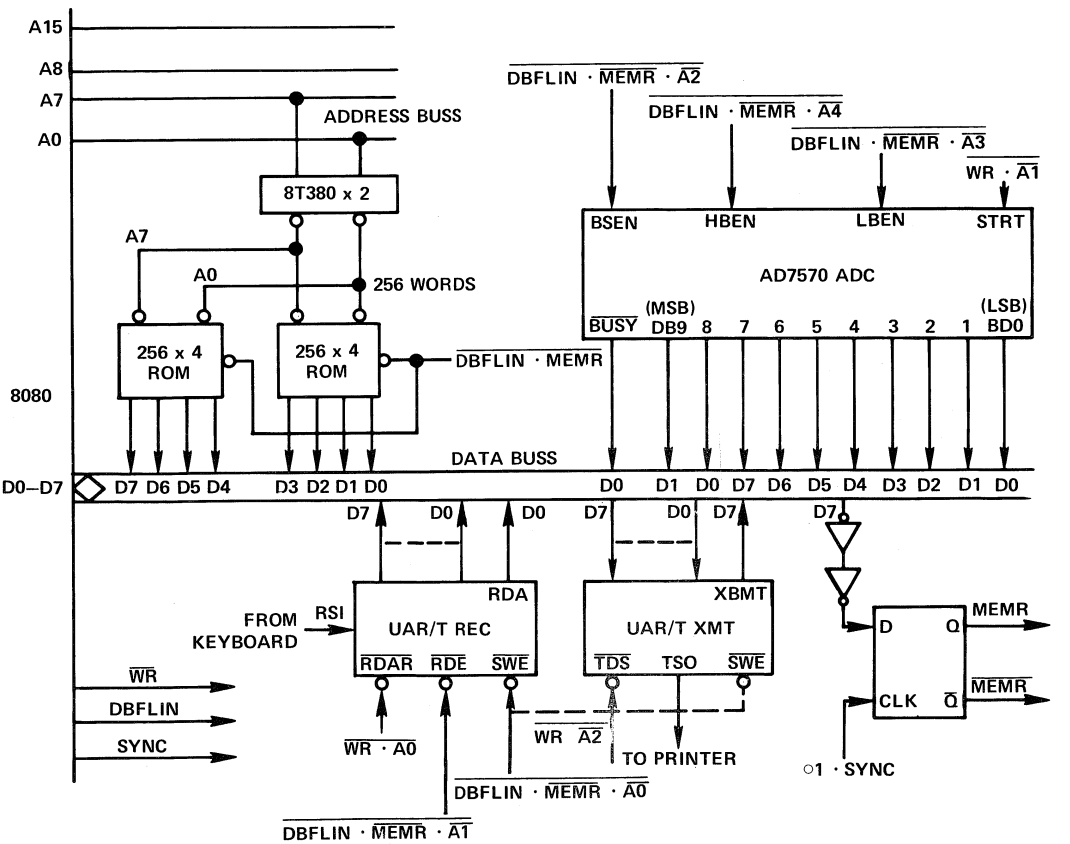


Figure 16. Microprocessor Controlled TTY/ADC Interface

TERMINOLOGY

Resolution
Resolution is the relative value of the LSB, or 2^{-n} for binary devices, for n-bit converters. It may be expressed as 1 part in 2^n, as a percentage, in parts-per-million, or simply by "n bits."

Quantizing Uncertainty (or "Error")
The analog continuum is partitioned into 2^n discrete ranges for n-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is, therefore, an inherent quantization uncertainty of ±1/2LSB, associated with the *resolution,* in addition to the actual conversion errors. This uncertainty is a property of the *system* resolution.

Relative Accuracy
Relative accuracy error is the difference between the nominal and actual ratios to full scale of the analog value corresponding to a given digital input, independently of the full-scale calibration. This error is a function of the linearity of the converter, and is usually specified at less than ±1/2LSB.

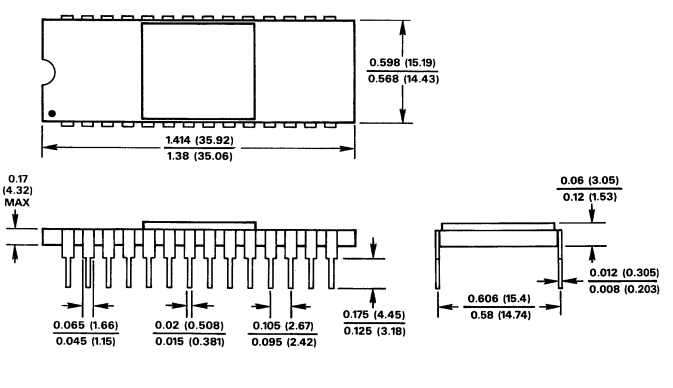
Gain Error
The "gain" of a converter is that analog scale factor setting that establishes the nominal conversion relationship, e.g., 10V full scale. It is adjusted either by setting the feedback resistor of a DAC, the input resistor in a current-comparing ADC, or the reference (voltage or current).

Differential Nonlinearity
In a converter, differential linearity error describes the variation in the analog value of transitions between adjacent pairs of digital numbers, over the full range of the digital input or output. If each transition is equal to its neighbors (i.e., 1LSB), the *differential nonlinearity* is zero. If a transition differs from one of its neighbors by more than 1LSB (e.g., if, at the transition 011. .11 to 100. . .00, the MSB is low by 1.1LSB), a D/A converter can be *non-monotonic,* or an A/D converter using it may miss one or more codes. A specified maximum differential nonlinearity of 1LSB ensures that monotonic behavior exists.

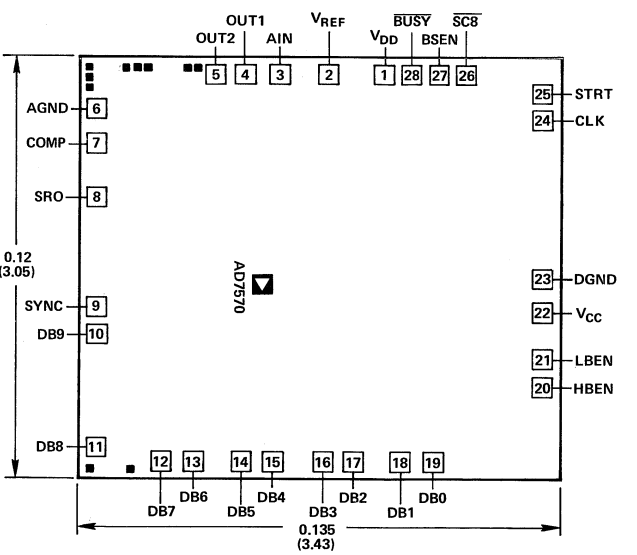
Output Leakage Current
Current which appears at the OUT1 terminal when all digital output (DB0 through DB9) are LOW, or on the OUT2 terminal when all digital outputs are HIGH. The effect of output leakage current will be on the offset of the A/D converter.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



28 Pin Ceramic Dip



Bonding Diagram

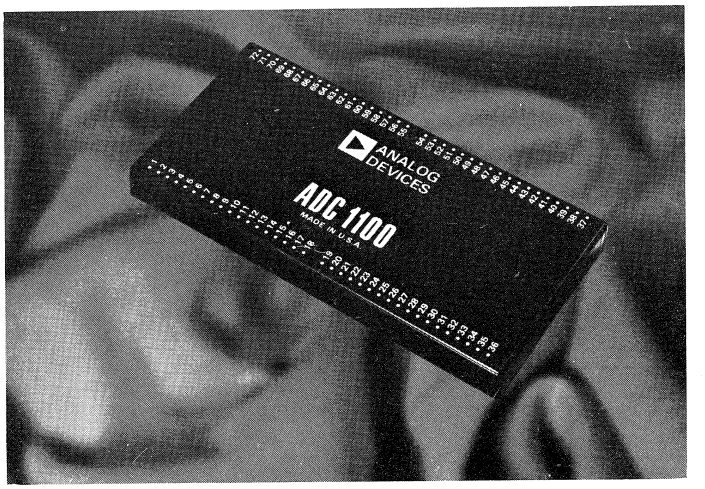
ANALOG DEVICES

Low Cost Dual Slope A/D Converter

ADC1100

FEATURES

- 3½ BCD Digits or 11 Bits Plus Sign
- Accepts Bipolar or Unipolar Input Signals
- Requires Only +5V Power
- 40dB Normal Mode Noise Rejection
- Analog Input Overvoltage Protected
- Automatic Zero Correction
- Can Drive Display and/or Feed Computer
- User Choice of Three Triggering Methods
- Capable of Ratiometric Operation



GENERAL DESCRIPTION

The ADC1100 is a dual slope integrating analog-to-digital converter with 3½ BCD digit or 11 binary bit resolution. It accepts an analog input signal within the nominal range of ±200mV, and converts the average value during the input integration time period to parallel output sign-magnitude BCD or sign-magnitude binary data. The unit is packaged in a small 2″ x 4″ x 0.4″ module, and requires only +5V power.

EXCELLENT NOISE REJECTION

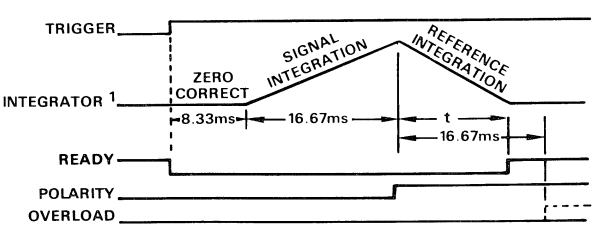
Because the ADC1100's output is based on the average value of the input signal during the input integration time period, inaccuracies due to noise spikes are greatly suppressed. In addition, with the input integration time period set equal to one cycle of the power line, the integral of any power line noise is equal to zero. This results in a normal mode power line noise rejection ratio of at least 40dB. By locking the input integration time precisely to one period of the power line using an external phase locked loop, this ratio can be increased to over 80dB. Since the excellent noise rejection is achieved without any input filtering, the analog input settling time required prior to the commencement of a conversion is zero.

APPLICATIONS

With the only power required being +5V, and with its excellent noise rejection, the ADC1100 is an ideal choice for installation at transducer locations. The BCD coded version is also well suited for many behind-the-panel applications because it allows the instrument designer complete freedom in choosing a display. For example, it may be desirable to share a single display with more than one digital output device, or to display a digital output scaled quite differently from the ADC1100/BCD's ±199.9mV input range.

TIMING INFORMATION

As shown in Figure 1, each conversion begins with an automatic zero correction cycle. Polarity data is valid anytime after the completion of the input signal integration time period, and it remains latched in one polarity until such time as a conversion is performed with an input signal of the opposite polarity. The digital output data is valid no later than 50ns prior to the READY output's "0" to "1" transition. This "set up" time is sufficient to allow the output data to be strobed into a following register or latch on the READY output's "0" to "1" edge. In the event of an overrange input signal, the OVERLOAD output will go from "0" to "1" at the end of the conversion. It will remain latched in the "1" state until a normal conversion has been performed.



[1] Reference integration time $t \cong \frac{E_{IN}}{200mV} \times 16.67ms$. In the event of an overloaded input, t_{max} = 50ms. (The times shown are those obtained when the unit is set for 60Hz noise rejection.)

Figure 1. Timing Diagram

SPECIFICATIONS (typical @ +25°C and +5.0V dc unless otherwise noted)

MODEL	ADC1100/BCD	ADC1100/BIN
RESOLUTION	3½ BCD digits plus sign	11 Bits Plus Sign
ACCURACY		
Relative to Full Scale	±0.05%	*
Absolute	±0.1%	*
TEMPERATURE COEFFICIENTS		
Gain TC	±50ppm/°C max	*
Offset TC	±2ppm/°C max	*
INPUT CHARACTERISTICS		
Input Range	±199.9mV	±204.7mV
Input Resolution	0.1mV/LSB	*
Input Impedance	10^8 ohms min	*
Input Bias Current	1.5nA max	*
Overvoltage Protection	±20V[1]	*
Normal Mode Rejection	40dB min @ 60Hz[2]	*
CONVERSION TIME		
Normal Conversion	42ms max[3]	*
Overload Conversion	70ms max	*
CONVERSION RATE		
Internal Trigger	4/sec	*
External Trigger	0 to 20/sec	*
Automatic	20 to 40/sec	*
DIGITAL OUTPUTS[4]		
Data Output	Positive True Logic	*
Polarity	Logic "0" = Positive Signal	*
	Logic "1" = Negative Signal	*
Ready	Logic "0" = Busy	*
	Logic "1" = Ready	*
Overload	Logic "0" = Normal	*
	Logic "1" = Overload	*
LOGIC INPUTS[5]		
Trigger Input	2 TTL Unit Loads	*
Hold Input	2 TTL Unit Loads	*
POWER SUPPLY REQUIREMENTS	+5.00V dc ±5% @ 200mA typ, 250mA max	*
POWER SUPPLY SENSITIVITY	0.01%/%ΔV_S	*
TEMPERATURE RANGE		
Operating	0 to +70°C	*
Storage	-25°C to +85°C	*

[1] Maximum voltage that can be applied to the input continuously without risking damage to the unit. Up to ±50V can be applied momentarily.

[2] Normal mode rejection at 50Hz is also 40dB minimum when unit is calibrated for 50Hz normal mode noise rejection.

[3] A normal conversion will take 42ms max when the unit is calibrated for 60Hz noise rejection. When set for 50Hz noise rejection, a normal conversion will take 50ms max.

[4] All digital outputs are rated at 6 TTL unit loads each, with a Logic "1" ≥ +2.4V @ 240μA max, and a Logic "0" ≤ +0.4V @ -9.6mA max.

[5] The trigger and hold inputs are internally tied to pull-up resistors. It is thus assured that these inputs are maintained in the high state with no connections to them. For both inputs, a Logic "1" ≥ +2.0V, and a Logic "0" ≤ +0.8V @ -3.2mA max.

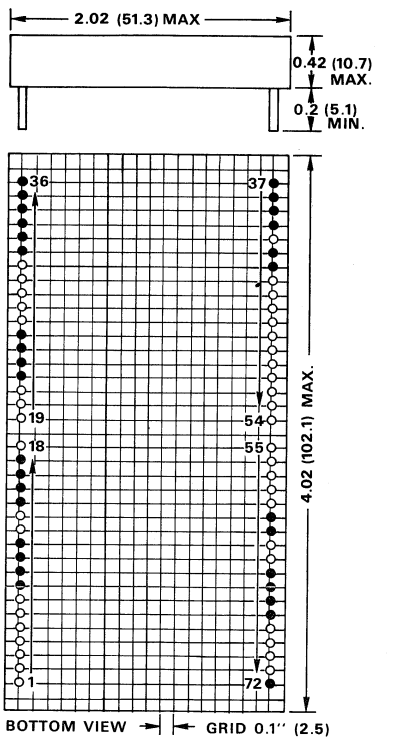
Specifications subject to change without notice.

DATA OUTPUT PIN DESIGNATIONS

PIN	14	15	16	17	22	23	24	25	31	32	33	34	35
ADC1100/BCD	1	2	4	8	10	20	40	80	100	200	400	800	1000
ADC1100/BIN	LSB	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	—	—	MSB

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

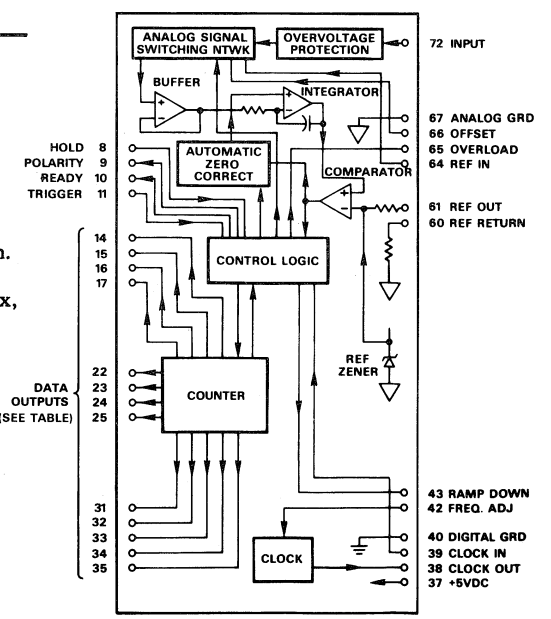
Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations. Pins 33 and 34 installed in ADC1100/BCD only. All pins are gold plated half-hard brass, (MIL-G-45 204), 0.019 (0.48) dia 0.2 (5.1) min. length.

For plug-in mounting card order Board No. AC1550

BLOCK DIAGRAM AND PIN DESIGNATIONS



CLOCK CONNECTIONS

The ADC1100 is normally connected to its own internal clock. This is accomplished by jumpering CLOCK OUT (pin 38) to CLOCK IN (pin 39). The internal clock is factory set to operate at a nominal frequency of 120kHz, which results in an input signal integration time period of 16 2/3ms. Since 16 2/3ms is equal to one cycle of a 60Hz power line, any 60Hz noise appearing on the input will have an integral of zero, and thus will not affect the digital output.

Under certain circumstances, it may be desirable to be able to adjust the internal clock's frequency. Figure 2 shows how this may be accomplished with suitable connections to pin 42 (which otherwise would have nothing connected to it).

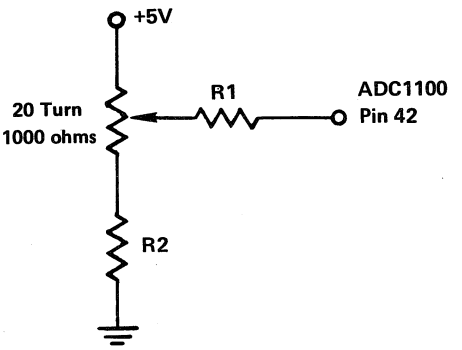


Figure 2. Clock Frequency Adjustment

With R1 = 2200 ohms and R2 = 470 ohms, this circuit can be used to optimize the rejection of 60Hz normal mode noise. The potentiometer is used to adjust the input integration time period to be exactly equal to one cycle of a power line that has a nominal frequency of 60Hz. With R1 = 470 ohms and R2 = 2700 ohms, the clock will operate at a nominal frequency of 100kHz. This gives an input integration time of 20ms, which is equal to one cycle of a 50Hz power line. The potentiometer is then used to optimize the rejection of 50Hz noise.

GAIN ADJUSTMENT

The gain of the ADC1100 is set with a 50 ohm, 20 turn potentiometer whose wiper is connected to pin 64. One end of the potentiometer is connected to pin 60, and the other end to pin 61. BCD coded units are calibrated by applying an input signal of 199.85mV and then adjusting the gain adjustment potentiometer until the converter's output is just on the verge of switching between output codes 1998 and 1999. Binary coded units are calibrated by applying a 204.65mV input and adjusting the gain potentiometer until the converter's output is just on the verge of switching from 11111111110 to 11111111111. If exact gain calibration is not required, the gain adjustment potentiometer can be deleted, and pins 60, 61, and 64 are then jumpered together.

OFFSET ADJUSTMENT

The ADC1100 goes into an automatic zero correction cycle at the beginning of each conversion. It does not, therefore, require any external zero or offset adjustment. However, in the event the input signal contains an externally generated offset of up to ±1mV, it could be cancelled out with the circuit shown in Figure 3 (pin 66 normally has nothing connected to it).

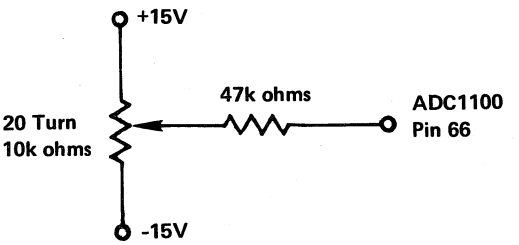


Figure 3. Offset Adjustment

TRIGGERING CONVERSIONS

The ADC1100 may be triggered in any of three ways. The first is the easiest to implement. With no connections to TRIGGER (pin 11) or HOLD (pin 8), the unit will continuously perform conversions at the rate of about 4 conversions/second. With no connections to TRIGGER (pin 11), and with HOLD (pin 8) jumpered to READY (pin 10), the ADC1100 will perform continuous conversions, with a new conversion beginning as soon as the conversion in progress is completed. The READY output (pin 10) remains at a Logical "1" for approximately 100ns between conversions. The conversion rate depends upon the magnitude of the input signal. With the clock operating at 120kHz (for optimum rejection of 60Hz noise), and with a nonoverloaded input, that rate will vary from about 23/sec. to about 40/sec.

Finally, the ADC1100 can be commanded to make a conversion upon receipt of an externally generated pulse. Figure 4A shows how the unit is triggered with a positive-going pulse, and Figure 4B describes triggering with a negative-going pulse.

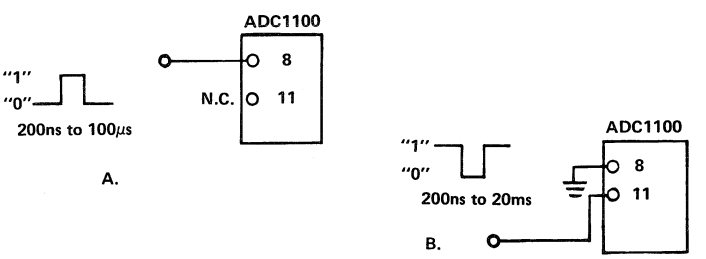


Figure 4. External Triggering

When using a positive-going trigger pulse the conversion commences (and the READY output goes from "1" to "0") approximately 100ns after the leading edge ("0" to "1" transition) of the trigger pulse. When using a negative-going pulse, the conversion begins about 100ns following the pulse's trailing edge ("0" to "1" transition). Should a trigger pulse be received while a conversion is in progress, it will be ignored, and the conversion in progress will continue to completion.

POWER AND GROUND CONNECTIONS

Digital ground (pin 40) and analog ground (pin 67) should be tied together externally with a good ground bus connection. Care should be taken to ensure that no digital ground return signals are carried in the analog input's ground return lead. The +5V power input is internally bypassed with a 10μF capacitor, but additional bypass capacitance can be added externally if desired. Analog Devices' model 906 modular power supply is an ideal power source for the ADC1100. It supplies +5V at up to 250mA.

LATCHED DATA OUTPUTS

When the digital outputs of the ADC1100/BCD are used to drive a display, it may be desirable to have the data latched to keep the display from blinking. This can be easily accomplished using only two external digital ICs, as shown in Figure 5. Note that no latching circuitry is shown for the overload, sign, and "1000" outputs. None is required. These outputs are latched, and, therefore, do not require external latching. The latched data is updated on the "0" to "1" transition of the READY output (pin 10), which occurs at the completion of each conversion.

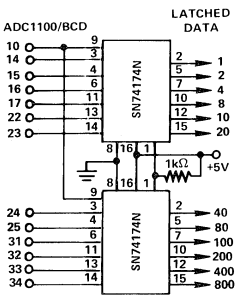


Figure 5. External Data Latches

MAXIMUM POWER LINE NOISE REJECTION

When maximum rejection of power line originated noise is needed, the circuitry shown in Figure 6 may be used to give the ADC1100 a power line noise rejection ratio of over 80dB. This circuit is a phase locked loop that locks the input signal integration time period to be exactly equal to one cycle of the line voltage applied to the primary of the 115V ac to 6.3V ac transformer.

It can be used with either 50Hz or 60Hz power lines. Because of the long time constant in the phase locked loop, it may take as long as three minutes for the loop to lock onto the power line frequency following initial power turn-on.

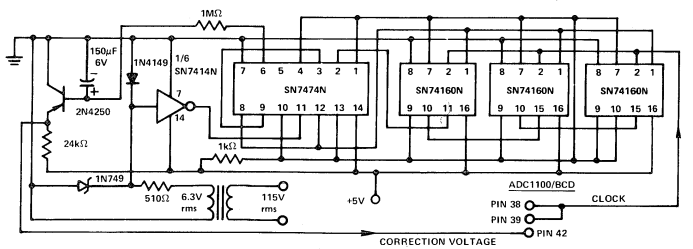


Figure 6a. Phase Locked Clock Circuitry For ADC1100/BCD

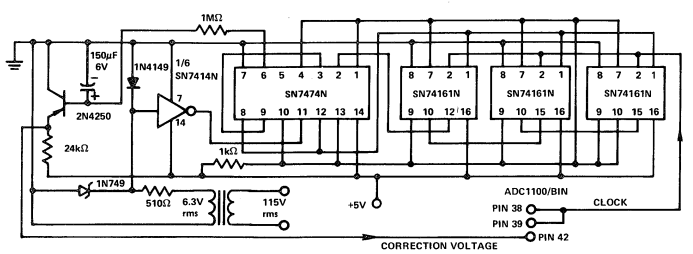


Figure 6b. Phase Locked Clock Circuitry For ADC1100/BIN

USING EXTERNAL COUNTERS

The ADC1100 can be used to produce an output pulse train, the number of pulses in which is proportional to the analog input voltage. This pulse train output can be applied to external counters to implement nearly any counting scheme desired. For example, Figure 7 shows a circuit using the ADC1100/BCD which gives a full scale count of 9995, where the least significant digit has only two possible values, 0 or 5. The counter would count in the following sequence: 1890, 1895, 1900, 1905, etc.

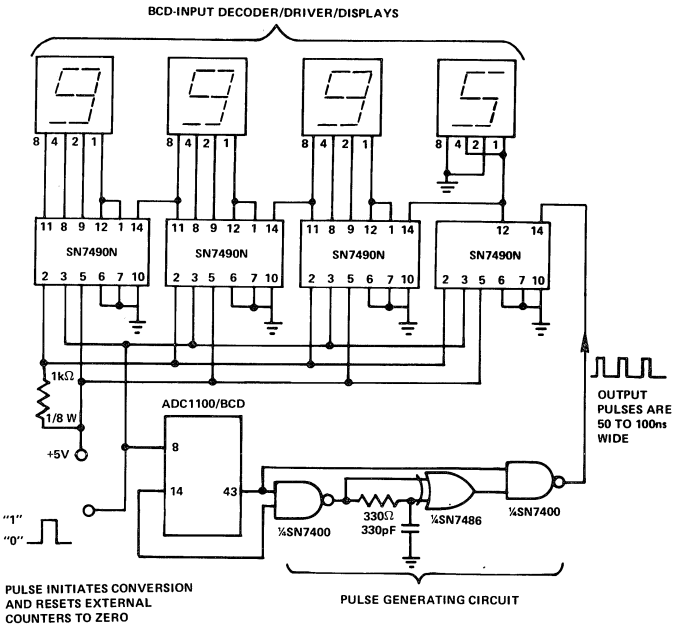


Figure 7. External Count-by-5 Counter

When designing external counter systems, it is only necessary to remember that BCD coded units produce exactly 1999 pulses and binary coded units produce exactly 2047 pulses for plus or minus full scale inputs. Smaller inputs yield proportionately smaller numbers of pulses. The "Pulse Generating Circuit" of Figure 7 can be used with either binary or BCD coded units.

RATIOMETRIC OPERATION

There may be instances where it would be desirable to measure the ratio of two voltages, rather than the specific value of one voltage. For example, the ratio of a strain gauge load cell's output to its excitation voltage may be highly accurate and repeatable, but the excitation voltage itself may vary somewhat. If the excitation voltage is applied to the reference input (pin 64) and the cell's output is applied to the analog input (pin 72), then the ADC1100's digital output will be the ratio of the two: digital output = V_{IN}/V_{REF} x (Full Scale Digital Output). Thus, variations in the excitation voltage will not affect the digital output. The voltage source driving the reference input should have a source impedance of 1000ohms or less. For best operation, the reference input voltage should be kept within the range of +100mV to +300mV, but in any case cannot exceed ±1V without risking damage to the unit. Care should be taken to ensure that the reference voltage is accurately referred to analog ground (pin 67). The ADC1100 will exhibit a gain TC of ±15ppm/°C or better in this mode of operation.

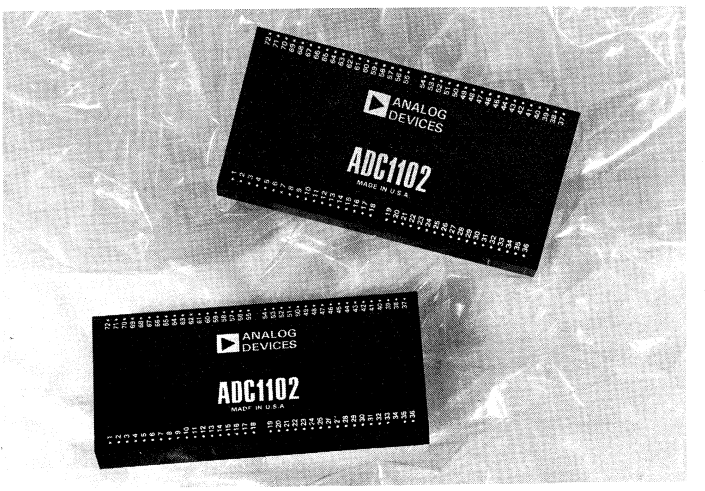
ANALOG DEVICES

High Speed Analog to Digital Converter

ADC1102

FEATURES

- 12-Bit Resolution and Accuracy
- Fast 8μs Conversion Time
- Low 10ppm/°C Maximum Gain TC
- User Choice of Input Range
- No Missing Codes 0 to +70°C
- Short Cycle Capability
- Small Module Size



GENERAL DESCRIPTION

The ADC1102 is a high speed analog-to-digital converter, packaged in a small 2" x 4" x 0.4" (51 x 102 x 10mm) module, which performs complete 12-bit conversions in less than 8μs. Using the successive approximations technique, it converts analog input voltages into natural binary, offset binary, or two's complement coded outputs. Data outputs are provided in both parallel and non-return-to-zero serial form.

Four analog input ranges are available: 0 to +20V, 0 to +10V, ±10V, ±5V. The user selects the desired range by making various connections to the module terminals. The ADC1102 can also be connected so as to perform conversions of less than 12-bit resolution with a proportionate decrease in conversion time.

Performance specifications include ±½LSB maximum error relative to full scale, ±10ppm/°C maximum gain temperature coefficient, and ±3ppm/°C differential nonlinearity temperature coefficient. The ADC1102 has no missing codes from 0 to +70°C.

TIMING

As shown in Figure 1, the leading edge of the convert command sets the MSB output to logic "0" and the CLOCK OUT, STATUS, $\overline{\text{MSB}}$, and BIT 2 through BIT 12 outputs to Logic "1". Nothing further happens until the convert command returns to Logic "0", at which time the clock starts to run and the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-to-analog converter's output is compared with the analog input.

If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB to Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic "0" and another comparison is made. This process continues through each successive bit until the BIT 12 (LSB) comparison is completed. At this point the STATUS and CLOCK OUT return to Logic "0" and the conversion cycle ends.

The serial data output is of the non-return-to-zero (NRZ) format. The data is available, MSB first, 20ns after each of the twelve "0" to "1" clock transitions.

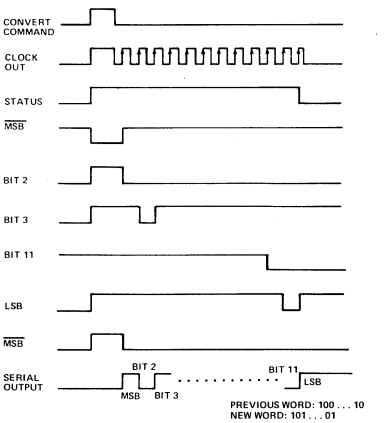
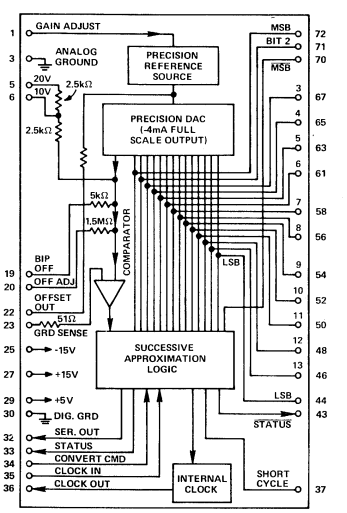


Figure 1. Timing Diagram



Block Diagram and Pin Designations

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

MODEL	ADC1102
RESOLUTION	12 Bits
CONVERSION TIME	8μs (max)
ACCURACY	
Error Relative to Full Scale	±½LSB (max)
Quantization Error	±½LSB (max)
Differential Nonlinearity Error	±½LSB (max)
Missing Codes	No Missing Codes from 0 to +70°C
TEMPERATURE COEFFICIENTS	
Gain	±7ppm/°C (±10ppm/°C max)
Unipolar Offset	±0.7ppm/°C (±3ppm/°C max)
Bipolar Offset	±3ppm/°C (±7ppm/°C max)
Differential Nonlinearity	±3ppm/°C (±8ppm/°C max)
INPUT VOLTAGE RANGES	±5V, ±10V, +10V, +20V
INPUT IMPEDANCE (10V RANGE)	2500Ω
CONVERT COMMAND	Positive Pulse, 100ns min Width, Leading Edge Resets, Trailing Edge Starts, TTL/DTL Compatible
PARALLEL DATA OUTPUT	
Unipolar	Positive True Binary
Bipolar	Positive True Offset Binary, Two's Complement
SERIAL DATA OUTPUT	
Unipolar	Positive True Binary
Bipolar	Positive True Offset Binary
STATUS OUTPUT	"1" During Conversion. Complement also available. TTL/DTL Compatible.
LOGIC FANOUTS AND LOADINGS	
Convert Command Input	1TTL Unit Load
Clock Input	3TTL Unit Loads
Short Cycle Input	1TTL Unit Load
Parallel Data Outputs	3TTL Unit Loads/Bit
Serial Data Output	8TTL Unit Loads
STATUS Output	2TTL Unit Loads
STATUS Output	12TTL Unit Loads
Clock Output	4TTL Unit Loads
ADJUSTMENT RANGES	
Gain	±12LSB
Offset	±10LSB
POWER REQUIREMENTS	+15V ±10% @ 40mA -15V ±10% @ 60mA +5V ±5% @ 250mA
POWER SUPPLY SENSITIVITY	
To ±15V Tracking Supplies	
Gain	±4.5ppm/%ΔV_S
Offset	±4.5ppm/%ΔV_S
To ±15V Non-Tracking Supplies	
Gain	±10ppm/%ΔV_S
Offset	±7ppm/%ΔV_S
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C

Specifications subject to change without notice.

PARALLEL DATA OUTPUT CODING

ANALOG INPUT		DIGITAL OUTPUT
0 to +10V Range	0 to +20V Range	Binary Code
+9.9976V	+19.9951V	111111111111
+5.0000V	+10.0000V	100000000000
+1.2500V	+2.5000V	001000000000
+0.0024V	+0.0048V	000000000001
+0.0000V	+0.0000V	000000000000

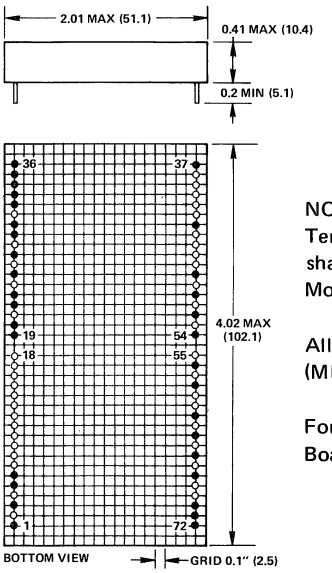
Table 1. Nominal Unipolar Input-Output Relationships

ANALOG INPUT		DIGITAL OUTPUT	
±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.9976V	+9.9951V	111111111111	011111111111
+2.5000V	+5.0000V	110000000000	010000000000
+0.0024V	+0.0048V	100000000001	000000000001
0.0000V	0.0000V	100000000000	000000000000
-5.0000V	-10.0000V	000000000000	100000000000

Table 2. Nominal Bipolar Input-Output Relationships

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

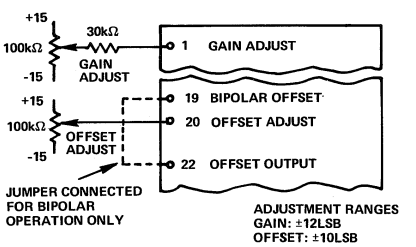


NOTE:
Terminal pins installed only in shaded hole locations.
Module weight: 3.5 ounces (99.3 grams).
All pins are gold plated half-hard brass (MIL–G–45204), 0.019" ±0.001" (0.48 ±0.03mm) dia.
For plug-in mounting card order Board No. AC1546

OFFSET CALIBRATION

For 0 to +10V unipolar units set the input voltage precisely to +0.0012V; for 0 to +20V units set it to +0.0024V. Adjust the zero potentiometer until the converter is just on the verge of switching from 000000000000 to 000000000001.

For ±5V bipolar units set the input voltage precisely to -4.9988V; for ±10V units set it to -9.9976V. Adjust the zero potentiometer until Offset Binary coded units are just on the verge of switching from 000000000000 to 000000000001 and Two's Complement coded units are just on the verge of switching from 100000000000 to 100000000001.



Adjustment Connections

GAIN CALIBRATION

Set the input voltage precisely to +19.9927V for 0 to +20V units, +9.9963V for 0 to +10V units, +4.9963V for ±5V units, or +9.9927V for ±10V units. Note that these values are 1½LSB's less than nominal full scale. Adjust the gain potentiometer until Binary and Offset Binary coded units are just on the verge of switching from 111111111110 to 111111111111 and Two's Complement coded units are just on the verge of switching from 011111111110 to 011111111111.

SHORT CYCLE CONNECTIONS

When the ADC1102 is operated as a 12-bit device, Pin 37 is left open. If, however, it is to perform conversions of less than 12 bits, Pin 37 is connected to the N+1 bit output (where N is the number of bits in the conversion). The conversion time in this mode of operation is 8μs x N/12.

ANALOG DEVICES

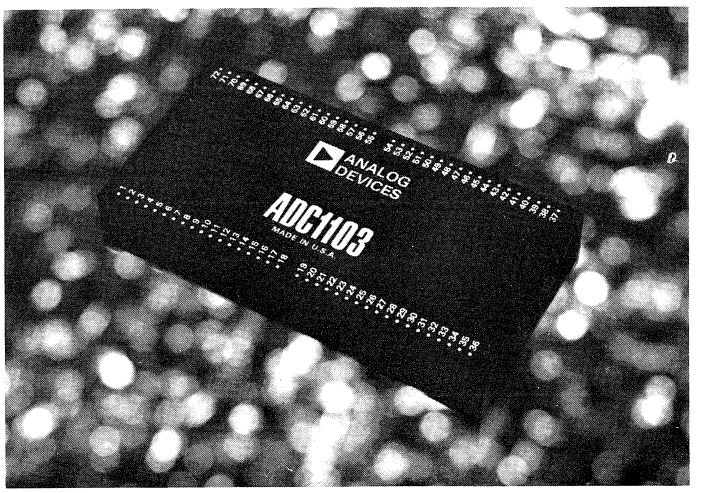
Fast A/D Converter

ADC1103

FEATURES

High Speed
- **8 Bits in 1.0μs max**
- **10 Bits in 1.5μs max**
- **12 Bits in 3.5μs max**

Error Relative to Full Scale ±1LSB max
Gain TC ±10ppm/°C max
User Choice of Three Input Ranges
Small 2" x 4" x 0.75" Module



GENERAL DESCRIPTION

The ADC1103 is a high speed analog-to-digital converter packaged in a small 2" x 4" x 0.75" module. It is available in 8, 10, and 12 bit versions. The 8 bit model performs a conversion in 1.0μs max, the 10 bit version in 1.5μs max, and the 12 bit unit in 3.5μs max. The ADC1103 uses the successive approximations technique to convert analog input voltages into natural binary, offset binary, or two's complement coded parallel output digital data. Careful design and the use of Schottky TTL have resulted in a very fast A/D converter that features an error relative to full scale of only ±1LSB max. The unit has a maximum gain TC of only ±10ppm/°C.

Three analog input ranges are available. The user, with connections at the module pins, can select the 0 to +10V range, the -5V to +5V range, or the -10V to +10V range. When using the 0 to +10V range, the output coding is natural binary. However, when using either the -5V to +5V range or the -10V to +10V range, either offset binary or two's complement coding can be selected. The user can also choose to short cycle the converter (i.e., have it perform conversions of less than the maximum number of bits).

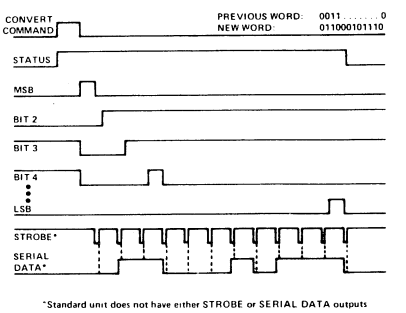
APPLICATIONS

The ADC1103 is a general purpose fast A/D converter. It is especially well suited for applications requiring high throughput rates with no compromise in accuracy. A typical application would be a multiple channel data acquisition system, where a high throughput rate/channel is needed. The ADC1103's high speed makes it an excellent choice for such applications as fast Fourier transform analysis, radar pulse analysis, conversion of analog data acquired from simultaneous sample-and-hold data collection systems, and for conversion of analog data to be fed into digital filters and correlators.

TIMING

As shown in Figure 1, the Status output is set to a Logic "1" on the leading edge of the convert command pulse. On the trailing edge of the convert command pulse, the MSB output is set to a Logic "1", the remaining bit outputs are set to "0", and the conversion commences.

The output data is valid 4ns prior to the "1" to "0" transition of the STATUS output (or "0" to "1" transition of the $\overline{\text{STATUS}}$ output). This set-up time is sufficient to allow the output data to be strobed into a following Schottky TTL register on either of these two edges. If a standard TTL register is used, data should not be strobed into it until at least 16ns after the STATUS and $\overline{\text{STATUS}}$ transitions occur. The SERIAL DATA output (which does not appear on the standard unit) is of the nonreturn-to-zero type (NRZ). The data is available, MSB first, on successive "0" to "1" DATA STROBE transitions.



*Standard unit does not have either STROBE or SERIAL DATA outputs

Figure 1. Timing Diagram

SPECIFICATIONS (typical @ +25°C and nominal supply voltages, unless otherwise noted)

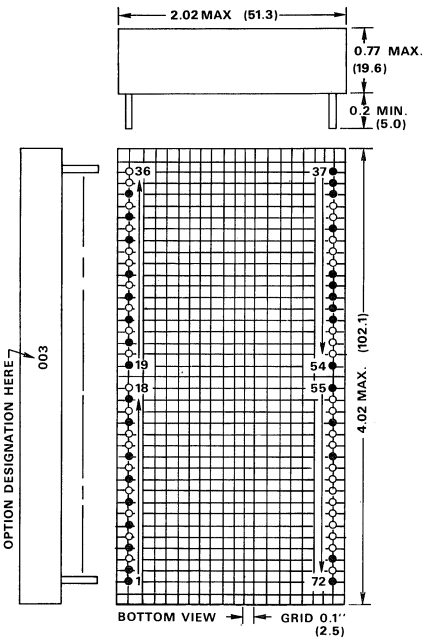
RESOLUTION	
ADC1103-001	8 Bits
ADC1103-002	10 Bits
ADC1103-003	12 Bits
CONVERSION TIME	
ADC1103-001	1.0μs, max
ADC1103-002	1.5μs, max
ADC1103-003	3.5μs, max
ACCURACY[1]	
Error Relative to Full Scale[2]	±1LSB max
Quantization Error	±½LSB max
Differential Nonlinearity Error[2]	±1LSB max
Missing Codes[3]	No missing codes from 0 to +70°C
TEMPERATURE COEFFICIENTS	
Gain TC	±10ppm/°C of reading, max
Zero TC (Unipolar Input)	±5ppm/°C of full scale, max
(Bipolar Input)	±10ppm/°C of range, max
Differential Nonlinearity TC	±5ppm/°C of range, max
INPUT VOLTAGE RANGES	0 to +10V, ±10V, ±5V
INPUT IMPEDANCE	
0 to +10V and ±5V Ranges	2.50k ohms
±10V Range	5.00k ohms
CONVERT COMMAND	Positive pulse, 50ns min width, 1μs max rise and fall times, TTL compatible
PARALLEL DATA OUTPUT	
With Unipolar Input Range	Positive true binary
With Bipolar Input Range	Positive true offset binary or two's complement
SERIAL DATA OUTPUT[4]	Bits valid on successive "0" to "1" transitions of Data Strobe pulses, with MSB first. TTL compatible.
STATUS OUTPUT	"1" during conversion. Complement also available. TTL compatible.
LOGIC FANOUTS AND LOADINGS	
Convert Command Input	5 TTL unit loads
Parallel Data Outputs	8 TTL unit loads/bit
STATUS Output	8 TTL unit loads
$\overline{\text{STATUS}}$ Output	8 TTL unit loads
Serial Data Output[4]	8 TTL unit loads
Clock Inhibit Input	1 TTL unit load
Data Strobe Output[4]	8 TTL unit loads
ADJUSTMENTS	
Zero (or Offset)	External 100k ohm potentiometer across ±15V with slider to pin 46.
Gain	External 100k ohm potentiometer across ±15V with slider to pin 70.
POWER REQUIREMENTS	+15V dc ±3% @ 85mA max -15V dc ±3% @ -80mA max +5V dc ±5% @ 525mA max
POWER SUPPLY SENSITIVITY[5]	±0.003%/%△V (±15V only) typical ±0.007%/%△V (±15V only) max
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +125°C

[1] Warm-up time to rated accuracy is 5 minutes.
[2] ±½LSB for the ADC1103-001 and ADC1103-002.
[3] Except the ADC1103-003 which is guaranteed to have no missing codes at +25°C.
[4] The standard unit does not have a serial output, or a data strobe output. Contact the factory for price and availability of models with serial output.
[5] This specification is valid only when the +15V supply tracks the -15V supply (or vice versa).

Specifications subject to change without notice.

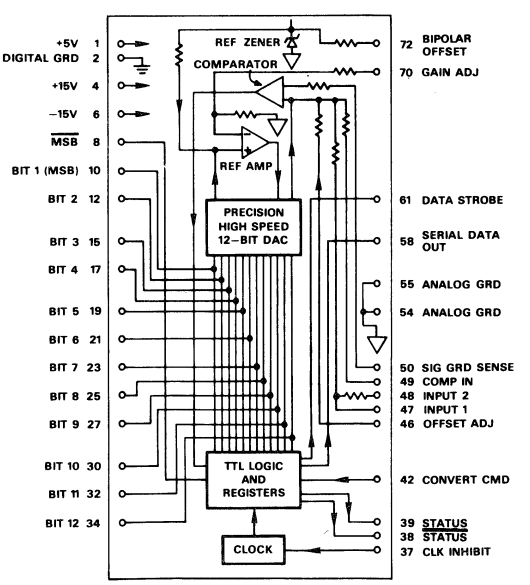
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
All pins are 0.019" ±0.001" (0.48mm ±0.03mm) dia. half-hard brass, gold plated per MIL-G-45204B, Class I, Type II.
For plug-in mounting card, order Board No. AC1549

BLOCK DIAGRAM AND PIN DESIGNATIONS



NOTE:
The standard model does not have a serial output, and therefore pins 58 and 61 are deleted from it.
The ADC1103-002 does not contain pins 32 and 34. The ADC1103-001 does not contain pins 27, 30, 32 and 34.

ANALOG SIGNAL INPUT CONNECTIONS

The ADC1103 offers a choice of three input ranges, any of which may be selected by the user. The table below shows the connections required for each range.

INPUT RANGE SELECTION

Input Range in Volts	Connect Input Signal To	Connect Pin 49 To
0 to +10V	Pin 47	Pins 54 and 55*
-5V to +5V	Pin 47	Pin 72
-10V to +10V	Pin 48	Pin 72

*Also connect a 3.0kΩ ±5% resistor between pin 72 and pins 54 and 55.

Signal ground sense (pin 50) should normally be jumpered to analog ground (pins 54 and 55). However, in the event there is an offset in the ground wiring, it may be possible to eliminate it by connecting pin 50 instead directly to the signal or analog ground of the device feeding the analog input signal to the ADC1103. In any case, pin 50 *must not* be left open with nothing connected to it.

If a high input impedance is required, it can be achieved by using a high speed operational amplifier as an input buffer. Analog Devices' model 48 fast settling differential amplifier, packaged in a small 1.125" x 1.125" x 0.4" module, is an ideal choice.

OUTPUT CODING

When using the 0 to +10V range, the ouput coding is natural binary, positive true. When using the ±5V or ±10V ranges, the coding can be either positive true offset binary or positive true two's complement at the user's option. The only difference between the two codes is the state of the MSB. The MSB output (pin 10) is used for offset binary coding, while the $\overline{\text{MSB}}$ output (pin 8) is used for two's complement coding.

GAIN AND OFFSET ADJUSTMENTS

Gain and offset adjustments are performed with external 100k ohm, 20 turn potentiometers connected across the ±15V power supply. The slider of the gain adjustment potentiometer is connected to pin 70, and the slider of the offset potentiometer is connected to pin 46. The gain adjustment potentiometer has a range of about ±20 LSB's, and the offset potentiometer has a range of about ±10 LSB's.

Proper gain and offset calibration requires great care, and the use of extremely sensitive and accurate reference instruments. The voltage source used as a signal source must be very stable. It should be capable of being set to within 1/10LSB of the desired value at both ends of its range.

The gain and offset calibrations will be independent of each other if the offset adjustment (or zero adjustment, if using the 0 to +10V range) is made first. These adjustments are not made with zero and full scale input signals, and it may be helpful to understand why. An A/D converter will produce a given digital word output for a small range of input signals, the average width of the range being one LSB. If the input test signal is set at a point where the converter should be on the verge of switching to the next value, the unit can be calibrated so that it does switch to the next value at just that point. With a high speed convert command rate and a visual display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices' *Analog-Digital Conversion Notes* gives more detailed information on testing and calibrating A/D and D/A converters.

The following table will be useful in calculating the input voltage settings needed during gain and offset calibration.

VOLTAGE EQUIVALENT OF ½LSB FOR CONVERTERS OF VARIOUS RESOLUTIONS AND INPUT VOLTAGE RANGES

Converter Resolution	Input Voltage Range*		
	5 Volts	10 Volts	20 Volts
8 Bits	9.77mV	19.53mV	39.06mV
10 Bits	2.44mV	4.88mV	9.77mV
12 Bits	0.61mV	1.22mV	2.44mV

*Where range = +F.S. – (-F.S.)

OFFSET (OR ZERO) CALIBRATION

Set the input voltage precisely to ½LSB above zero when using the 0 to +10V range, or to ½LSB above nominal minus full scale when using either the ±5V or ±10V range. Then adjust the offset potentiometer until the converter is just on the verge of switching between all "0's" and having just its LSB on.

GAIN CALIBRATION

Set the input voltage precisely to a value equal to ½LSB less than the point where the converter would have all bits at a Logic "1". Note that this is 1½LSB's less than nominal full scale. For example, full scale of a 0 to +10V 12 bit A/D converter is actually +9.9976 Volts. Gain adjustment should be made with an input ½LSB less than that value, or +9.9963 Volts. Adjust the gain potentiometer to the point where the last bit just comes on. In a 12 bit converter, this would be where the output code just barely changes from 111111111110 to 111111111111.

CLOCK INHIBIT CONNECTIONS

Clock Inhibit (pin 37) normally must be externally jumpered to $\overline{\text{STATUS}}$ (pin 38). The only exception to this would occur when it is desired to short cycle the converter (i.e., have it perform a conversion of less than the maximum number of bits). In such an instance, pin 37 would instead be jumpered to the N + 1 bit output, where N is the number of bits in the conversion. For example, the 12 bit ADC1103-003 would perform 7 bit conversions if pin 37 were jumpered to the Bit 8 output (pin 25). The conversion time would be 7/12 x 3.5μs max = 2.04μs max.

When operating the converter in the short cycle mode, the STATUS (pin 39) and $\overline{\text{STATUS}}$ (pin 38) outputs are no longer valid. Instead, the N + 1 bit output becomes a $\overline{\text{STATUS}}$ output (i.e., "0" during a conversion).

WIRING CONSIDERATIONS

Because of the ADC1103's very high speed and its 12 bit capability, good wiring practices are essential for best performance. Care should be taken to ensure that the analog ground connection is a good, solid connection. The digital inputs and outputs should be kept away from the analog signals. Analog ground and digital ground are tied together internally, but it is important that no digital ground signals be present in a path serving as an analog ground return. When de-

signing a PC board to accept the ADC1103, it is suggested that as much ground plane area as possible be left underneath the ADC1103.

The +5V and ±15V power inputs are internally bypassed, but it is recommended that additional bypass capacitors be added externally. The capacitors should be located as near the module pins as possible. The +5V bypass capacitor should be connected between the +5V input (pin 1) and digital ground (pin 2). The ±15V bypass capacitors should be connected between pin 4 and analog ground, and pin 6 and analog ground. The capacitors would typically be 10μF (or greater) tantalum types.

RECOMMENDED POWER SUPPLIES

The ADC1103 requires +15 volts at 85mA max, -15V at 80mA max, and +5V at 525mA max. Analog Devices' model 902 ±15V modular power supply is rated at 100mA, making it an ideal choice for the ADC1103's ±15 volt power requirements. Analog Devices' model 905 modular power supply puts out +5V at up to 1.0 amperes, which makes it well suited to supplying the ADC1103's +5V needs.

IMPROVING POWER SUPPLY REJECTION

Most of the power supply sensitivity called out in the specifications is due to variations in the voltage applied to the gain and offset adjustment potentiometers. This specification can therefore be improved by at least an order of magnitude by using the circuit shown below in Figure 2.

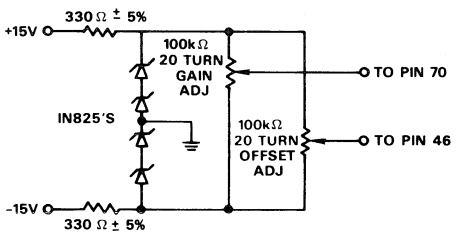


Figure 2. Zener Diode Isolated Adjustment Pots

SERIAL OUTPUT

The standard ADC1103 *does not* include a serial output. For this reason, SERIAL OUTPUT (pin 58) and DATA STROBE (pin 61) do not appear on the standard unit.
The conversion time on any units containing a serial output is increased by about 20ns/bit. The data is transmitted MSB first, and the coding is natural binary for a unipolar input, or offset binary for a bipolar input. Each serial data bit is valid beginning 16ns prior to the rising edge ("0" to "1" transition) of its strobe pulse. This permits the serial data to be clocked into a receiving shift register on successive strobe pulse rising edges. Each of the strobe pulses is between 16ns and 22ns wide, and in a complete conversion there are exactly as many strobe pulses as there are bits.

THE AC1549 MOUNTING CARD

The ADC1103's very high speed demands that considerable thought be given to the wiring connected to the module, even when simply evaluating the unit in a temporary laboratory bench set-up. To assist with such evaluations, an AC1549 Mounting Card is available. This 4½" x 6" printed circuit card has sockets that allow an ADC1103 to be plugged directly onto it. It also has provisions for an Analog Devices' model 48 fast settling op amp which, if used, serves as an input buffer. The card includes gain and offset adjustment potentiometers, and power supply bypass capacitors. It mates with a Cinch 251-22-30-160 (or equivalent) edge connector, which is supplied with the card.

REPETITIVE CONVERSIONS

When making repetitive conversions, a small time interval must be allowed between the completion of one conversion and the beginning of the next. This results in a maximum throughput rate of 769kHz for the ADC1103-001, 526kHz for the ADC1103-002 and 250kHz for the ADC1103-003.

The ADC1103 can be interrupted during a conversion with a new convert command. The unit will reset and begin a new conversion. However, if it is so interrupted, the convert command pulse should be at least 300ns wide for the ADC1103-001, at least 400ns for the ADC1103-002, and at least 500ns wide for the ADC1103-003. This will give the ADC1103's clock sufficient time to reset before beginning the new conversion.

HIGH THROUGHPUT RATE DATA ACQUISITION

The ADC1103's high speed allows it to be used in data acquisition applications where a high throughput rate is required. For example, Figure 3 shows a sequentially addressed, eight channel data acquisition subsystem capable of acquiring data to 12 bit accuracy at a 220kHz throughput rate. The system uses an Analog Devices' MPS-8A Multiplexer, SHA-2A Sample-and-Hold Amplifier, and an ADC1103-003. Its sampling rate/channel is a very respectable 27.5kHz.

When using this system, the convert command should be at least 500ns wide. This allows the SHA-2A to settle to 12 bit accuracy before the ADC1103 commences its conversion. The SHA-2A is switched into the HOLD mode on the rising edge of the convert command pulse, but the conversion does not actually begin until the falling edge of the convert command pulse occurs.

The MPX-8A is advanced to the next channel at the same time the SHA-2A is switched into the HOLD mode. This allows the multiplexer to settle to a new analog input while the conversion of the previous channel's input is in progress. In this way, the MPX-8A's settling time does not affect the maximum throughput rate.

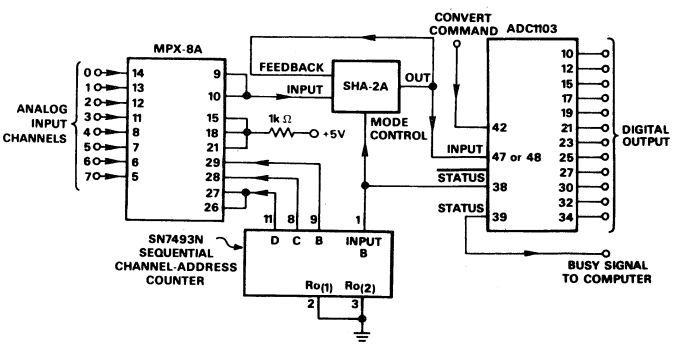
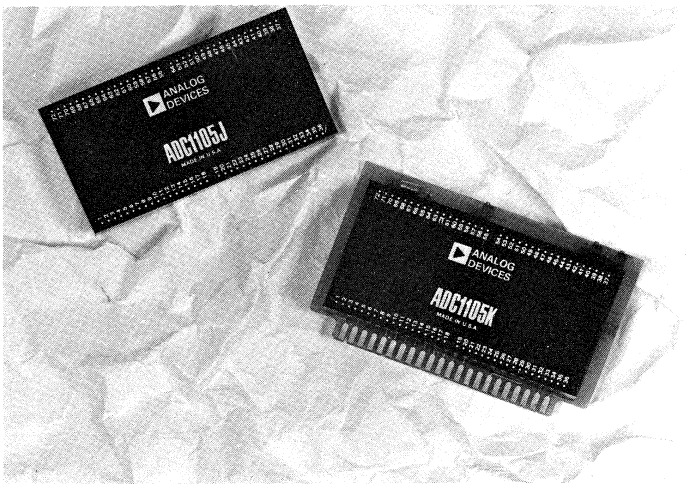


Figure 3. High Speed Data Acquisition Subsystem

High Linearity, High Resolution, Dual Slope A/D Converter

ADC1105

FEATURES
- Ultra-High Linearity (Nonlinearity ≤±1 Count)
- Output Versatility With External Counters and Registers
- High Resolution
  - Up to 1:40,000 (ADC1105K)
  - Up to 1:4,000 (ADC1105J)
- Excellent Zero Stability
- User Choice of Input Ranges
- Accepts Unipolar or Bipolar Inputs
- Low Profile 2" x 4" x 0.6" Module
- Special Mounting Card Available
- Ratiometric Capability
- Automatic Sample Capability



GENERAL DESCRIPTION

The ADC1105 is a precision dual slope analog-to-digital converter which is designed for use with external counters and registers. With this product, the designer can build conversion systems which utilize any desired counting scheme and which have resolutions up to and including 4 BCD digits (or 14 binary bits) plus 100% overrange plus sign. This versatility is particularly useful in instrumentation applications where it is desired to have outputs scaled directly in terms of engineering or physical units (e.g. pounds and ounces).

Performance specifications for the ADC1105 include 2μV/°C zero stability, 5ppm/°C gain temperature coefficient, and ±0.0015%/%V_S power supply sensitivity.

The ADC1105 is compatible with TTL/DTL as well as certain older RTL systems. It can be configured to perform conversions on command or automatically at a rate controlled by simple external circuitry. The ADC1105 also offers both a ±10V and a ±1V input range, each with 100% overrange capability.

BASIC OPERATION

As a dual slope converter, the ADC1105 produces a pulse train output, the number of pulses in which is proportional to the analog input voltage. It also provides all of the signals needed to properly control the external counters and registers. A simple parallel output analog-to-digital converter built around the ADC1105 is shown in Figure 1.

Although this represents a typical arrangement it is by no means the only one possible. Detailed timing diagrams and descriptions of terminal input/output characteristics will be presented in a later section to aid the designer in adapting the ADC1105 to his system's particular requirements.

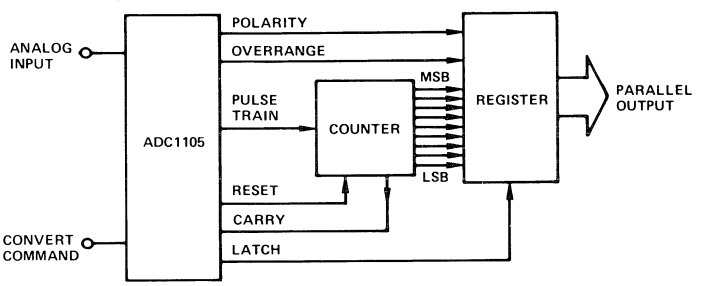


Figure 1. Basic Converter Block Diagram

The conversion cycle begins when the convert command is applied. The counter is reset to zero, input integration begins, and output pulses are generated. When the counter reaches full scale, a carry signal is sent back to the ADC1105 to initiate reference integration. When the integrator voltage returns to zero, the pulse train stops and the output register is strobed. The polarity signal is generated at the end of the input integration period; the overrange signal is generated during the reference integration period and is valid at the end of conversion.

SPECIFICATIONS (typical @ +25°C and nominal supply voltages, unless otherwise noted)

MODEL	ADC1105J	ADC1105K
RESOLUTION	Up to 3½BCD Digits or 10 Binary Bits Plus Sign	Up to 4½BCD Digits or 14 Binary Bits Plus Sign
NON-LINEARITY[3]	⩽±1 Count	⩽±1 Count
ANALOG INPUT RANGES[1]	±1V Full Scale	*
	±10V Full Scale	*
INPUT IMPEDANCE	100kΩ/Volt ±1%	*
TEMPERATURE COEFFICIENTS		
Gain[2]	±10ppm/°C max	±5ppm/°C max
Offset	±2μV/°C max; 1V Range	*
	±20μV/°C max; 10V Range	*
Reference	±20ppm/°C max	±5ppm/°C max
CONVERSION TIME	See Table 2	*
CONVERSION RATE	See Table 2	*
REFERENCE VOLTAGE		
Fixed Reference	±6.2V ±5%	*
Ratiometric	±20V max	*
CLOCK FREQUENCY	200kHz ±10%	*
Adjustment Range	±10kHz	*
DIGITAL INPUTS	See Digital Input Characteristics Text	
DIGITAL OUTPUTS	See Digital Output Characteristics Text	
POWER SUPPLY REQUIREMENTS	+5V ±5% @ 120mA	*
	+15V ±5% @ 45mA	*
	-15V ±5% @ 35mA	*
POWER SUPPLY SENSITIVITY	±0.0015%/%V_S	*
TEMPERATURE RANGE		
Operating	0 to +50°C	*
Storage	-25°C to +85°C	*
MTBF (CALCULATED)	70,000 Hours	*

*Same as ADC1105J.

[1] Each input range has 100% overrange capability, thereby permitting inputs of ±2V and ±20V respectively.

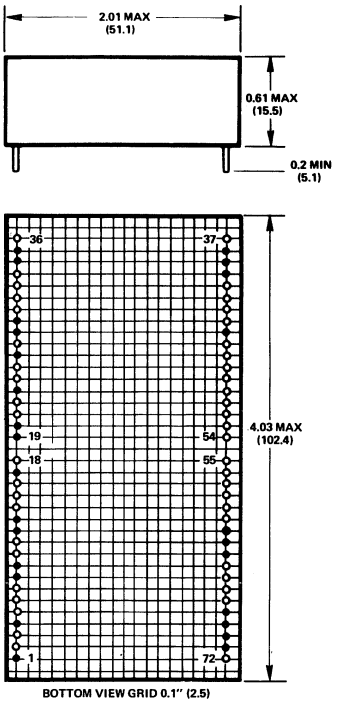
[2] Exclusive of reference.

[3] Difference between the actual input-output transfer function and the theoretically perfect straight-line through zero and + or – full scale.

Specifications subject to change without notice.

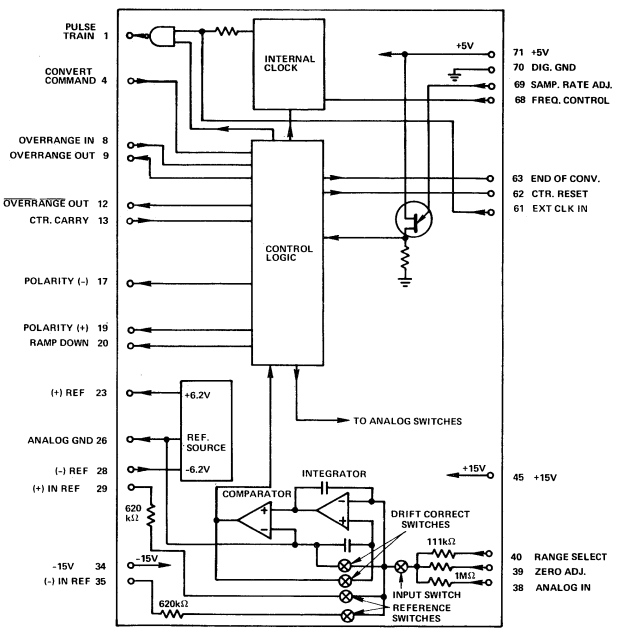
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
Module weight: 4 ounces (114 grams).
All pins are gold-plated half-hard brass plated per MIL-G-45204; 0.019" ±0.001" dia. (0.48mm ±0.03mm).

BLOCK DIAGRAM AND PIN DESIGNATIONS



ORDERING GUIDE:

ADC1105J	(Module Only)
ADC1105K	(Module Only)
ADC1105J/AC1547J	(Module Mounted on Card)
ADC1105K/AC1547K	(Module Mounted on Card)

CONVERSION SEQUENCE

Figures 2a and 2b below illustrate the interaction of the ADC1105's various inputs and outputs during two conversion cycles. Figure 2a shows the sequence of events for a negative polarity, overrange input of -12V while Figure 2b shows the sequence for a positive, in-range input of +8V. Both examples assume that the 10V range of the ADC1105 is selected and that a 4 digit BCD counter with a full scale count of 9999 is being used.

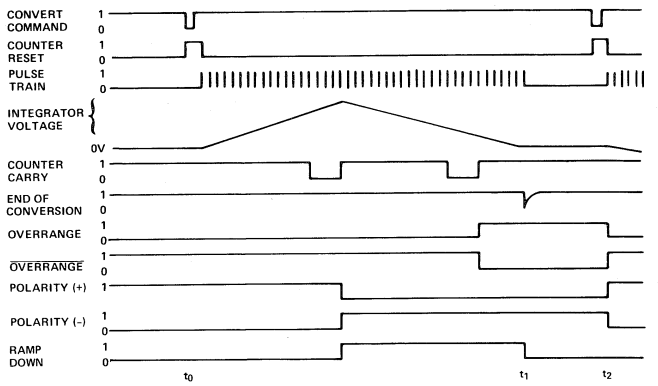


Figure 2a. Timing Diagram

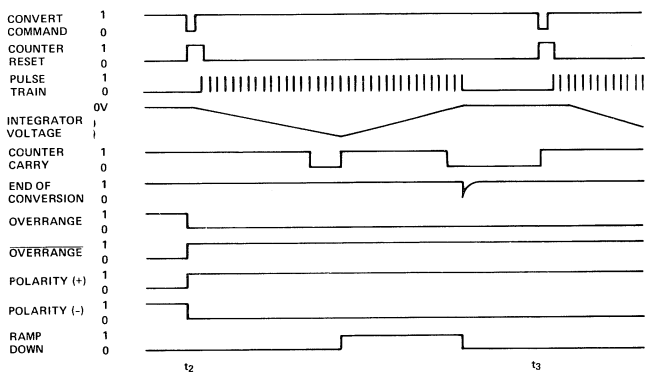


Figure 2b. Timing Diagram

At time t_0 a conversion is commanded by the "1" to "0" transition of the CONVERT COMMAND input (Pin 4). This causes a 1μs positive pulse to be generated at the COUNTER RESET terminal (Pin 62) which sets the counter to 0000. After the counter is reset, a 200kHz pulse signal is generated at the PULSE TRAIN OUTPUT terminal (Pin 1), the integrator comes out of drift correct, and input integration begins. The pulse train causes the counter to increment upwards and when the transition from 9999 to 0000 finally occurs, a "0" to "1" transition is sensed at the COUNTER CARRY INPUT terminal (Pin 13). This causes reference integration to begin. Since the input signal was negative, the POLARITY (+) output (Pin 19) goes to a "0" and the POLARITY (-) output (Pin 17) goes to a "1" at this time. The RAMP DOWN output (Pin 20) also goes to a "1" indicating that reference integration is in progress.

Because the input signal exceeds -10V, the integrator does not fully discharge before the counter reaches 9999. Therefore, when the counter goes from 9999 to 0000, a "0" to "1" transition is sensed at the OVERRANGE IN terminal (Pin 8) causing the OVERRANGE output (Pin 9) to go to a "1" and the $\overline{\text{OVERRANGE}}$ output (Pin 12) to go to a "0". At time t_1 the integrator finally discharges and a 1μs negative pulse is generated at the END OF CONVERSION output (Pin 63). The pulse train stops and the RAMP DOWN output returns to "0".

At time t_2 another conversion is commanded with the analog input at +8V. The events which occur are identical to those of the previous conversion except that on the "1" to "0" transition of the CONVERT COMMAND input, the $\overline{\text{OVERRANGE}}$ and the POLARITY (+) are reset to "1" and the OVERRANGE and the POLARITY (-) are reset to "0". Because the input signal is positive, the POLARITY (+) and POLARITY (-) outputs do not change state at the start of reference integration and since the integrator fully discharges before the external counter carries, the OVERRANGE and $\overline{\text{OVERRANGE}}$ do not change state.

CONVERSION TIME

The conversion time of the ADC1105 consists principally of the input and reference integration periods. The length of the input integration period (T_{IN}) depends on the clock frequency (f_c) and the counter's full scale setting (C_{FS}) as expressed by the following equation:

$$T_{IN}\ (\text{ms}) = \frac{C_{FS}}{f_c\ (\text{kHz})}$$

The following table, Table 1, lists input integration periods for various counter configurations at the nominal 200kHz clock frequency.

Counter Size	Input Integration Period
8 Bit Binary	1.28ms
10 Bit Binary	5.12ms
12 Bit Binary	20.48ms
14 Bit Binary	81.92ms
3 Digit BCD	5.00ms
4 Digit BCD	50.00ms

Table 1. Input Integration Period

Note that because of the OVERRANGE and POLARITY outputs, the total converter resolution will be greater than the counter size. For example, a converter using an 8 bit binary counter can have a 10 bit sign-magnitude binary coded output.

The reference integration period (T_{REF}) is related to the input integration period (T_{IN}) by the following expression:

$$T_{REF}\ (\text{ms}) = T_{IN} \times \frac{V_{IN}}{V_{FS}}$$

; V_{IN} = analog input in volts

V_{FS} = 10V or 1V (depending on the range selected)

Because the 100% overrange condition represents the maximum permissible input level, the maximum reference integration period is twice the input integration period. Table 2 below lists the maximum total conversion times and resulting minimum conversion rates for various counter configurations at the nominal 200kHz clock frequency

Counter Size	Total Conversion Time	Conversion Rate
8 Bit Binary	3.84ms	260/sec
10 Bit Binary	15.36ms	65/sec
12 Bit Binary	61.44ms	16/sec
14 Bit Binary	245.76ms	4/sec
3 Digit BCD	15.00ms	66/sec
4 Digit BCD	150.00ms	6/sec

Table 2. Maximum Total Conversion Time and Minimum Conversion Rates

DIGITAL INPUT CHARACTERISTICS

Convert Command (Pin 4)

A "1" to "0" transition with a 2μs max fall time initiates conversion. The "0" state must be held for at least 100ns. If conversions are to be commanded by the automatic sample rate circuitry, this input must be tied to ground. 1TTL load (max).

Counter Carry (Pin 13)

A "0" to "1" transition at this terminal indicates that the external counter has reached full scale and returned to zero. The "1" state must be held for at least 30ns. 2TTL loads (max).

Overrange In (Pin 8)

A "0" to "1" transition at this terminal indicates that the external counter has reached full scale and returned to zero. It is used to determine if an overrange condition has occurred and in normal operation is jumpered to Pin 13. 2TTL loads (max).

External Clock In (Pin 61)

An external clock with a maximum frequency of 250kHz will override the internal clock when connected to this terminal. In this mode of operation the convert command must be synchronized to the 1 to 0 transition of the clock pulse. 1TTL load (max).

DIGITAL OUTPUT CHARACTERISTICS

Gated Pulse Train (Pin 1)

This is a 200kHz (nominal) positive pulse output with a 1μs pulse duration. It is capable of driving 10TTL loads (min).

Counter Reset Output (Pin 62)

This is a 1μs positive pulse which is used to reset the counter at the start of conversion. The output circuit consists of an NPN emitter-follower with a 39Ω series resistor which is capable of supplying 40mA (max). When a 270Ω resistor is connected between this pin and ground, one standard TTL load can be driven.

End of Conversion (Pin 63)

This is a 1μs negative pulse which is used to signal the end of conversion and/or strobe an external register. The output circuit consists of an NPN emitter follower with a 22Ω series resistor which is capable of supplying 40mA (max). When a 270Ω resistor is connected between this pin and ground, one standard TTL load can be driven.

Polarity (-) (Pin 17)

This output is set to a "0" each time a conversion is commanded. If the analog input signal is negative it will go to "1" at the start of reference integration and remain there until the next conversion. This output is capable of driving 8TTL loads (min).

Polarity (+) (Pin 19)

This is the complement of the signal at Pin 19. It is also capable of driving 8TTL loads (min).

Overrange (Pin 9)

This output is set to "0" each time a conversion is commanded. If an overrange condition is detected during reference integration it will go to a "1" and remain there until the next conversion. This output is capable of driving 10TTL loads (min).

Overrange (Pin 12)

This is the complement of the signal at Pin 9. It is also capable of driving 10TTL loads (min).

Ramp Down (Pin 20)

This output goes from a "0" to a "1" at the end of input integration and returns to "0" at the end of conversion. It is capable of driving 4TTL loads (min). The "1" state indicates that reference integration is in progress.

OTHER EXTERNAL CONNECTIONS

Sample Rate Control

The ADC1105 will automatically perform conversions at a rate which can be varied from 0.2 to 260 conversions per second if the external circuitry of Figure 3 is connected.

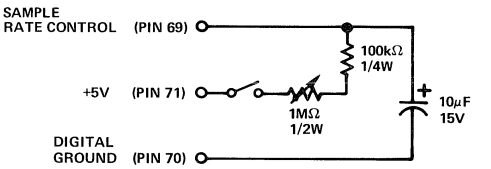


Figure 3. External Sample Rate Control Circuit

Range Selection

The nominal ±1V and ±10V input ranges will accept inputs of ±2V max and ±20V max because of their 100% overrange capability. Figure 4 shows a switching arrangement which allows selection of either input range.

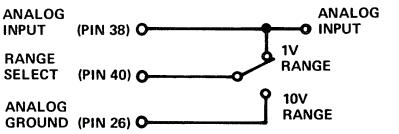


Figure 4. Range Selection Circuit

Clock Frequency Adjustment

The internal clock runs at 200kHz ±10%. If the external circuitry of Figure 5 is connected, this clock frequency can be varied by as much as ±10kHz.

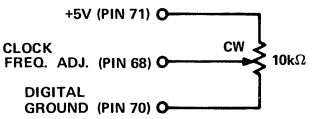


Figure 5. Clock Frequency Adjust Circuit

Zero Adjustment

The circuit of Figure 6 is used to precisely adjust the zero point. A detailed description of the adjustment procedure follows in a later section.

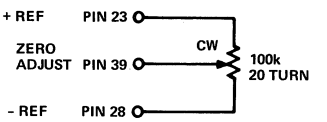


Figure 6. Zero Adjust Circuit

Gain Adjustment

The circuit of Figure 7 is used to set the +FS and -FS points once the zero point has been adjusted. A detailed description of the adjustment procedure follows in a later section.

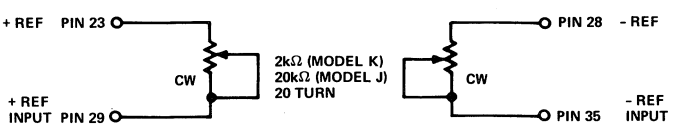


Figure 7. Gain Adjust Circuits

External Reference Connections

As shown in Figure 8, external reference sources may be used in place of the ADC1105's internal references. These external sources must supply +6.2V ±5% @ +10μA and -6.2V ±5% @ -10μA respectively.

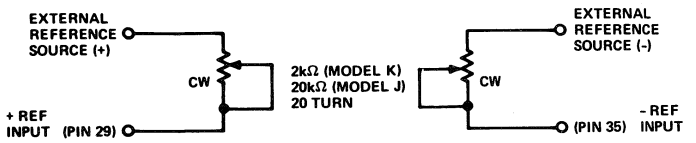


Figure 8. External Reference Connections

Two quadrant ratiometric operation is achieved by applying any voltage between 0 and +20V to the EXTERNAL REFERENCE SOURCE (+) input of Figure 8 while the same voltage is applied with opposite polarity to the EXTERNAL REFERENCE SOURCE (–) input. The converter's output (C_{OUT}) in this case is related to the analog input (V_{IN}) and the magnitude of the reference signal (V_{REF}) by the following equations:

$$C_{OUT} = 6.2C_{FS} \times \frac{V_{IN}}{V_{REF}} \text{ ; for the 1V range}$$

$$= 0.62C_{FS} \times \frac{V_{IN}}{V_{REF}} \text{ ; for the 10V range}$$

Where C_{FS} is the counter's full scale count.

In no case should values of V_{IN} and V_{REF} be applied which would result in a C_{OUT} which exceeds 2 $C_{FULL\ SCALE}$. A typical external circuit used to implement ratiometric operation is shown below in Figure 9.

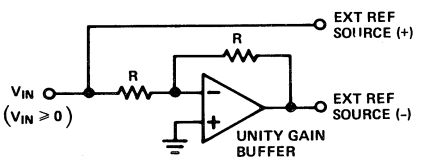


Figure 9. Additional Circuit for 2-Quadrant Ratiometric Operation

Power Supply Connections

The power supplies should be connected as shown below in Figure 10.

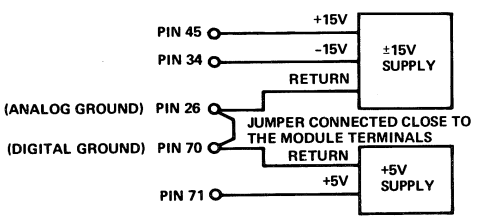


Figure 10. Power Supply Connections

Appropriate bypass capacitors have been included to reduce the effects of stray high frequency noise on the power supply busses.

THE AC1547 MOUNTING CARD

The AC1547 is an optional 4.50" x 2.77" printed circuit mounting card which has been specifically designed for use with the ADC1105 module. This card contains the three required adjustment potentiometers (+Gain, –Gain, and Zero), plated-through holes which are drilled out if external references are used, and a capacitor which simplifies connection of the external sample rate control circuit. When both an ADC1105 and an AC1547 are ordered, the module and card are soldered together and shipped as a single unit. Connections to the card are made with a Cinch 251-22-30-160 (or equivalent) dual 22 pin edge connector. The pin designations are listed below in Table 3.

Card Pin	Function	Module Pin	Card Pin	Function	Module Pin
1	END OF CONVERSION	63	A	POLARITY (–)	17
2	COUNTER CARRY	13	B	NC	–
3	NC	–	C	POLARITY (–)	17
4	NC	–	D	CLOCK FREQ. ADJ.	68
5	OVERRANGE IN	8	E	EXT. CLOCK IN	61
6	OVERRANGE OUT	9	F	CONVERT COMMAND	4
7	OVERRANGE OUT	12	H	RAMP DOWN	20
8	GATED PULSE TRAIN	1	J	NC	–
9	DIGITAL GROUND	70	K	DIGITAL GROUND	70
10	+5V	71	L	+5V	71
11	SAMPLE RATE CONTROL	69	M	POLARITY (+)	19
12	–15V	34	N	–15V	34
13	+15V	45	P	+15V	45
14–20	NC	–	R	COUNTER RESET	62
21	+ REF	23	S–W	NC	–
22	– REF	28	X	ANALOG INPUT	38
			Y	RANGE SELECT	40
			Z	ANALOG GROUND	26

Table 3. Pin Designations

The two plated-through holes located between the +Gain and –Gain potentiometers must be drilled out to disconnect the module's internal references if external reference sources are to be used. When this is done, the circuit of Figure 8 results, with mounting card pins 21 and 22 representing the External Reference Source (+) and External Reference Source (–) inputs respectively.

The external sample rate control circuit may be configured in several ways. If the circuit of Figure 3 is connected external to the mounting card, the sample rate can be varied from 4 conversions per minute to 86 conversions per second. If this same circuit is used but the +15V rather than the +5V supply is used, the sample rate can be varied from 0.2 to 260 conversions per second. If a fixed sample rate is desired, mounting card pin 11 is connected to the +5V supply and a 1/4W resistor is substituted for the jumper which is physically located between the zero adjust pot and the 10μF capacitor. A resistance decade box can be used to empirically determine the value of resistance needed to achieve the desired sample rate.

Figure 11 below shows the outline dimensions and layout of the AC1547 mounting card.

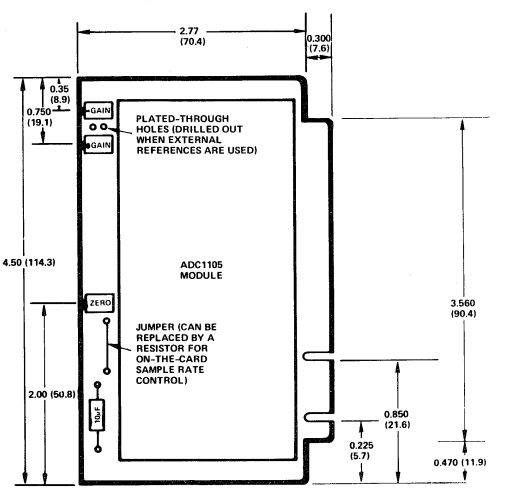


Figure 11. AC1547 Mounting Board Outline Dimensions Dimensions Shown in Inches and (mm)

ADJUSTMENT PROCEDURE

The adjustment procedure described in this section should be carefully followed to take full advantage of the ADC1105's high degree of resolution and accuracy. The voltage standard used in this procedure must be capable of providing stable outputs with ±1/10LSD resolution and accuracy in the region of ZERO, +FULL SCALE, and -FULL SCALE.

To adjust the zero point, apply a small positive signal to the analog input (e.g., +1mV for the 1V scale of a 4½ digit BCD converter). Use the zero adjust potentiometer to increase the counter output until it just changes to the correct value. Reverse the analog input polarity and observe that the polarity output has changed and that the counter output is within one count of the previous reading. Apply small adjustments to the zero adjust potentiometer as necessary until the counter output is the same for the positive and negative inputs.

Once the zero point has been adjusted, apply a +FULL SCALE analog input. Use the +GAIN adjustment potentiometer to increase the counter output until it just changes to one count above +FULL SCALE. Reverse the analog input polarity and repeat the procedure this time using the -GAIN potentiometer.

APPLICATIONS

Several converter configurations are shown below to demonstrate the versatility of the ADC1105. Because so many different TTL counters and registers are available, each one having its own interface requirements, block diagrams rather than schematics are used.

Figure 12 below shows the ADC1105 connected as a 14-bit sign-magnitude binary coded converter. Because of the nature of sign-magnitude code, the POLARITY (+) output is equivalent to the MSB. The OVERRANGE output is used as the next least significant bit and three 4-bit binary counters are used for the remaining 12 bits. A simple flip-flop is used to indicate the status of the digital output. The CONVERT COMMAND sets the STATUS output to a "1" and the END OF CONVERSION pulse resets it to a "0". The digital output is only valid while the STATUS output is low.

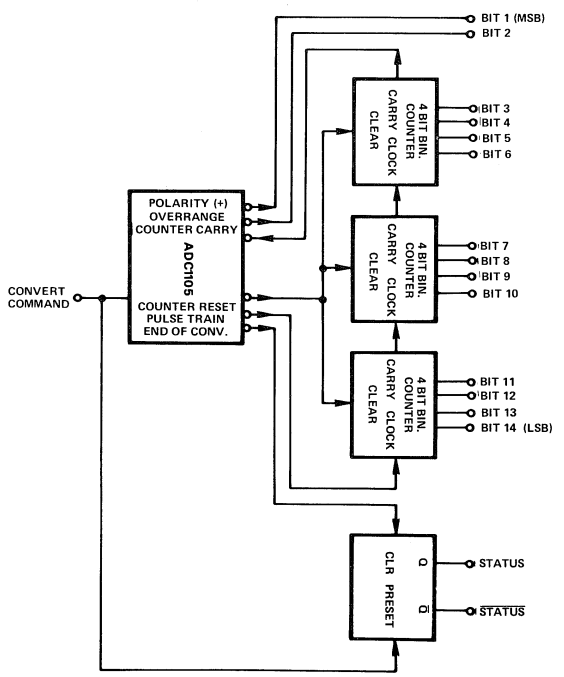


Figure 12. 14-Bit Sign-Magnitude Binary Converter

The converter of Figure 13 demonstrates how the external counter can be configured to give outputs expressed directly in engineering units. In this case the ADC1105 is used in a simple weighing system to receive analog inputs from a load cell and send latched BCD outputs (199 lbs. 15 oz. max) to a display. The 0 to 15 count which corresponds to the number of ounces is implemented with a 4-bit binary counter and a Binary-to-BCD converter. The 2½ digits corresponding to the number of pounds are generated by two decade counters and the OVERRANGE output. In this type of application the external sample rate control circuit would be used to provide automatic repetitive conversions.

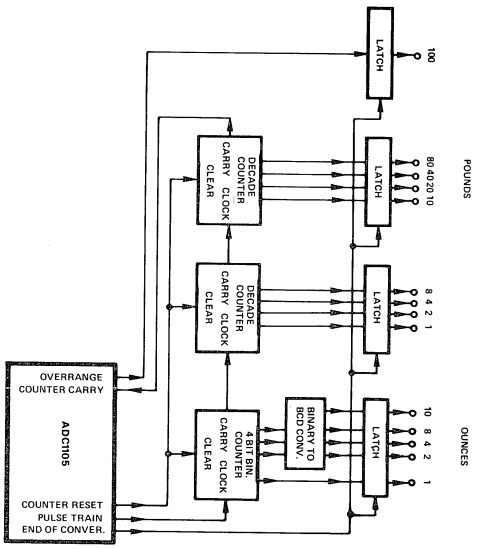


Figure 13. Simple Weighing System

Note that exclusive of polarity, the ADC1105K can resolve up to one part in 20,000 while the ADC1105J can resolve up to one part in 2000. When designing a converter which uses a specialized counting scheme, the number of possible counter states must be computed to determine which version to use. In the above example, the full scale count was 199:15 and, therefore, the number of possible states is 200 x 16 = 3200. It is clear that the ADC1105K would be the proper model to choose.

High Speed Analog to Digital Converter

ADC1109

FEATURES
High Speed: 10 Bits in 4μs Max
Error Relative to Full Scale: ±½LSB
User Choice of Unipolar or Bipolar Input
Small 2" x 3" x 0.4" Module

GENERAL DESCRIPTION

The ADC1109 is a high speed analog-to-digital converter packaged in a compact 2" x 3" x 0.4" module. It uses the successive approximations technique to perform complete 10 bit conversion in less than 4μs with ±½LSB relative accuracy.

The ADC1109 can be configured by the user to accept either unipolar or bipolar input signals and to produce Binary, Offset Binary, or Two's Complement coded outputs. The data outputs are fully DTL/TTL compatible and are available in both parallel and serial form.

TIMING

As shown in Figure 1, the "0" to "1" transition of the CONVERT COMMAND input sets the MSB output to Logic "0" and the STATUS, MSB, and BIT 2 through BIT 10 outputs to Logic "1". Nothing further happens until the CONVERT COMMAND returns to Logic "0", at which time the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-to-analog converter's output is compared with the analog input. If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB to Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic "0" and another comparison is made. This process continues through each successive bit until the BIT 10 (LSB) comparison is completed. At this time the STATUS output returns to Logic ' 0" and the conversion cycle ends.

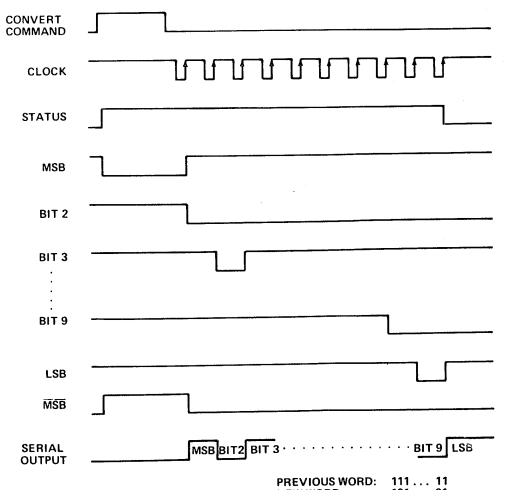


Figure 1. Timing Diagram

The SERIAL DATA output is of the non-return-to-zero (NRZ) type. The data is available, MSB first, 40ns after each of the ten "0" to "1" clock transitions.

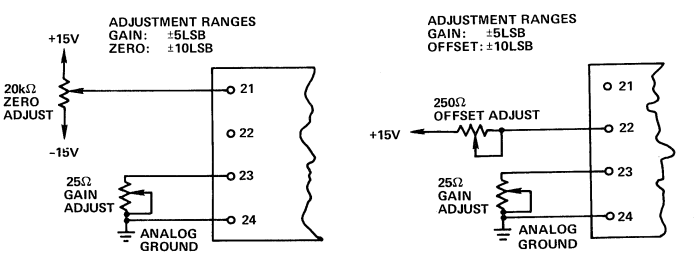
ZERO AND OFFSET CALIBRATION

For unipolar units set the input voltage precisely to +0.0049V and adjust the 20kΩ zero potentiometer until the converter is just on the verge of switching from 0000000000 to 0000000001.

For bipolar units set the input voltage precisely to -4.9951V and adjust the 250Ω variable offset resistor until Offset Binary coded units are just on the verge of switching from 0000000000 to 0000000001, and Two's Complement coded units are just on the verge of switching from 1000000000 to 1000000001.

GAIN CALIBRATION

Set the input voltage precisely to +9.9853 for unipolar units or +4.9853V for bipolar units. Note that these values are 1½LSB's less than nominal full scale. Adjust the 25Ω variable gain resistor until binary and offset binary coded units are just on the verge of switching from 1111111110 to 1111111111 and Two's Complement coded units are just on the verge of switching from 0111111110 to 0111111111.



UNIPOLAR **BIPOLAR**

ADJUSTMENT CONNECTIONS

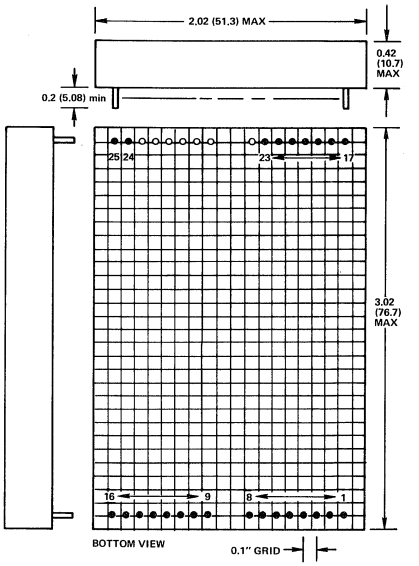
SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

MODEL	ADC1109
RESOLUTION	10 Bits
CONVERSION TIME[1]	3.8μs (4μs max)
ACCURACY[2]	
Error Relative to Full Scale	±½LSB
Quantization Error	±½LSB
Differential Nonlinearity Error	±½LSB
TEMPERATURE COEFFICIENTS	
Gain	±30ppm/°C of Reading (±50ppm/°C max)
Zero (Unipolar Inputs)	±200μV/°C (±500μV/°C max)
Offset (Bipolar Inputs)	±200μV/°C (±500μV/°C max)
Differential Nonlinearity	±7ppm/°C (±11ppm/°C max)
INPUT VOLTAGE RANGES	±5V, 0 to +10V
INPUT IMPEDANCE	10kΩ
CONVERT COMMAND	Positive Pulse, TTL Compatible, 100ns min Width
PARALLEL DATA OUTPUT	
Unipolar Inputs	Positive True Binary
Bipolar Inputs	Positive True Offset Binary or Two's Complement
SERIAL DATA OUTPUT	
Unipolar Inputs	Positive True Binary
Bipolar Inputs	Positive True Offset Binary TTL Compatible, NRZ Format, MSB First
STATUS OUTPUT	Logic "1" During Conversion, TTL Compatible
CLOCK OUTPUT	TTL Compatible, 190ns Width
LOGIC FANOUTS AND LOADING	
Convert Command	1TTL Load
Parallel Data Outputs	5TTL Loads/Bit
Status Output	8TTL Loads
Serial Data Output	6TTL Loads
Clock Output	10TTL Loads
ADJUSTMENT RANGES	
Gain	±5LSB
Zero	±10LSB
Offset	±10LSB
POWER REQUIREMENTS	+5V dc ±5% @ 125mA (135mA, max) +15V dc ±3% @ 35mA (40mA, max)[3] -15V dc ±3% @ 35mA (40mA, max)
POWER SUPPLY SENSITIVITY	
Gain (to +15V Supply)	±7.5mV/V (±15mV/V, max)
Zero (to +15V Supply)	±15mV/V (±20mV/V, max)
(to -15V Supply)	±5mV/V (±10mV/V, max)
Offset (to +15V Supply)	±400mV/V (±500mV/V, max)
(to -15V Supply)	±5mV/V (±10mV/V, max)
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C

[1] Conversion time is measured from trailing edge of the convert command to "1" to "0" transition of status output.
[2] Warmup time to rated accuracy is 5 minutes.
[3] Values shown are for the unipolar mode; values for the bipolar mode are 45mA (50mA, max).
Specifications subject to change without notice.

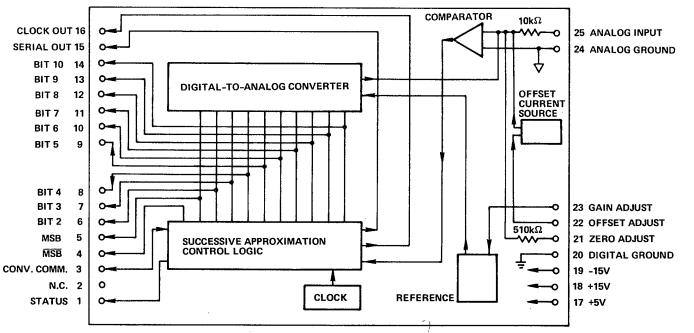
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Pins are installed only in shaded hole locations.
Pins are half hard brass, gold plated per MIL-G-45204B, Class I, Type II.
Pin Diameter is 0.019" (0.483mm) ±0.001" (0.025mm).
For plug-in mounting card 4.000" (101.6mm) x 4.500" (114.3mm), order Board No. AC-1520

BLOCK DIAGRAM AND PIN DESIGNATIONS



ANALOG INPUT	DIGITAL OUTPUT
	BINARY CODE
+9.9902V	1111111111
+5.0000V	1000000000
+1.2500V	0010000000
+0.0098V	0000000001
+0.0000V	0000000000

Table I. Nominal Unipolar Input-Output Relationships

ANALOG INPUT	DIGITAL OUTPUT	
	OFFSET BINARY	TWO'S COMPLEMENT
+4.9902	1111111111	0111111111
+2.5000	1100000000	0100000000
0.0000	1000000000	0000000000
-2.5000	0100000000	1100000000
-5.0000	0000000000	1000000000

Table II. Nominal Bipolar Input-Output Relationships

SERIAL DATA OUTPUT

The serial data output, available on pin 15, is of the non-return-to-zero format. The data is transmitted MSB first and is Binary coded for unipolar units and Offset Binary coded for bipolar units.

Figure 3, shown below, indicates one method for transmitting data serially using only three wires (plus a digital ground). The data is clocked into a receiving shift register using the delayed clock output of the ADC1109.

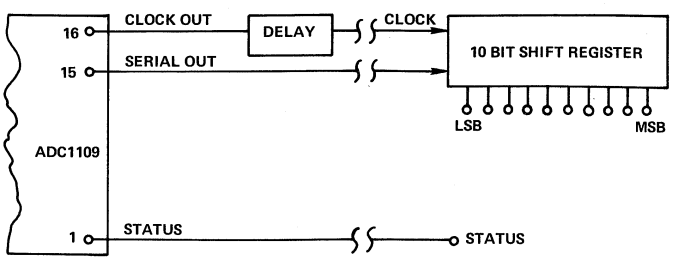
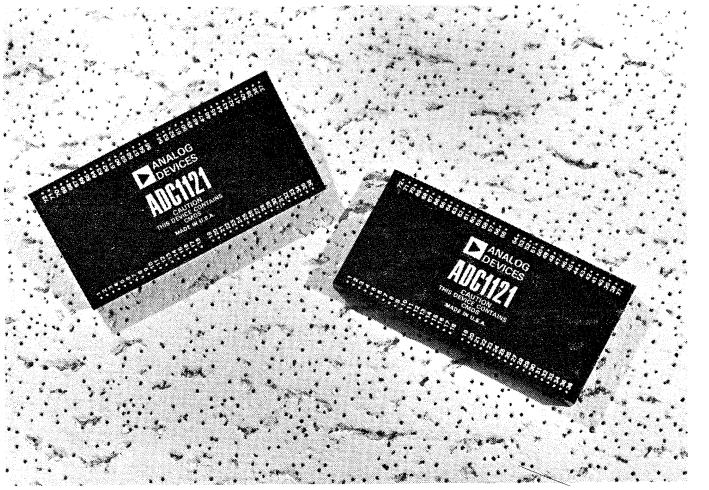


Figure 3. Serial Data Transmission

Low Power 12 Bit Analog to Digital Converter

ADC1121

FEATURES
- **12 Bit Resolution and Accuracy**
- **CMOS Compatible**
- **Very Low Power Consumption**
- **Exceptional Power Supply Rejection**
- **Can Operate From Single Battery**
- **No Missing Codes, 0 to +70°C**



GENERAL DESCRIPTION

The CMOS compatible ADC1121 requires less than 6 microjoules of energy to perform a complete, 12 bit analog-to-digital conversion. In addition, it has ±0.01% relative accuracy, a 70μs maximum conversion time, a maximum power consumption of 100mW for continuous conversions, and no missing codes from 0 to +70°C. Power may be supplied by a single +12V to +15V source, but the logic portions of the converter may also be powered by a separate +5V to +15V supply to permit logic level matching. If batteries are used as a power source, the resulting voltage droop will have little effect on the ADC1121 accuracy due to its excellent power supply rejection.

The ADC1121 accepts analog inputs in the range of 0 to +5V, 0 to +10V, ±5V, or ±10V and produces both parallel and serial digital outputs. Parallel outputs are binary, offset binary, or two's complement coded; serial outputs are binary or offset binary coded.

The special combination of high performance and low power exhibited by this 2" x 4" x 0.4" (51 x 102 x 10mm) module makes it ideal for use in applications such as remote and portable instrumentation, and large data handling networks.

TIMING

When the convert command is set to Logic "1", the internal clock starts to run. The first "1" to "0" clock transition sets the STATUS output to Logic "1" and sets the MSB through LSB and SERIAL output lines to Logic "0". The CONVERT COMMAND input may be returned to Logic "0" 100ns after this clock transition but may also remain at Logic "1" until 500ns before the sixth clock transition. The MSB decision process starts on the second negative-going clock edge and concludes one clock period later. The bit decisions continue at the rate of one per clock cycle until the LSB decision has finally been made. After the LSB decision, the clock returns to Logic "1" and the STATUS output returns to Logic "0"

The serial data output is of the non-return-to-zero (NRZ) type. The data is available, MSB first, at the third and subsequent positive-going clock transitions.

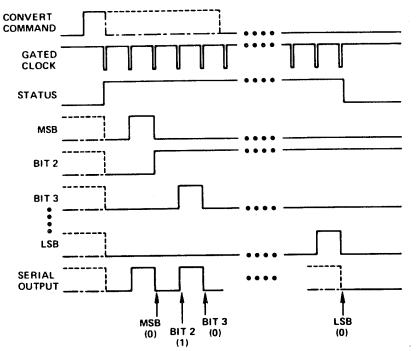
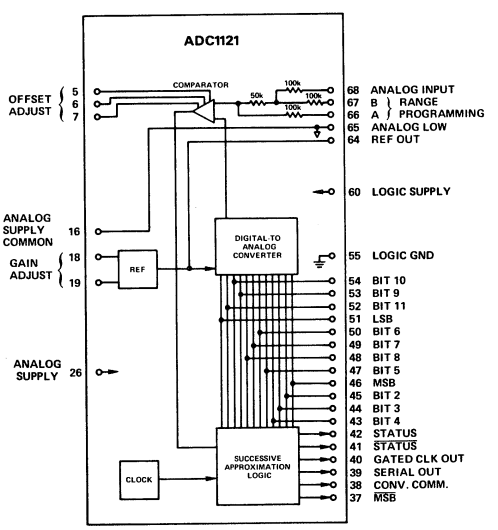


Figure 1. Timing Diagram



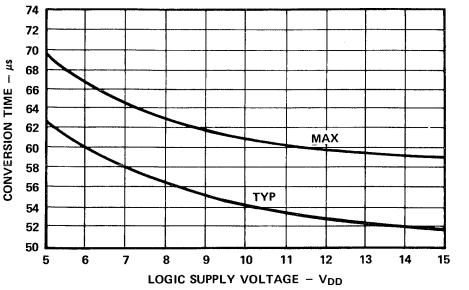
Block Diagram and Pin Designations

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

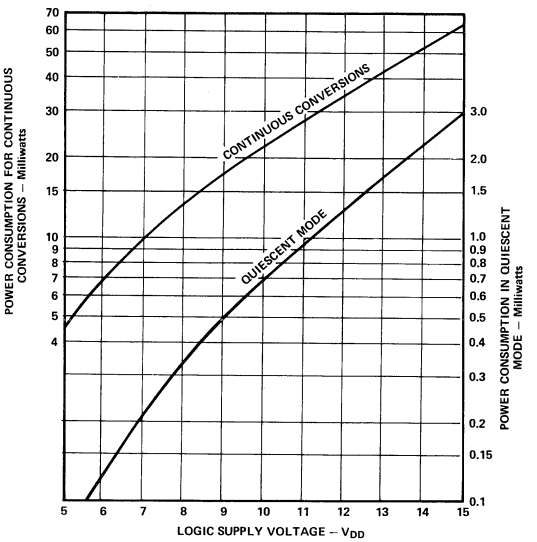
RESOLUTION	12 Bits
ACCURACY	
Error Relative to Full Scale	±½LSB max
Differential Nonlinearity Error	±½LSB max
Missing Codes	No Missing Codes from 0 to +70°C
TEMPERATURE COEFFICIENT	
Gain	±20ppm/°C of Reading, max [1]
Unipolar Zero	±8ppm/°C of Range, max[2]
Bipolar Offset	±20ppm/°C of Range, max[2]
Differential Nonlinearity	±5ppm/°C of Range, max[2]
CONVERSION TIME[3]	
+5V Logic Supply	63μs (70μs max)
+10V Logic Supply	54μs (61μs max)
+15V Logic Supply	52μs (59μs max)
INPUT VOLTAGE RANGES	0 to +5V, 0 to +10V, ±5V, ±10V
INPUT IMPEDANCE	
0 to +5V Range	400kΩ min
0 to +10V Range	144kΩ min
±5V Range	144kΩ min
±10V Range	120kΩ min
DIGITAL OUTPUTS	
Logic Levels	CMOS Compatible (see next page)
Parallel Output Codes	
Unipolar	Positive True Binary
Bipolar	Positive True Offset Binary, or Two's Complement
Serial Output Codes	
Unipolar	Positive True Binary, NRZ Format, MSB First
Bipolar	Positive True Offset Binary, NRZ Format, MSB First
Status Output	Logic "1" During Conversion
CONVERT COMMAND INPUT	
Logic Levels	CMOS Compatible (see next page)
Pulse Width	6μs min, 15μs max;
Rise and Fall Times	1μs max
POWER SUPPLY REQUIREMENTS[4]	
Analog Supply (V_S)	+12V to +15V
Logic Supply (V_{DD})	+5V to +15V
POWER CONSUMPTION	See Graphs
POWER SUPPLY SENSITIVITY[5]	
Gain	±¼LSB
Unipolar Zero	±¼LSB
Bipolar Offset	±¼LSB
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +125°C
ADJUSTMENT RANGES	
Gain	±0.2% of Range[2]
Offset	±0.2% of Range[2]

[1] Reading for bipolar operation is defined as: Actual Reading – (-Full Scale)
[2] Range for unipolar operation is defined as: + Full Scale
Range for bipolar operation is defined as: 2 (+ Full Scale)
[3] Conversion time is measured from the rising edge of the convert command pulse to the falling edge of the STATUS output. A graph showing conversion time as a function of logic supply voltage is shown on following page.
[4] Power supply current for both the analog and logic supplies is very transient in nature; peak current for both is less than 100mA.
[5] Maximum change as analog supply voltage varies from +12V to +15V.

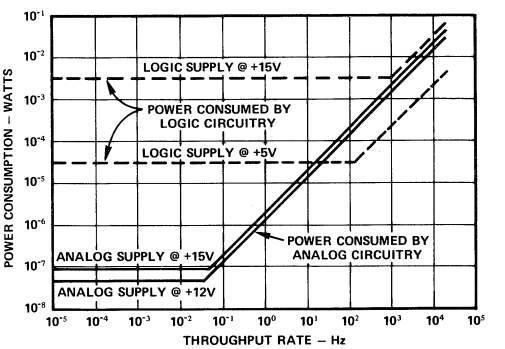
Specifications subject to change without notice.



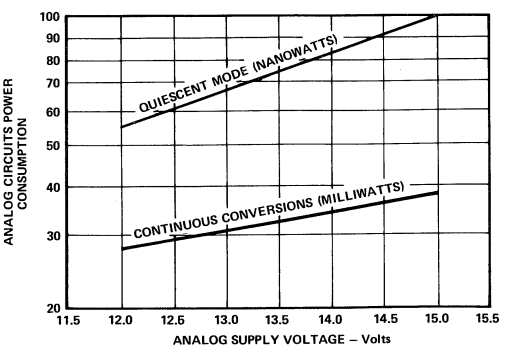
Conversion Time Vs. Logic Supply Voltage



Logic Circuits Power Consumption



Power Consumption Vs. Throughput Rate and Supply Voltages



Analog Circuits Power Consumption

ANALOG INPUT CHARACTERISTICS

The input circuit of the ADC1121 is shown below in block diagram form in Figure 2.

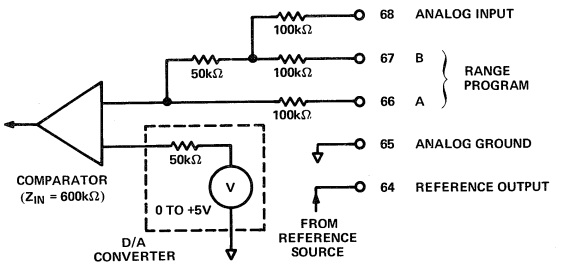


Figure 2. Analog Input Configuration

Analog signals in the range of 0 to +5V, 0 to +10V, ±5V, or ±10V are applied between pins 68 and 65. The range programming circuitry serves to offset and divide these signals as necessary to provide the comparator with a 0 to +5V input which is then compared to the 0 to +5V D/A converter output. Table I, below, shows the range programming connections required for the various input ranges and also shows the resulting input impedances.

INPUT RANGE	CONNECTIONS		INPUT IMPEDANCE
	PIN 66 TO:	PIN 67 TO:	
0 to +5V	68	68	500kΩ min
0 to +10V	65	68	180kΩ min
±5V	64	68	180kΩ min
±10V	64	65	150kΩ min

Table I. Range Programming

PARALLEL DATA OUTPUT CODING

ANALOG INPUT		DIGITAL OUTPUT
0 TO +5V RANGE	0 TO +10V RANGE	BINARY CODE
+4.9988V	+9.9976V	111111111111
+2.5000V	+5.0000V	100000000000
+0.6250V	+1.2500V	001000000000
+0.0012V	+0.0024V	000000000001
+0.0000V	+0.0000V	000000000000

Table II. Nominal Unipolar Input-Output Relationships

ANALOG INPUT		DIGITAL OUTPUT	
±5V RANGE	±10V RANGE	OFFSET BINARY CODE	TWO'S COMPLEMENT CODE
+4.9976V	+9.9951V	111111111111	011111111111
+2.5000V	+5.0000V	110000000000	010000000000
+0.0024V	+0.0049V	100000000001	000000000001
+0.0000V	+0.0000V	100000000000	000000000000
-5.0000V	-10.0000V	000000000000	100000000000

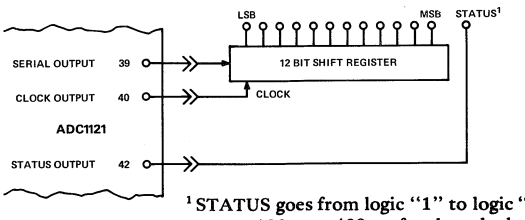
Table III. Nominal Bipolar Input-Output Relationships[1]

[1] For two's compliment code the MSB is represented by $\overline{\text{MSB}}$ on pin 37.

SERIAL DATA OUTPUTS

The serial data output, available at pin 39, is of the non-return-to-zero format. The data, which is transmitted MSB first, is binary coded for unipolar units and offset binary coded for bipolar units.

Figure 3, below, indicates one method for transmitting data serially using only three wires (plus a digital ground). The data is clocked into a receiving shift register by the positive-going transitions of the gated clock output. Since these clock transitions occur typically 250 to 550ns after each bit of serial output data becomes valid, ample time is allowed for shift register set-up.



[1] STATUS goes from logic "1" to logic "0" approx. 100ns to 400ns after last clock transition.

Figure 3. Serial Data Transmission

LOGIC LEVELS

The logic levels of the ADC1121's CMOS digital outputs are as shown below:

$V_{DD} \geqslant$ Logic "1" $\geqslant V_{DD}$ - 0.1V; where V_{DD} is the logic supply voltage.

0.1V $\geqslant$ Logic "0" $\geqslant$ 0.0V

Although TTL logic levels can be achieved by setting the logic supply voltage to +5V, the MSB through LSB output gates do not have sufficient current sink capability to drive standard TTL logic. They can, however, readily drive low power TTL such as the series 74L devices. The remaining digital outputs (STATUS, $\overline{\text{STATUS}}$, SERIAL OUT, CLOCK OUT, and $\overline{\text{MSB}}$) have a 4mA current sink capability and, thus, can be used directly with standard TTL logic.

CONVERT COMMAND, the only digital input, will respond to logic levels of:

$V_{DD} \geqslant$ Logic "1" $\geqslant 0.7\ V_{DD}$

$0.3\ V_{DD} \geqslant$ Logic "0" $\geqslant$ 0.0V

GAIN AND OFFSET ADJUSTMENTS

The potentiometers used for making gain and offset adjustments are connected as shown in Figure 4. These potentiometers should be small 10 or 20 turn cermet type devices mounted as close to the module pins as possible.

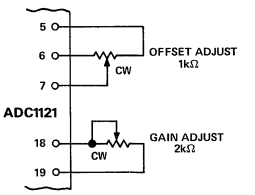


Figure 4. Adjustment Potentiometer Connections

OFFSET CALIBRATION

For 0 to +5V units set the input voltage precisely to +0.0006V; for 0 to +10V units set it to +0.0012V. Adjust the offset potentiometer until the converter is just on the verge of switching from 000000000000 to 000000000001.

For ±5V units set the input voltage precisely to +0.0012V; for ±10V units set it to +0.0024V. Adjust the offset potentiometer until offset binary coded units are just on the verge of switching from 100000000000 to 100000000001 and two's complement coded units are just on the verge of switching from 000000000000 to 000000000001.

GAIN CALIBRATION

Set the input voltage precisely to +4.9982V for 0 to +5V units, to +9.9963V for 0 to +10V units, to +4.9963V for ±5V units, or to +9.9927V for ±10V units. Note that these values are 1½LSB's less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 111111111110 to 111111111111 and two's complement coded units are just on the verge of switching from 011111111110 to 011111111111.

REPETITIVE CONVERSIONS

When making repetitive conversions, a new convert command pulse may be initiated any time after the "1" to "0" transition of the STATUS output. If the $\overline{\text{STATUS}}$ output is connected to the CONVERT COMMAND input, a new conversion will automatically begin as soon as the conversion in progress has been completed. The $\overline{\text{STATUS}}$ line will remain in the Logic "1" state for approximately 4μs between conversions in this mode of operation.

POWER SUPPLY AND GROUNDING CONNECTIONS

The ADC1121 has independent analog and logic supply inputs which may be powered from a single source or from separate sources. Figures 5 and 6, below, show the proper connections for both cases. The analog supply ground, pin 16, and the digital supply ground, pin 55, are not connected internally but should be jumpered together close to the module pins. Although the analog supply ground and analog signal ground, pin 65, are joined inside the module, pin 65 should never be used as a power supply return. Due to the transient nature of the supply currents encountered in a device of this type, it is recommended that 15μF, 35V tantalum bypass capacitors be added across the analog and digital supplies at a location close to the module pins.

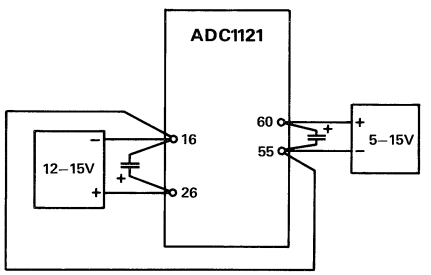


Figure 5. Two Source Connection

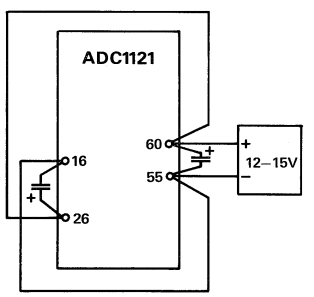


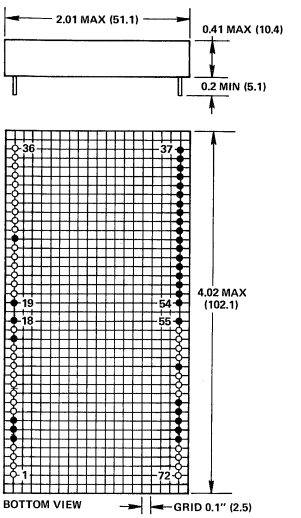
Figure 6. Single Source Connection

HANDLING CONSIDERATIONS

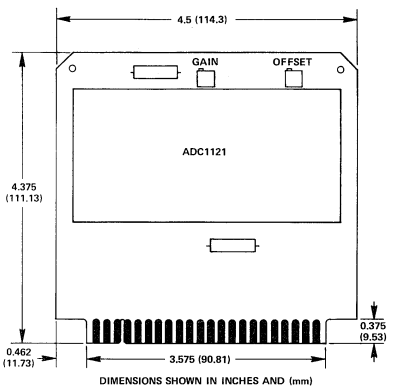
Care must be taken in the handling of the ADC1121 to prevent electrostatic damage to its CMOS logic. The unit should be transported on conductive foam or other suitable material and should be handled only by properly grounded personnel. Ground connections must be made before power is applied. Electrostatic damage, should it occur, would be manifested by excessive logic current drain and/or complete failure of one or more logic IC's.

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

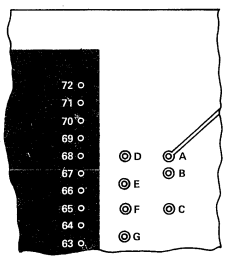
Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
All pins are gold plated half-hard brass (MIL-G-45204), 0.019" ±0.001" (0.48 ±0.03mm) dia.
For plug-in mounting card order Board No. AC1521



AC1521 Outline Drawing



INPUT VOLTAGE RANGE	JUMPER CONNECTIONS
0 to +5V	E-D, B-A
0 to +10V	E-F, B-A
±5V	E-G, B-A
±10V	E-G, B-C

AC1521 Range Programming

PIN	FUNCTION	PIN	FUNCTION
A	MSB	1	$\overline{\text{MSB}}$
B	Bit 2	2	Convert Command
C	Bit 3	3	Serial Output
D	Bit 4	4	Gated Clock Out
E	Bit 5	5	$\overline{\text{Status}}$
F	Bit 6	6	Status
H	Bit 7	7	
J	Bit 8	8	
K	Bit 9	9	N.C.
L	Bit 10	10	
M	Bit 11	11	
N	LSB	12	Logic Supply
P	Logic Ground	13	N.C.
R	N.C.	14	Analog Supp. Comm.
S	+ Analog Supply	15	
T		16	
U		17	
V		18	N.C.
W	N.C.	19	
X		20	
Y		21	
Z	Analog Low	22	Analog Input

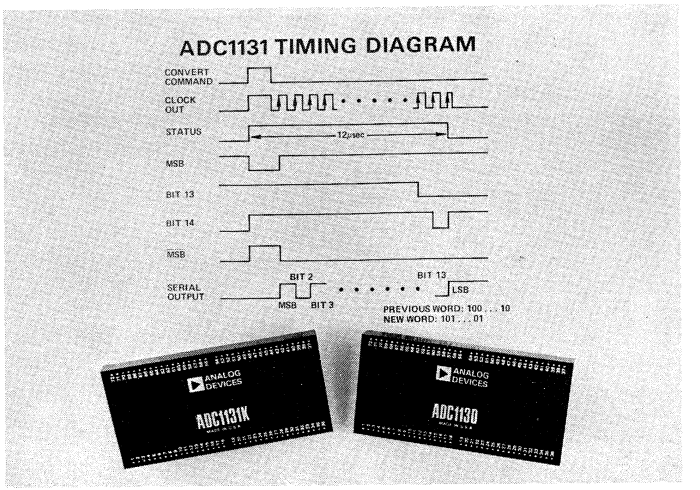
Table IV. AC1521 Pin Designations

14 Bit High Speed Analog to Digital Converters

ADC1130, ADC1131

FEATURES
14 Bit Resolution and Accuracy
Fast 12μs Conversion Time (ADC1131J/K)
Low 10ppm/°C Maximum Gain TC
User Choice of Input Range
No Missing Codes

APPLICATIONS
Wide Band Data Digitizing
Multi-Channel Computer Interface
High Accuracy Data Acquisition
X-Ray Tomography
Nuclear Accelerator Instrumentation



GENERAL DESCRIPTION

The ADC1130 and ADC1131 are high speed analog-to-digital converters packaged in a small 2" x 4" x 0.4" (51 x 102 x 10mm) module, which perform complete 14 bit conversions in 25μs and 12μs respectively. Using the successive approximations technique, they convert analog input voltages into natural binary, offset binary, or two's complement coded outputs. Data outputs are provided in both parallel and non-return-to-zero serial form.

Four analog input ranges are available: 0 to +20V, 0 to +10V, ±10V, ±5V. The user selects the desired range by making appropriate connections to the module terminals. The ADC1130 and ADC1131 can also be connected so as to perform conversions of less than 14 bit resolution with a proportionate decrease in conversion time.

TIMING

As shown in Figure 1, the leading edge of the convert command set the MSB output to Logic "0" and the CLOCK OUT, STATUS, $\overline{\text{MSB}}$, and BIT 2 through BIT 12 outputs to Logic "1". Nothing further happens until the convert command returns to Logic "0", at which time the clock starts to run and the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-to-analog converter's output is compared with the analog input. If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB to Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic "0" and another comparison is made. This process continues through each successive bit until the BIT 14 (LSB) comparison is completed. At this point the STATUS and CLOCK OUT return to Logic "0" and the conversion cycle ends.

The serial data output is of the non-return-to-zero (NRZ) format. The data is available, MSB first, 20ns after each of the fourteen "0" to "1" clock transitions.

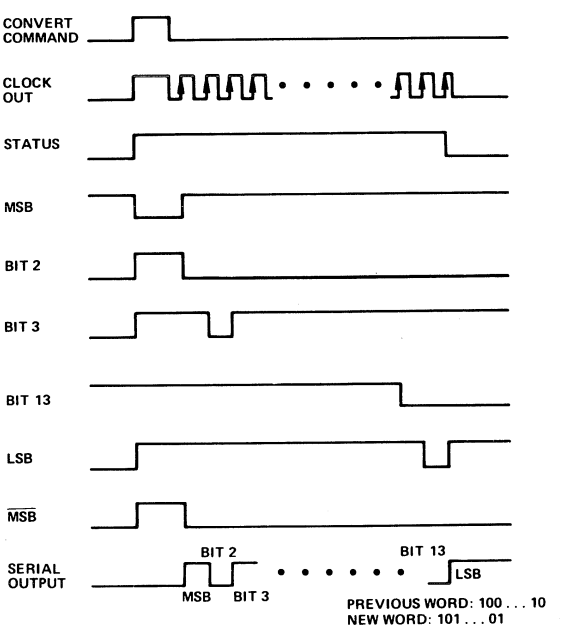


Figure 1. Timing Diagram

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODEL	HIGH SPEED 12μs ADC1131 J	K	MEDIUM SPEED 25μs ADC1130
RESOLUTION, BITS	14	14	14
CONVERSION TIME (max)	12μs	12μs	25μs
ACCURACY			
Integral Nonlinearity Error (LSB)	±1/2 (max)	*	*
Differential Nonlinearity Error (LSB)	±1/2 (1 max)	±1/2 (max)	±1/2 (1 max)
Missing Codes	No missing codes	*	*
TEMPERATURE COEFFICIENTS			
Gain ppm/°C	±12 (max)	±7 (+10 max)	±12 max
Unipolar Offset	±0.7 (±3 max)	*	*
Bipolar Offset	±3 (±7 max)	*	*
INPUT VOLTAGE RANGES	±5V, ±10V, +10V, +20V	*	*
INPUT IMPEDANCE (10V RANGE)	2500Ω	*	*
CONVERT COMMAND	Positive Pulse, 200ns min, 400ns max Leading Edge Resets, Trailing Edge Starts, TTL/DTL Compatible	*	*
PARALLEL DATA OUTPUT			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary, Two's Complement	*	*
SERIAL DATA OUTPUT			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary	*	*
STATUS OUTPUT	"1" During Conversion. Complement also available TTL/DTL Compatible.	*	*
LOGIC FANOUTS AND LOADINGS			
Convert Command Input	1TTL Unit Load	*	*
Clock Input	3TTL Unit Loads	*	*
Short Cycle Input	1TTL Unit Load	*	*
Parallel Data Outputs	3TTL Unit Loads/Bit	*	*
Serial Data Output	8TTL Unit Loads	*	*
STATUS Output	2TTL Unit Loads	*	*
$\overline{\text{STATUS}}$ Output	12TTL Unit Loads	*	*
Clock Output	4TTL Unit Loads	*	*
POWER REQUIREMENTS	+15V ±5% @ 40mA	*	*
	-15V ±5% @ 60mA	*	*
	+5V ±5% @ 250mA	*	*
POWER SUPPLY SENSITIVITY			
To ±15V Tracking Supplies			
Gain	±4.5ppm/%Δ V_S	*	*
Zero	±4.5ppm/%Δ V_S	*	*
To ±15V Non-Tracking Supplies			
Gain	±10ppm/%Δ V_S	*	*
Zero	±7ppm/%Δ V_S	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C	*	*
Storage	-55°C to +85°C	*	*

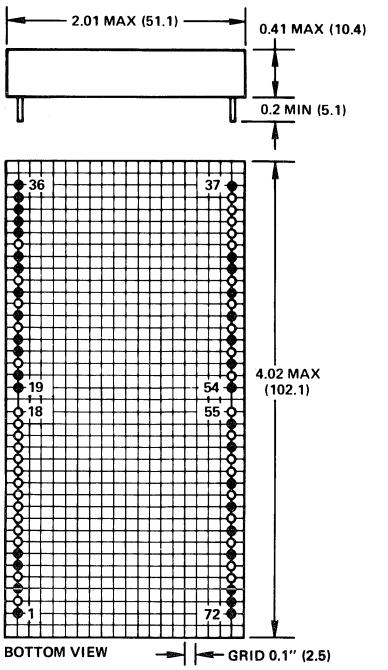
*Same Specifications as ADC1131J.

NOTES:
[1] Offset (zero) and gain errors are adjustable to zero by means of external potentiometers. See Figure 5 for proper connection.
[2] Recommended power supply: Analog Devices model 902 and model 906.

Specifications subject to change without notice.

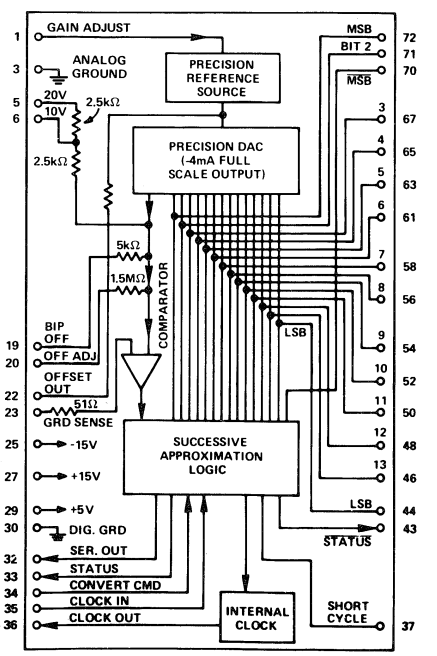
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
Module weight: 3.5 ounces (99.3 grams).
All pins are gold plated half-hard brass (MIL–G–45204), 0.019" ±0.001" (0.48 ±0.03mm) dia.

BLOCK DIAGRAM AND PIN DESIGNATIONS



ANALOG INPUT CHARACTERISTICS

The input circuit of the ADC1130 and ADC1131 are shown in block diagram form.

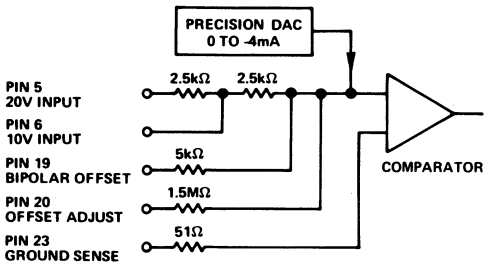


Figure 2. Input Circuit Block Diagram

When the converters are connected as a unipolar device, Pin 19 is left open circuit and, thus, no offset current is applied to the comparator input. The 0 to +10V input signal applied to Pin 6 (or the 0 to +20V input signal applied to Pin 5) develops a 0 to +4mA current which is compared to the 0 to -4mA output of the D/A converter. A voltage between +15V and -15V can be applied to Pin 20 from the wiper of a 100kΩ potentiometer to adjust the zero point by ±40LSB. To reduce the range of this trim padding resistors should be used.

With the offset output, Pin 22, connected to Pin 19, a +2mA offset current is applied to the comparator input. The ADC1130 and ADC1131 will then accept bipolar inputs of ±5V at Pin 6, or ±10V at Pin 5 and compare the 0 to +4mA sum of the offset and input signal currents to the 0 to -4mA D/A converter output. The offset adjustment potentiometer is once again used as described in the preceding paragraph.

Signal ground sense, Pin 23, should normally be jumpered to analog ground, Pin 3. In the event that an offset voltage is developed in the ground wiring, it may be possible to eliminate its effect by connecting Pin 23 directly to the signal or analog ground of the device feeding the analog input signal to the ADC. In any case, Pin 23 must not be left open.

If a high input impedance is required, it can be achieved by using a high speed operational amplifier as an input buffer.

PARALLEL DATA OUTPUT

These converters produce natural Binary Coded outputs when configured as a unipolar device. As a bipolar device, they can produce either Offset Binary or Two's Complement output codes. The most significant bit is represented by Pin 72 (MSB output) for Binary and Offset Binary codes, or by Pin 70 ($\overline{\text{MSB}}$ output) for the Two's Complement code. Tables I and II illustrate the relationship between analog input and digital output for all three codes.

ANALOG INPUT		DIGITAL OUTPUT
0 to +10V Range	0 to +20V Range	Binary Code
+9.9994V	+19.9988V	11111111111111
+5.0000V	+10.0000V	10000000000000
+1.2500V	+2.5000V	00100000000000
+0.0006V	+0.0012V	00000000000001
+0.0000V	+0.0000V	00000000000000

Table 1. Nominal Unipolar Input-Output Relationships

±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.9994V	+9.9988V	11111111111111	01111111111111
+2.5000V	+5.0000V	11000000000000	01000000000000
+0.0006V	+0.0012V	10000000000001	00000000000001
+0.0000V	+0.0000V	10000000000000	00000000000000
-5.0000V	-10.0000V	00000000000000	10000000000000

Table 2. Nominal Bipolar Input-Output Relationships

SERIAL DATA OUTPUT

The serial data output, available on Pin 32, is of the non-return-to-zero format. The data is transmitted MSB first and is Binary coded for unipolar units and Offset Binary coded for bipolar units.

Figure 3, shown below, indicates one method for transmitting data serially using only three wires (plus a digital ground). The data is clocked into a receiving shift register using the delayed clock output of the converter.

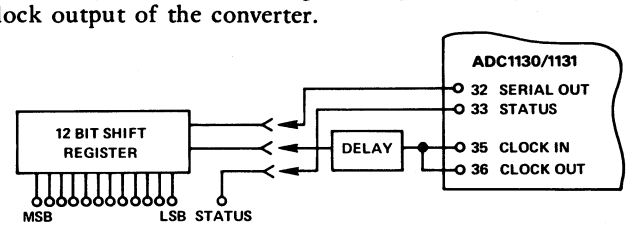


Figure 3. Serial Data Transmission

The timing diagram presented in Figure 4 shows that the converter's clock output must be delayed by an amount of time greater than or equal to the sum of the receiving shift register setup time plus the 20ns clock output to serial output delay.

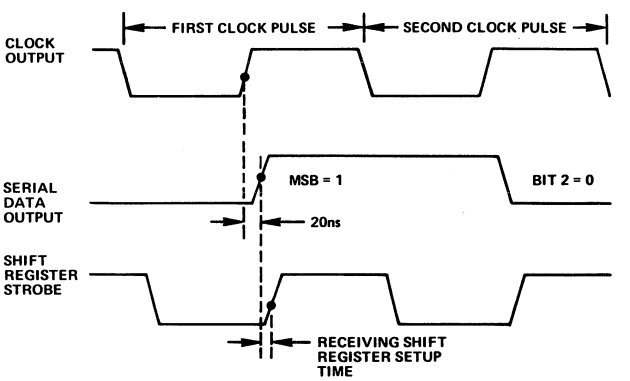


Figure 4. Serial Data Timing Diagram

The 50ns span between the time that the last serial output bit is available and the time that the STATUS output returns to zero insures that the data in the shift register will be valid on the "1" to "0" transition of the STATUS signal.

GAIN AND OFFSET ADJUSTMENTS

The potentiometers used for making gain and offset adjustments are connected as shown in Figure 5. Note that a jumper

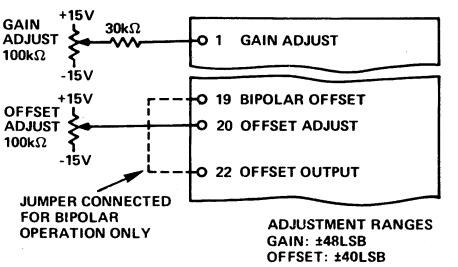


Figure 5. Adjustment Connections

is connected between Pin 19 and Pin 22 for bipolar operation; these pins *must* be left open for unipolar operation.

Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable. It should be capable of being set to within 1μV of the desired value at both ends of its range.

The gain and offset calibrations will be independent of each other if the offset adjustment is made first. These adjustments are not made with zero and full scale input signals and it may be helpful to understand why. An A/D converter will produce a given digital output for a small range of input signals, the nominal width of the range being one LSB. If the input test signal is set to a value which should cause the output of the converter to be on the verge of switching from one digital value to the adjacent digital value, the unit can be calibrated so that it does change values at just that point. With a high speed convert command rate and a visual display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices' *Analog-Digital Conversion Notes* gives more detailed information on testing and calibrating A/D and D/A converters.

OFFSET CALIBRATION

For the 0 to +10V unipolar range set the input voltage precisely to +0.0003V; for 0 to +20V units set it to +0.0006V. Adjust the zero potentiometer until the converter is just on the verge of switching from 00 . . . . 0 to 00 . . . . 1.

For the ±5V bipolar range set the input voltage precisely to -4.9997V; for ±10V units set it to -9.9994V. Adjust the zero potentiometer until offset binary coded units are just on the verge of switching from 00 . . . . 0 to 00 . . . . 1 and two's complement coded units are just on the verge of switching from 100 . . . 0 to 100 . . . 1.

GAIN CALIBRATION

Set the input voltage precisely to +19.9982V for 0 to +20V units, +9.9991V for 0 to +10V units, +4.9991V for ±5V units, or +9.9982V for ±10V units. Note that these values are 1½LSB's less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11 . . . 0 to 11 . . . 1 and two's complement coded units are just on the verge of switching from 011 . . . 10 to 011 . . . 11.

POWER SUPPLY AND GROUNDING CONNECTIONS

These converters do not have an internal connection between analog power ground and digital ground and, thus, a connection must be provided in the external circuitry. The choice of an optimum "star" point for these grounds is an important consideration in the performance of the system. No strict rules can be given, only the general guidelines that the grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. One suggested approach is shown in Figure 6.

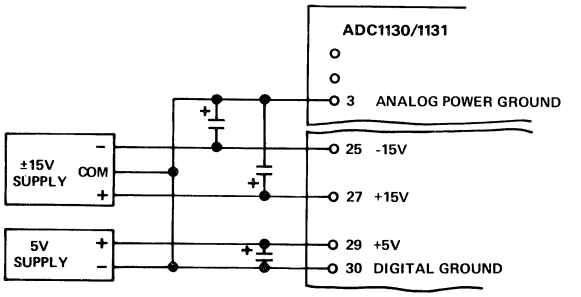


Figure 6. Power Supply and Grounding Connections

The ±15V and +5V power supplies must be externally bypassed with 15μF (+35V tantalum) capacitors. These capacitors should be connected between Pin 27 and Pin 3, between Pin 25 and Pin 3, and between Pin 29 and Pin 30. Capacitor connections should be made as close to the module pins as possible.

CLOCK CONNECTIONS

When the converters are used with their own internal clock, Pin 36 is simply jumpered to Pin 35. When the internal clock is not used, Pin 36 is grounded and an external clock capable of driving three TTL loads is connected to Pin 35. The convert command should be synchronized with the external clock.

REPETITIVE CONVERSIONS

When making repetitive conversions, a new convert command may be initiated any time after the "1" to "0" transition of the STATUS output. The STATUS output may not, however, be connected directly to the CONVERT COMMAND input for the purpose of automatically generating convert command pulses.

SHORT CYCLE CONNECTIONS

When the converters are operated as a 14 bit device, Pin 37 is left open. If, however, it is to perform conversions of less than 14 bits, Pin 37 is connected to the N + 1 bit output (where N is the number of bits in the conversion). The conversion time in this mode of operation is T_C x N/14 where T_C is the conversion time of the particular model when operated at 14 bit resolution.

High Performance Analog to Digital Converter

ADC1133

FEATURES
12 Bit Resolution
Very Small Module Package
No Missing Codes: 0 to +70°C
25μs Conversion Time
Programmable Input Ranges

GENERAL DESCRIPTION

The ADC1133 is a high performance, 12-bit A/D converter packaged in an exceptionally compact 2" x 2" x 0.4" (51 x 51 x 10mm) module. Using the successive approximations technique, it performs complete conversions in less than 25μs. Performance specifications include ±7.5ppm/°C gain temperature coefficient, ±½LSB linearity error and no missing codes from 0 to +70°C.

The ADC1133 combines the AD562 integrated circuit D/A with a precision reference source, a high speed comparator, and successive approximations logic to form a complete converter package. The laser trimmed AD562, which consists of precision current switches and a very stable thin film resistor network, provides the ADC1133 with very good performance over temperature and makes possible its small module size.

TIMING

As shown in Figure 1, the "0" to "1" transition of the CONVERT COMMAND input sets the MSB output to Logic "0" and the CLOCK, STATUS, $\overline{\text{MSB}}$, and BIT 2 through BIT 12 outputs to Logic "1". Nothing further happens until the CONVERT COMMAND returns to Logic "0", at which time the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-to-analog converter's output is compared with the analog input. If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic "0" and another comparison is made. This process continues through each successive bit until the BIT 12 (LSB) comparison is completed. At this time the STATUS output returns to Logic "0" and the conversion cycle ends.

The SERIAL DATA output is of the non-return-to-zero (NRZ) type. The data is available, MSB first, 40ns after each of the twelve "0" to "1" clock transitions.

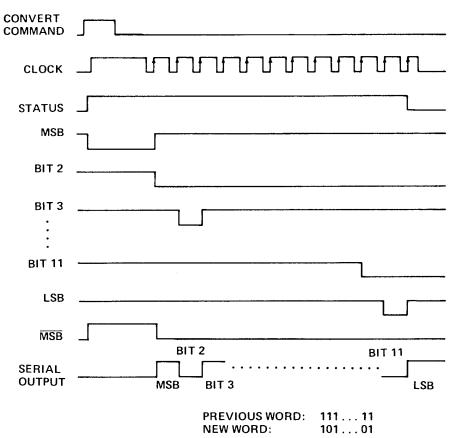
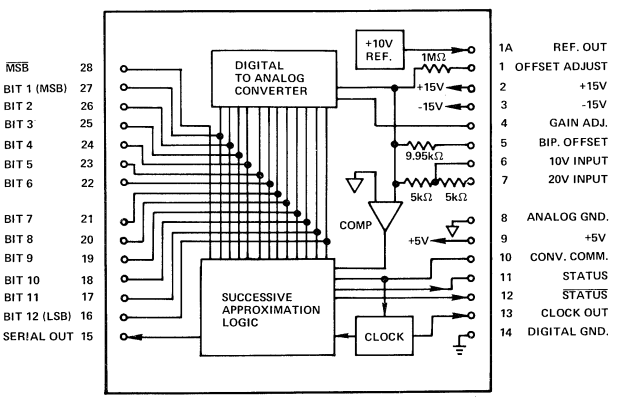


Figure 1. Timing Diagram

BLOCK DIAGRAM AND PIN DESIGNATIONS



SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

RESOLUTION	12 Bits
CONVERSION TIME[1]	25μs max
ACCURACY[2]	
Error Relative to Full Scale	±½LSB max
Quantization Error	±½LSB max
Differential Nonlinearity Error	±½LSB (±1LSB max)
TEMPERATURE COEFFICIENTS	
Gain	±7.5ppm/°C (±15ppm/°C max)
Offset (Unipolar Inputs)	±25μV/°C (±40μV/°C max)
Offset (Bipolar Inputs)	±25μV/°C (±40μV/°C max)
Differential Nonlinearity	±2.8ppm/°C (±3ppm/°C max)
Missing Codes	No Missing Codes 0 to +70°C
INPUT VOLTAGE RANGES	±5V, ±10V, 0 to +10V
INPUT IMPEDANCE	
±5V, 0 to +10V Range	5kΩ
±10V Range	10kΩ
CONVERT COMMAND	Positive Pulse, TTL Compatible 100ns min width
PARALLEL DATA OUTPUT	
Unipolar Inputs	Positive True Binary
Bipolar Inputs	Positive True Offset Binary or Two's Complement
SERIAL DATA OUTPUT	
Unipolar Inputs	Positive True Binary
Bipolar Inputs	Positive True Offset Binary, TTL Compatible, NRZ Format, MSB First
STATUS OUTPUT	Logic "1" During Conversion TTL Compatible
CLOCK OUTPUT	480kHz, TTL Compatible
LOGIC FANOUTS AND LOADING	
Convert Command	1TTL Load
Parallel Data Outputs	6TTL Loads/Bit
Status Output	4TTL Loads
Status Output	10TTL Loads
Serial Data Output	6TTL Loads
Clock Output	9TTL Loads
ADJUSTMENT RANGES	
Gain	±5LSB min
Offset	±10LSB min
POWER REQUIREMENTS	+5V dc ±5% @ 120mA (160mA max) +15V dc ±3% @ 15mA (20mA max) -15V dc ±3% @ 25mA (30mA max)
POWER SUPPLY SENSITIVITY[3]	
Gain	±1.5mV/V
Offset	±1.5mV/V
Reference	±0.5mV/V
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +85°C

[1] Conversion time is measured from the trailing edge of the convert command to the "1" to "0" transition of the status output.

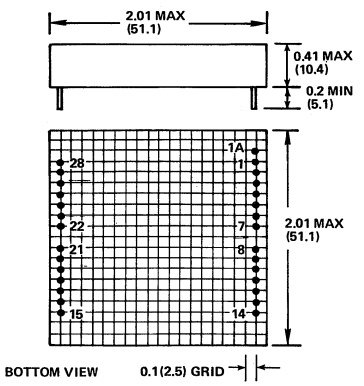
[2] Warmup time to rated accuracy is 5 minutes.

[3] Specification applies only when tracking +15V and -15V supplies are used, and for slowly occuring variations in power supply voltages.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Pins are half hard brass, gold plated per MIL–G-45204B, Class I, Type II.
Pin Diameter is 0.019" (0.483mm) ±0.001" (0.025mm).
For plug-in mounting card, order Board No. AC1505

MODULE CONNECTIONS

Figure 2 shows the connections required to operate the ADC1133 with a ±10V input range (except for connections to the bit and STATUS digital outputs, which are obvious).

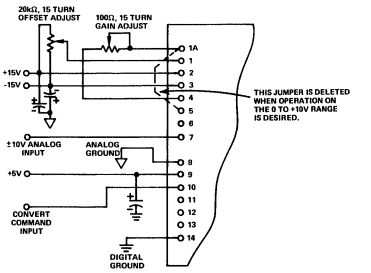


Figure 2. Module Connections

The ADC1133 can be operated with an input range of ±5V by connecting the analog input to pin 6 instead of pin 7. Operation on the 0 to +10V range is achieved by deleting the jumper between pins 1A and 5, and connecting the analog input to pin 6.

PARALLEL DATA OUTPUT CODING

ANALOG INPUT	DIGITAL OUTPUT
	BINARY CODE
+9.9976V	111111111111
+5.0000V	100000000000
+1.2500V	001000000000
+0.0024V	000000000001
+0.0000V	000000000000

Table I. Nominal Unipolar Input-Output Relationships

ANALOG INPUT		DIGITAL OUTPUT	
±5V RANGE	±10V RANGE	OFFSET BINARY CODE	TWO'S COMPLEMENT CODE
+4.9976V	+9.9951V	111111111111	011111111111
+2.5000V	+5.0000V	110000000000	010000000000
+0.0024V	+0.0049V	100000000001	000000000001
+0.0000V	+0.0000V	100000000000	000000000000
-5.0000V	-10.0000V	000000000000	100000000000

Table II. Nominal Bipolar Input-Output Relationships

OFFSET CALIBRATION

For unipolar units set the input voltage precisely to +0.0012V and adjust the offset potentiometer until the converter is just on the verge of switching from 000000000000 to 000000000001.

For ±5V bipolar units set the input voltage precisely to -4.9988V; for ±10V units set it to -9.9976V. Adjust the offset potentiometer until Offset Binary coded units are just on the verge of switching from 000000000000 to 000000000001 and Two's Complement coded units are just on the verge of switching 100000000000 to 100000000001.

GAIN CALIBRATION

Set the input voltage precisely to +9.9963V for unipolar units, +4.9963V for ±5V units, or +9.9926V for ±10V units. Note that these values are 1½LSB's less than nominal full scale. Adjust the 100Ω variable gain resistor until Binary and Offset Binary coded units are just on the verge of switching from 111111111110 to 111111111111 and Two's Complement coded units are just on the verge of switching from 011111111110 to 011111111111.

Dual Slope Integrating ADC

ADC-141/171

FEATURES
- Excellent Stability
- 14 Binary Bits Plus Sign
- 4½BCD Digits Plus Sign
- 0.01% Accuracy
- Automatic Error Correction
- High Noise Rejection

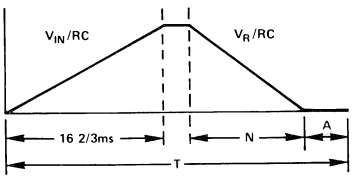
APPLICATIONS
- Weighing Systems
- Analytical Ratiometric Measurements
- Bio-Medical/Oceanographic Data Transmission, Reduction and Display
- Process Control Instrumentation

GENERAL DESCRIPTION

The ADC-I is the first high resolution analog-to-digital converter using a dual-slope integrating technique to be contained in a 3″ x 4″ x 0.4″ module. Two models offer a choice of either a 14-bit binary word output or a 4½ digit BCD output. Both models provide polarity and automatic overload outputs. Designed for applications where noise immunity is a critical requirement, the ADC-I features 0.01% accuracy, excellent temperature stability, automatic zero correction, and low cost.

INTEGRATING TECHNIQUE

Operation of the ADC-I is based on the time relationship between two integration intervals (see Figure 1). Upon convert command the analog input is integrated. After a known time interval, the polarity of the integrated input is determined. The counter is reset to zero and with a reference applied to the integrator, clock pulses are counted until a comparator detects a zero output. The counter then provides a digital representation of the analog input.



WHERE: V_{IN} = ANALOG INPUT
V_R = REFERENCE VOLTAGE
N = COUNT REPRESENTS ANALOG INPUT
A = AUTOMATIC ZERO COMPENSATION PERIOD

Figure 1. Simplified Timing Diagram

Internal control logic provides a polarity indication as the reference integration begins. An overload output occurs if the reference integration requires a longer time interval than the input integration.

Following the conversion cycle or after an overload is detected the integrator is automatically zeroed and ready for another conversion.

ADVANTAGES OF DUAL-SLOPE

In the successive approximation converter, where high speed is offered the major limitation is resolution and accuracy due to noise interference. In contrast to this approach, integrating

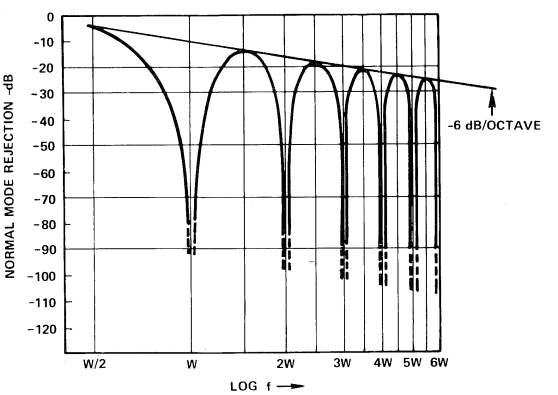


Figure 2. Normal Mode Rejection

SPECIFICATIONS (typical @ +25°C and rated supply unless otherwise noted)

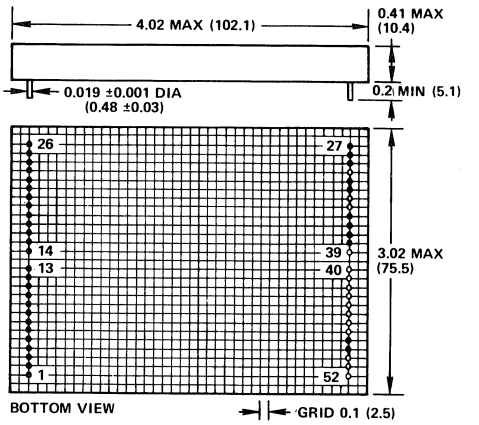
RESOLUTION	
ADC-14I	14 Binary Bits plus sign
ADC-17I	4½BCD digits plus sign
ACCURACY	
Relative	Adjustable to 0.01% of reading ±1 Bit
Calibration	Recommended 6 months calibration cycle
Monotonicity	Guaranteed
INPUT CHARACTERISTICS	
Analog Input	±10V FS (20% overrange on ADC-17I)
Continuous Overload	±100V max (with or without power)
Peak Series Mode	±75V max dynamic range
Series Mode Rejection	-70dB
Input Impedance	180kΩ
REFERENCE VOLTAGES	
Internal	±6.2V ±5%, balanced to 0.01%
	±2mA current drain
	<1Ω output impedance
External	±7.5V max for ratiometric operation
	100kΩ input impedance
TEMPERATURE COEFFICIENT	
Zero	±10μV/°C (0 to +40°C)
	±30μV/°C (+40°C to +70°C)
Gain	±5ppm of reading/°C (exclusive of ref.)
Reference	
Positive Reference	5ppm/°C
Negative Reference	10ppm/°C
CONVERSION TIME	40ms max (see Table 1)
Input Integration	16-2/3ms (see Table 1)
Sample Rate	25/sec (see Table 1)
CONVERT COMMAND	Positive pulse, 100ns min, 100μs max
(TTL/DTL Compatible)	Leading edge resets previous data
	Trailing edge initiates conversion
CLOCK (TTL/DTL Compatible)	
Internal	720kHz (see Table 1)
Stability	200ppm/°C
External	1.2MHz max
Input Fan In	1 TTL load
OUTPUTS (TTL/DTL Compatible)	
Parallel Data	
Sign Plus Magnitude BCD	10.000V FS (11.999 with overrange)
Sign Plus Magnitude BIN	10V—LSB FS (MSB included)
Polarity (Fan Out 8)	Logic "0" indicates positive input
(Fan Out 2)	Logic "1" indicates negative input
$\overline{\text{Status}}$ (Fan Out 9)	Logic "0" during conversion
$\overline{\text{Ramp Up}}$ (Fan Out 2)	Logic "0" during ramp up
$\overline{\text{Ramp Down}}$ (Fan Out 2)	Logic "0" during ramp down
Overload (Fan Out 10)[1]	Logic "1" after conversion indicates overload
POWER SUPPLY REQUIREMENTS[2]	±15V dc @ 30mA
	+5V dc @ 200mA
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55°C to +125°C
ADJUSTMENTS	
Zero	Automatic Internal Compensation
Gain	(3) 200Ω Trim Pots
	See Adjustment Procedures
DIMENSIONS	3" x 4" x 0.4"

[1] Overload is Logic "1" during conversion. At the end of a normal (non-overload) conversion, i.e., when Status goes high "overload" goes to Logic "0". Overload remains Logic "1" at the end of an overload conversion.
[2] Recommended Power Supply: Analog Devices models 904 and 903.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

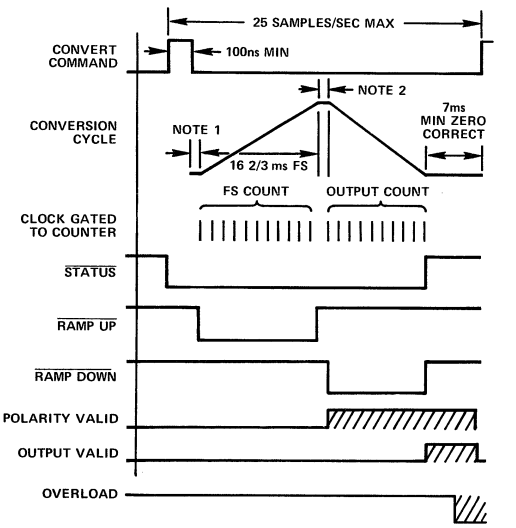
Dimensions are shown in inches and (mm).

ADC-17I



NOTE: On the ADC-14I;
Pins 6, 7 and 8 are omitted.
Bits 3 through 14 are located at pins 9 through 20, respectively.

TIMING DIAGRAM



[1] Maximum delay of one clock pulse to synchronize with clock.
[2] Delay of 1½ clock pulses to reset counter and strobe comparator for polarity data.

ORDERING GUIDE:

ADC – XX I

- 14 - 14 Binary Bits plus sign
- 17 - 4½BCD digits plus sign

the input sacrifices conversion speed but achieves high resolution due to the excellent noise rejection. The ADC-I integrates the analog input for exactly one ac line period – clearly the most prevalent source of noise error. Adjustment of this interval is possible by changing the clock frequency or through use of an external clock. This allows the user to obtain optimum noise rejection operating with a 60Hz or a 50Hz line frequency.

In addition to its ability to maintain resolution in the presence of noise the dual-slope technique offers excellent temperature performance. This is possible since errors due to drift in the integrator time constant or clock affect both integrations and are therefore cancelled. This reduces output error source almost solely to the accuracy of the reference voltages, allowing long term adjustment free operation.

GROUND CONNECTIONS

Analog ground and power ground are NOT internally connected and must be connected externally. Difference in potential must be <0.1V at the module.

CLOCK OPERATION

An external clock may be connected directly to pin 24. The continuous running internal clock may be used by connecting pins 24 and 25. The internal clock frequency for binary and BCD models differs to maintain an input integration period of approximately 16-2/3ms. Optimum line noise rejection is achieved by adjustment of this frequency with an

Line Frequency	60Hz	50Hz
Clock Frequency		
ADC-14I	983kHz	819.2kHz
ADC-17I	720kHz	600kHz
Ramp Up Period	16-2/3ms	20ms
Conversion Time	40ms max	50ms max
Max Sample Rate	25/sec	20/sec

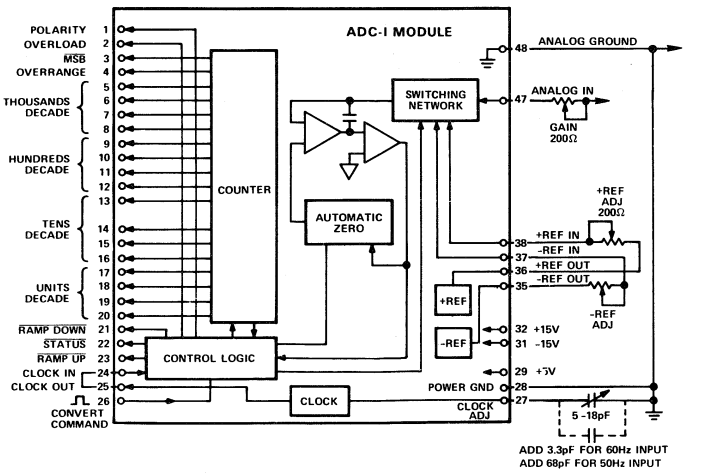
Table 1. Optimum Clock Frequencies

external trimmer capacitor between pins 27 and 28. A 68pF capacitor in parallel with the trimmer allows adjustment for 50Hz line operation. The adjustment can be made with a frequency counter or by measuring the $\overline{\text{RAMP UP}}$ period at pin 23. The latter method requires a convert command signal.

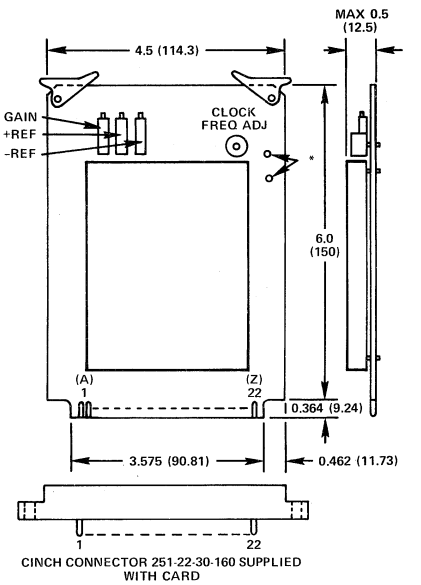
ACCURACY ADJUSTMENTS

Zero correction is automatically made after every conversion as indicated in the timing diagram. Trim pots shown in the block diagram allow for adjustment of gain. The reference adjustments are used to balance positive and negative outputs fro a known input. Future gain adjustment can then be made with the single pot in series with the analog input without affect on the polarity balance. With the gain pot set to center position the recommended procedure is to adjust the -REF with +8.7500V input, reverse the polarity of the input and adjust the +REF. The ideal outputs are:

ADC-14I	(BIN)	11100 0
ADC-17I	(BCD)	8750



Block Diagram and Pin Designations



*Provision is made for addition of 33pF capacitor for 50Hz input. Mounting board complete with trim pots and clock adjustment. Model AC1500

ADC-17I			
Analog Input	1	A	Analog Ground
Analog Ground	2	B	Analog Ground
+Ref In	3	C	+Ref Out
-Ref In	4	D	-Ref Out
Power Ground	5	E	Power Ground
Polarity	6	F	MSB Bit 1
Overload	7	H	Bit 2
$\overline{\text{MSB Bit 1}}$	8	J	Bit 3
N.C.	9	K	Bit 4 (N.C.)
N.C.	10	L	Bit 5
N.C.	11	M	Bit 6 (Bit 3)
$\overline{\text{Ramp Down}}$	12	N	Bit 7 (Bit 4)
$\overline{\text{Status}}$	13	P	Bit 8 (Bit 5)
$\overline{\text{Ramp Up}}$	14	R	Bit 9 (Bit 6)
Clock In	15	S	Bit 10 (Bit 7)
Clock Out	16	T	Bit 11 (Bit 8)
Convert Command	17	U	Bit 12 (Bit 9)
N.C.	18	V	Bit 13 (Bit10)
+15V	19	W	Bit 14 (Bit11)
-15V	20	X	Bit 15 (Bit12)
N.C.	21	Y	Bit 16 (Bit13)
+5V	22	Z	LSB Bit 17 (Bit 14)

NOTE: Changes for ADC-14I shown in parenthesis.

#AC1500 Mounting Board and Pin Connections. Dimensions shown in inches and (mm).

RATIOMETRIC OPERATION

The ADC-I is ideally suited for ratiometric measurement analytical instrumentation, strain gages, or resistance bridges. This is easily implemented since normal operation of the converter is based on the ratio of two integration intervals.

A ratio measurement is performed in the same manner with the exception of the ramp down interval being determined by an external reference functioning as the Y input. To normalize the ratio to any required scaling, a series resistor (R_N) is added in this Reference Input. This should be a low T.C. (5ppm) wirewound or Vishay resistor. With R_N of approximately 54k a reading of 10000 will be obtained with X = Y. It should be noted that progressively less accurate division is obtained as Y → 0.

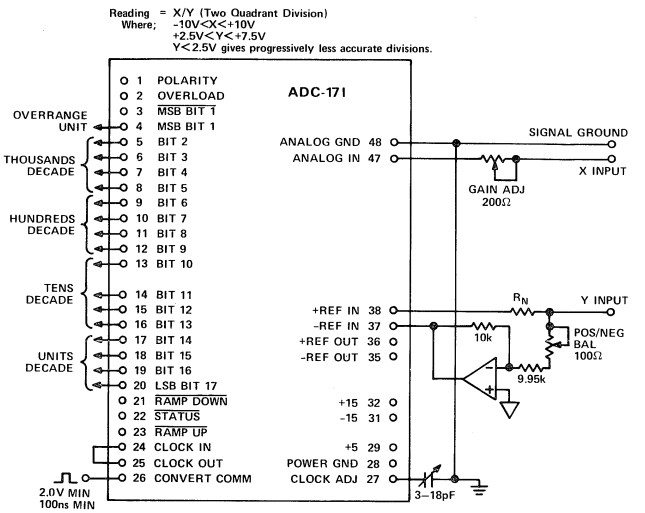


Figure 3. Ratiometric Operation With Adjustments

TWO QUADRANT RATIO

Use of an external unity gain inverter as shown in Figure 3, makes two quadrant ratio possible. For greatest accuracy and freedom from drift, this should be a chopper stabilized amplifier such as Analog Devices' 235, or 233; IC amplifiers, like the AD504 or AD508, may be used. The balance pot is adjusted for identical readings with both polarities of X input.

ONE QUADRANT RATIO

For one quadrant operation a Y input must be applied to the appropriate reference. When Analog Input (X) is positive a negative Y is required; when X is negative a positive Y is required.

SERIAL PULSE TRAIN OUTPUT

Gating the ramp down signal with the clock in signal gives an output pulse train during ramp down only. Use of 7400 series logic elements is recommended. The number of pulses out is equal to the ramp down count which is proportional to the input value, "X".

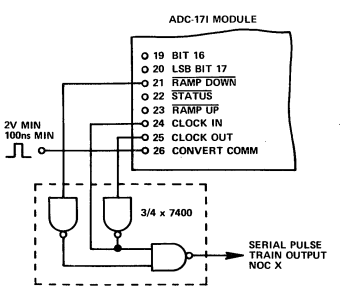


Figure 4. Serial Pulse Train Output

OUTPUT STORAGE REGISTER

An output storage register may be required for driving a non-blinking display, or where a conversion has to be separately called for (see Figure 5).

Data is transferred to the storage latches (7475), after conversion, during a ½μs strobe pulse provided by the monostable 74121. The 7440 is a buffer driver supplying the clock lines to the 7475 (which have a total fan in of 32). Complementary outputs are also available from the 7475.

A reset or load for an external counter may be provided before the pulse train by either of the following logic signals:

1. Conv. Command (Prior to Conversion)
2. Ramp Up (During Conversion)

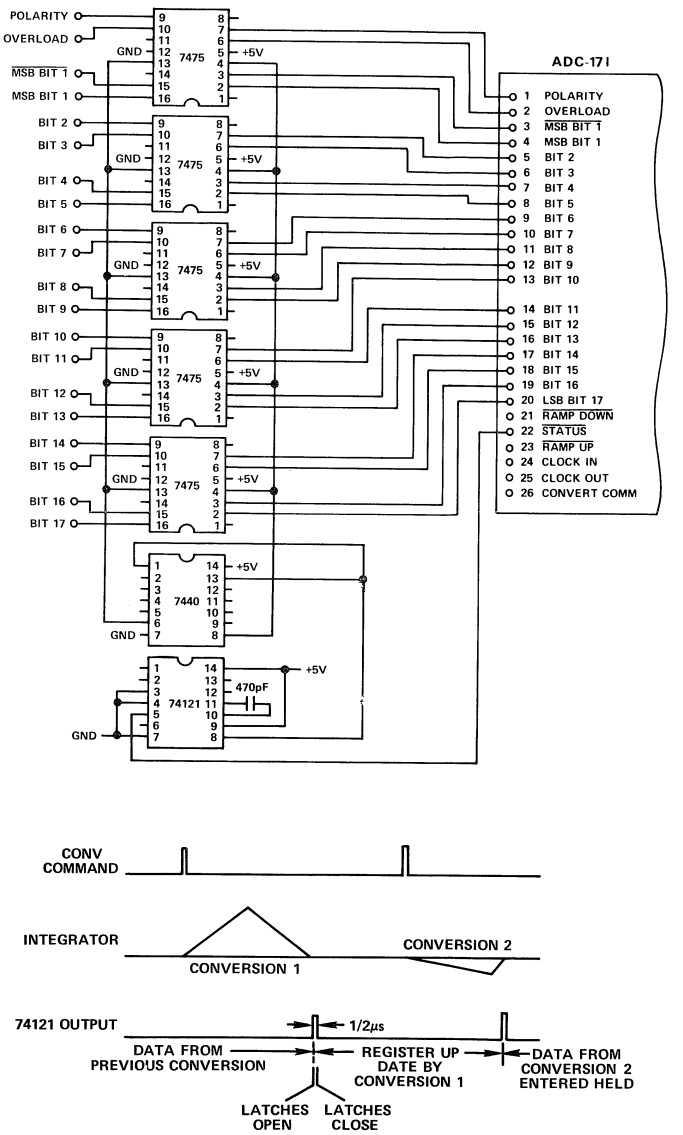


Figure 5. Storage Register Output and Timing Diagram

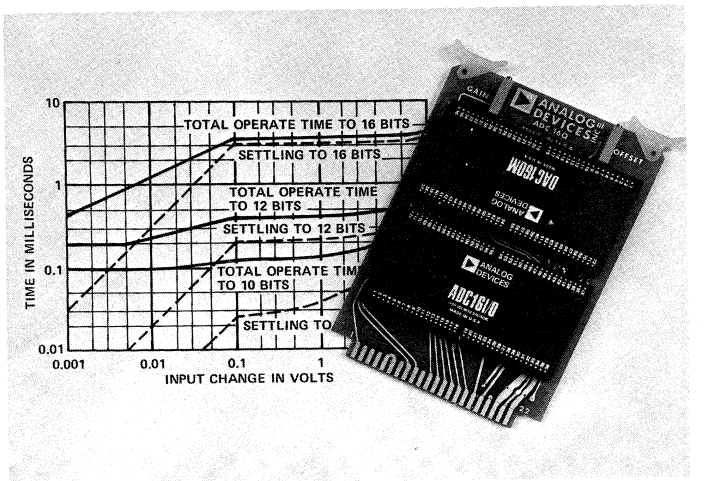
ANALOG DEVICES

High Resolution A/D Converter

ADC-16Q

FEATURES
- **16-Bit Resolution**
- **High Common Mode Rejection**
- **Nonlinearity ±0.0015%**
- **Stability – Long Term**
  - **Linearity 0.0005%**
  - **Gain 0.003%**
  - **Zero 0.001%**
- **TTL/DTL Compatible**

APPLICATIONS
- **Data Acquisition Requiring:**
  - **High Accuracy**
  - **Wide Dynamic Range**
  - **High Stability**
  - **Extreme Resolution**
- **Stability Measurements**
- **Testing ADC's and DAC's**



GENERAL DESCRIPTION

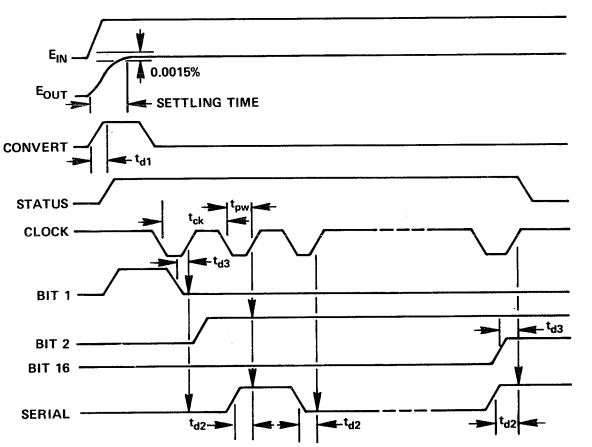
The ADC-16Q is a 16-bit binary Analog-to-Digital converter of the successive approximations type, consisting of a 4½" x 6" PC card holding two modules. One of the modules is a standard DAC-16QM Digital-to-Analog converter; the other module contains all the needed logic, the input buffer, and comparator. All options are selectable by the user either with jumpers on the mounting board, or by connections at the PC receptacle. Only by the use of the absolute best of all available components is such a converter built successfully in production without compromise.

UNPRECEDENTED LINEARITY AND STABILITY

The ADC-16Q owes its linearity and stability excellence to the use of monolithic quad current switches in its DAC section, for only with these excellent monolithic components has it been feasible to produce a commercially practical converter with stability appropriate for 16-bit performance. Recalibration at 30 day intervals holds the ADC-16Q within 0.0015% accuracy for long periods.

HIGH PERFORMANCE INPUT BUFFER

In a 16-bit converter operating with input range of 10VFS, the LSB value is 152μV. It is reasonable to assume that a user cannot transmit a signal to be measured over several feet of wire without generating appreciably more than one LSB of common mode noise! Consequently, the ADC-16Q has, as its input buffer, a true differential instrumentation amplifier of unity gain. The common mode rejection of this buffer is adequate to allow full accuracy of the converter in the presence of common mode signals of at least 150mV @ 60Hz. Actual common mode performance in a given installation depends critically on details of the wiring between signal source and converter. Later sections of this bulletin provide useful installation hints.



ADC-16Q Timing Diagram

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

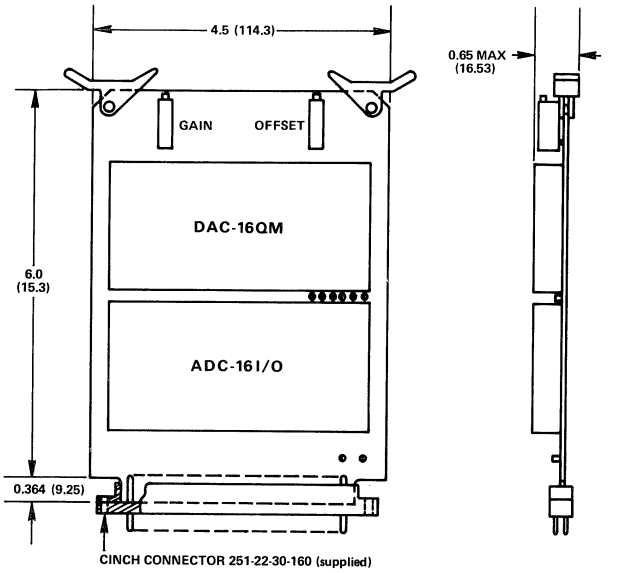
INPUT CHARACTERISTICS	
Ranges	±10V, ±5V, 0 to +10V (Jumper Selectable)
Overload	±15V Supply Can Be Applied to Input Buffer from Input to Input, or Either Input to Ground, Without Damage.
Impedance	w/o Buffer: 10k (±10V), 5k (±5V or 0 to 10V) w/Buffer: $10^9\Omega$ Typ Shunted by 13pF typ
Input Capacitance Mismatch	4pF typ (Buffer)
Settling Time to Rated Accuracy	w/o Buffer: 10μs (max) w/Buffer: $E_{in} \geq 100mV$ 5ms typ $E_{in} < 100mV$ 50μs/mV typ
CMRR of Input Buffer	w/1k Source Unbalance and $-11V < E_{in} < +11V$: dc to 100Hz: 100dB typ at dc: 80dB min at 100Hz: 60dB min
CONVERT COMMAND	TTL Compatible Positive Pulse. Leading Edge Resets Logic. Trailing Edge Initiates Conversion. User Determines Pulse Width Appropriate to Allow Settling Time for Input Buffer. 5TTL Loads
OUTPUT CHARACTERISTICS	
Resolution	16 Bits
Short Cycle Provision	Jumper Allows Adjustment to Operate at any Word Length to 16 Bits
Code	Binary, Offset Binary, 2's Complement (Selected at Connector) Positive True
Format	Parallel and Serial with Clock, TTL Compatible 0V ≤ "0" ≤ +0.4V @ 16mA (min) +2.4V ≤ "1" ≤ +5.0V @ −400μA (min)
Clock Rate	8μs/bit w/internal Timing Capacitor Provides 10–12 Bit Accuracy 25μs/bit w/external 0.015μF cap (Provided) Yields 16 Bit Accuracy
ACCURACY PARAMETERS	(Specified as a Percentage of Range)
Monotonicity	Guaranteed from +20°C to +30°C
Linearity Error	
+20°C to +30°C	±0.0015% +0.0005% max
0 to +70°C	±0.005% max
Temperature Coefficients	
Zero	±0.0002%/°C ±25μV/°C max
Gain	±0.0008%/°C max
Stability (at Constant Temperature and Humidity)	
24 Hours	Zero: ±0.0002% max Gain: ±0.0003% max Linearity: ±0.00005% max
30 Days	Zero: ±0.001% max Gain: ±0.003% max Linearity: ±0.0005% max
1 Year	Zero: ±0.01% max Gain: ±0.03% max Linearity: ±0.001% max
Power Supply Rejection dc to 60Hz	±0.004%/%V_S max ±0.0002%/%V_L max
Power Requirements	
$+V_S$	+15V dc ±2% @ 25mA (max), 18mA typ
$-V_S$	−15V dc ±2% @ 55mA (max), 41mA typ
$+V_L$	+5V dc ±5% @ 465mA (max), 350mA typ
Dissipation	3.5W max, 2.6W typ
WARMUP TIME	
To Rated Accuracy	1 Hour (max)
ADJUSTMENTS (Supplied)	
Offset	Control has Range of ±0.023% typ
Gain	Control has Range of ±0.05% typ
ENVIRONMENTAL	
Operating Temperature	0 to +70°C
Storage Temperature	−25°C to +100°C
PHYSICAL SIZE	4.5" x 6" Edge Connector Card 0.65" Thickness Overall

[1] Recommended Power Supply: Analog Devices models 902 and 905.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 MSB	A	BIT 1 MSB
2	NC	B	BIT 2
3	NC	C	BIT 3
4	NC	D	BIT 4
5	INTERLOCK	E	BIT 5
6		F	BIT 6
7	NC	H	BIT 7
8	EXTERNAL CAPACITOR	J	BIT 8
9	FOR CLOCK RATE	K	BIT 9
10	NC	L	BIT 10
11	BIT 14	M	BIT 11
12	BIT 15	N	BIT 12
13	BIT 16 LSB	P	BIT 13
14	SERIAL OUTPUT	R	CLOCK OUTPUT
15	CONVERT INPUT	S†	SHORT CYCLE RETURN
16	STATUS OUTPUT	T	STATUS OUTPUT
17	DIGITAL 5V COMMON	U	+5V dc INPUT (V_L)
18	+15V dc INPUT ($+V_S$)	V	−15V dc INPUT ($-V_S$)
19‡	±15V COMMON	W‡	±15V COMMON
20*	SIGNAL (−) INPUT	X*	SIGNAL (−) INPUT
21	SIGNAL (+) INPUT	Y*	SIGNAL (−) INPUT
22*	SIGNAL (−) INPUT	Z*	SIGNAL (−) INPUT

*Pins 20, 22, X, Y, Z All Connected Internally To Signal (−) Input. Do Not Use As Tie Points For Any Function Other Than Signal Input.
‡Pins 19 And W Are Connected Together Internally. Use One For Power Ground And The Other For Signal Source Ground Return.
†Must Be Tied To Pin #17 For 16 Bit Operation.

INPUT RANGE SELECTION

Make Connections Indicated On Terminals On The PC Board

Input Option	Connect Trim Res. from A to	Jumper D to	Jumper F to	Jumper J to
∓10V Buffered	C	B	—	—
∓5V Buffered	C	E	—	—
+10V Buffered	—	E	—	—
∓10V Direct	C	—	B	H
∓5V Direct	C	—	E	H
+10V Direct	—	—	E	H

NOTES:
[1] In buffered modes, input is true differential. Thus reversal of input connections would yield ranges of 0 to −10V, ±10V, and ±5V.
[2] When shipped, units will be jumpered for ∓10V operation with buffer.

WIDE DYNAMIC RANGE CAPABILITY

Clearly a 16-bit A/D converter is fully equivalent to a 10-12 bit ADC preceded by an auto-ranging buffer amplifier with 4-6 bit gain range! If desired, the ADC-16Q can be operated with faster clock to improve the throughput rate, while holding accuracy at any desired level (as shown in Figure 4). If, for instance, it is desired to use the machine for wide range 0.05% measurements, total throughput rate can be 2kHz.

ACCURACY AND INSTALLATION CONSIDERATIONS

The extremely high resolution and linearity of the ADC-16Q demanded a systems approach to the design. Problems like common mode noise pickup in just a few feet of wire, or the thermocouple effect of connections of dissimilar materials, cannot be neglected in a 16-bit design. For these and other reasons, users of the ADC-16Q should take exceptional care in planning installations, in order to minimize the effects of environmental conditions on system accuracy.

A. The unit and its connector and signal wiring should be located with an eye to optimum isolation from sources of RFI and EMI.

B. Special care must be observed in running input signal wiring to the buffer inputs, in order to avoid degrading the common mode rejection at ac.

Figure 1 shows a simplified equivalent circuit of the input system for common mode purposes, the points marked 1 and 2 being the input signal terminals, E_S and Z_S being the signal source and source resistance, and Z_T and C_T being the transmission line impedances. The circuit is a bridge, and if it is balanced there is no differential component of E_{CM} appearing across the input terminals.

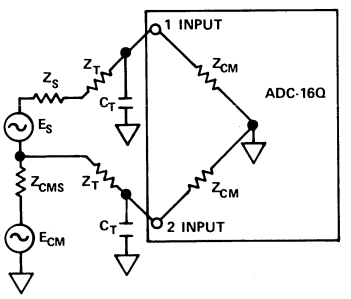
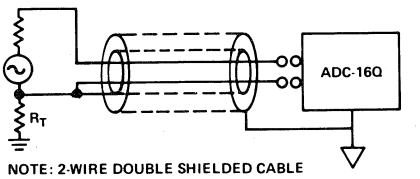


Figure 1. Simplified Equivalent Circuit Differential Input System

It is clearly of great importance to maintain balance in Z_T and C_T when a signal source is wired to the converter input. Only a few pF of capacitance unbalance is enough to wipe out the common mode rejection at 60Hz.

Figure 2 shows a recommended interconnection of a signal source to the ADC-16Q. Two-wire double-shielded cable should be used, with the inner shield connected to the "low" side of the signal, to act as a guard. Outer shield is grounded, and a dc path from signal source to ground MUST be provided, if it is not inherent in the design. To optimize common mode rejection, the double-shielded cable should also be capacitance-balanced. (Such cables with a specification on maximum capacitance unbalance per unit length are available from several manufacturers.)



NOTE: 2-WIRE DOUBLE SHIELDED CABLE IS TROMPETER ELECTRONICS INC. P/N QRC-78-2 OR BELDEN EQUIVALENT

Figure 2. Shielding of Input Wiring

C. The unit, its connector and wiring should be located in a region of constant, stable temperature. Popular electronic wiring materials almost always involve use of more than one metal, and we must remember that junctions of two metals will act as thermocouples, and will generate error voltages proportional to temperature difference between junctions, as well as to temperature gradients along wires. We cannot ignore these effects when the value of an LSB is 152μV!

REFERENCE LOADING

The exceptional accuracy parameters of the ADC-16Q required exceptional care in design, as well as the use of the finest aged temperature-compensated reference zener diodes that are commercially available. The reference supply, contained within the DAC-16QM module, should not be loaded by the user – and for this reason, a reference supply terminal is NOT provided on the PC board connector. For test purposes, the reference supply may be reached at terminal #52 of the DAC-16QM module. Only very high input impedance voltmeters should be used for checking.

ACCURACY VS CONVERSION TIME

Several different aspects of A/D converter design result in a need to clock the converter logic at a slower rate as the need for accuracy increases. In a 16-bit converter, if we wish to attain 16-bit relative accuracy, more settling time must be allowed for the various amplifiers in the system than would be necessary for a 12-bit converter.

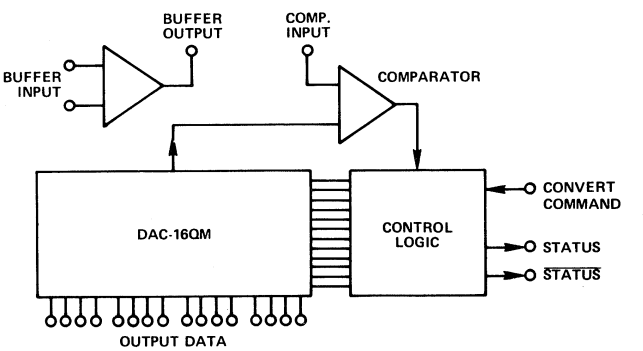


Figure 3. Block Diagram ADC-16Q

In a 16-bit A/D converter, as pointed out earlier, it is most likely an absolute necessity to have available a true differential input with high CMRR. The simplified block diagram shows how this is provided in the ADC-16Q, as well as showing the facility to operate without it, in those few cases when that may be feasible. Settling time of the input buffer to rated accuracy (±0.0008% of F.S.) is 5ms for input changes larger than 100mV. There are many situations where it may be desirable to have the ability to convert at a faster rate, and accept the inaccuracy that may result. The user

may adjust the width of his convert command pulse to provide the desired settling time for the input buffer. See Figure 4, which shows the relationship of settling time and conversion plus settling time to relative accuracy for changing values of E_{IN}.

The user should keep in mind the fact that the ADC-16Q is a successive approximation converter. All successive approximation converters are capable of making unexpectedly large errors in reading if the input signal is allowed to vary while the conversion process in progressing. This fact must be kept in mind whenever the buffer is not allowed to settle to full accuracy for the converter resolution involved.

OPERATING THE ADC-16Q AT UNDER 16 BIT RESOLUTION

The ADC-16Q may be operated with any resolution between 1 and 16 bits. For operation at reduced resolution, jumper from pin S of the PC connector to the pin for the $(n + 1)$ bit. The conversion program will proceed as usual until the $(n + 1)$ bit is reached. The $(n + 1)$ bit will be left in the "1" state. For example, if 12-bit performance is desired, jumper from pin S to pin P. Of course, when this is done, less settling time is required for all circuits involved, allowing an increase in clock rate and a reduction in settling time allowance for the input buffer. The information in Figure 4 will be useful. Pin S should be grounded to pin #17 for 16 bit operation.

CHANGE OF CLOCK RATE

Your ADC-16Q shipment included a 0.015μF capacitor, required to be connected between pins 8 and 9 of the PC board receptacle in order that the clock time of the converter will be 25μs, as needed for 16-bit resolution. Without the capacitor, clock time will be 6–8μs. Of course, you may connect intermediate values of capacitor if you should desire clock periods between those limits.

CHOOSING CODES (PARALLEL OUTPUT)

Binary code (for unipolar range) or Offset Binary (for bipolar ranges) are obtained by connecting to PIN A (for the MSB) through to PIN 13 (LSB for 16-bit resolution). If 2's complement code is preferred for bipolar ranges, all connections are the same except for Bit 1, which connects to PIN 1 ($\overline{\text{MSB}}$).

ADJUSTMENT OF OFFSET AND GAIN

If the ADC-16Q is to be kept within specification for extended periods, offset and zero adjustments should be made at roughly 30 day intervals. For adjustment purposes, a voltage source calibrated to extreme precision is required.

OFFSET (Unipolar): Set input voltage to ADC precisely at 0 Volts +½LSB.
(Bipolar): Set input voltage to -F.S. plus ½LSB.

OFFSET ADJUST: With proper input signal, rotate the "offset" control to the point where the converter just switches in its LSB.

GAIN: Set input voltage to ADC precisely at ½LSB less than "all bits on" input value. Note that the "all bits on" input is 1LSB less than nominal full scale rating. With input voltage precisely set, rotate "gain" control until the last bit just switches on.

For a 16-bit binary converter:

Range	Value of LSB	½LSB
10V	152μV	76μV
20V	305μV	152μV

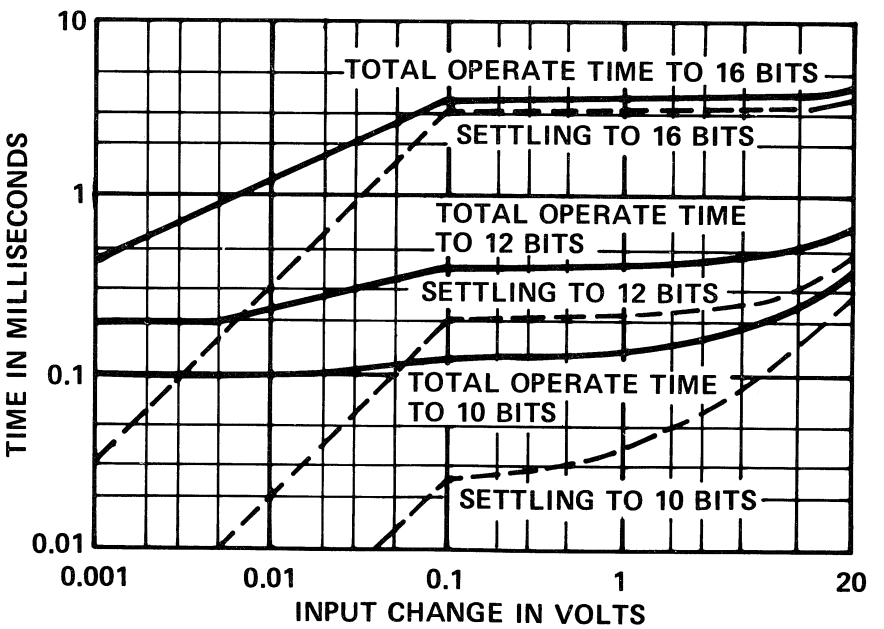
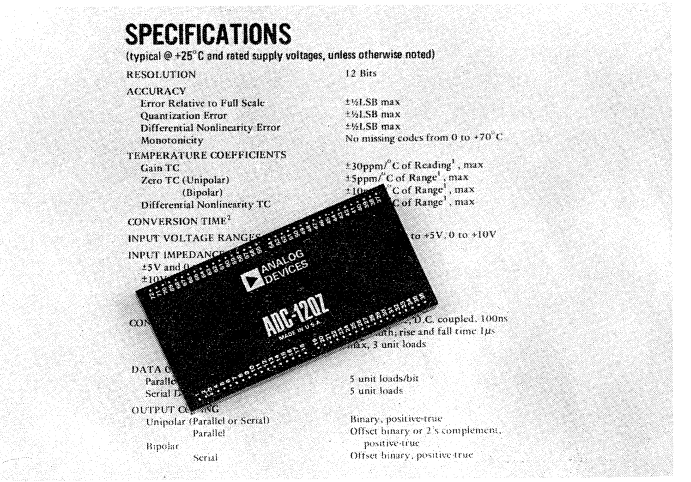


Figure 4. Settling Time of Input Buffer vs. Accuracy and Total Operate Time vs. Accuracy for Various Values of ΔE_{IN}

Low Cost General Purpose Analog-to-Digital Converter

ADC-12QZ

FEATURES
- 12 Bit Resolution and Accuracy
- Very High Performance/Cost Ratio
- No Missing Codes from 0 to +70°C
- 40μs Conversion Time
- Low Profile Module
- Parallel and Serial Outputs
- TTL/DTL Logic Levels
- User Selected Input Ranges
- Input Buffer Option Available



GENERAL DESCRIPTION

The ADC-12QZ is a 12-bit successive approximation type general purpose analog-to-digital converter that offers moderate speed and good performance at very low cost. Analog Devices' proprietary monolithic quad switches and a unique combination of thin film and hybrid technology have been incorporated in the ADC-12QZ, resulting in a converter that has the basic performance of a much higher priced unit. It has no missing codes from 0 to +70°C, and has a maximum error of ±½LSB relative to full scale at room temperature. The ADC-12QZ is packaged in a convenient, small, low profile module, and all of its logic inputs and outputs are fully TTL/DTL compatible.

EASY TO USE

The ADC-12QZ was designed specifically to make it easy to use. It contains its own temperature-compensated precision voltage reference, and any of four input ranges (0 to +10V, ±10V, 0 to +5V, ±5V) can be selected with jumpers and connections at the module terminals. If a high input impedance is required, the ADC-12QZ can be special ordered with an input buffer.

Binary output coding is used for unipolar operation, but for operation in the bipolar mode, the parallel output data can be either two's complement or offset binary at the user's option. The two codes differ only in that the MSB output (pin 72) is used for offset binary coding, while its complement, $\overline{\text{MSB}}$ (pin 70) is used for two's complement coding. STATUS, which indicates when the parallel output data is valid, and its complement, $\overline{\text{STATUS}}$, are both available.

A latched serial output having a nonreturn-to-zero (NRZ) format is taken from the output of a TTL flip-flop. The serial data is transmitted MSB first in binary code for unipolar operation and in offset binary code for bipolar operation. The STROBE output is used to clock the serial data into a receiving shift register.

TIMING

As shown in Figure 1, the leading edge ("0" to "1" transition) of the convert command pulse sets the STATUS and MSB outputs to the "1" state, and the outputs of bits 2-12 to "0". The conversion program begins on the trailing edge of the convert command pulse with the starting of the internal clock. The bit decisions are made on successive "1" to "0" clock pulse transitions, with the MSB decision occurring first. The 200ns wide strobe pulses are used to synchronize the transmission of serial data. Serial data bits are valid on successive leading edges ("0" to "1" transitions) of the strobe pulses. At the completion of the conversion, the STATUS output returns to zero, signaling that the parallel output data is valid.

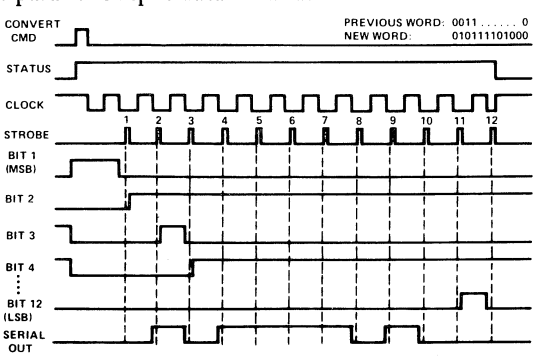


Figure 1. ADC-12QZ Timing Diagram

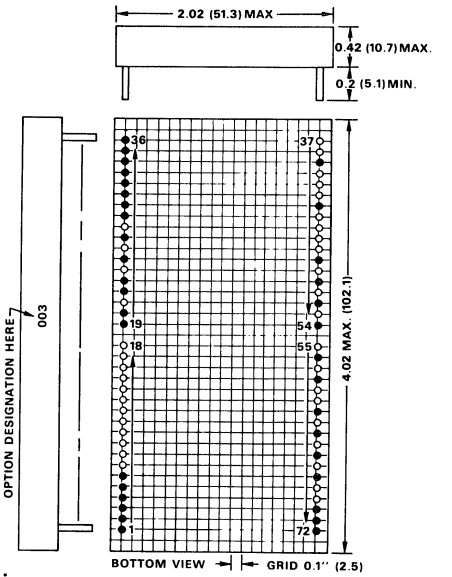
SPECIFICATIONS (typical @ +25°C and rated supply voltages, unless otherwise noted)

RESOLUTION	12 Bits
ACCURACY	
Error Relative to Full Scale	±½LSB max
Quantization Error	±½LSB max
Differential Nonlinearity Error	±½LSB max
Missing Codes	No missing codes from 0 to +70°C
TEMPERATURE COEFFICIENTS	
Gain TC	±30ppm/°C of Reading[1], max
Zero TC (Unipolar)	±5ppm/°C of Range[1], max
(Bipolar)	±10ppm/°C of Range[1], max
Differential Nonlinearity TC	±10ppm/°C of Range[1], max
CONVERSION TIME[2]	40μs max
INPUT VOLTAGE RANGES	±5V, ±10V, 0 to +5V, 0 to +10V
INPUT IMPEDANCE	
±5V and 0 to +10V Ranges	5k ohms
±10V Range	10k ohms
0 to +5V Range	2.5k ohms
Buffered[3]	1000 Megohms min
CONVERT COMMAND[4]	Positive Pulse, D.C. coupled, 100ns min width; rise and fall time 1μs max, 3 unit loads
DATA OUTPUTS[4]	
Parallel Data	5 unit loads/bit
Serial Data	5 unit loads
OUTPUT CODING	
Unipolar (Parallel or Serial)	Binary, positive-true
Bipolar { Parallel	Offset binary or 2's complement, positive-true
Bipolar { Serial	Offset binary, positive-true
LOGIC OUTPUTS[4]	
Status	"1" during conversion, "0" otherwise; 5 unit loads
$\overline{\text{Status}}$	"0" during conversion, "1" otherwise; 5 unit loads
Strobe	Serial data synchronization, 5 unit loads
POWER SUPPLY REQUIREMENTS	
Analog	+15V ±5% @ 20mA
	-15V ±5% @ 30mA
Digital	+5V ±5% @ 210mA
POWER SUPPLY SENSITIVITY[5]	
Gain	±20ppm/%ΔV_s
Zero	±10ppm/%ΔV_s
TEMPERATURE RANGE[6]	
Operating	0 to +70°C
Storage	-55°C to +125°C
EXTERNAL ADJUSTMENTS	
Zero	20kΩ, 20 turn potentiometer across ±15V supply with 1.5MΩ resistor connected between slider and pin 20.
Gain	20kΩ, 20 turn potentiometer across ±15V supply with 150kΩ resistor connected between slider and pin 1.
DIMENSIONS	2" x 4" x 0.4" Module, Nominal

NOTES:
[1] Range for unipolar operation ≡ +F.S.; Range for bipolar operation ≡ 2 (+F.S.). Reading for bipolar input is defined as |Actual Reading - (-F.S.)|.
[2] Conversion time is measured from trailing edge of convert command pulse to "1" to "0" transition of status output.
[3] Units with buffer available on special order only.
[4] All digital inputs and outputs are completely TTL compatible. One unit load is identical to that defined for standard 54/74 Series TTL.
[5] For ±15V supply only, and with +15V and -15V supplies tracking.
[6] Extended operating temperature version (-55°C to +125°C) is available on special order; the extended temperature range for 12 Bit units is -25°C to +85°C.
Specifications subject to change without notice.

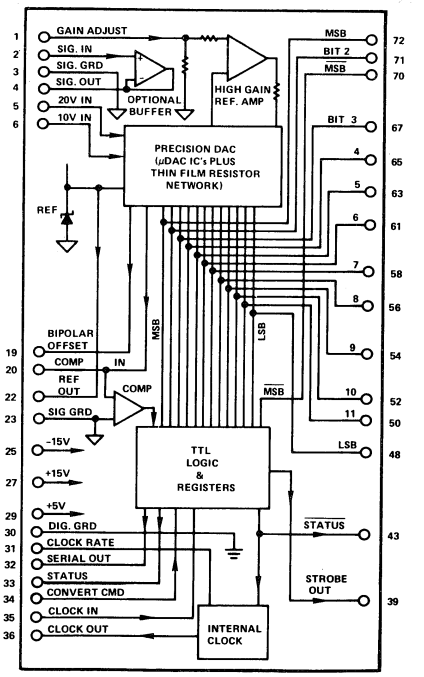
OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
Module Dimensions in CM: 10.29 max by 5.11 max by 1.04 max.
All pins are gold plated rodar, (MIL-G-45 204), 0.019" ±0.001" dia., 0.2" min. length.
For plug-in mounting card, order Board No. AC1548

BLOCK DIAGRAM AND PIN DESIGNATIONS



ORDERING GUIDE*

ADC-12QZ-XXX

OPTION DESIGNATOR	INPUT BUFFER	TEMP RANGE
003	NO	STANDARD
013	NO	EXTENDED
023	YES	STANDARD
033	YES	EXTENDED

*Note: Only -003 is standard. All other variations must be special ordered.

INPUT RANGE SELECTION

Four input ranges are available; 0 to +5V, ±5V, 0 to +10V and ±10V. If the ADC-12QZ has been ordered with the optional input buffer, any of these ranges can be buffered to provide an input impedance of 1000 Megohms. The chart below shows the connections required for each of the ranges.

RANGE SETTING INSTRUCTIONS

Input Range in Volts	Buffered Input	Range and Buffer Select			Offset Select Jumper pin 19 to
		Input to pin	Jumper pin 4 to	Jumper pin 20 to	
0 to +10V	NO	6	–	–	23
	YES*	2	6	–	23
±5V	NO	6	–	–	20
	YES*	2	6	–	20
±10V	NO	5	–	–	20
	YES*	2	5	–	20
0 to +5V	NO	6	–	5	23
	YES*	2	6	5	23

*Buffered input can be used only with units ordered with optional input buffer.

ZERO AND GAIN ADJUSTMENT

The ADC-12QZ is normally used with external zero and gain calibration potentiometers. However, if maximum accuracy is not required, they may be omitted. With no connections to either pin 1 or pin 20, gain calibration will be within approximately ±2LSB, and zero calibration will be within approximately ±10LSB.

If gain and zero adjustment potentiometers are used, they should be connected as shown in Figure 2. The zero control has a range of about ±20LSB, and the gain control has a range of about ±13LSB.

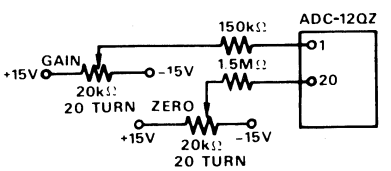


Figure 2. Zero and Gain Potentiometers

Proper gain and zero calibration requires great care and the use of extremely sensitive and accurate instruments. The voltage source used as a signal input must be very stable. It also should be capable of being set to within 1/10LSB at both ends of its range.

The ADC-12QZ's zero and gain adjustments are independent of each other if the zero (or offset) adjustment is made first. These adjustments are not made with zero and full scale input test signals, and it may be helpful to appreciate why. An analog-to-digital converter has a given digital output code for a small range of input signals (the nominal width of the range being one LSB). If properly adjusted, the converter will switch from one output code to the adjacent output code when the analog input signal is halfway between the two. With the input test signal set at that halfway point, the potentiometer can be adjusted until the converter does switch at just that point. By using this technique with a high speed convert command rate and a visual display of the output code, zero and gain adjustments can be performed in a very sensitive and accurate manner.

ZERO ADJUSTMENT PROCEDURE

1. For unipolar ranges:
   a) Set input voltage precisely to +½LSB.
   b) Adjust zero control until converter is just barely switching from 000000000000 to 000000000001.
2. For bipolar ranges:
   a) Set input voltage precisely to ½LSB above – F.S.
   b) Adjust zero control until converter is just barely switching from 000000000000 to 000000000001.

GAIN ADJUSTMENT PROCEDURE

1. Set input voltage precisely to ½LSB less than "all bits on" value. Note that this is 1½LSB less than nominal full scale.
2. Adjust gain control until converter is just barely switching from 111111111110 to 111111111111.

The table below summarizes the zero and gain adjustment procedure, and shows the proper input test voltages used in calibrating the ADC-12QZ.

CALIBRATION DATA

Input Voltage Range	Adjustment	Input Voltage	Adjust control to point where converter is just on the verge of switching between the two codes shown*
0 to +5V	ZERO	0.61mV	000000000000 000000000001
	GAIN	4.9982V	111111111110 111111111111
0 to +10V	ZERO	1.22mV	000000000000 000000000001
	GAIN	9.9963V	111111111110 111111111111
±5V	ZERO	-4.9988V	000000000000 000000000001
	GAIN	4.9963V	111111111110 111111111111
±10V	ZERO	-9.9976V	000000000000 000000000001
	GAIN	9.9927V	111111111110 111111111111

*Codes shown are natural binary for unipolar input ranges and offset binary for bipolar input ranges.

OUTPUT CODE

When using a unipolar input range the ADC-12QZ's parallel output data is in natural binary code. When using a bipolar input range, the parallel output data can be either two's complement or offset binary code at the user's option. The only difference between the two codes is the state of the most significant bit. MSB, pin 70, is used for two's complement coding. MSB, pin 72, is used for offset binary coding.

GROUNDING PRACTICE AND POWER SUPPLY BYPASSING

The ADC-12QZ's digital and analog grounds are not tied together internally. A connection must therefore be provided externally. It is recommended that the two grounds be connected with a jumper at the module terminals from SIGNAL GROUND (pin 23) to DIGITAL GROUND (pin 30).

The ADC-12QZ's +5V, +15V and -15V power inputs are each internally bypassed to ground with 0.1μF capacitors. Further power supply noise suppression can be achieved by adding additional bypass capacitors externally. Such capacitors would typically be 2μF (or greater) tantalum types. For best results they should be located near the module's power input terminals.

CONNECTING THE CLOCK

Although the ADC-12QZ contains its own internal clock oscillator, connection to it is accomplished with an external jumper between pins 35 and 36 of the module. This jumper between CLOCK OUT (pin 36) and CLOCK IN (pin 35) must be installed because unless otherwise specified, the ADC-12QZ is intended to operate only with the internal clock. If operation with an external clock is required, contact the factory for further information.

The internal clock is set to run at the maximum permissible rate. Although running it at a slower rate will not improve the converter's accuracy, in some applications a slower conversion time may permit synchronization or compatibility with interfacing equipment. This may be accomplished by connecting a capacitor externally between CLOCK OUT (pin 36) and CLOCK RATE ADJ (pin 31). The conversion time can be extended to at least 35ms in this manner. The capacitor's value is determined by the formula:

$$\text{Conversion Time (in } \mu\text{s)} \approx 35\left(1 + \frac{C_{ext}}{2200}\right)$$

where C_{ext} = external capacitance in pF.

SERIAL DATA OUTPUT

A latched serial output (taken from the output of a TTL flip-flop) is brought out to pin 32. The data is transmitted MSB first, and is coded positive-true binary for unipolar input ranges, or positive-true offset binary for bipolar input ranges. Prior to the beginning of a conversion this output will match the state of the twelfth bit (LSB) of the previous conversion (assuming the previous conversion was allowed to go to completion). In most applications the state of the serial output prior to the beginning of a conversion will be of no consequence.

Figure 3, shown below, indicates one method for transmitting data serially to a remote location using only three wires (plus a digital ground). The data is clocked into a receiving shift register using the ADC-12QZ's strobe output as a clock source for the shift register.

The Timing Diagram (Figure 1) shows that the serial data bits are valid on successive strobe pulse leading edges ("0" to "1" transitions). This allows the strobe pulse to clock the shift register directly, since the shift register transfers information on "0" to "1" transitions of the clock input. The first bit, which is the MSB, is valid on the first strobe pulse's leading edge. Each complete conversion has exactly twelve strobe pulses, one for each bit.

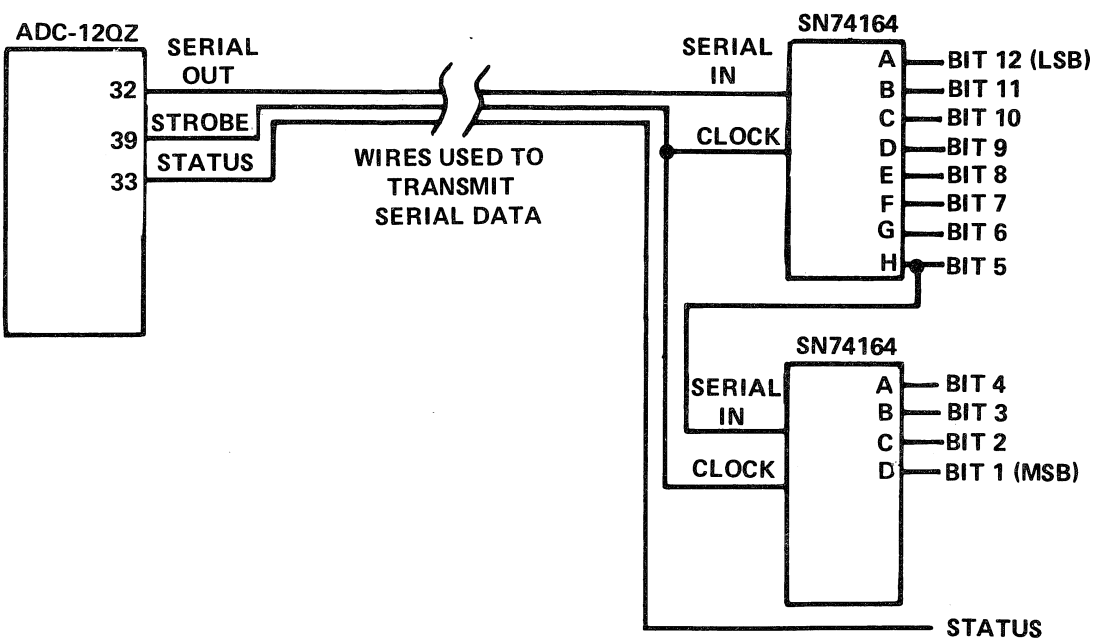


Figure 3. Block Diagram — Serial Data Transfer

V/F and F/V Converters

Orientation
V/F and F/V Converters

VOLTAGE-TO-FREQUENCY CONVERTERS

Voltage-to-frequency converters (VFC's) convert analog voltage or current levels to pulse trains or square waves in a logic-compatible form (usually TTL) at frequencies that are accurately proportional to the analog quantity. The output continuously tracks the input signal, responding directly to changes in the input signal; external-clock synchronization is not required. V/f converters find applications in analog-to-digital converters with high resolution, long-term high-precision integrators, two-wire high-noise-immunity digital transmission, and digital voltmeters.

FREQUENCY-TO-VOLTAGE CONVERTERS

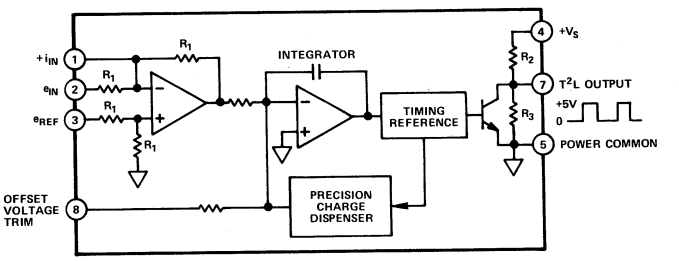
Frequency-to-voltage converters (FVC's) perform the inverse operation; they accept a wide variety of periodic waveforms and produce an analog output proportional to frequency. Combining adjustable threshold, gain, and output offset with low linearity-error, F/V converters offer economical solutions to a wide variety of applications where it is required to convert frequency to an analog voltage. Examples are motor-speed controllers, power-line frequency monitors, and VCO stabilization circuits. In analog-to-analog data transmission, they convert serially transmitted data in the form of pulse streams back to analog voltage.

Applications of both forms of conversion, as appropriate to specific device types, are illustrated with varying degrees of detail on the individual data sheets.

FACTORS IN CHOOSING VFC's AND FVC's

Voltage-to-frequency converters are available from Analog Devices in both module- and monolithic-IC- form. The output of modular types, ranging from 10kHz to 1MHz F.S., is a train of pulses of constant height and width, with very low duty cycle for small analog inputs. The output of the AD537, a monolithic integrated circuit, is unique in that its output is square-wave, an advantage in some applications. Apart from performance specifications, the tradeoffs between module and IC are conventional: modules have the advantages of completely specified performance; they do not rely on the specifications of critical external components, because the complete self-contained functional package requires no external components; trims are optional. IC's, on the other hand, have the advantages of lower cost and smaller size, and – in the case of the AD537– versatility of output and input connections, flexibility of frequency range, low power, single-supply operation, low external-component count, plus built-in voltage– and temperature– references. Modules offer better linearity, lower gain drift, and higher full-scale frequencies.

The most-popular VFC designs (Figure 1) contain an integrator, which charges at a rate proportional to the value of the input signal. Each time the integrator's charge has been increased by a precisely metered increment, the threshold crossing produces a pulse of accurately known area. The pulse serves both as the output (via a buffer) and as a subtractive charge



MODEL	FULL SCALE OUTPUT	R_1	R_2	R_3
458	100kHz	20kΩ	10kΩ	4.7kΩ
460	1MHz	10kΩ	2kΩ	910Ω

Figure 1. Block Diagram – Models 458, 460 VFC's

increment to reduce the integrator's net charge. The next pulse is triggered when the net integral has again reached the threshold. The relationship between the pulse rate and the input level is linear. The AD537 operates on a somewhat different principle (Figure 2): an input current charges a capacitor between 2 threshold levels. first in one direction, then in the other, in an emitter-coupled astable multivibrator circuit. Since the time required to reach the switching threshold is inversely proportional to the analog input, the frequency is directly proportional. For constant analog input, the charging rate and the discharge rate are equal, so the output is a square wave.

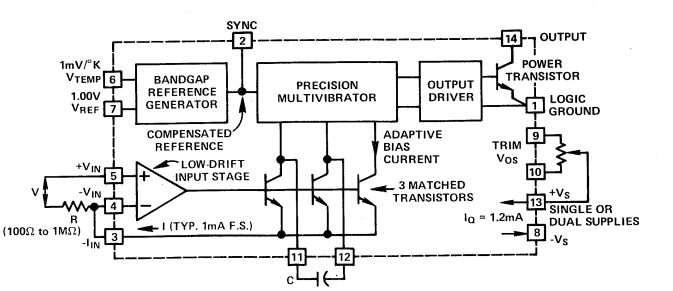
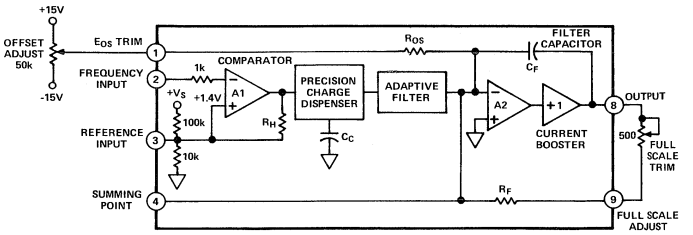


Figure 2. Block Diagram of the AD537



MODEL	CF	ROS	RH	RF
451	0.015μF	3.3MΩ	2.2MΩ	18kΩ
453	0.001μF	3.9MΩ	1.0MΩ	22kΩ

Figure 3. Block Diagram — Models 451 & 453 FVC's

Frequency-to-voltage-converter modules (Figure 3) average a train of equal-area pulses that are generated internally by a precision charge dispenser, in response to each crossing of an input threshold. The analog output voltage is proportional to the sum of the pulse areas over a given period. F/V conversion can also be obtained by using the IC AD537 VFC in a phase-locked loop; the VFC's output frequency is forced by feedback to be equal to the input frequency, hence the VFC input must be proportional to frequency.

SPECIFICATIONS

The salient specifications for VFC's are *(non)linearity*, as a percentage of full-scale frequency; *frequency range*, the greater the frequency range, the greater the resolution for a given counting period; *full-scale-calibration error; gain-temperature coefficient*, in ppm of signal per °C, where "gain" is the ratio of full-scale frequency to full-scale voltage, *input-offset temperature coefficient; overrange capability*, within rated specifications, and *step response*, the worst-case time interval required for the frequency to respond to a full-scale-step input change.

For FVC's, important specs, in addition to accuracy specs corresponding to the above, include *output ripple* (for specified input frequencies), *threshold* (for recognition that another cycle has been initiated, and for versatility in interfacing various types of sensors directly), *hysteresis*, to provide a degree of insensitivity to noise superimposed on a slowly-varying input waveform, and *dynamic response* (important in motor control).

Definitions of some critical specifications, and the conditions for adjusting or measuring them, are detailed on individual data sheets. A brief selection guide is shown below.

Selection Guide

V/F Converters

Max F.S. Frequency	Model	Other	See Page
10kHz	450	Module, 0.005% max nonlinearity, max tempcos: offset — 20μV/°C: gain — 25ppm/°C	481
10kHz	456	Module, 0.02% max nonlinearity, max tempcos: offset — 100μV/°C: gain — 80ppm/°C	481
20kHz	454	Module, 0.005% max nonlinearity, max tempcos: offset — 20μV/°C: gain — 25ppm/°C	481
100kHz	AD537	IC, 0.07% max nonlinearity, max tempcos: offset — 10μV/°C: gain — 50ppm/°C	475
100kHz	452	Module, 0.015% nonlinearity, max tempcos: offset — 30μV/°C: gain — 50ppm/°C	491
100kHz	458	Module, 0.01% nonlinearity, max tempcos: offset — 30μV/°C: gain — 5ppm/°C	495
1MHz	460	Module, 0.015% nonlinearity, max tempcos: offset — 30μV/°C: gain — 15ppm/°C	495

F/V Converters

Max F.S. Frequency	Model	Other	See Page
100Hz–20kHz Adjustable	451	Module, 0.008% max nonlinearity, 30ms to full scale, max gain tempco — 50ppm/°C	485
1kHz–200kHz Adjustable	453	Module, 0.008% max nonlinearity, 4ms to full scale, max gain tempco — 50ppm/°C	485

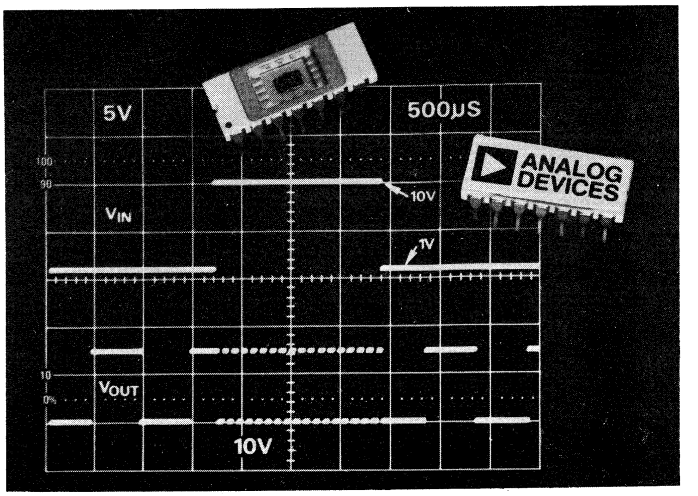
ANALOG DEVICES

Integrated Circuit Voltage to Frequency Converter

AD537

FEATURES

- Low Cost A-D Conversion
- Versatile Input Amplifier
  - Positive or Negative Voltage Modes
  - Negative Current Mode
  - High Input Impedance, Low Drift
- Single Supply, 5 to 36 Volts
- Linearity: ±0.05%
- Low Power: 1.2mA Quiescent Current
- Full Scale Frequency up to 100kHz
- 1.00 Volt Reference
- Thermometer Output (1mV/°K)
- F-V Applications



PRODUCT DESCRIPTION

The AD537 is a monolithic V-F converter consisting of an input amplifier, a precision oscillator system, an accurate internal reference generator and a high current output stage. Only a single RC network is required externally to set up any full scale (F.S.) frequency up to 100kHz and any F.S. input voltage up to ±30V. Linearity error is as low as ±0.05% for 10kHz F.S., and operation is guaranteed over an 80dB dynamic range. The converter performs very well even at very low frequencies, maintaining linearity down to 0.001Hz; accuracy at this level is limited only by input offset voltage and current. The overall temperature coefficient (excluding the effects of external components) is typically ±30ppm/°C. The AD537 operates from a single supply of 5 to 36V and consumes only 1.2mA quiescent current.

A temperature-proportional output, scaled to 1.00mV/°K, enables the circuit to be used as a reliable temperature-to-frequency converter; in combination with the fixed reference output of 1.00V, scales down to 0°C or 0°F can be generated.

The low drift (1µV/°C typ) input amplifier allows operation directly from small signals (e.g. thermocouples or strain gauges) while offering a high (250MΩ) input resistance. Unlike most V-F converters, the AD537 provides a square-wave output, and can drive up to 12 TTL loads, LEDs, very long cables, etc.

The excellent temperature characteristics and long-term stability of the AD537 are guaranteed by the primary band-gap reference generator and the low T.C. silicon chromium thin film resistors used throughout.

The circuit is available in a hermetically-sealed 14 pin DIL package and in three grades: the AD537J and K for 0 to +70°C operation and the AD537S, specified from -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD537 is a complete V-F converter requiring only an external RC timing network to set the desired full scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full-scale input voltage range from 100mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of timing resistor. The full scale frequency is then set by the timing capacitor from the simple relationship, f = V/10RC.
2. The power supply requirements are minimal, only 1.2mA quiescent current is drawn from a single positive supply from 4.5 to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to ($+V_S$ - 4) volts. Negative inputs can easily be connected for below ground operation.
3. F-V converters with excellent characteristics are also easy to build by connecting the AD537 in a phase-lock loop, application particulars are shown in Figure 13.
4. The versatile open-collector NPN output stage can sink up to 20mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic form with either positive or negative logic levels.
5. Every AD537 is subjected to long term stabilization bakes and temperature cycled 10 times from -65°C to +150°C to final test to insure reliability and long-term stability.

SPECIFICATIONS (typical @ +25°C with V_S (total) = 5 to 36V, unless otherwise noted)

MODEL	AD537J	AD537K	AD537S
ANALOG INPUT AMPLIFIER			
(Voltage-to-Current Converter)			
Voltage Input Range			
Single Supply	0 to ($+V_S$ - 4) Volts (min)	*	*
Dual Supply	$-V_S$ to ($+V_S$ - 4) Volts (min)	*	*
Input Bias Current			
(Either Input)	100nA	*	*
Input Resistance (Non-Inverting)	250MΩ	*	*
Input Offset Voltage			
(Trimmable to Zero)	5mV max	2mV max	**
vs. Supply	100μV/V max	*	*
vs. Temp (T_{min} to T_{max})	5μV/°C	1μV/°C	10μV/°C max
Safe Input Voltage (Note 1)	$\pm V_S$	*	*
CURRENT-TO-FREQUENCY CONVERTER			
Frequency Range	0 to 150kHz	*	*
Nonlinearity (Note 2)			
f_{max} = 10kHz	0.15% max (0.1% typ)	0.07% max	**
f_{max} = 100kHz	0.25% max (0.15% typ)	0.1% max	**
Full Scale Calibration Error			
C = 0.0100μF, I_{IN} = 1.000mA	±7% max	±5% max	**
vs. Supply, ($f_{max} < 100kHz$)	±0.1%/V max (0.01% typ)	*	*
vs. Temp. (T_{min} to T_{max})	±150ppm/°C max (50ppm typ)	50ppm/°C max (30ppm typ)	150ppm/°C max
REFERENCE OUTPUTS			
Voltage Reference			
Absolute Value	1.00 Volt ±5% max	*	*
vs. Temp. (T_{min} to T_{max})	50ppm/°C	100ppm/°C max	**
vs. Supply	±0.03%/V max	*	*
Output Resistance (Note 4)	380Ω	*	*
Absolute Temperature Reference (Note 3)			
Nominal Output Level	1.00mV/°K	*	*
Initial Calibration @ +25°C	298mV ±5mV typ	±5mV max	**
Slope Error from 1.00mV/°K	±0.02mV/°K	*	*
Slope Nonlinearity	±0.1°K	*	*
Output Resistance (Note 4)	900Ω	*	*
OUTPUT INTERFACE (Open Collector Output)			
(Symmetrical Square Wave)			
Output Sink Current in Logic "0"			
(V_{OUT} = 0.4V max, T_{min} to T_{max})	20mA min	*	10mA min
Output Leakage Current in Logic "1"			
(T_{min} to T_{max})	200nA max	*	2μA max
Logic Common Level Range	$-V_S$ to ($+V_S$ - 4) Volts	*	*
Rise/Fall Times (C_T = 0.01μF)			
I_{IN} = 1mA	0.2μs	*	*
I_{IN} = 1μA	1μs	*	*
POWER SUPPLY			
Voltage, Rated Performance			
Single Supply	4.5 to 36V	*	*
Dual Supply	±5 to ±18V	*	*
Quiescent Current	1.2mA	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*

*Specifications same as AD537J.
**Specifications same as AD537K.

Note 1 Maximum voltage input level is equal to the supply on either input terminal. However, large negative voltage levels can be sensed at the negative terminal if the input is scaled to a nominal 1mA full scale through an appropriate value resistor. (See Figure 3)

Note 2 Nonlinearity is specified for a current input level (I_{IN}) to the converter from 0.1 to 1000μA. Converter has 100% overrange capability up to I_{IN} = 2000μA with slightly reduced linearity. Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.

Specifications subject to change without notice.

Note 3 Temperature reference output performance is specified from 0 to +70°C for "J" and "K" devices, -55°C to +125°C for "S" model.

Note 4 Loading the 1.0 volt or 1mV/°K outputs can cause a significant change in overall circuit performance, as indicated in the applications section. To maintain normal operation, these outputs should be operated into the internal buffer or an external amplifier.

CIRCUIT OPERATION

A block diagram of the AD537 is shown in Figure 1. A versatile operational amplifier (BUF) serves as the input stage; its purpose is to convert and scale the input voltage signal to a drive current in the NPN follower, preferably arranged so that at the full scale input voltage, a 1mA drive current is delivered to the current-to-frequency converter. The drive current to the current-to-frequency converter (an astable multivibrator) provides both the bias levels and the charging current to the externally connected timing capacitor. The "adaptive" bias scheme allows the oscillator to provide low nonlinearity over the entire current input range of 0.1 to 2000μA. The square wave oscillator output goes to the output driver which provides a floating base drive to the NPN power transistor. This floating drive allows the logic interface to be referenced to a different level than $-V_S$. The "SYNC" input allows the oscillator to be slaved to an external master oscillator; this input can also be used to shut off the oscillator.

The reference generator uses a band-gap circuit (this allows single-supply operation to 4.5 volts – not possible with low T.C. zeners) to provide the reference and bias levels for the amplifier and oscillator stages. The reference generator also provides the precision, low T.C. 1.00 volt output and the V_{TEMP} output which tracks absolute temperature at 1mV/°K.

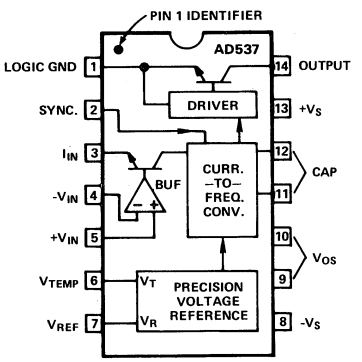


Figure 1. Block Diagram and Pin Connections

AD537 CHIPS

The AD537 is also available in passivated chip form guaranteed to "J" specifications. Consult factory for pricing and application particulars. Figure 2 shows the chip metallization layout and bonding pads.

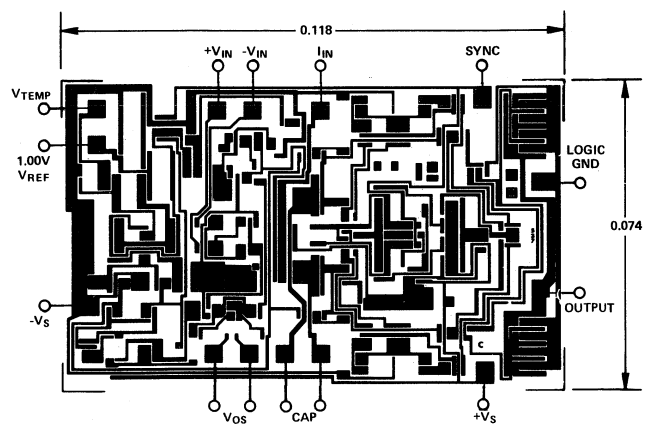


Figure 2. Chip Bonding Diagram

V-F CONNECTION FOR POSITIVE INPUT VOLTAGES

The positive voltage input range is from $-V_S$ (ground in single supply operation) to 4 volts below the positive supply. The connection shown in Figure 3 provides a very high (250MΩ) input impedance. The input voltage is converted to the proper drive current at pin 3 by selecting a scaling resistor. The full scale current is 1mA, so a 10 volt range would require a nominal 10kΩ resistor, and so on. The trim range required will depend on capacitor tolerance. Full scale currents other than 1mA can be chosen, but linearity over the whole range will be reduced; 2mA is the maximum allowable drive.

As indicated by the scaling relationship in Figure 3, a 0.01μF timing capacitor will give a 10kHz full scale frequency, and 0.001μF will give 100kHz with a 1mA drive current. The maximum frequency is 150kHz. Polystyrene or NPO ceramic capacitors are preferred for T.C. and dielectric absorption; polycarbonate or mica are acceptable; other types will affect linearity. The capacitor should be wired very close to the AD537.

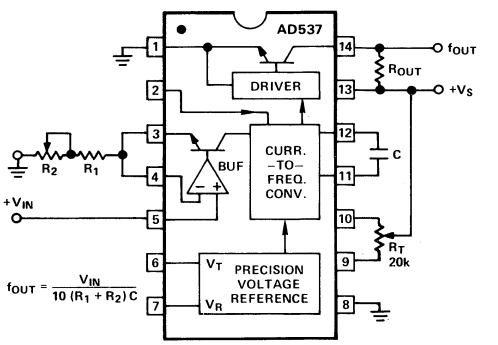


Figure 3. Standard V-F Connection for Positive Input Voltages

V-F CONNECTIONS FOR NEGATIVE INPUT VOLTAGE OR CURRENT

A wide range of negative input voltages can be accommodated with proper selection of the scaling resistor, as indicated in Figure 4. This connection is not high impedance as is the buffered positive connection since the 1mA F.S. drive current must be supplied by the signal source. However, very large negative voltages beyond the supply can be handled easily; just modify the scaling resistors appropriately. Diode CR1 and the 1k resistor are necessary for overload and latchup protection for current or voltage inputs.

If the input signal is a true current source, R_1 and R_2 are not used. Full scale calibration can be accomplished by connecting a 200kΩ pot in series with a fixed 27kΩ from pin 6 to ground.

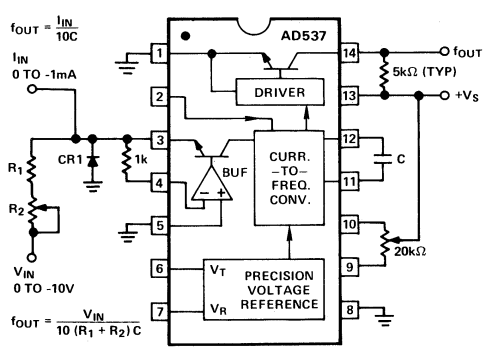


Figure 4. V-F Connections for Negative Input Voltage or Current

INTERFACING RESISTIVE TRANSDUCERS

Most types of resistive element transducers, such as servo-pots, level indicators, thermistors, photosensors, strain gauges, and so on, can be directly driven from the AD537 reference output, as shown here in Figure 5. The sense point of the pot or bridge is connected to the non-inverting input of the buffer amplifier. Calibration is accomplished by adjusting the 1kΩ potentiometer. Total resistance values R_{TOT} from 3kΩ to 100kΩ are easily accommodated; values below 3kΩ will load the reference beyond its drive capability; input bias current errors will be noticeable above 100kΩ. The scale correction factor, K, is a function of R_{TOT}; it varies from 0.65 to 0.98 for values from 3kΩ to 100kΩ; at 10kΩ it is 0.82. Using a panel potentiometer for R_{TOT} provides a very linear variable oscillator which is not subject to the problems of placing variable timing components distant from the circuitry.

An alternate method for driving resistive sensors such as thermistors or photosensors can be accomplished by connecting the sensor from pin 3 to ground. Driving the input at pin 5 with V_R from pin 7 will thus apply a constant 1.00 volt to the sensor (up to 2mA output current). The frequency will then be inversely proportional to resistance (but the oscillator period will be linear with R).

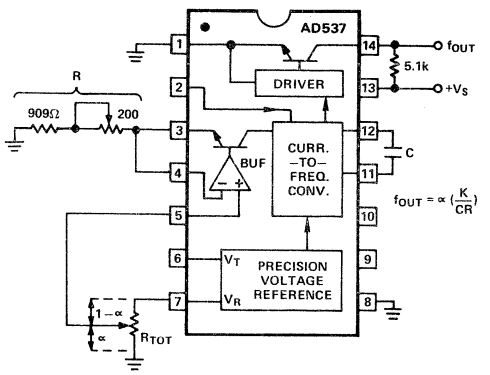


Figure 5. Direct Drive Connection for Resistive Transducers

OPERATION WITH NON-ZERO TC

The good temperature stability of the AD537 can only be realized using stable timing components. However, compensation for capacitors having a negative TC (such as polystyrene, -150 ±80ppm/°C) can be easily introduced by adding a resistor between the +1mV/°K output and $-V_S$. The value should be selected from the curve given in Figure 6. Over this range of compensation the scale factor is only slightly affected; the error is about +0.03%/ppm/°K in frequency (e.g. 150ppm shift would change the scale factor 4.5%).

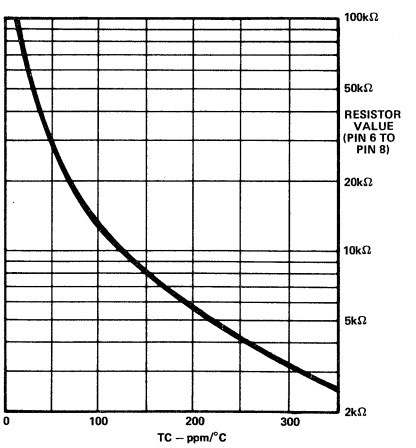


Figure 6. Positive T.C. Induced Versus Correction Resistance

NONLINEARITY SPECIFICATION

The preferred method for specifying linearity error is in terms of the maximum deviation from the ideal relationship after calibrating the converter at full scale and "zero". This error will vary with the full scale frequency and the mode of operation. The AD537 operates best at a 10kHz full scale frequency with a negative voltage input; the linearity is typically with ±0.02%. Operating at higher frequencies or with positive inputs will degrade the linearity as indicated in the specifications. The shape of a typical linearity plot is given in Figure 7.

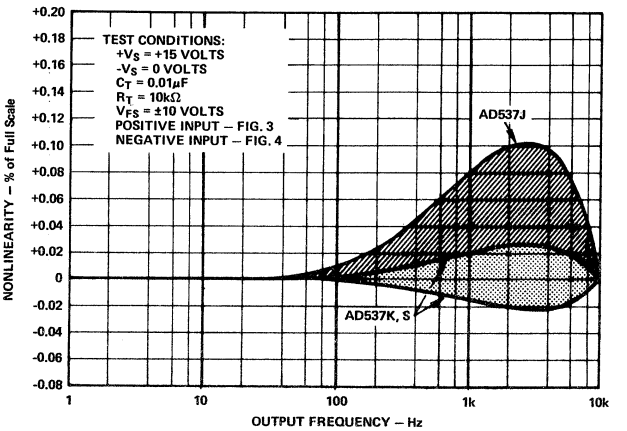


Figure 7a. Typical Nonlinearity Error Envelopes with 10kHz F.S. Output

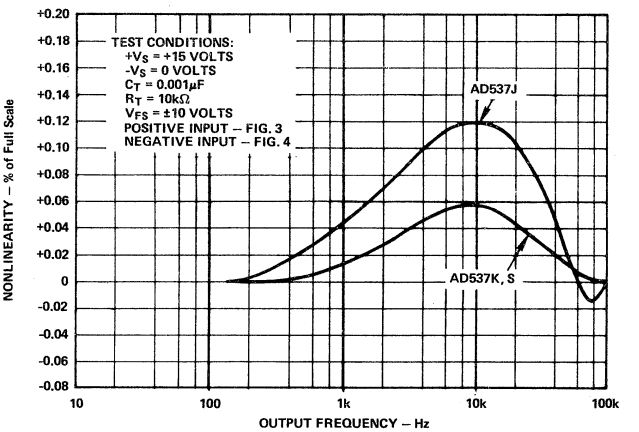
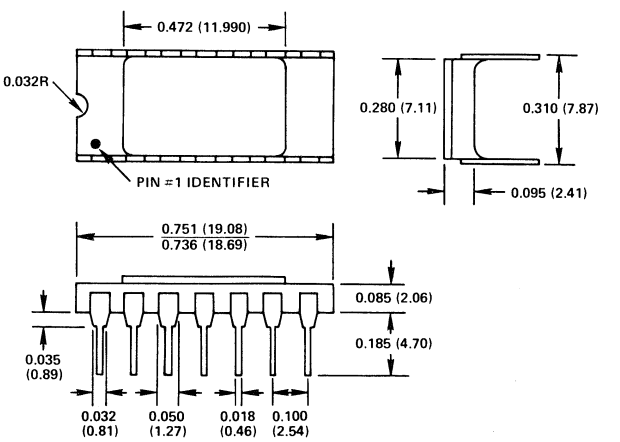


Figure 7b. Typical Nonlinearity Error with 100kHz F.S. Output



14 PIN DUAL IN LINE

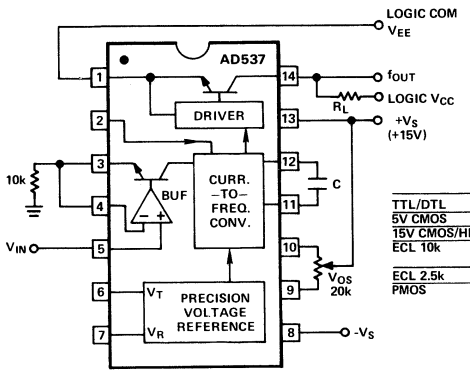
Dimensions shown in inches and (mm).

Figure 8. Physical Dimensions

OUTPUT INTERFACING CONSIDERATIONS

The design of the output stage makes for easy interfacing to all digital logic families. The collector and emitter of the output NPN transistor are both uncommitted; the emitter can be tied to any voltage between $-V_S$ and 4 volts below $+V_S$. The open collector can be pulled up to a voltage 36 volts above the emitter regardless of $+V_S$. The high power output stage can supply up to 20mA (12 TTL loads) at a maximum saturation voltage of 0.4 volts. The stage limits the output current at 25mA; it can handle this limit indefinitely without damaging the device.

Figure 9 shows the AD537 with a standard 0 to +10 volt input connection and the output stage connections. The values for the logic common voltage, pull-up resistor, positive logic level, and $-V_S$ supply are given in the accompanying chart for several logic forms.



	V_{CC}	V_{EE}	R_L	$-V_S$
TTL/DTL	+5	GND	5k	GND
5V CMOS	+5	GND	20k	GND
15V CMOS/HNIL	+15	GND	10k	GND
ECL 10k	0	-8	5k	-8 to -15
ECL 2.5k	+1.3	-2	5k	-5
PMOS	0	-15	10k	-15

Figure 9. Interfacing Standard Logic Families

TRUE TWO-WIRE DATA TRANSMISSION

Figure 10 shows the AD537 in a true two-wire data transmission scheme. The twisted-pair transmission line serves the dual purpose of supplying power to the device and also carrying frequency data in the form of current modulation. The PNP circuit at the receiving end represents a fairly simple way for converting the current modulation back into a voltage square wave which will drive digital logic directly. The 0.6 volt square wave which will appear on the supply line at the device terminals does not affect the performance of the AD537 because of its excellent supply rejection. Also, note that the circuit operates at nearly constant average power regardless of frequency.

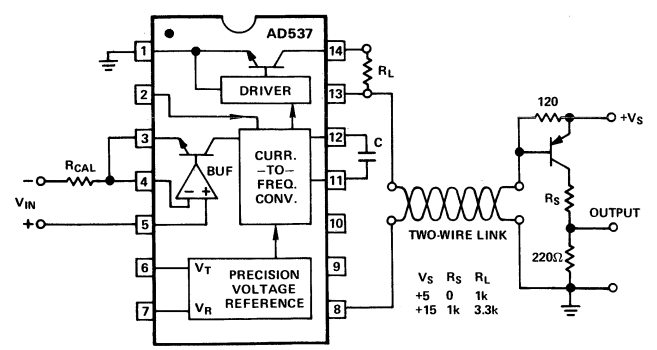


Figure 10. True Two-Wire Operation

MULTIPLEXING

Several AD537 devices can be multiplexed onto the same data line (or bus) quite easily by use of the open-collector output stage feature. A single pull-up resistor is then used for the entire V/F string. The individual devices are controlled at their uncommitted emitter (Logic COM, pin 1) by a one-out-of-N address decoder with open collector outputs. Opening all gates but one will then disable all but the desired output stage. Connecting the SYNC pin to $+V_S$ will also serve to stop the oscillator, but this is a less satisfactory multiplex mode. (Do not connect SYNC to GND or $-V_S$.)

SYNCHRONOUS OPERATION

The SYNC terminal at pin 2 can be used to synchronize a free running AD537 to a master oscillator, either as a multiple or a sub-multiple of the primary frequency. The preferred connection is shown in Figure 11. The diodes are used to produce the proper drive magnitude from high level signals. The SYNC terminal can also be used to shut off the oscillator. Shorting the terminal to $+V_S$ will stop the oscillator, and the output will go high (output NPN off).

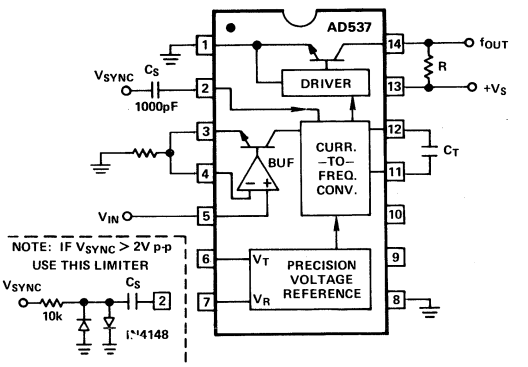


Figure 11. Connection for Synchronous Operation

Figure 12 shows the maximum pull-in range available at a given signal level; the optimum signal is a 0.8 to 1.0 volt square; signals below 0.1 volt will have no effect; signals above 2 volts p-p will disable the oscillator. The AD537 can normally be synchronized to a signal which forces it to a higher frequency up to 30% above the nominal free-running frequency, it can only be brought down about 1-2%.

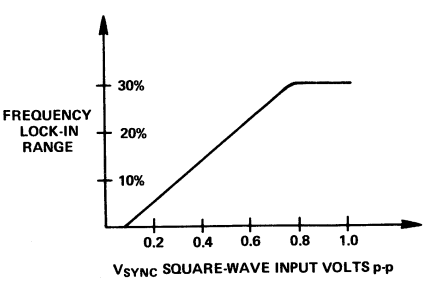


Figure 12. Maximum Frequency Lock-In Range Versus Sync. Signal

F-V CONVERTERS

The AD537 can be used as a high linearity VCO in a phase-locked loop to accomplish frequency-to-voltage conversion. By operating the loop without a low-pass filter in the feedback path (first-order system), it can lock to any frequency from zero to an upper limit determined by the design, and respond in three or four cycles to a step change of input frequency. In practice, the overall response time is determined by the characteristics of the averaging filter which follows the PLL.

Figure 13 shows a connection using a low-power TTL quad-nor open-collector gate which serves as the phase comparator. The input signal should be a pulse train or square wave with characteristics similar to TTL or 5-volt CMOS outputs. Any duty cycle is acceptable, but the minimum pulse width is 40μs. The output voltage is one volt for a 10kHz input frequency. The output as shown here is at a fairly high impedance level; for many situations an additional buffer may be required.

Trimming is similar to V-F application trimming. First set the V_{OS} trimmer to mid-scale. Apply a 10kHz input frequency and trim the 2kΩ potentiometer for 1.00 volts out. Then apply a 10Hz waveform and trim the V_{OS} for 10mV out. Finally, re-trim the full scale output at 10kHz. Other frequency scales can be obtained by appropriate scaling of timing components.

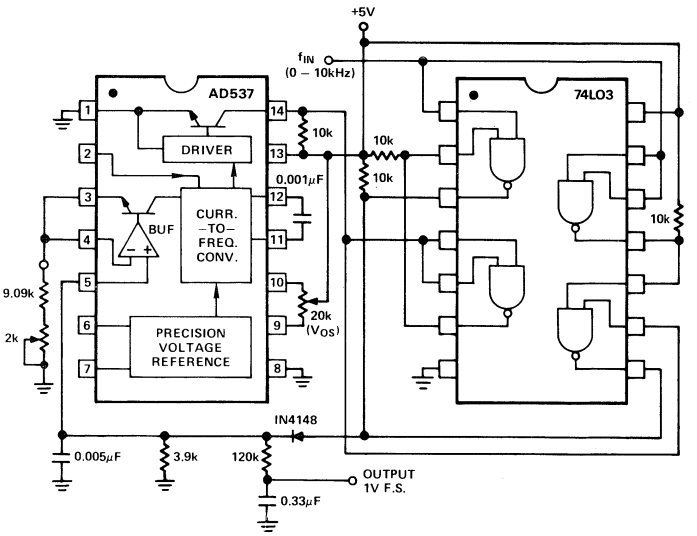


Figure 13. 10kHz F-V Converter

TEMPERATURE-TO-FREQUENCY CONVERSION

The linear temperature-proportional output of the AD537 can be used as shown in these applications to perform various direct temperature-to-frequency conversion functions; it can also be used with other external connections in a temperature sensing or compensation scheme. If the sensor output is used externally, it should be buffered through an op amp, since loading that point will cause significant error in the sensor output as well as in the main V-F converter circuitry.

The low nominal power requirement of the AD537 results in very low errors due to self-heating. To keep these errors at a minimum, use a single 5 volt supply and as large an output pull-up resistor as practical for the application (preferably at least 10kΩ).

An absolute temperature (° Kelvin) -to-frequency converter is very easily accomplished, as shown in Figure 13. The 1mV per °K output serves as the input to the buffer amplifier, which then scales the oscillator drive current to a nominal 298μA at +25°C (298°K). Use of a 1000pF capacitor results in a corresponding frequency of 2.98kHz. Setting the single 2kΩ trimmer for the correct frequency at a well-defined temperature near +25°C will normally result in an accuracy of ±2°C from -55°C to +125°C (using an AD537S). An NPO ceramic capacitor is recommended to minimize nonlinearity due to capacitance drift.

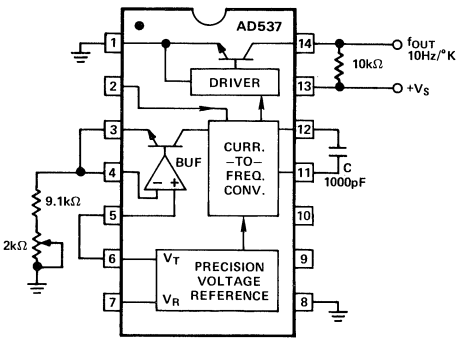


Figure 14. Absolute Temperature to Frequency Converter

OFFSET TEMPERATURE SCALES

Many other temperature scales can be set up by offsetting the temperature output with the voltage reference output. Such a scheme is shown by the Celsius-to-frequency converter in Figure 15. Corresponding component values for a Fahrenheit-to-frequency converter which gives 10Hz/°F are given in parentheses.

A simple calibration procedure which will provide ±2°C accuracy requires substitution of a 7.27k resistor for the series combination of the 6.04k with the 2k trimmer; then simply set the 500Ω trimmer to give 250Hz at +25°C.

High accuracy calibration procedure:

1. Measure room temperature in °K.
2. Measure temperature output at pin 6 at that temperature.
3. Calculate offset adjustment as follows:

$$\text{Offset Voltage (mV)} = \frac{V_{TEMP}\ \text{(pin 6) (mV)}}{\text{Room temp (°K)}} \times 273.2$$

4. Temporarily disconnect 49Ω resistor (or 500Ω pot) and trim 2kΩ pot to give the offset voltage at the indicated node. Reconnect 49Ω resistor.
5. Adjust slope trimmer to give proper frequency at room temperature (+25°C = 250Hz).
   Adjustment for °F or any other scale is analogous.

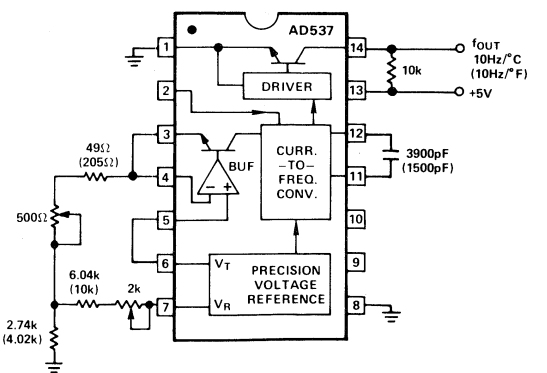


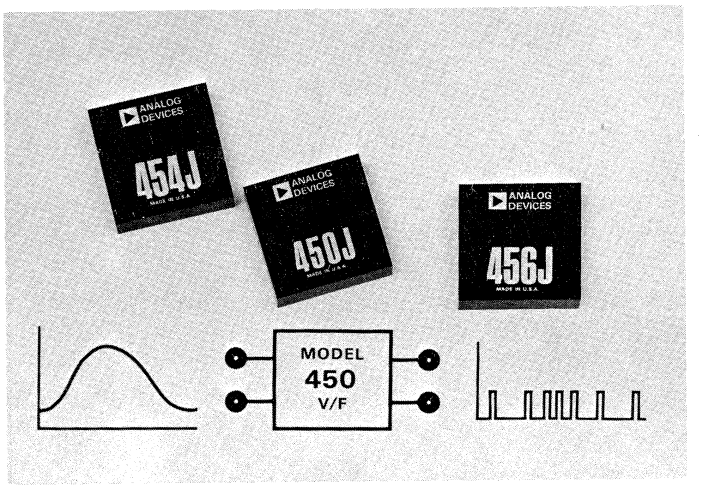
Figure 15. Offset Temperature Scale Converters-Centigrade and (Fahrenheit) to Frequency

Low Cost, High Performance, 10/20kHz Voltage to Frequency Converters

MODELS 450, 454, 456

FEATURES
- Low Cost
- Low Nonlinearity: ±50ppm max; Model 450K
- High Stability: ±25ppm/°C max; Model 450K
- Versatility: Voltage or Current Inputs; Model 454J/K
  - 10V or 20V Full Scale Inputs
  - Bipolar Inputs; Model 454J/K
- Wide Dynamic Range: >86dB; Model 454J/K
- Meet MIL-STD-202E Environmental Testing
- TTL/DTL or CMOS/HNIL Compatible Output

APPLICATIONS
- Long Term Precision Integrator
- Ratiometric Measurements
- High CMV Analog Isolator
- A/D Converter with 13 Bit Accuracy
- 2 Wire High Noise Immunity Digital Transmission



GENERAL DESCRIPTION

Models 450, 454 and 456 comprise a new family of modular voltage to frequency converters that provide exceptional linearity and temperature stability over a wide input signal dynamic range. Available in two convenient full scale frequency ranges of 10kHz or 20kHz, these new low cost models can be easily applied to perform ±0.01% analog measurements while directly interfacing with digital circuits.

WHERE TO USE MODELS 450, 454 AND 456

Pin compatible with existing popular models, these new designs offer economical solutions to a range of demanding applications; in Chemical Analysis and Gas Chomatography – as long-term precision integrators; in Process Control and Remote Data Acquisition Systems – two wire data transmission over long distances; in 3½ digit DVM's – as low cost A/D converters featuring monotonic 13-bit performance and no missing codes; in Blood Analysis – accurate ratiometric measurements over wide dynamic range; in Medical Instruments – isolation using single low cost optical isolator; in Test Instrumentation – as low cost programmable square wave generators.

MODEL SELECTION GUIDE

These compact modules are available in six versions with performance features aimed at meeting key application requirements:

Economy, 10kHz: Model 456 offers the lowest cost for applications requiring 0.1% (10-bit) accuracy. Available in two selection grades, model 456J has 0.03% max nonlinearity with 120ppm/°C max gain drift; model 456K offers 0.02% max nonlinearity and 80ppm/°C gain drift.

High Performance, 10kHz: For all general purpose applications, model 450 should be considered. Nonlinearity is 0.01% max (450J) and 0.005% max (450K) with full scale gain drift guaranteed at 50ppm/°C max (450J) and 25ppm/°C max (450K). Model 450K can achieve 0.01% (13-bit) accuracy over the 1mV to +15V signal range.

Versatility: Model 454 accepts 0 to +20V or 0 to 0.67mA inputs and can be operated with bipolar signals up to ±10V. Nonlinearity is 0.01% max (454J) and 0.005% max (454K); gain drift is 50ppm/°C max (454J) and 25ppm/°C max (454K).

DESIGN APPROACH – PRECISION CHARGE BALANCE

All models incorporate a superior charge balance technique that results in high linearity and temperature stability. Linearity is maintained for inputs below 1mV and operation is free of latch-up.

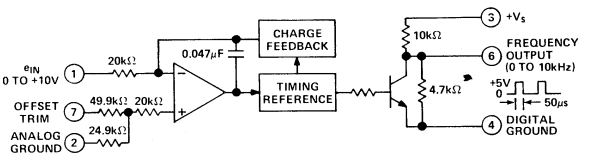


Figure 1. Block Diagram – Models 450 and 456

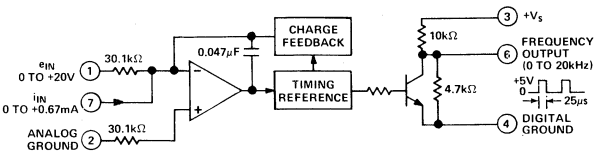


Figure 2. Block Diagram – Model 454

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	ECONOMY 10kHz 456 J	ECONOMY 10kHz 456 K	HIGH PERFORMANCE 10kHz 450 J	HIGH PERFORMANCE 10kHz 450 K	VERSATILE 20kHz 454 J	VERSATILE 20kHz 454 K
TRANSFER FUNCTION						
Voltage Input	$f_{OUT} = (10^3 \frac{Hz}{V}) e_{IN}$		$f_{OUT} = (10^3 \frac{Hz}{V}) e_{IN}$		$f_{OUT} = (10^3 \frac{Hz}{V}) e_{IN}$	
Current Input	–		–		$f_{OUT} = (3 \times 10^4 \frac{Hz}{mA}) i_{IN}$	
ANALOG INPUT						
Voltage Signal Range (e_{IN})	0 to +10V min		0 to +10V min		0 to +20V min	
Current Signal Range (i_{IN})	–		–		0 to 0.67mA min	
Overrange	50% min		50% min		10% min	
Impedance (e_{IN})	20kΩ		20kΩ		30kΩ	
Impedance (i_{IN})	–		–		0Ω	
Max Safe Input Voltage (e_{IN})	+25V, $-V_S$		+25V, $-V_S$		+25V, $-V_S$	
Max Safe Input Current (i_{IN})	–		–		+1mA	
ACCURACY						
Warm-Up Time	1 minute		1 minute		1 minute	
Nonlinearity						
e_{IN} = +1mV to +15V	±0.03% max	±0.02% max	±0.01% max	±0.005% max	–	
e_{IN} = +1mV to +22V	–		–		±0.01% max	±0.005% max
Full Scale Error[1]	(+½, +1½)% max		(+½, +1½)% max		(+½, +1½)% max	
Gain						
vs. Temperature (0 to +70°C)	±120ppm/°C max	±80ppm/°C max	±50ppm/°C max	±25ppm/°C max	±50ppm/°C max	±25ppm/°C max
vs. Supply Voltage	±400ppm/%		±200ppm/% max		±200ppm/% max	
vs. Time	±150ppm/day		±100ppm/day		±100ppm/day	
Input Offset Voltage[1]	±10mV		±5mV max		±5mV max	
vs. Temperature (0 to +70°C)	±100µV/°C max		±50µV/°C	±20µV/°C max	±50µV/°C	±20µV/°C max
vs. Supply Voltage	±10ppm/%		±10ppm/% max		±10ppm/% max	
vs. Time	±20µV/day		±10µV/day		±10µV/day	
RESPONSE						
Settling Time for +10V Step Input	120µs		120µs		120µs	
Overload Recovery Time	15ms		15ms		22ms	
OUTPUT[2]						
Waveform	train of TTL/DTL compatible pulses		train of TTL/DTL compatible pulses		train of TTL/DTL compatible pulses	
Pulse Width	50µs		50µs		25µs	
Rise/Fall Time	200ns/100ns		200ns/100ns		200ns/100ns	
Pulse Polarity	positive		positive		positive	
Logic "1" (High) Level	+2.4V min		+2.4V min		+2.4V min	
Logic "0" (Low) Level	+0.4V max		+0.4V max		+0.4V max	
Capacitive Loading	1000pF max		1000pF max		1000pF max	
Fan Out Loading	10 TTL loads min		10 TTL loads min		10 TTL loads min	
Impedance	3.3kΩ		3.3kΩ		3.3kΩ	
POWER SUPPLY[3]						
Voltage, Rated Performance	±15V dc		±15V dc		±15V dc	
Voltage, Operating	±(12 to 18)V dc		±(12 to 18)V dc		±(12 to 18)V dc	
Current, Quiescent	(+15, -9)mA		(+15, -9)mA		(+15, -9)mA	
TEMPERATURE RANGE						
Rated Performance	0 to +70°C		0 to +70°C		0 to +70°C	
Operating	-25°C to +80°C		-25°C to +80°C		-25°C to +80°C	
Storage	-55°C to +85°C		-55°C to +85°C		-55°C to +85°C	
CASE SIZE	1.5" x 1.5" x 0.4"		1.5" x 1.5" x 0.4"		1.5" x 1.5" x 0.4"	

[1] Adjustable to zero; refer to Adjustment Procedure on next page.
[2] Protected for continuous short-circuit to ground. CAUTION: DO NOT SHORT OUTPUT TO -15V SUPPLY.
[3] Recommended ADI power supply: model 904, ±15V @ 50mA

Specifications subject to change without notice.

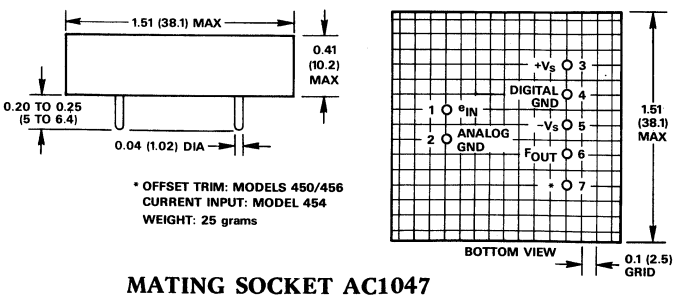
All Units Meet the Requirements of MIL-STD-202E as Outlined Below

TEST	METHOD	CONDITION
High Temperature Storage	108A	D (Non-Operating)
Moisture Resistance	106D	(10 Days)
Solderability	208C	
Thermal Shock	107D	A (5 Cycles)
Terminal Strength	211A	A (Pull Test; 10 lbs)
Temperature Cycling	102A	D (-55°C/+85°C)
Vibration	204C	B (15g Peak)
Barometric Pressure	105C	B (50,000 Feet)

TABLE 1. Environmental Specifications

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET AC1047

VOLTAGE TO FREQUENCY OPERATION

Models 450, 454 and 456 provide accurate conversion of analog signals into a train of constant width and constant amplitude pulses at a rate directly proportional to the analog signal amplitude. The output continuously tracts the input signal responding directly to changes in the input signal; external clock synchronization is not required. The output pulse train is TTL/DTL compatible, permitting direct interface to low cost digital processing circuits.

Dynamic Range: Models 450 and 456 accept unipolar, single ended input signals from 0V to +10V with 50% minimum overrange. The corresponding output frequency is dc to 10kHz. Model 454 is designed for either bipolar or unipolar single ended input signals. It accepts 0V to +20V or 0mA to 0.67mA input signals directly with 10% min overrange; the corresponding output frequency is dc to 20kHz.

ADJUSTMENT PROCEDURE

All models may be used directly with no external trim potentiometers required. Overall accuracy and dynamic range may be improved by using two optional trim adjustments as shown in Figures 3 and 4; FULL SCALE and OFFSET adjust. Low temperature coefficient trims must be used to maintain the drift specifications of the V/F model. The T.C. of the trim pot will add to the FULL SCALE DRIFT for each model.

Calibration Procedure: Allow a five minute warm-up after initial power turn on. Using a precision, stable voltage source, set the input voltage, e_{IN}, to +1.00mV. Adjust the OFFSET trim, R_O, for an output pulse interval of 1 second (1Hz). Set the input voltage to +10.000V and adjust the FULL SCALE trim for an output pulse interval of 100μs (10kHz). The V/F may now be used without further adjustment.

PERFORMANCE SPECIFICATIONS

Nonlinearity: Nonlinearity is specified as a % of full scale input: 10V for models 450 and 456; 20V for model 454 – and is guaranteed for each model over the specified input range: 0.005% max, models 450K and 454K; 0.01% max, models 450J and 454J; 0.03% max, model 456J and 0.02% max, model 456K. Typical nonlinearity performance is illustrated for model 450J in Figure 5. Below 1mV input, nonlinearity error remains within the specified limits, but is masked by zero offset stability, input noise and adjustment accuracy.

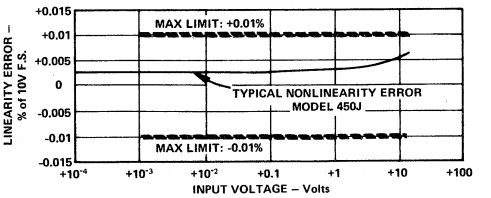


Figure 5. Model 450J: Nonlinearity Error Versus Input Signal

Gain Temperature Stability: Gain drift is specified in ppm of full scale and is guaranteed for each model over the 0 to +70°C temperature range. Typical performance is half the guaranteed limits.

OUTPUT FREQUENCY SCALING

Lowering Full Scale Frequency: The full scale frequency of a V/F converter can be reduced by three techniques; (1) adding a series trim potentiometer, such as 10kΩ, with the input; (2) adding a voltage divider network at the input; or (3) adding a digital divider at the output. Both input techniques (1) and (2), degrade the full scale gain drift by the added T.C. of the input resistors. By using a frequency divider connected to the V/F output, full scale frequency can be conveniently reduced without degradation of the converter's full scale drift performance. By adding successive frequency dividers, as illustrated in Figure 6, a precision, low cost, voltage controlled square wave generator can be designed.

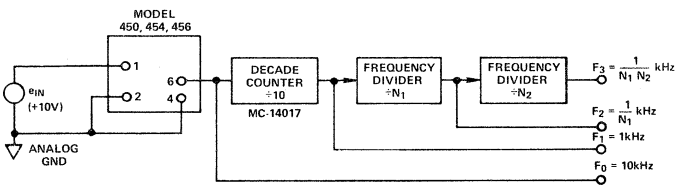


Figure 6. Voltage Controlled Square Wave Generator Using Digital Dividers and V/F Converter

Offsetting Full Scale Frequency; Model 454: The summing input terminal of model 454 (i_{IN} terminal) may be used to conveniently offset the output frequency to permit bipolar input signals up to ±10V, as well as improve the dynamic response to low level input signals. As shown in Figure 7, a

(continued on next page)

V/F INTERCONNECTION

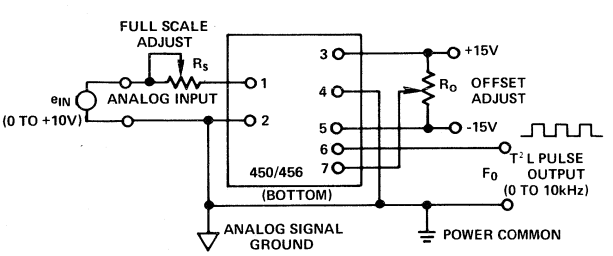


Figure 3. Models 450/456

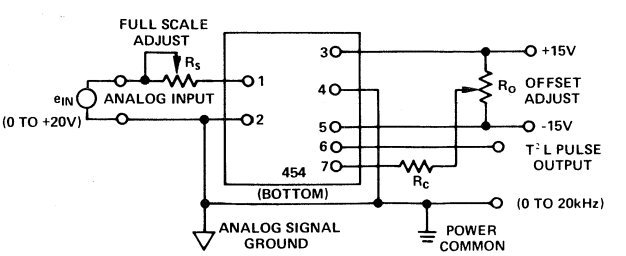


Figure 4. Model 454

EXTERNAL CONNECTIONS FOR VOLTAGE TO FREQUENCY OPERATION, WITH OPTIONAL INPUT OFFSET VOLTAGE AND FULL SCALE OUTPUT FREQUENCY ADJUSTMENTS

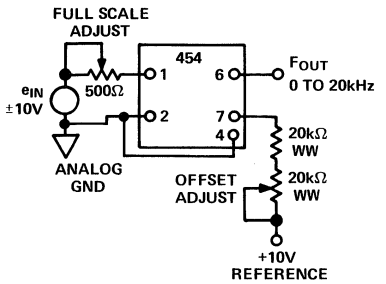
R_S = FULL SCALE ADJUSTMENT; 500Ω (Use low T.C. Cermet, <50ppm/°C or equivalent)
R_O = INPUT OFFSET ADJUSTMENT; 50kΩ (Use low T.C. Cermet, <50ppm/°C or equivalent)
R_C = 20MΩ

CAUTION: DO NOT SHORT OUTPUT TO -15V

(continued from previous page)

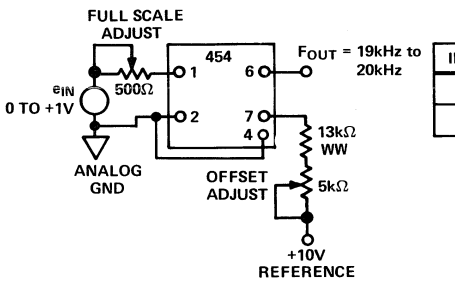
current is fed through an external resistor from a voltage reference to the current terminal. A low cost precision +10V voltage reference, such as ADI model AD2700, is recommended to retain the stability and accuracy of model 454.

As illustrated in Figure 8, the output may also be scaled up so that low amplitude signals – (i.e. e_{IN} = 1V) – will give full scale output frequency – (e_o = 20kHz). The step response for a 1 volt input change improves to only 50μs, compared to 1ms before offsetting.



INPUT	OUTPUT
+10V	20kHz
0	10kHz
-10V	0

Figure 7. Offsetting Model 454 Output for Bipolar Inputs



INPUT	OUTPUT
+1V	20kHz
0	19kHz

Figure 8. Offsetting Model 454 Output for Improved Dynamic Response

SQUARE WAVE OUTPUT

Using a type D flip-flop connected to the output of the V/F converter offers a simple low cost technique to obtain a voltage controlled, variable frequency, square wave signal; see Figure 9. Using model 454 with current offsetting, a 10kHz full scale square wave output can be achieved with 10V input signal.

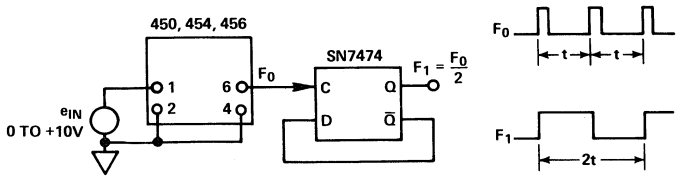


Figure 9. Square Wave Output Using Type D Flip-Flop

DRIVING HIGH NOISE IMMUNITY LOGIC

Adding a 680Ω resistor from the output terminal to the +15V supply provides 4V noise immunity for driving high noise immunity logic (HNIL) and CMOS logic (see Figure 10).

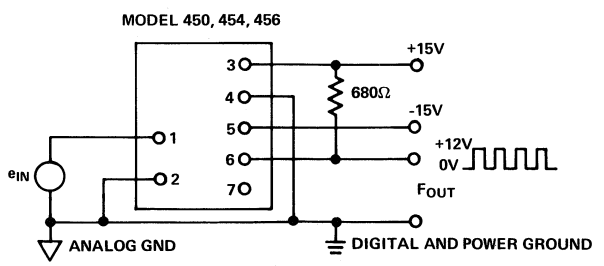


Figure 10. Driving High Noise Immunity Logic and CMOS

CURRENT TO FREQUENCY CONVERSION

In addition to accepting voltage inputs, models 450, 454 and 456 can be applied as very linear (to ±50ppm max) current to frequency (I/F) converters by the addition of a shunt input resistor network. As illustrated in Figure 11, 0 to 10mA inputs can be accurately converted using a 1kΩ shunt network. The current source must have a +10V compliance. In applications using low compliance current transducers, model 454, offering a direct current input capability, should be selected. Model 454 will convert input currents up to +0.67mA to frequencies up to 20kHz, without external components, if the input current is directly applied to the i_{IN} terminal (pin 7). By adding external resistor networks a full scale output can be achieved with greater input levels as shown in Figure 12. In this example model 454 is connected to convert 0 to 20mA signals to a 0 to 20kHz output frequency. All resistors must be low temperature coefficient types (wirewound or cermet) to ensure that accuracy will not be significantly degraded due to temperature changes and self-heating effects.

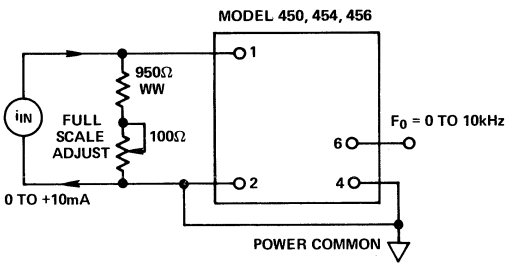


Figure 11. Current-to-Frequency Using Voltage Input Terminal

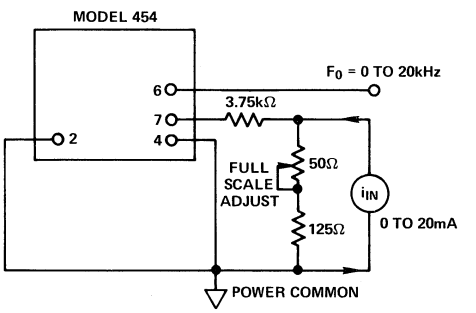


Figure 12. Current-to-Frequency Using Current Input Terminal

Interfacing 4–20mA Current Sources: By adding an offset current directly at the input as shown in Figure 13, model 454 can be applied to convert 4–20mA inputs to 0 to 10kHz frequencies.

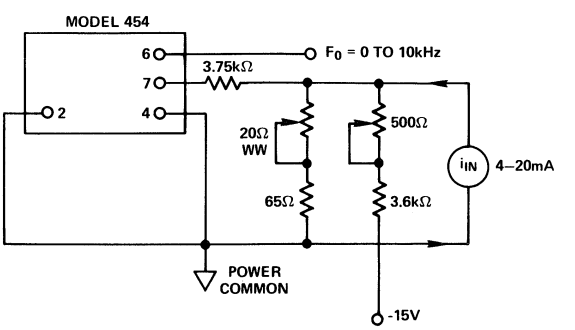


Figure 13. 4–20mA Interface Using Model 454

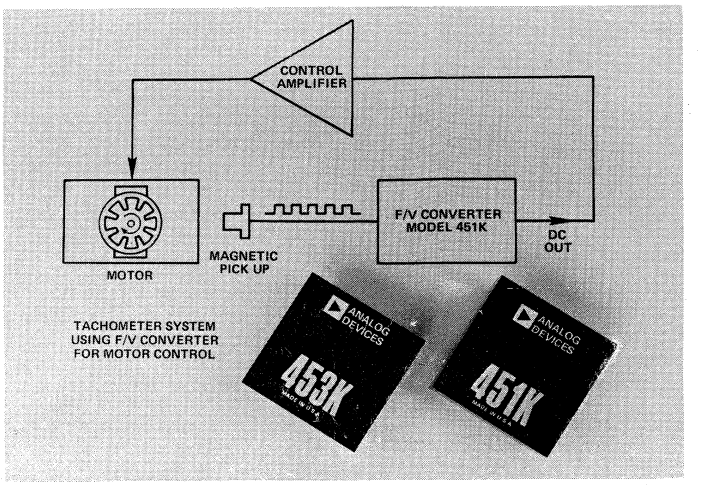
ANALOG DEVICES

Low Cost, Versatile, 10/100kHz Frequency to Voltage Converters

MODELS 451, 453

FEATURES
- **Low Cost**
- **Versatility: Adjustable Threshold, Gain & Output Offset**
- **Guaranteed Low Nonlinearity: 80ppm Max, 451L and 453L**
- **Accepts TTL, CMOS, HNIL, Sinewave, Pulse, Squarewave and Triangle Wave Input Signals**
- **No External Components to Meet Rated Performance**
- **+20mA Output to Operate Relays and Meters**
- **Low Profile Package, 0.4" Case Height**
- **Meet MIL-STD-202E Environmental Testing**

APPLICATIONS
- **Motor Control and Speed Monitor**
- **Line Frequency Monitor and Alarm Indicator**
- **Fluid Flow Measurements and Control**
- **FM Demodulation and VCO Stabilization**
- **Frequency vs. Amplitude Response Measurements**



GENERAL DESCRIPTION

Models 451 and 453 are low cost 10kHz and 100kHz frequency to voltage converters that feature excellent low nonlinearity to less than 80ppm, output current of +20mA and the capability of interfacing with TTL, HNIL, CMOS, sinewave, squarewave, pulse and triangular input signals. External components are not required to achieve rated performance, however, extreme versatility is maintained by allowing access to all critical points of the design. This versatility allows programmable input threshold, gain, and output offset voltage.

Both models 451 and 453 are available in three selections, each offering guaranteed maximum nonlinearity error as well as maximum gain drift error. Models 451J and 453J offer 0.03% max nonlinearity and 100ppm/°C max gain drift. Models 451K and 453K offer 0.015% max nonlinearity and 50ppm/°C max gain drift. Models 451L and 453L offer 0.008% max nonlinearity and 50ppm/°C max gain drift.

WHERE TO USE FREQUENCY TO VOLTAGE CONVERTERS

Pin compatible with existing popular models, these versatile new designs offer economical solutions to a wide variety of applications where it is required to convert frequency to an analog voltage.

Process Control Systems: For motor speed controllers, power line frequency monitoring and fluid flow measurements where flow transducers, such as variable reluctance magnetic pickups, provide pulse train outputs as a linear function of flow rate.

Audio and Accoustic Systems: For wow and flutter measurements with tape recorders and turntables, FM demodulation and speaker response measurements.

Test Instrumentation: For VCO stabilization, analog readout frequency meter, vibrational analysis and frequency versus amplitude X-Y plots where the vertical axis presents the normal amplitude signal and the horizontal axis presents the output signal from the F/V converter.

Data Acquisition Systems: For converting serially transmitted data back to analog voltages.

DESIGN FEATURES AND USER BENEFITS

The combination of low cost and high performance provided by models 451 and 453 offers exceptional quality and value to the OEM designer. These compact modules have been designed to provide maximum versatility, thereby increasing their utility in a broad scope of applications.

Adjustable Input Threshold: Threshold level is externally resistor programmable from 0 to ±12V, permitting simple, direct interface with low level signals, e.g. 10mV p-p, as well as with high level inputs such as CMOS and HNIL logic levels, e.g. 0 to +12V.

Adjustable Gain: Model 451 can be adjusted to provide full scale output voltage for any input frequency from 100Hz to 20kHz. Model 453 can be adjusted to provide full scale output voltage for any input frequency from 1kHz to 200kHz. This adjustable gain feature enables the user to easily match the maximum frequency output from a wide class of frequency transducers to the +10V full scale output from models 451 and 453. Increased signal conversion sensitivity with higher resolution results.

Adjustable Output Offset Voltage: The output offset is adjustable from -10V to +10V, enabling bipolar outputs or expanded scale measurements or setting the input frequency where zero output voltage occurs.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	10kHz FULL SCALE 451 J	451 K	451 L	100kHz FULL SCALE 453 J	453 K	453 L
TRANSFER FUNCTION	$E_O = (10^{-3}V/Hz)(F_{IN})$			$E_O = (10^{-4}V/Hz)(F_{IN})$		
FREQUENCY INPUT						
Frequency Range	dc to 10kHz min			dc to 100kHz min		
Overrange	10% min			10% min		
Waveforms	Sine, Square, Triangle, Pulse Train			Sine, Square, Triangle, Pulse Train		
Pulse Width (Pulse Train Input)	20µs min			2µs min		
Threshold	+1.4V			+1.4V		
With External Adjustment	0V to ±12V			0V to ±12V		
Hysteresis	±50mV			±100mV		
Levels (TTL Compatible) High	+1.45V to +12V			+1.5V to +12V		
Low	-12V to +1.35V			-12V to +1.3V		
Max Safe Input Voltage[1]	±V_S			±V_S		
Impedance	10MΩ‖10pF			10MΩ‖10pF		
ACCURACY						
Warm-Up Time	one minute			one minute		
Nonlinearity[2]						
F_{IN} = 1Hz to 11kHz	±0.03% max	±0.015% max	±0.008% max	–	–	–
F_{IN} = 1Hz to 110kHz	–	–	–	±0.03% max	±0.015% max	±0.008% max
Gain vs. Temperature[3] (0 to +70°C)	±100ppm/°C max	±50ppm/°C max	±50ppm/°C max	±100ppm/°C max	±50ppm/°C max	±50ppm/°C max
vs. Supply Voltage	±300ppm/%			±350ppm/%		
vs. Time	±30ppm/month			±30ppm/month		
RESPONSE						
Step Response to ±0.5% of Final Value						
F_{IN} = dc to Full Scale	4ms			0.8ms		
F_{IN} = Full Scale to dc	30ms			4ms		
Internal Filter Time Constant	200µs			24µs		
External Filter Time Constant	20ms/µF			20ms/µF		
OUTPUT[4]						
Voltage (F_{IN} = Full Scale)[5]	+9.85V min; +9.95V max			+9.85V min; +9.95V max		
Current (E_O = +10V, -10V)	(+20, -2)mA min			(+20, -2)mA min		
Offset Voltage[6] @ +25°C	±7.5mV max			±7.5mV max		
vs. Temperature (0 to +70°C)	±30µV/°C max			±30µV/°C max		
vs. Supply Voltage	±100µV/% max			±50µV/% max		
vs. Time	±100µV/month			±100µV/month		
Ripple						
F_{IN} = 1Hz	3mV p-p			55mV p-p		
F_{IN} = 10kHz	80mV rms			35mV rms		
F_{IN} = 100kHz	–			35mV rms		
Impedance	0.1Ω			0.1Ω		
Offset Scale Factor[7]	-56µA/V			-45µA/V		
POWER SUPPLY[8]						
Voltage, Rated Performance	±15V dc			±15V dc		
Voltage, Operating	±(12 to 18)V dc			±(12 to 18)V dc		
Current, Quiescent	(+10, -8)mA			(+10, -8)mA		
TEMPERATURE RANGE						
Rated Performance	0 to +70°C			0 to +70°C		
Operating	-25°C to +85°C			-25°C to +85°C		
Storage	-55°C to +85°C			-55°C to +125°C		
MECHANICAL						
Case Size	1.5" x 1.5" x 0.4"			1.5" x 1.5" x 0.4"		
Weight	25 grams			25 grams		
Mating Socket	AC1050			AC1050		

[1] F_{IN} and REF terminals can be shorted to ±V_S indefinitely without damage.
[2] Nonlinearity error is specified as a percentage of 10V full scale output level.
[3] Gain temperature drift is specified in ppm of output signal level.
[4] OUT terminal can be shorted indefinitely to ±V_S and ground without damage.
[5] Adjustable to +10.000V using FULL SCALE ADJUST trim pot.
[6] Adjustable to zero using 50kΩ OFFSET ADJUST trim pot.
[7] Current into the SUM PT terminal to offset the output voltage positive.
[8] Recommended power supply, ADI model 904, ±15V @ ±50mA output

Specifications subject to change without notice.

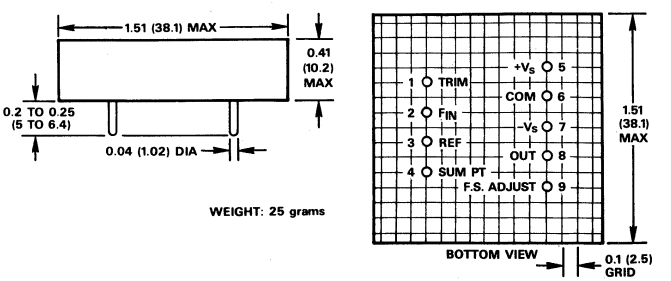
All Units Meet the Requirements of MIL-STD-202E as Outlined Below

TEST	METHOD	CONDITION
High Temperature Storage	108A	D (Non-Operating)
Moisture Resistance	106D	(10 Days)
Solderability	208C	
Thermal Shock	107D	A (5 Cycles)
Terminal Strength	211A	A (Pull Test; 10 lbs)
Temperature Cycling	102A	D (-55°C/+85°C)
Vibration	204C	B (15g Peak)
Barometric Pressure	105C	B (50,000 Feet)

TABLE 1. Environmental Specifications

OUTLINE DIMENSIONS

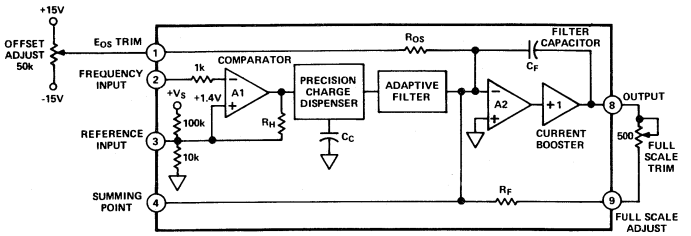
Dimensions shown in inches and (mm)



MATING SOCKET AC1050

FREQUENCY TO VOLTAGE OPERATION

Models 451 and 453 accept virtually any signal waveshape providing accurate conversion into an output voltage proportional to the input signal frequency. The only restriction is that the input signal must remain above the threshold level for 20μs when using model 451, and 2μs when using model 453. Linear, stable conversion over four decades of input range for model 451 and five decades of input range for model 453, is achieved using a precision charge-dispensing design approach. Figure 1 represents a functional block diagram for both models 451 and 453 frequency to voltage converters.



MODEL	C_F	R_{OS}	R_H	R_F
451	0.015μF	3.3MΩ	2.2MΩ	18kΩ
453	0.001μF	3.9MΩ	1.0MΩ	22kΩ

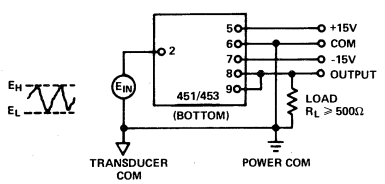
Figure 1. Block Diagram — Models 451 & 453 F/V Converters

THEORY OF OPERATION

Input signals are applied directly to a comparator, A1, which is internally set to provide a +1.4V threshold with ±50mV hysteresis for model 451 and ±100mV hysteresis for model 453. This threshold level offers excellent noise immunity for TTL input levels. Following the input comparator is a precision charge dispensing circuit and output amplifier where the comparator signal is converted to a dc voltage. When the input comparator changes state, C_C is alternately charged from a precision voltage reference and discharged through the summing point of an output amplifier, A2. A fixed amount of charge, Q, is controlled during each charge/discharge cycle. The higher the input frequency, the higher the average current into the summing point of A2. A current to voltage conversion is then accomplished by R_F. The current pulses from the charge dispensing circuit are integrated by C_F to reduce ripple. Added filtering for low frequency input signals is provided by an adaptive filter at the output of the charge dispensing circuit.

BASIC F/V HOOK-UP

Models 451 and 453 can be applied directly to achieve rated performance without external trim potentiometers or other components. Figure 2 illustrates the basic wiring connection for either F/V converter model. Using the basic hookup as shown, full scale output voltage accuracy is +10V, -½% to -1½%. The output offset voltage is 0V to ±7.5mV. The Full Scale and Output Offset errors can be eliminated by using the FINE TRIM PROCEDURE.



MODEL	INPUT VOLTAGE RANGE		INPUT FREQUENCY RANGE
	High (E_H)	Low (E_L)	(F_{IN})
451	+1.45V to +12V	-12V to +1.35V	0 to 11kHz
453	+1.5V to +12V	-12V to +1.3V	0 to 110kHz

Figure 2. Basic Wiring Interconnection

FINE TRIM PROCEDURE

Connect the F/V converter as shown in Figure 3 and allow a five minute warm-up after initial power turn-on. Adjust the OFFSET ADJUST pot, R_O, for an output of 0.000V. The input terminal, F_{IN}, can be left open or tied to COM without affecting OFFSET ADJUST. Using a precision, stable frequency source connected to F_{IN} terminal, set the input frequency to 10.000kHz for model 451 or 100.000kHz for model 453. Adjust the FULL SCALE ADJUST trim pot, R_S, for an output of +10.000V.

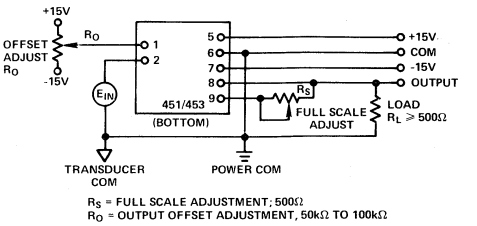


Figure 3. Wiring Interconnection Showing Fine Adjustment Trims for Offset and Full Scale Frequency

ADDITIONAL TRIM CAPABILITY

Adjusting Input Threshold: The input comparator of models 451 and 453 shown in Figure 1, conditions the input signals providing protection against noisy environments as well as preventing double triggering with slow rise-time signals. Input levels up to the supply voltages, $\pm V_S$, will not cause damage to the input comparator.

Threshold voltage level, V_T, is internally set for both models 451 and 453 at +1.4V. Hysteresis, V_H, for model 451 is ±50mV, and ±100mV for model 453. Signals of virtually any waveshape which exceed the combined threshold and hysteresis levels, $V_T \pm V_H$, will trigger the F/V converter. The REF terminal permits the user to conveniently adjust the input threshold over the range fron. 0 to ±12V to achieve optimum noise rejection or increased triggering sensitivity.

Increasing Threshold for Greater Noise Immunity: Connecting an external resistor from the REF terminal to the positive supply voltage, $+V_S$, increases the input threshold level above +1.4V, offering increased input noise immunity. Optimum noise immunity is generally determined by adjusting the threshold level to a point mid-way between the high and low input signal levels. For example, for a 0 to +12V input swing — representative of CMOS and HNIL logic signals — a 17.6kΩ resistor from +15V to the REF terminal results in a +6V threshold.

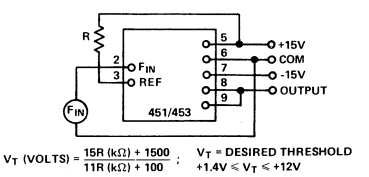


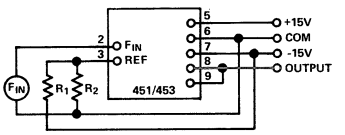
Figure 4. Increasing Threshold Above +1.4V for Greater Noise Immunity

Changes in impedance at the REF terminal result in changes to the hysteresis. Hysteresis levels can be calculated by assuming the comparator output is switching between ±12V. This ±12V signal is attenuated by a resistor-divider network formed by

R_H (see Figure 1) and the parallel combination of all resistors attached at the comparator positive input. For example, with a 17.6kΩ resistor connected to the REF terminal, hysteresis becomes ±35mV for model 451 and ±75mV for model 453. The F/V converter will, therefore, trigger at +6V ±35mV for model 451 and +6V ±75mV for model 453.

Decreasing Threshold for Signals Less Than +1.4V: A resistor connected from the REF terminal to the negative power supply, $-V_S$, will increase the input triggering sensitivity for operation with signals below $+1.4V_{PK}$. As shown in Figure 5, a minimum threshold of zero volts is obtained with a 100kΩ resistor. The triggering level, $V_T \pm V_H$, will be established by the resulting hysteresis levels. With a 100kΩ to -15V, model 451 hysteresis will be ±50mV and model 453 hysteresis will be ±60mV.

To reduce the hysteresis for greater triggering sensitivity, a 1kΩ resistor can be connected from the REF terminal to COM. Signals exceeding ±5mV (10mV p-p) with model 451 and ±15mV (30mV p-p) for model 453, will operate the F/V converter. A 1kΩ resistor from REF to COM is the minimum value recommended to reduce hysteresis and achieve reliable operation.



MODEL	R_1	R_2	THRESHOLD (V_T)	HYSTERESIS (V_H)	TRIGGER LEVELS ($V_T \pm V_H$)
451	∞	∞	+1.4V	±50mV	+1.45V; +1.35V
	100kΩ	∞	0V	±20mV	±20mV (40mV p-p)
	100kΩ	1kΩ	0V	±5mV	±5mV (10mV p-p)
453	∞	∞	+1.4V	±100mV	+1.5V; +1.3V
	100kΩ	∞	0V	±60mV	±60mV (120mV p-p)
	100kΩ	1kΩ	0V	±15mV	±15mV (30mV p-p)

Figure 5. Decreasing Threshold Below +1.4V to Increase Triggering Sensitivity for Low Level Input Signals

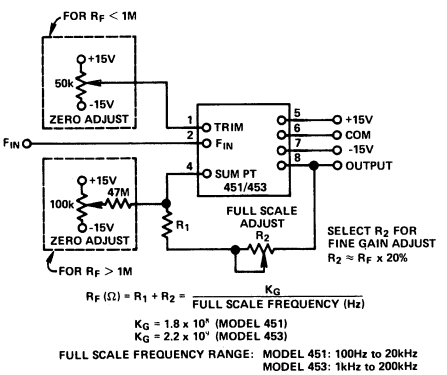


Figure 6. Selecting External Gain Resistor R_F

Adjusting Gain: Connect the FULL SCALE ADJUST terminal to the OUTPUT terminal to set the gain of model 451 at 10^{-3}V/Hz for a 10kHz full scale input frequency and the gain of model 453 at 10^{-4}V/Hz for a 100kHz full scale input frequency. Connecting an external resistor from the SUM PT terminal to the OUTPUT terminal and leaving the FULL SCALE ADJUST terminal open, facilitates gain adjustment. Model 451 can be adjusted over the range from 10^{-1}V/Hz to 5 x 10^{-4}V/Hz resulting in a full scale input frequency from 100Hz to 20kHz respectively. The gain of model 453 can be adjusted over the range from 10^{-2}V/Hz to 5 x 10^{-5}V/Hz resulting in a full scale input frequency from 1kHz to 200kHz respectively. The gain adjustment procedure is capable of increasing full scale frequency beyond the rated ranges for each model, however, nonlinearity will increase above 300ppm.

When using large values of R_F to externally set gain of the F/V converter, the output amplifier gain increases resulting in an increase in sensitivity when using the OFFSET ADJUST trim pot. For improved resolution in high gain applications ($R_F >$ 1MΩ), an alternate method of trimming offset is shown in Figure 6.

Offsetting the Output: The output of models 451 and 453 can be offset over the range from -10V to +10V, enabling scale expansion for increased signal sensitivity as well as bipolar output swings up to 20V p-p.

Current introduced at the SUM PT terminal results in shifts of the output voltage directly proportional to the Offset Scale Factor, K_S. For model 451, K_S = -56μA/V and for model 453, K_S = -45μA/V. The offset current can be generated using an external resistor from a voltage reference to the SUM PT terminal. A stable, well regulated supply voltage, such as ADI's model 904 is recommended. To shift the output positive, 0 to +10V, connect the current resistor to the negative, $-V_S$ supply. To shift the output negative, 0 to -10V, connect the current resistor to the positive, $+V_S$, supply.

The example using model 451 illustrated in Figure 7 provides a 0 to +5V output change in response to a 5kHz to 10kHz input change. With this input, a bipolar output from -2.5V to +2.5V can be obtained by increasing the output voltage shift from -5V, (R_C = 53.6kΩ) to -7.5V, (R_C = 35.7kΩ).

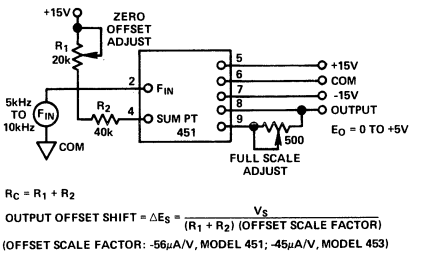


Figure 7. Selecting External Output Offset Resistor, R_C

SCALE EXPANSION

By combining both gain and output offset voltage adjustments, signals which exhibit a center frequency with small frequency changes, can be converted with improved resolution. Representative signals benefiting from the Scale Expansion procedure outlined below, are tachometer and frequency modulated signals. In the case of tachometer outputs, the speed is often set at an idle point and changes in output frequency represent changes in motor loading conditions. In the case of FM signals, the F/V converter can be applied such that the carrier frequency produces zero output. The resulting output voltage from the F/V converter represents the modulating signal.

Procedure for Scale Expansion: The following procedure incorporates both gain and output offset adjustments to achieve scale expansion. An example is illustrated in Figure 8 for an FM signal with a 50kHz carrier frequency and ±5kHz modulating signal.

1) Determine the Gain: $G = \Delta E_O / \Delta F_{IN}$ where ΔE_O is the total output voltage change desired in volts, and ΔF_{IN} is the total input frequency change in Hz.

2) Calculate the external gain resistor, R_F;
   $R_F(\Omega) = G(1.8 \times 10^7)$, model 451
   $R_F(\Omega) = G(2.2 \times 10^8)$, model 453

3) Calculate the Output Offset Shift, ΔE_S, required to achieve the desired maximum output voltage, E_O (max) with the max input frequency, F_{IN} (max), and the new gain;

$$\Delta E_S \text{ (volts)} = G\, F_{IN} \text{ (max)} - E_O \text{ (max)}$$

4) Calculate the offset current resistor, R_C;

$$R_C\ (\Omega) = \frac{V_S\, G}{(\Delta E_S)\,(k_s)}$$

$k_s = 56 \times 10^{-9}$, model 451
$k_s = 45 \times 10^{-10}$, model 453

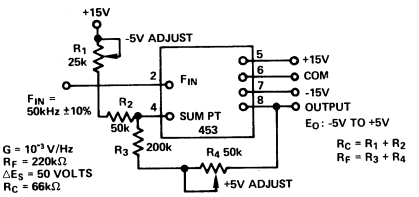


Figure 8. Application of Model 453 in FM Demodulation

INTERFACING SIGNALS WITH DC OFFSETS > 10V

Signals with dc levels up to ±10V can be directly connected to the input terminal of models 451 and 453. Capacitive coupling, as shown in Figures 9 and 10, is used for inputs with dc offsets greater than ±10V. The 1MΩ resistor illustrated in Figure 9 provides a dc return path to power common for the input comparator bias current. Threshold adjustments can be made following the capacitor, to set the F/V input sensitivity to match the ac signal peak-to-peak amplitude. Signals as low as 10mV p-p with model 451 and 30mV p-p model 453 are acceptable. Refer to Figures 4 and 5.

AC signals greater than $\pm V_S$ should be attenuated with a resistive divider network following the capacitor. When large input transients ($>\pm V_S$) are possible due to either a noisy environment or power turn-on surges, protection is provided with the addition of two diodes as shown in Figure 10.

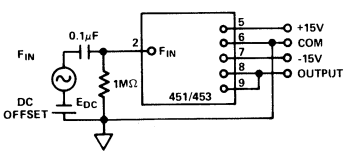


Figure 9. Interfacing Signals With DC Offsets Greater Than ±10V

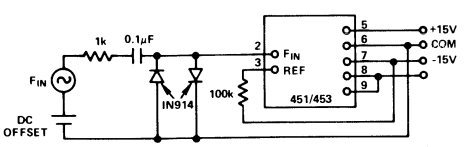


Figure 10. Input Diode Protection for High Voltage Transients

PERFORMANCE SPECIFICATIONS

Nonlinearity: Nonlinearity error is specified as a % of 10V full scale output voltage and is guaranteed for each model over the specified input range. Model 451 is rated over 1Hz to 11kHz range and model 453 is rated over 1Hz to 110kHz range. Typical nonlinearity performance is shown for all models in Figure 11.

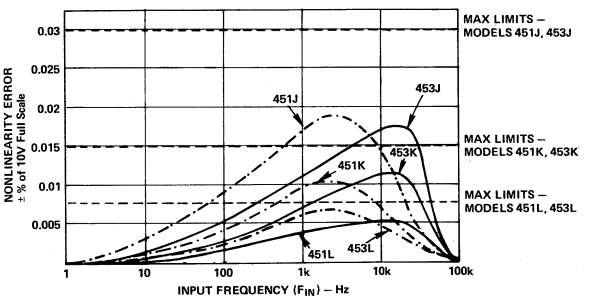


Figure 11. Nonlinearity Error Versus Input Frequency

Gain Temperature Stability: Gain Drift is specified in ppm of output signal and is guaranteed for each model over the 0 to +70°C temperature range. Models 451K, 451L, 453K and 453L offer ±50ppm/°C maximum gain drift. Models 451J and 453J offer ±100ppm/°C maximum gain drift. Gain drift is typically half the guaranteed limits.

OUTPUT RIPPLE

The output contains an ac ripple signal which increases in amplitude with input frequency. Adding external capacitance in parallel with the internal filter capacitor will reduce output ripple as shown in Figures 12 and 13.

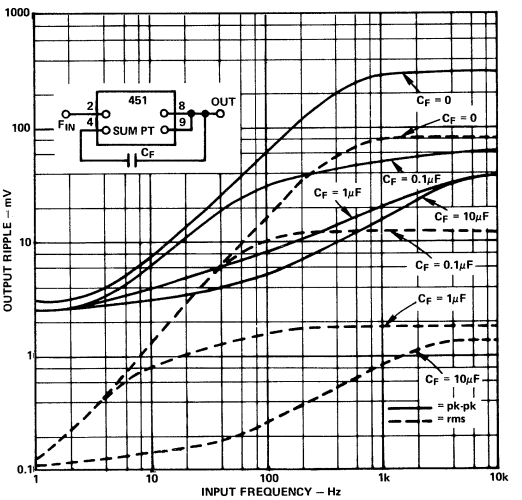


Figure 12. Output Ripple Versus External Filter Capacitor (C_F) – Model 451

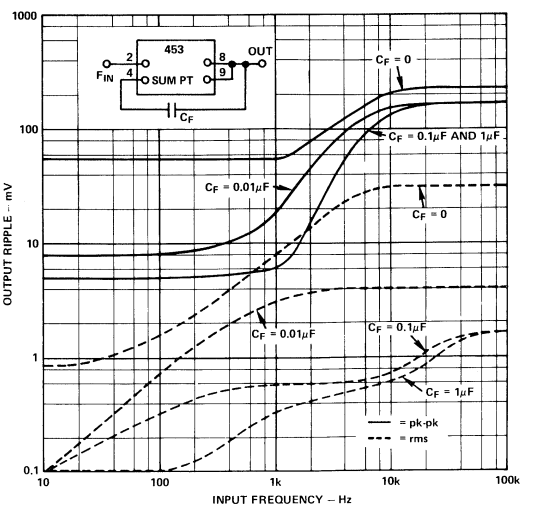


Figure 13. Output Ripple Versus External Filter Capacitor (C_F) – Model 453

SETTLING TIME

Increasing the external filter capacitor to reduce output ripple will increase the settling time to step changes in frequency occurring at the input. Figure 14 shows curves of settling time to ±0.5% of final value for both increasing and decreasing full scale step changes. As C_F increases in value, the total filter time constants for models 451 and 453 approach equal values, resulting in identical settling time.

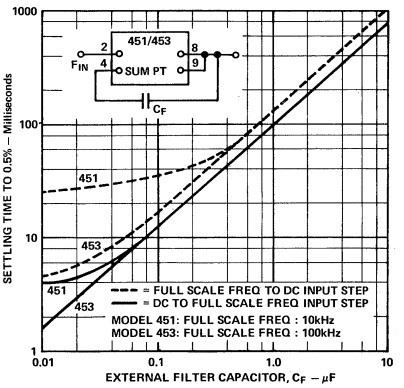


Figure 14. Settling Time Versus External Filter Capacitor

APPLICATIONS IN PROCESS CONTROL SYSTEMS

MOTOR CONTROLLER

In making rpm measurements, transducers are often encountered that have pulse-train outputs from variable-reluctance magnetic pickups (in which the output frequency is a function of rpm). These low level signals are generally in the range of 0 to 200mV peak. The adjustable input threshold feature of models 451 and 453 enables direct connection to low level transducers, offering simple, reliable interfacing.

The motor speed control and monitoring application shown in Figure 15 illustrates the F/V converter applied in a closed loop control system. R1 sets the threshold to +60mV with ±50mV hysteresis for model 451.

The +20mA output current capability of both models 451 and 453, enables direct interface to low impedance loads, up to 500Ω, such as analog meters or relays.

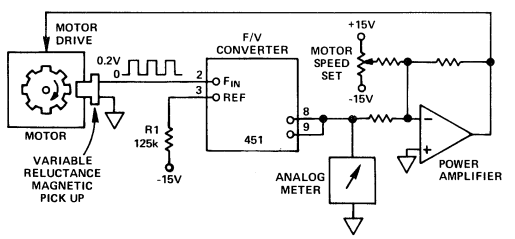


Figure 15. Application of F/V Converter to Control and Monitor Motor Speed in Closed Loop System

SPEED SWITCH

With the addition of a low cost comparator and relay, the F/V converter provides a reliable approach to controlling heavy generator loads after the generator has reached a specified speed. As shown in Figure 16, the relay will remain open until the output from the F/V converter reaches a preset POWER ON trip level. The F/V output signal is linearly related to the speed of the motor, permitting precise control of the POWER ON set point.

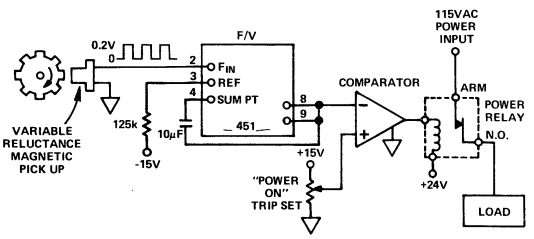


Figure 16. Application of F/V Converter to Control Load Power

APPLICATION IN INSTRUMENTATION SYSTEMS

FREQUENCY MONITORING

Small input frequency changes can be monitored more readily by using the programmable gain feature of models 451 and 453 to achieve greater signal sensitivity. In the application of model 451 illustrated in Figure 17, gain has been set to 0.1V/Hz, resulting in a 100Hz full scale frequency range. The output resolution for small changes occurring in the 60Hz line frequency has been improved. An additional advantage of this approach is the reduced accuracy and stability requirements placed on the relay trip levels, set by the voltage levels at the comparators. A precision voltage reference supply is not required.

Since both models 451 and 453 tolerate input signals up to the supply levels, $\pm V_S$, costly input protection is eliminated in most applications.

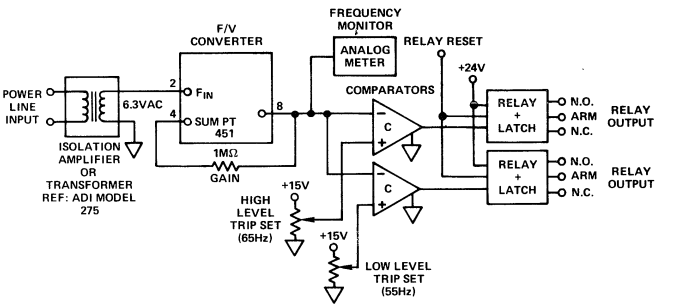


Figure 17. Application of F/V Converter to Monitor 60Hz Line Frequency

APPLICATION IN DATA ACQUISITION SYSTEMS

HIGH NOISE IMMUNITY TRANSMISSION

F/V converters are excellent companion products to V/F converters for use in low cost, two wire data transmission systems. As shown in Figure 18, this V/F/V approach utilizes the continuous self-clocking feature of the V/F converter thereby eliminating the need for costly additional twisted pair cable for external synchronization. Model 610 instrumentation amplifier amplifies the low level differential transducer signal to the 10V full scale of models 450 and 456 10kHz V/F converters. A differential line driver is used to drive a twisted pair cable through a noisy environment. A differential line receiver is used to drive model 451 10kHz F/V converter. The low cost of the V/F and F/V converters in addition to the simple twisted pair cabling approach make it economical to use a V/F/V converter pair for each channel in a data acquisition system.

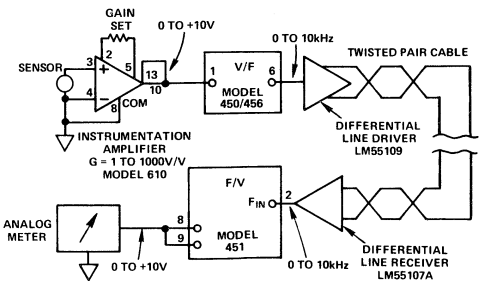


Figure 18. Application of F/V Converter in a Low Cost, High Noise Rejection Two-Wire Data Transmission System

Low Cost, General Purpose, 100kHz Voltage to Frequency Converter

MODEL 452

FEATURES
- Wide Dynamic Range: 100μV to 11V
- Versatility: Voltage or Current Inputs
  Bipolar Inputs: 10V p-p
- High Stability: 50ppm/°C max; Model 452L
- Low Nonlinearity: 150ppm max
- Meet MIL-STD-202E Environmental Testing
- TTL/DTL or CMOS/HNIL Compatible Output

APPLICATIONS
- Long Term Precision Integrator
- Ratiometric Measurements
- High CMV Analog Isolator
- A/D Converter with >16 Bit Resolution
- 2 Wire High Noise Immunity Digital Transmission

GENERAL DESCRIPTION

Model 452 is a low cost 100kHz voltage to frequency converter with performance features that make it an excellent choice for all analog-to-digital applications. This design offers resolution of better than 16 bits with low nonlinearity error of 0.015% max for overall accuracy of greater than 12 bits. While directly interfacing digital circuits, this new low cost model also offers inherently high noise rejection, monotonic performance and no missing codes over the complete 0 to +70°C operating temperature range.

Offering the versatility of either current or voltage inputs, model 452's excellent low nonlinearity over the complete signal ranges (100μV to 11V or 5nA to 550μA) is guaranteed to be less than 0.015% of full scale. Three low drift selections are available offering guaranteed full scale drift error; model 452L: 50ppm/°C max; model 452K: 100ppm/°C max; model 452J: 150ppm/°C max.

Supplied in a compact epoxy module, no external adjustments or components are required to achieve rated performance; optional adjustments are available for trimming full scale frequency and input offset voltage. Optional scaling is also available for bipolar input signals and to improve dynamic response.

WHERE TO USE MODEL 452

Pin compatible with existing popular models, this new design offers an economical solution to a range of demanding applications: in Chemical Analysis and Gas Chromatography — as long-term precision integrators; in Process Control and Remote Data Acquisition Systems — two wire data transmission over long distances; in 4 digit DVM's — as A/D converters featuring monotonic 16 bit performance, no missing codes, lower power, lower price and high noise rejection; in Blood Analysis — accurate ratiometric measurements over wide dynamic range; in Medical Instruments — isolation using a single low cost optical isolator; in Test Instrumentation — as low cost programmable square wave generators.

DESIGN FEATURES AND USER BENEFITS

Adjustable Scaling: The current input terminal of model 452 can be used to conveniently shift full scale frequency to achieve faster conversion rates in analog-to-digital applications. (See OFFSETTING INPUT). An offset current of 50μA, equivalent to a 1V input signal, will shift the full scale output from 100kHz to 110kHz. This will result in an improvement of conversion time from 10ms to 1μs, for a 10mV input signal.

Bipolar Inputs: Bipolar input signals up to 10V peak-to-peak range can be converted by using the summing input terminal to offset the input. (See OFFSETTING INPUT). When counted by a binary counter, the digital output will be offset-binary-coded (identical to 2's complement with the most significant bit complemented).

DESIGN APPROACH — PRECISION CHARGE BALANCE

Model 452 incorporates a superior charge balance design that results in high linearity and temperature stability — see Figure 1. Linearity is maintained for inputs below 0.1mV and operation is free of latch-up.

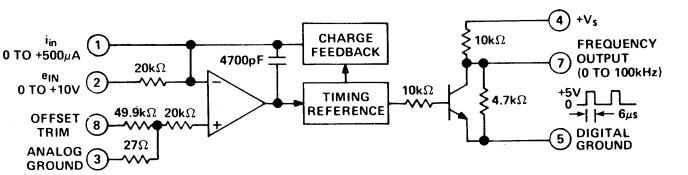


Figure 1. Block Diagram — Model 452

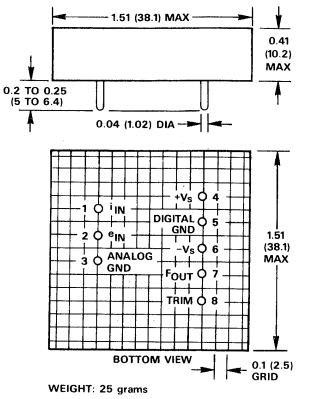
SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	452J	452K	452L
ANALOG INPUT			
Voltage Signal Range (e_{in})	0 to +10V dc min	*	*
Current Signal Range (i_{in})	0 to +0.5mA min	*	*
Overrange	10% min	*	*
Impedance (e_{in})	20kΩ	*	*
Impedance (i_{in})	0Ω	*	*
Max Safe Input Voltage (e_{in})	+25V, $-V_S$	*	*
Max Safe Input Current (i_{in})	±5mA	*	*
TRANSFER FUNCTION			
Voltage Input	$f_{out} = (10^4 \frac{Hz}{V})e_{in}$	*	*
Current Input	$f_{out} = (2 \times 10^5 \frac{Hz}{mA})i_{in}$	*	*
ACCURACY			
Warm-Up Time	10 minutes	*	*
Nonlinearity			
e_{in} = +0.1mV to +11V	±0.015% of F.S. max	*	*
i_{in} = +5nA to +550μA	±0.015% of F.S. max	*	*
Full Scale Error[1]	(+½, +1½)%	*	*
Gain			
vs. Temperature (0 to +70°C)	±150ppm/°C max	±100ppm/°C max	±50ppm/°C max
vs. Supply Voltage	±300ppm/%	*	*
vs. Time	±25ppm/day	*	*
Input Offset Voltage[1]	±7.5mV max	*	*
vs. Temperature (0 to +70°C)	±30μV/°C max	*	*
vs. Supply Voltage	±50μV/%	*	*
vs. Time	±10μV/day	*	*
RESPONSE			
Settling Time for +10V Step Input	22μs	*	*
Overload Recovery Time	1.5ms	*	*
OUTPUT[2]			
Waveform	Train of TTL/DTL Compatible Pulses	*	*
Pulse Width	6μs	*	*
Rise/Fall Time	200ns/50ns	*	*
Pulse Polarity	Positive	*	*
Logic "1" (High) Level	+2.4V min	*	*
Logic "0" (Low) Level	+0.4V max	*	*
Capacitive Loading	1500pF max	*	*
Fan Out Loading	10 TTL Loads min	*	*
Impedance (Logic "1" Level)	3.3kΩ	*	*
POWER SUPPLY[3]			
Voltage, Rated Performance	±15V dc	*	*
Voltage, Operating	±(12 to 18)V dc	*	*
Current, Quiescent	(+25, -10)mA	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	*
Operating	-25°C to +85°C	*	*
Storage	-55°C to +85°C	*	*
CASE SIZE	1.5" x 1.5" x 0.4"	*	*

*Specifications same as model 452J.
[1] Adjustable to zero
[2] Protected for continuous short circuit to ground. CAUTION: DO NOT SHORT OUTPUT TO -15V SUPPLY.
[3] Recommended ADI power supply: model 904, ±15V @ 50mA
Specifications subject to change without notice.

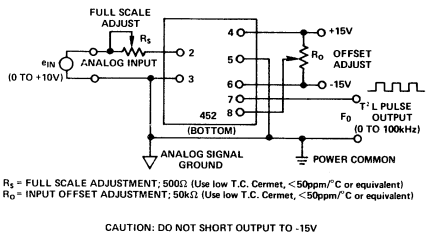
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



WEIGHT: 25 grams

Mating Socket AC1047



Rs = FULL SCALE ADJUSTMENT; 500Ω (Use low T.C. Cermet, <50ppm/°C or equivalent)
Ro = INPUT OFFSET ADJUSTMENT; 50kΩ (Use low T.C. Cermet, <50ppm/°C or equivalent)

CAUTION: DO NOT SHORT OUTPUT TO -15V

Figure 2. External Connections for Voltage to Frequency Operation, with Optional Input Offset Voltage and Full Scale Output Frequency Adjustments

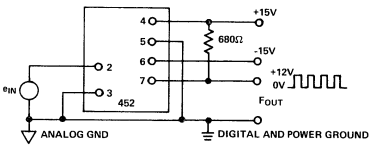


Figure 3. Driving High Noise Immunity Logic and CMOS

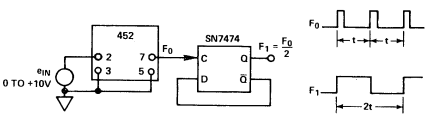


Figure 4. Square Wave Output Using Type D Flip-Flop

All Units Meet the Requirements of MIL-STD-202E as Outlined Below

TEST	METHOD	CONDITION
High Temperature Storage	108A	D (Non-Operating)
Moisture Resistance	106D	(10 Days)
Solderability	208C	
Thermal Shock	107D	A (5 Cycles)
Terminal Strength	211A	A (Pull Test; 10 lbs)
Temperature Cycling	102A	D (-55°C/+85°C)
Vibration	204C	B (15g Peak)
Barometric Pressure	105C	B (50,000 Feet)

TABLE 1. Environmental Specifications

ADJUSTMENT PROCEDURE

Model 452 may be used directly with no external trim potentiometers to achieve rated performance. Overall accuracy and dynamic range may be improved by using two optional trim adjustments as shown in Figure 2 above; FULL SCALE and OFFSET adjust. Low temperature coefficient trims must be used to maintain the drift specifications of the V/F converter. The T.C. of the trim pot will add to the FULL SCALE DRIFT specification as follows:

FULL SCALE DRIFT CONTRIBUTION =

$$\left[\frac{R_{ext}}{R_{ext} + 20k\Omega}\right] \times \left[\text{T.C. } R_{ext}\right] \quad /°C$$

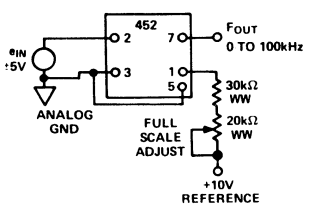
VOLTAGE TO FREQUENCY OPERATION

Model 452 provides accurate conversion of analog signals into a train of constant width and constant amplitude pulses at a rate directly proportional to the analog signal amplitude. The output continuously tracks the input signal, responding directly to changes in the input signal; external clock synchronization is not required. The output pulse train is TTL/DTL compatible, permitting direct interface to low cost digital processing circuits.

Dynamic Range: Model 452 accepts unipolar, single ended voltage or current input signals from 0V to +10V, or 0mA to +0.5mA directly, with 10% min overrange; the corresponding output frequency is dc to 100kHz. By offsetting the input using the current terminal, model 452 will accept bipolar input voltages up to ±5V.

Calibration Procedure: Allow a ten minute warm-up after initial power turn on. Using a precision, stable voltage source, set the input voltage, e_{in}, to +10mV. Adjust the OFFSET trim, R_O, for an output pulse interval of 0.1 second (100Hz). Set the input voltage to +10.000V and adjust the FULL SCALE trim for an output pulse interval of 10μs (100kHz). Model 452 may now be used without further adjustment.

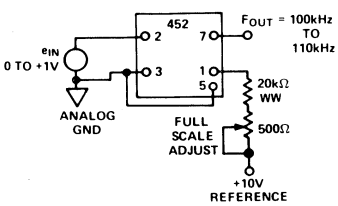
Offsetting Input: The input summing terminal, i_{in}, may be used to improve model 452's dynamic response as well as scale the output frequency to directly convert bipolar input voltages. An offset current is fed through an external resistor from a stable voltage reference. As shown in Figure 5, input voltages of ±5V min can be converted directly.



INPUT	OUTPUT
+5V	100kHz
0	50kHz
-5V	0

Figure 5. Offsetting Input to Accept Bipolar (±5V) Input

By scaling the output frequency, the step response for low amplitude input signals will significantly improve. As shown in Figure 6, an offset current of 450μA will shift the full scale output from 10kHz to 100kHz for a 1V max input. The step response improves to 22μs, compared to 202μs before offsetting.



INPUT	OUTPUT
+1V	100kHz
0	90kHz

Figure 6. Offsetting Input to Achieve Improved Dynamic Response

DYNAMIC RESPONSE

Overload Recovery: Model 452 can safely withstand input overloads up to +25V, $-V_S$. Overload recovery time will depend on the input polarity. Worst case overload recovery occurs following a sustained negative overload. The recovery time depends upon the input voltage applied after removal of the overload and is given by:

$$t_r(ms) = \frac{1.5}{E\ (volts)}$$

where E is the voltage applied following overload. Recovery from positive overloads up to the max safe input occurs within 2 microseconds after removal of the overload condition.

Step Response: The output settling time for step input changes is a function of the final output frequency. Settling time is specified as 2μs plus 2 output pulses of the new frequency. (e.g. for a 10V step input, the settling time will be 22μs.) Figure 7 shows typical timing relationships between input and output for input voltages of 2V and 10V.

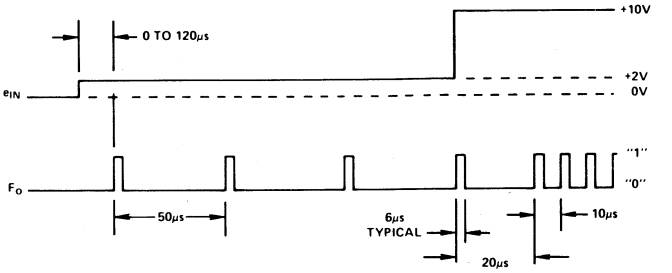


Figure 7. Timing Waveforms; Input/Output

PERFORMANCE SPECIFICATIONS

Nonlinearity: Nonlinearity error is specified as ±0.015% of 10V full scale (150ppm), and is guaranteed over the 0.1mV to 11V operating signal range. Typical nonlinearity performance is illustrated in Figure 8. Below 0.1mV, nonlinearity error remains within the specified limits, but is masked by zero offset stability, input noise and adjustment accuracy.

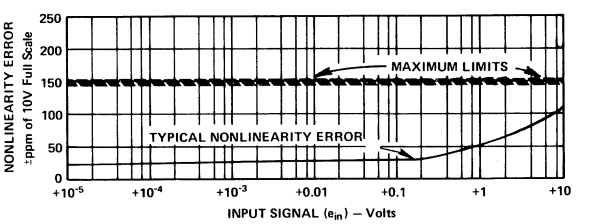


Figure 8. Nonlinearity Error Versus Input Voltage Signal

Full Scale Temperature Stability: Gain drift is specified in ppm of input signal, and is guaranteed over the 0 to +70°C temperature range; ±50ppm/°C, 452L; ±100ppm/°C, 452K; ±150ppm/°C, 452J. The curves of Figure 9 illustrate the drift limits over the specified operating temperature range for each grade. Typical performance is half the guaranteed limits.

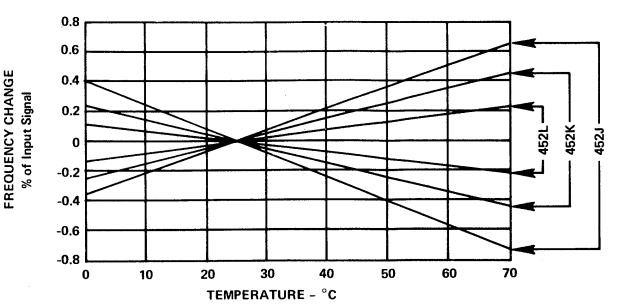


Figure 9. Frequency Drift (Worst Case)

LONG TERM PRECISION INTEGRATOR

In critical applications, such as pollution monitoring where it is required to integrate for periods greater than 1 hour with overall accuracy of 0.1%, the V/F converter offers a superior low cost approach when compared to the traditional operational integrator circuit. As shown in Figure 10, the analog signal is applied to a precision amplifier, model 52K, and then to the V/F input. Model 452's output is connected to a high capacity counter and display, operating as a totalizer. The total pulse count is equal to the time integral of the analog input signal. A feature of this approach is the infinite hold capability, without errors due to time drift, since the counter may be held at any time without affecting the output reading.

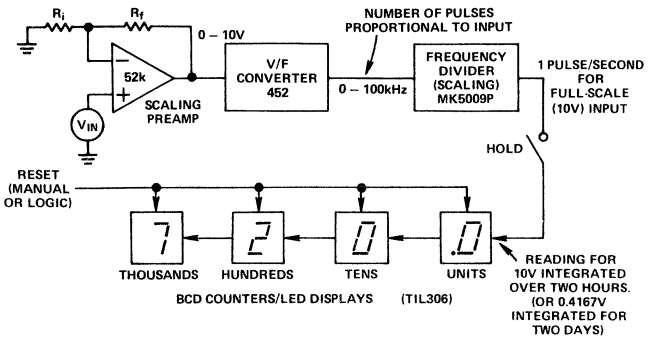


Figure 10. Model 452 as Long Term Integrator with Arbitrary Display Calibration. Frequency Division Ratio Can Otherwise Be Chosen to Provide Direct Readout in Any Desired Units.

RATIOMETRIC MEASUREMENTS

The circuit shown in Figure 11 illustrates a simple and inexpensive way of using two 100kHz V/F converters to achieve ratiometric measurements with less than 0.1% error over a dynamic range of 10,000 to 1. One converter is used as the input V/F to a digital counter and display, while a second converter, with a digital divide-by-N circuit is used as the time base for the counter. The counting time is one half the output period of the divide-by-N circuit, resulting in an output count of $2NV_1/V_{REF}$.

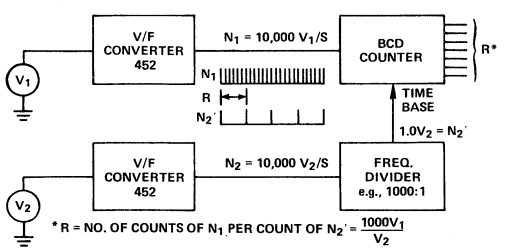


Figure 11. Wide-Range Ratiometer

LOW COST, HIGH RESOLUTION, A/D CONVERTER

Model 452 can be applied as a low cost 12–16 bit A/D converter by the use of a digital counter and time base as shown in Figure 12. The time base determines the A/D conversion time and sets overall resolution (i.e. with a 1 sec. time base, model 452 has a resolution of 1 part in 100,000 – which is better than a 16 bit A/D: 1 part in 65,536). With a longer time base greater resolution may be achieved, with a sacrifice in conversion speed.

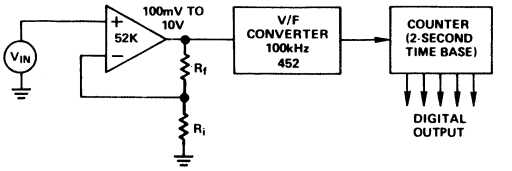


Figure 12. Model 452 Applied as a Nearly 18 Bit (5½ BCD) A/D Converter. Resolution is 1 Pulse in 200,000, or 0.05% of Smallest Input Signal (or 5ppm of Full Scale).

PRECISION HIGH CMV ANALOG ISOLATOR

By combining the V/F converter with a floating power supply and optical isolator as shown in Figure 13, accurate low level measurements in the presence of high common mode voltages may be achieved. Only the CMV rating of the optical isolator and the breakdown rating of the power supply limit the CMV rating. Using this approach for isolating transducers, ground loop problems are eliminated. Cost and complexity are minimized since only a single optical isolator is required to couple the serial pulse output from the V/F to the digital readout.

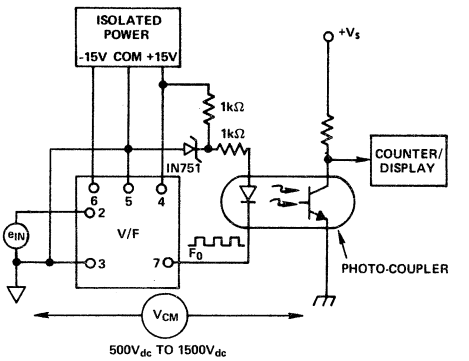


Figure 13. Optical Isolation Using LED Photo Isolator to Provide Up to 1500V dc CMV Isolation

HIGH NOISE IMMUNITY DATA TRANSMISSION

An inexpensive method of accurately transmitting analog data through high noise environments is illustrated in Figure 14. This approach utilizes the self clocking output of model 452, and eliminates the need for costly additional twisted pair for external synchronization. Model 610 amplifies the low level differential transducer signal up to the 10V full scale V/F input level. A differential line drive is used to drive a twisted pair cable. A differential line receiver is used to drive a digital counter and display. The differential line driver and receiver offer high noise immunity to common mode noise signals. The low cost of the V/F converter as well as the simple twisted pair cabling approach make it economical to use a converter for each channel in a high resolution data acquisition system.

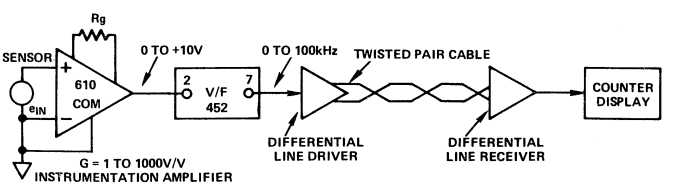


Figure 14. Application of Model 452 in Digital Transmission

ANALOG DEVICES

High Accuracy, 100kHz and 1MHz Voltage to Frequency Converters

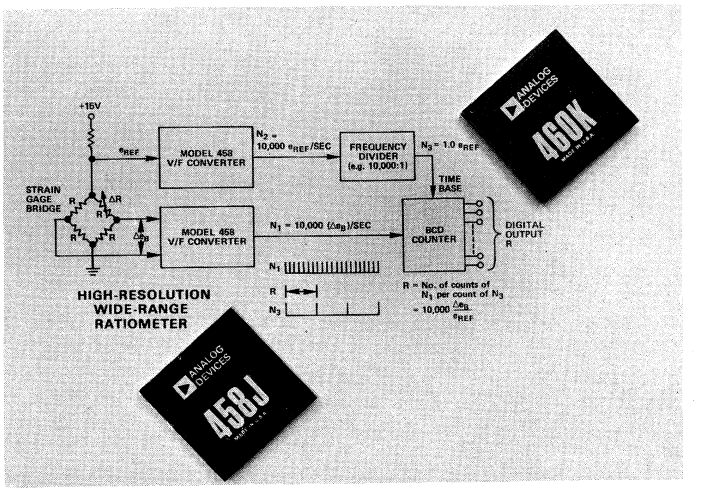
MODELS 458 and 460

FEATURES

High Stability: 5ppm/°C max, Model 458L
15ppm/°C max, Model 460L
Low Nonlinearity: 100ppm max, Model 458
150ppm max, Model 460
Versatility: Differential Input Stage
Voltage and Current Inputs
Floating Inputs: ±10V CMV
Wide Dynamic Range: 6 Decades, Model 460
TTL/DTL or CMOS/HNIL Compatible Output

APPLICATIONS

Fast Analog-to-Digital Converter
High Resolution Optical Data Link
Ratiometric Measurements
2-Wire High Noise Immunity Digital Transmission
Long Term Precision Integrator



GENERAL DESCRIPTION

Models 458 and 460 are high performance, differential input, voltage to frequency modular converters designed for analog to digital applications requiring accuracy and fast data conversion. Model 458 offers a 100kHz full scale frequency, guaranteed nonlinearity of ±0.01% maximum over five decades (1Hz to 100kHz) of operation and guaranteed low maximum gain drift in three model selections; model 458L: 5ppm/°C max; model 458K: 10ppm/°C max; and model 458J: 20ppm/°C max. Model 460 offers a 1MHz full scale frequency, guaranteed maximum nonlinearity of ±0.015% over six decades (1Hz to 1MHz) of operation and guaranteed low maximum gain drift in three selections; model 460L: 15ppm/°C max; model 460K: 25ppm/°C max; and model 460J: 50ppm/°C max. Model 460L is the industries' first 1MHz V/F converter to offer 15ppm/°C maximum gain drift.

The differential input stage of models 458 and 460 provide the versatility of either direct interface to off-ground 0 to +11V input signals with common mode voltages (CMV) to ±10V, as well as ground referenced positive, 0 to +11V or negative, 0 to -11V signals. Both models also accept positive current signals: 0 to +½mA, model 458; 0 to +1mA, model 460 for current to frequency (I/F) applications.

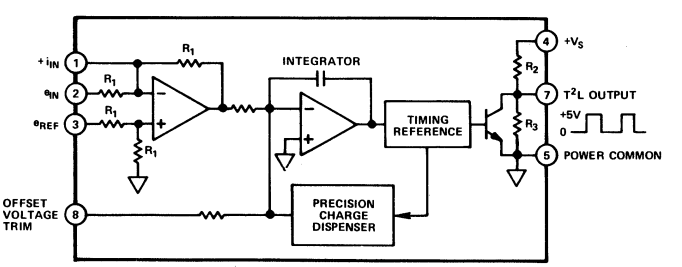
The rated performance of both models 458 and 460 is achieved without the need for external components or adjustments. Optional adjustments are available for trimming full scale frequency and the input offset voltage.

WHERE TO USE MODELS 458 AND 460

The combination of low gain drift, low nonlinearity and the versatility of a differential input with both high speed (100kHz/1MHz) models, offer excellent solutions to a wide variety of demanding applications; in high speed remote data acquisition systems – two wire data transmission over long wires; in 5½ digit DVMs – featuring high resolution A/D conversion, monotonic performance, no missing codes and high noise rejection; in strain gage bridge weighing applications – accurate ratiometric measurements over wide dynamic range.

DESIGN APPROACH - PRECISION CHARGE BALANCE

Models 458 and 460 incorporate a superior charge balance design that result in high linearity and temperature stability - see Figure 1. Both models accept unipolar, single-ended voltage or current input signals directly. By offsetting the input using the current terminal, models 458 and 460 will accept bipolar input voltages up to ±5V.



MODEL	FULL SCALE OUTPUT	R_1	R_2	R_3
458	100kHz	20kΩ	10kΩ	4.7kΩ
460	1MHz	10kΩ	2kΩ	910Ω

Figure 1. Block Diagram - Models 458, 460

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

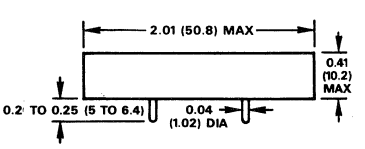
MODEL	100kHz Full Scale 458 J	458 K	458 L	1MHz Full Scale 460 J	460 K	460 L
TRANSFER FUNCTION						
Voltage Input	$f_{OUT} = (10^4 Hz/V)\ e_{IN}$			$f_{OUT} = (10^5 Hz/V)\ e_{IN}$		
Current Input	$f_{OUT} = (2 \times 10^5 Hz/mA)\ i_{IN}$			$f_{OUT} = (10^6 Hz/mA)\ i_{IN}$		
ANALOG INPUT						
Configuration	Differential			Differential		
Voltage Signal Range						
e_{IN} Terminal (e_{REF} = 0)	0 to +10V dc min			0 to +10V dc min		
e_{REF} Terminal (e_{IN} = 0)	0 to -10V dc min			0 to -10V dc min		
Differential ($e_{IN} - e_{REF}$)	0 to +10V dc min			0 to +10V dc min		
Overrange	+10% min			+10% min		
Current Signal Range (i_{IN})	0 to +0.5mA min			0 to +1mA min		
Common Mode Voltage	±10V			±10V		
Common Mode Rejection	40dB			40dB		
Impedance, e_{IN} Terminal	20kΩ			10kΩ		
e_{REF} Terminal	40kΩ			20kΩ		
i_{IN} Terminal	0Ω			0Ω		
Max Safe Input	$\pm V_S$			$\pm V_S$		
ACCURACY						
Warm Up Time	5 Seconds to 0.01%			2 Minutes to 0.02%		
Nonlinearity, V_{IN} = 0.1mV to 11V	±0.01% of Full Scale, max			±0.015% of Full Scale, max		
Full Scale Error[1]	+0.1% to +2%, max			+0.1% to +2%, max		
Gain vs. Temperature (0 to +70°C)	±20ppm/°C max	±10ppm/°C max	±5ppm/°C max	±50ppm/°C max	±25ppm/°C max	±15ppm/°C max
vs. Supply Voltage	±15ppm/%			±25ppm/%		
vs. Time	±10ppm/day			±10ppm/day		
Input Offset Voltage[2]	±10mV max			±10mV max		
vs. Temperature (0 to +70°C)	±30μV/°C max			±30μV/°C max		
vs. Supply Voltage	±10μV/%			±10μV/%		
vs. Time	±20ppm/day			±10ppm/day		
RESPONSE						
Settling Time, ±0.01% +10V Step	3 Output Pulses Plus 2μs			2 Output Pulses Plus 2μs		
Overload Recovery Time	10ms			1ms		
FREQUENCY OUTPUT[3]						
Waveform	TTL/DTL Compatible Pulses			TTL/DTL Compatible Pulses		
Pulse Width	5μs			500ns		
Rise and Fall Time	300ns/50ns			60ns/50ns		
Pulse Polarity	Positive			Positive		
Logic "1" (High) Level	+2.4V min			+2.4V min		
Logic "0" (Low) Level	+0.4V max			+0.4V max		
Capacitive Loading	500pF max			200pF max		
Fan Out Loading	10 TTL Loads min			10 TTL Loads min		
Impedance	3kΩ (High State)			670Ω (High State)		
POWER SUPPLY[4]						
Voltage, Rated Performance	±15V dc			±15V dc		
Voltage, Operating	±(13 to 18)V dc			±(13 to 18)V dc		
Current, Quiescent	(+25, -8)mA			(+25, -8)mA		
TEMPERATURE RANGE						
Rated Performance	0 to +70°C			0 to +70°C		
Operating	-25°C to +85°C			-25°C to +85°C		
Storage	-55°C to +125°C			-55°C to +125°C		
MECHANICAL						
Case Size	2" x 2" x 0.4"			2" x 2" x 0.4"		
Weight	45 Grams			45 Grams		
Mating Socket	AC1016			AC1016		

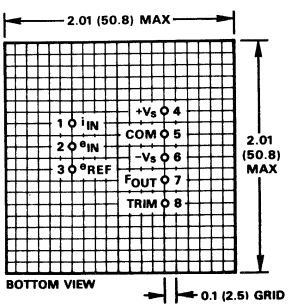
[1] Adjustable to zero using 500Ω potentiometer.
[2] Adjustable to zero using 50kΩ potentiometer.
[3] Protected for continuous short-circuits to ground and momentary (less than 1 sec) shorts to the $+V_S$ supply. Output is not protected for shorts to the $-V_S$ supply.
[4] Recommended power supply, ADI model 904, ±15V @ 50mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).





VOLTAGE TO FREQUENCY OPERATION

Models 458 and 460 provide accurate conversion of analog signals into a train of constant width and constant amplitude pulses at a rate directly proportional to the analog signal amplitude. The output continuously tracks the input signal, responding directly to changes in the input signal; external clock synchronization is not required. The output pulse train is TTL/DTL compatible, permitting direct interface to digital processing circuits. Adding a resistor from the output terminal, pin 7, to the +15V supply (1.2kΩ model 458; 820Ω model 460), shifts the output swing from 0 to +5V to 0 to +12V, providing a 4V noise immunity for driving high noise immunity logic (HNIL) and CMOS logic.

BASIC V/F HOOK-UP AND OPTIONAL TRIMS

Models 458 and 460 can be applied directly to achieve rated performance without external trim potentiometers or other components. Figures 2, 3 and 4 below illustrate the basic wiring connections for either V/F converter model. Using the basic hookup without trims, full scale (e_{IN} = 10V) accuracy is +0.1% to +2% and the input offset voltage is ±10mV max. The full scale and input offset voltage errors can be eliminated by using the FINE TRIM PROCEDURE.

FINE TRIM PROCEDURE

Connect the optional trims as shown in Figure 2, 3 or 4 and allow a five minute warm-up after initial power turn-on.

V/F INTERCONNECTIONS

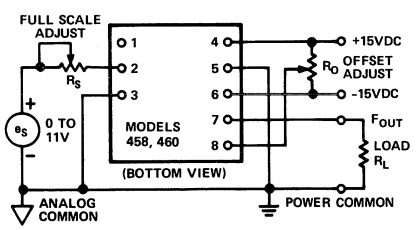


Figure 2. Positive Input Signal

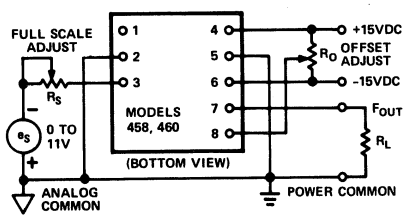


Figure 3. Negative Input Signal

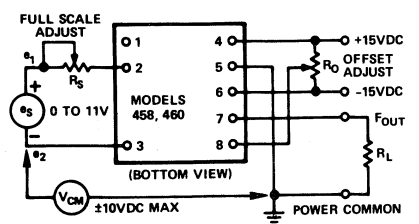


Figure 4. Floating Input Signal

EXTERNAL CONNECTIONS FOR VOLTAGE TO FREQUENCY OPERATION, WITH OPTIONAL INPUT OFFSET VOLTAGE AND FULL SCALE FREQUENCY ADJUSTMENTS

R_S = FULL SCALE ADJUSTMENT; 500Ω (Use low T.C. Cermet, <50ppm/°C or equivalent)
R_O = INPUT OFFSET ADJUSTMENT; 50kΩ (Use low T.C. Cermet, <50ppm/°C or equivalent)

CAUTION: DO NOT SHORT OUTPUT TERMINAL TO -15V

Using a precision, stable voltage source, set the input voltage, e_S, to 10mV. Adjust the OFFSET trim, R_O, for an output pulse interval of 0.1 sec (model 458) or 0.01 sec (model 460). Set the input voltage to +10.000V and adjust the FULL SCALE trim for an output pulse frequency of 100kHz (model 458), or 1MHz (model 460). The V/F converter may now be used without further adjustment.

DIFFERENTIAL INPUT

The e_{IN} and e_{REF} input terminals represent a true differential input capable of accepting a signal from a strain gage bridge, a balanced line, or a signal source sitting at a common mode voltage. The differential input eliminates the need for a differential amplifier to handle these signals.

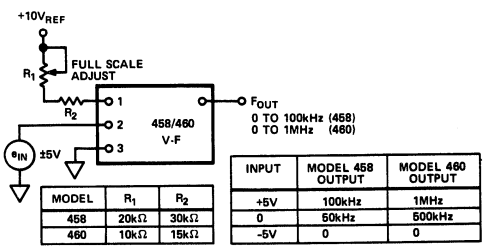
To apply the 458 or 460 voltage inputs differentially, the e_{IN} pin must always be positive with respect to the e_{REF} pin as shown in Figure 4. The differential signal source may be completely floating with common mode voltages up to ±10V max. For differential inputs the output frequency is:

$$F_{OUT} = \left[\underbrace{(e_1 - e_2)}_{\text{INPUT SIGNAL}} + \underbrace{\left(\frac{e_1 + e_2}{2}\right) \times \left(\frac{1}{CMR}\right)}_{\text{CMR ERROR}} \right] K_g$$

$K_g = 10^4$ Hz/V; model 458
10^5 Hz/V; model 460

OFFSETTING INPUT FOR BIPOLAR INPUTS

The input summing terminal, $+i_{IN}$, may be used to improve dynamic response as well as scale the output frequency to directly convert bipolar input voltages. An offset current is fed through an external resistor from a stable voltage reference. As shown in Figure 5, input voltages of ±5V min can be converted directly.

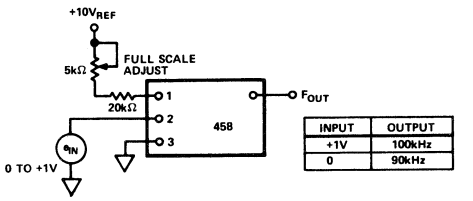


MODEL	R_1	R_2
458	20kΩ	30kΩ
460	10kΩ	15kΩ

INPUT	MODEL 458 OUTPUT	MODEL 460 OUTPUT
+5V	100kHz	1MHz
0	50kHz	500kHz
-5V	0	0

Figure 5. Offsetting Input to Accept ±5V Bipolar Inputs

The output may also be scaled up so that low amplitude signals, such as 1V will give full scale output frequency; 100kHz model 458 or 1MHz model 460. By scaling the output frequency for low level signals, the step response will significantly improve. As shown in Figure 6 for model 458, the step response for a 1 volt input decreases from 200μs before input scaling, to 20μs with scaling.



INPUT	OUTPUT
+1V	100kHz
0	90kHz

Figure 6. Offsetting Input to Achieve Improved Dynamic Response for Small Signal Inputs

PERFORMANCE SPECIFICATIONS

Nonlinearity: Nonlinearity error is specified as a % of 10V full scale input and is guaranteed over the 0.1mV to 11V operating signal range; ±0.01% max, models 458J/K/L, ±0.015% max, models 460J/K/L. Typical nonlinearity performance is illustrated in Figure 7.

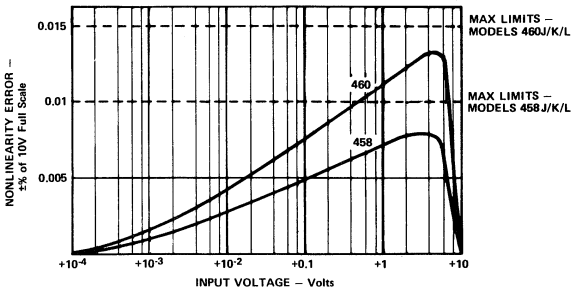


Figure 7. Nonlinearity Error Versus Input Voltage

Gain Temperature Stability: Gain drift is specified in ppm of output signal and is guaranteed for each model over the 0 to +70°C temperature range; 5ppm/°C (458L), 10ppm/°C (458K), 20ppm/°C (458J), 15ppm/°C (460L), 25ppm/°C (460K) and 50ppm/°C (460J) max.

LONG TERM PRECISION INTEGRATOR

In critical measurement applications, such as pollution monitoring where it is required to integrate for periods greater than 1 hour with overall accuracy of 0.05%, the V/F converter offers a superior low cost approach when compared to the traditional operational integrator circuit. As shown in Figure 8, the analog signal is applied to a precision input amplifier, model 52K and then to the V/F input. The V/F output is connected to a large capacity counter and display, operating as a totalizer. The total pulse count is equal to the time integral of the analog input signal. Since the output displayed is an accumulated pulse count, there is no integrator drift error. A feature of this approach is the infinite hold capability without errors due to time drift, since the counter may be held at any time without affecting the output reading.

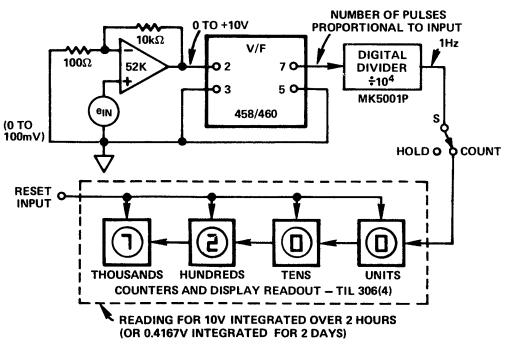


Figure 8. Models 458/460 as Long Term Integrator with Arbitrary Display Calibration. Frequency Division Ratio can Otherwise be Chosen to Provide Direct Readout in any Desired Units

RATIOMETRIC MEASUREMENTS

The circuit shown in Figure 9 illustrates a simple and inexpensive way of using two 100kHz V/F converters to achieve ratiometric measurements with less than 0.1% error over a dynamic range of 10,000 to 1. One converter is used as the input V/F to a digital counter and display, while a second converter, with a digital divide-by-N circuit is used as the time base for the counter. The counting time is one half the output period of the divide-by-N circuit, resulting in an output count of $2NV_1/V_{REF}$.

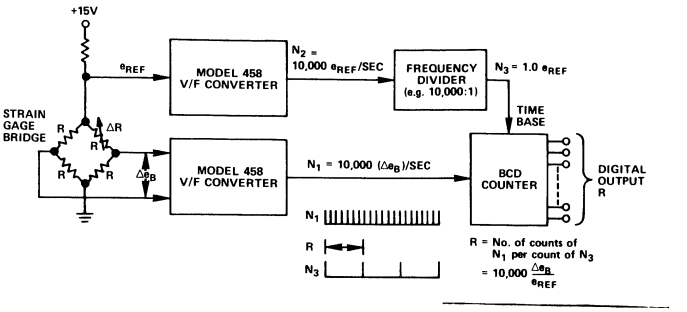


Figure 9. High Resolution, Wide-Range Ratiometer Using Model 458 V/F Converter

PRECISION HIGH CMV ANALOG ISOLATOR

By combining the V/F converter with a floating power supply and optical isolator as shown in Figure 10, accurate low level measurements in the presence of high common mode voltages may be achieved. Only the CMV rating of the optical isolator and the breakdown rating of the power supply limit the CMV rating. Using this approach for isolating transducers, ground loop problems are eliminated. Cost and complexity are minimized since only a single optical isolator is required to couple the serial pulse output from the V/F to the digital readout.

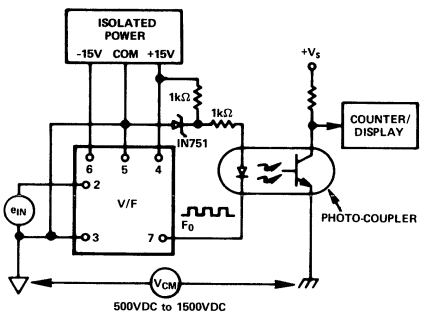


Figure 10. Optical Isolation Using LED Photo Isolator to Provide Up to 1500V dc CMV Isolation

APPLICATION IN DATA ACQUISITION SYSTEMS

High Noise Immunity Data Transmission: A method of accurately transmitting analog data through high noise environments is illustrated in Figure 11. This approach utilizes the self clocking output of models 458 and 460 and eliminates the need for costly additional twisted pair for external synchronization. Model 610 amplifies the low level differential transducer signal up to the 10V full scale V/F input level. A differential line driver is used to drive a twisted pair cable. The differential line driver and receiver offer high noise immunity to common mode noise signals.

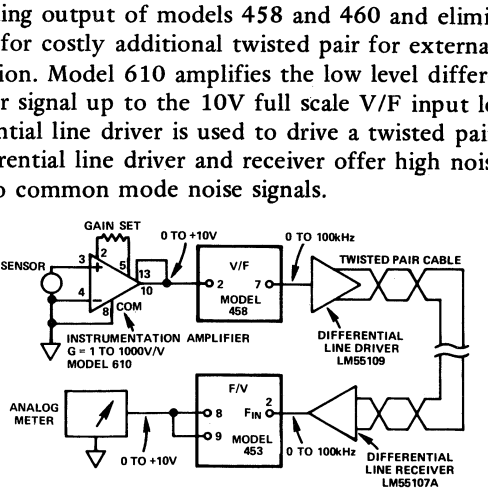


Figure 11. Application of Model 458 V/F Converter in a High Performance, High Noise Rejection Two-Wire Data Transmission System

S/D and D/S Converters

Orientation
S/D and D/S Converters

These products constitute a complete line of devices for the digital measurement and control of angular and linear displacements by means of synchros, resolvers, and Inductosyns. In addition to modules that perform the appropriate conversions, the line also includes modules that perform purely algebraic or logical functions; in some cases, solid-state circuitry emulates the functions of electromechanical devices.

The range of synchro processing modules now available covers a wide area of application. They are widely used in military and radar applications, but there are additional fields in which they could be used to advantage because of the proven ruggedness and high precision of the electromechanical hardware, their standardized specifications, and their low cost. They have a number of advantages over potentiometers and optical systems.

In this introductory section, there will be provided a set of device definitions. Detailed data and applications information is given in the data sheets, available upon request. For a complete introduction to synchro/digital conversion, Analog Devices provides a free 42-page booklet, APPLICATIONS OF SYNCHRO-DIGITAL CONVERSION, also available upon request.

In this section, and in much of the text, the word "Synchro" appears frequently. In many cases, the word "Resolver" could be used in its place. The modules make use of angular data in resolver form; if the input data is in three-wire synchro form, transformers in "Scott T" configuration convert it to resolver form; analog outputs are available in both forms. There are a number of voltage and frequency options.

REPRESENTATION OF ANGLES IN DIGITAL FORM

Binary

The most commonly used method of representing angles in digital form is simple natural binary weighting, where the most-significant bit (MSB) represents 180°, the next represents 90°, etc. The table shows the bit weights in degrees, degrees-and-minutes, and radians for this coding method.

Bit No.	Degrees	Degrees, minutes		Radians
1	180	180	0	3.141593
2	90	90	0	1.570796
3	45	45	0	0.785398
4	22.5	22	30	0.392699
5	11.25	11	15	0.196349
6	5.625	5	37.5	0.098175
7	2.8125	2	48.75	0.049087
8	1.40625	1	24.38	0.024544
9	0.70312	0	42.19	0.012272
10	0.35156	0	21.09	0.006136
11	0.17578	0	10.55	0.003068
12	0.08789	0	5.27	0.001534
13	0.04395	0	2.64	0.000767
14	0.02197	0	1.32	0.000383
15	0.01099	0	0.66	0.000192
16	0.00549	0	0.33	0.000096

BCD

When angular measures have to be displayed in visual form, BCD coding is used, through the use of binary-to-BCD converters, such as the BDM1616, which provides the necessary scaling and conversion, e.g., from 10100000000000 (180° + 45°) to 10 0010 0101.0000 0000 (or 225° 00′).

SYNCHRO CONVERSION DEVICES

Binary-to-Binary-Coded-Digital Converter (BDM1615/16/17)

A device that accepts angular data in binary form and converts it to BCD form, with fractional degrees either in decimal fractions of 1° or in arc-minutes. The BCD output is modulo 360°.

Digital-to-Synchro Converters (DSC1605/06/07)

Devices that accept parallel binary digital inputs (10, 14, or 16 bits) and an ac reference signal, and provide outputs in 3-wire synchro form.

Inductosyn-to-Digital Converter (IDC1703)

A device that produces a digital output capable of resolving (to 12 bits) intermediate distances within a single track-pitch of a Farrand linear-Inductosyn stator in displacement- and angle-measuring Inductosyn systems. The moving element is used as though it were a resolver input.

Solid-State Control Differential Transmitter (SCDX1623)

A device that accepts a digital angle input, together with a synchro (SCDX) angle input, and gives, as an output, synchro signals representing the difference between the two input angles. The function is similar to that of an electromechanical control differential transmitter (CDX), except that the mechanical input of the CDX has been replaced by a binary angle.

Solid-State Control Transformer (SSCT1621)

A device that accepts 3-wire (synchro) input information, together with a 14-bit digital angle input. Its output is a voltage, at the carrier frequency, having a magnitude proportional to the sine of the difference between the digital angle and the angle represented by the synchro input information. It performs a function identical to that of electromechanical control transformers, except that the mechanical inputs have been replaced by digital inputs. Its typical use is as an error generator in follow-up servo systems.

Synchro-to-Analog Converter (SAC1763)
A device that converts a synchro input to an analog voltage linearly proportional to angle, for recording angular data on chart-pen recorders, UV recorders, or FM tape recorders for subsequent analysis.

Digital Angle to Digital Sine/Cosine Converter (SCM1677)
A device that accepts a 14-bit digital angle input (θ) and outputs a 12-bit-plus sign digital V$\sin\theta$ or V$\cos\theta$, either alternately (switched internally or externally) or continuously.

Synchro-to-Digital Converter (SDC1602/1604/1700/1702/1704/1786)
A device that accepts either 3-wire synchro- or 4-wire resolver inputs, together with a 2-wire ac reference, and outputs angular binary data in a continuously tracking mode, employing a Type 2 servo loop. The inputs may be from either remote synchros or from electrically simulated synchros (e.g., DSC's).

Digital Converters and Processors for Two-Speed Synchros (TSL1612 and TSDC1608/09/10/11)
A two-speed processor takes as inputs two sets of digital information, representing the angles from coarse and fine synchros, and combines them to produce a single 19-bit word representing the actual angle of the "coarse" shaft. The TSL consists of the processing logic alone—it can be used with a pair of SDC's, which provide the two sets of digital information. The TSDC contains the coarse 10-bit SDC, along with the two-speed processing logic.

Selection Guide
S/D and D/S Converters

Model	Description	Page
BDM1615/1616/1617	Binary-to-BCD Converter Modulo 360°	504
DSC1605/1606/1607	Digital-to-Synchro Converters	503
IDC1703	Inductosyn-to-Digital Converter	504
SAC1763	Synchro-to-Voltage (Proportional to Angle) Converter	504
SCDX1623	Synchro-Input Solid-State Control Differential Transformer	504
SCM1677	Digital-Angle-to-Digital-Sine/Cosine Modular Converter	504
SDC1602/1604/1786	Synchro-to-Digital Converters	504
SDC1700/1702/1704	Low-Profile Synchro-to-Digital Converters	504
SSCT1621	Synchro-Input Solid-State Control Transformer	504
TSDC1608/1609/1610/1611	Two-Speed Synchro-to-Digital Conversion Adapter	503
TSL1612	Two-Speed Logic Processor	503

ANALOG DEVICES

S/D and D/S Converters

DIGITAL-TO-SYNCHRO CONVERTERS

The DSC1605 and 1606 series are digital to synchro converters capable of driving electromechanical loads of up to 1.3VA. Inputs are parallel natural binary angle plus a 60Hz or 400Hz reference. Outputs are 3 wire synchro or 4 wire resolver format. Reference input and synchro/resolver output are transformer isolated with up to a 500V dc common mode voltage capability. 60Hz versions have the transformers in a separate module.

The DSC1607 series feature 16 bit binary input. Power amplification and transformer isolation are not provided. The sine/cosine outputs are individually amplitude corrected vs. angle to better than 1%, a feature not included in the DSC1605/1606 series. This amplitude correction is important in type 1 servo control loop applications.

SPECIFICATIONS (typical @ +25°C and ±15V dc and +5V dc unless otherwise noted)

	Input Resolution Bits	Accuracy (See Note) Arc-Min	Signal & Ref. Freq. Hz	Signal Level V rms	Reference Level V rms	Minimum Output Load Z_{LL} Ohms	Output VA	Size (See Note)	Temp Range (See Note)	Settling Time Micro-Sec
DSC1605511	14	±4	400	11.8	26	107	1.3	A	C	100
DSC1605512	14	±4	400	90	115	6200	1.3	A	C	100
DSC1605507 plus STM1634522	14	±4	60	90	115	6200	1.3	A plus E	C	100
DSC1605711	14	±4	400	11.8	26	107	1.3	A	M	100
DSC1605712	14	±4	400	90	115	6200	1.3	A	M	100
DSC1605707 plus STM1634722	14	±4	60	90	115	6200	1.3	A plus E	M	100
DSC1606511	10	±30	400	11.8	26	107	1.3	A	C	80
DSC1606512	10	±30	400	90	115	6200	1.3	A	C	80
DSC1606507 plus STM1633522	10	±30	60	90	115	6200	1.3	A plus E	C	80
DSC1606711	10	±30	400	11.8	26	107	1.3	A	M	80
DSC1606712	10	±30	400	90	115	6200	1.3	A	M	80
DSC1606707 plus STM1633722	10	±30	60	90	115	6200	1.3	A plus E	M	80
DSC1607517	16	±1	50–1000	7.5	2	2000	N/A	A	C	150
DSC1607717	16	±1	50–1000	7.5	2	2000	N/A	A	I	150

Sizes: A is 3.125" x 2.625" x 0.8"
E is 4.5" x 2.0" x 1.5"

Temp Ranges: C is 0 to +70°C
I is -55°C to +85°C
M is -55°C to +105°C
full power to +85°C
½ power at +105°C

Accuracy applies: over operating temp range and ±10% reference frequency and amplitude changes and 10% harmonic distortion and ±5% power supply variation and any balanced load from no load to full load.

DSC1605 and DSC1606 models shown are synchro outputs. Consult factory for resolver versions.
DSC1607 is resolver form, without power amplifiers.

TWO SPEED S/D CONVERTERS

The TSL and TSDC series of converters provide a digital solution to the problem of combining the multiple speed outputs from a pair of two speed synchros to a single speed output word.

The TSL1612 provides the two speed logic for the non-binary speed ratios of either 36:1 or 18:1 (36:2) or 9:1 by simple programming of the input/outputs. The TSL1612 accepts a binary angle input of up to 14 bits from a fine channel converter plus a second input of up to 7 bits from a coarse channel converter and provides a single speed output word of up to 19 bits parallel binary angle.

The TSDC series provides a dual function: conversion of coarse channel synchro data to 10 bit binary via a tracking S to D converter plus performing two speed processing for binary speed ratios. The converter portion is identical to the SDC1603 specified elsewhere. Binary ratios of 8:1, 16:1, 32:1 and 64:1 together with a 10 bit converter are provided by the TSDC1608, TSDC1609, TSDC1610 and TSDC1611 series respectively. A fine channel converter of up to 16 bits binary completes this two speed set.

SPECIFICATION SUMMARY TSL1612500

(typical @ +25°C and +5V dc unless otherwise noted)

Fine Synchro Input:	up to 14 bits parallel binary angle
Coarse Synchro Input:	up to 7 bits parallel binary angle
Output:	up to 19 bits parallel binary angle
Logic Levels:	DTL/TTL compatible
Fan In:	5 TTL loads
Fan Out:	8 TTL loads
Conversion Time:	500 nanoseconds
Power:	+5V ±5% at 750mA
Size:	3.125" x 2.625" x 0.4"
Temperature:	0 to +70°C

Consult factory for extended temperature range versions

SPECIFICATION SUMMARY TSDC SERIES

The TSDC series units are SDC1603 units to which two speed logic has been added for binary ratios. All specifications are the same as an equivalent SDC1603 series unit except:

1. Speed ratio per above
2. A and B digital inputs

SYNCHRO-TO-DIGITAL CONVERTERS

The SDC series converters are continuous tracking, type 2 servo loop, synchro or resolver to digital converters intended for military and industrial control applications.

All units feature transformer isolation of the signal and reference inputs with up to 500V dc common mode voltage capability.

The SDC1700, SDC1702 and SDC1704 are unique in that transformers for 60Hz are included within the low profile height of 0.4".

All units provide a BUSY output line which indicates when the output counter is being changed. An INHIBIT input line is provided which prevents updates of the output.

Input/outputs are TTL compatible. The SDC1700 and SDC1704 have a velocity output pin which provides a dc voltage proportional to input angular velocity. This output can replace a separate tachometer in certain control loop applications.

Outputs are provided in parallel in natural binary angle. The MSB equals 180°, the next equals 90°, etc.

SPECIFICATIONS (typical @ +25°C and ±15V dc and +5V dc unless otherwise noted)

	Output Resolution Bits	Accuracy (See Note) Arc-Min	Signal Ref. Freq. Hz	Signal Level V rms	Reference Level V rms	Tracking Rate Deg/Sec	Acceleration for 1LSB Error Deg/Sec^2	Size (See Note)	Temp Range (See Note)	Frequency Range Hz
SDC160251Z	14	±4	400	11.8 or 90	26 or 115	2800	240	A	C	350–1500
SDC160261Z	14	±4	400	11.8 or 90	26 or 115	2800	240	A	M	350–1500
SDC1602507 plus STM1631522	14	±4	60	90	115	430	6	A plus D	C	50–450
SDC1602607 plus STM1631622	14	±4	60	90	115	430	6	A plus D	M	50–450
SDC160351Z	10	±30	400	11.8 or 90	26 or 115	2880	480	A	C	350–1500
SDC160361Z	10	±30	400	11.8 or 90	26 or 115	2880	480	A	M	350–1500
SDC1603507 plus STM1630522	10	±30	60	90	115	2880	48	A plus D	C	50–450
SDC1603607 plus STM1630622	10	±30	60	90	115	2880	48	A plus D	M	50–450
SDC1604507 plus STM163251Z	16	±1.3	400	11.8 or 90	26 or 115	360	60	A plus D	C	350–450
SDC1604707 plus STM163271Z	16	±2	400	11.8 or 90	26 or 115	360	60	A plus D	I	350–450
SDC178651Z	10	±30	400	11.8 or 90	26 or 115	8640	34,000	A	C	350–1500
SDC178661Z	10	±30	400	11.8 or 90	26 or 115	8640	34,000	A	M	350–1500
SDC1786507 plus STM1630522	10	±30	60	90	115	1260	850	A plus D	C	50–450
SDC1786607 plus STM1630622	10	±30	60	90	115	1260	850	A plus D	M	50–450
SDC170051Z	12	±8.5	400	11.8 or 90	26 or 115	12,960	10,800	B	C	350–1600
SDC170052Z	12	±8.5	60	11.8 or 90	26 or 115	1800	200	B	C	50–1200
SDC170054Z	12	±8.5	2600	11.8 or 90	26 or 115	27,000	54,000	B	C	2300–2700
SDC170061Z	12	±8.5	400	11.8 or 90	26 or 115	12,960	10,800	B	M	350–1600
SDC170062Z	12	±8.5	60	11.8 or 90	26 or 115	1800	200	B	M	50–1200
SDC170064Z	12	±8.5	2600	11.8 or 90	26 or 115	27,000	54,000	B	M	2300–2700
SDC170251Z	10	±22	400	11.8 or 90	26 or 115	12,960	10,800	B	C	350–1600
SDC170252Z	10	±22	60	11.8 or 90	26 or 115	1,800	200	B	C	50–1200
SDC170254Z	10	±22	2600	11.8 or 90	26 or 115	27,000	54,000	B	C	2300–2700
SDC170261Z	10	±22	400	11.8 or 90	26 or 115	12,960	10,800	B	M	350–1600
SDC170262Z	10	±22	60	11.8 or 90	26 or 115	1,800	200	B	M	50–1200
SDC170264Z	10	±22	2600	11.8 or 90	26 or 115	27,000	54,000	B	M	2300–2700
SDC170451Z	14	±2 ±1LSB	400	11.8 or 90	26 or 115	4320	720	B	C	350–1000
SDC170452Z	14	±2.6 ±1LSB	60	11.8 or 90	26 or 115	500	16	B	C	50–500
SDC170461Z	14	±2 ±1LSB	400	11.8 or 90	26 or 115	4320	720	B	M	350–1000
SDC170462Z	14	±2.6 ±1LSB	60	11.8 or 90	26 or 115	500	16	B	M	50–500

Sizes: A is 3.125" x 2.625" x 0.8"
B is 3.125" x 2.625" x 0.4"
D is 3.125" x 1.5" x 1.0"

Temp Ranges: C is commercial 0 to +70°C
I is industrial -55°C to +85°C
M is military -55°C to +105°C
Consult factory for other options.

Accuracy: Applies over operating temp range and ±10% frequency variation and ±10% signal and ref amplitude variation and 10% signal and ref harmonic distortion and ±5% power supply variation.

Z is replaced by a number, when ordering, to specify input t
Z = 1 signifies synchro, signal 11.8V, reference 26V
Z = 2 signifies synchro, signal 90V, reference 115V
Z = 8 signifies resolver, signal 11.8V, reference 26V

BINARY-TO-BCD CONVERTERS

The BDM series are binary to BCD converters which are scaled to be compatible with an angular range of 0 to 360 mechanical degrees. The parallel input is in binary angle measure (MSB = 180°, next = 90° etc.) and the output is 5 decade BCD, 8421 coding. Input/outputs are TTL. Conversion time is 500 nanoseconds. Consult factory for extended temperature range versions.

SPECIFICATION SUMMARY

(typical @ +25°C and +5V dc unless otherwise noted)

	BDM1615500	BDM1616500	BDM1617500
Input:	14 bits	14 bits	16 bits
Full Scale Output:	359.98°	359°59′	359.99°
Rounding Error:	0.02°	1′	0.005°
Size:	2" x 4" x 0.4"	2" x 4" x 0.4"	3.125" x 2.625" x 0.8"
Power:	+5V @ 350mA	+5V @ 350mA	+5V @ 400mA
Temp. Range:	0 to +70°C	0 to +70°C	0 to +70°C

OTHER PRODUCTS AVAILABLE

SCDX1623 a 14-bit input solid state differential transmitter, with 4 minute accuracy.

SSCT1621 a 14-bit input solid state control transformer, with 4 minute accuracy.

SCM1677 a 14-bit angle input to 13-bit sine/cosine output converter, with 2 microsecond converter time.

SAC1763 a synchro to linear dc converter with tracking conversion plus a velocity output.

IDC1703 is a 12-bit inductosyn to digital converter with 150 revs/sec tracking rate.

DSC1705 and DSC1706 are 14- and 12-bit digital-to-synchro converters featuring 1.3VA output and vector amplitude variation of less than 0.1%.

DTM1716 and DTM1717 are 14- and 12-bit digital trigonometric multipliers which multiply an analog voltage V_1 by digital θ to produce analog voltage outputs $V_1 \sin \theta$ and $V_1 \cos \theta$.

SBCD1752, SBCD1753, SBCD1756 and SBCD1757 are synchro-to-digital converters featuring 14-bit BCD outputs with 0.1° resolution.

Sample-Hold Amplifiers

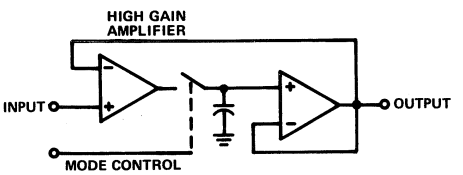
Orientation
Sample-Hold Amplifiers

The principal application for sample-hold amplifiers is to maintain an analog-to-digital converter's input constant during conversion, at a value representing the analog input as of a certain precisely known time. The characteristics of the SHA are crucial to system accuracy and the reliability of the digital data, especially in 12-bit and/or high-throughput-rate applications.

A sample-hold amplifier (s/h or SHA), as its name indicates, has two modes of operation, programmed by a digital control-input. In the *sample*– or *track*–mode, the output follows the input, usually with a gain of +1. When the mode-input switches to *hold*, the output of the SHA ideally retains the last value it had when the command to hold was given, and it retains that value until the logic input dictates *sample*, at which time the output ideally jumps to the input value and follows the input until the next *hold* command is given.

SHA CIRCUITRY AND HARDWARE

A sample-hold amplifier usually consists of a storage capacitor, input- and output buffer-amplifiers, and a switch and its drive-circuitry. During *sample*, the circuit is connected in a high-gain feedback loop to promote rapid charging of the capacitor. During *hold*, the capacitor is disconnected from its charging source and–ideally–retains its charge. The figure below shows a typical configuration (AD583, SHA1134): the input buffer is a high-gain differential amplifier with a current output that charges the capacitor through the logic-controlled switch. The capacitor is unloaded by a unity-gain buffer-follower. The output is fed back to the negative input (as in an op-amp follower configuration), and thus, in *sample*, the charge on the capacitor is compelled to follow the input. In *hold*, the input amplifier no longer drives the capacitor; it retains its charge, unloaded by the output follower. In another popular configuration, the capacitor is used as the feedback element of an inside-the-loop integrator (AD582, SHA-5).

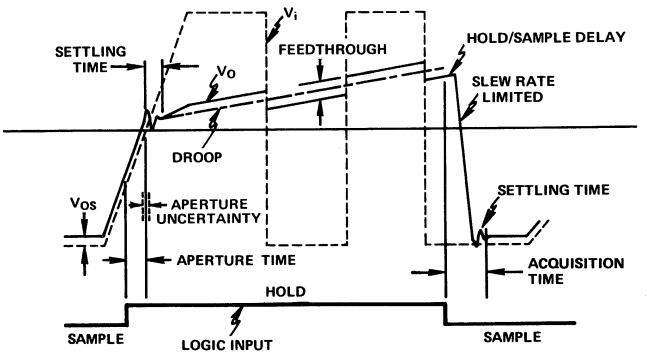


Since drive current is finite, and leakage current in *hold* is not zero, the capacitance–if large–limits the slewing rate in *sample* and–if small–converts leakage current to "droop" in *hold*. In s/h *modules*, the capacitance is usually fixed, and the properties of the complete device are optimized for one condition– and so specified. In s/h *monolithic ICs*, the capacitor is omitted, and furnished by the user (both for flexibility and because good capacitors for this purpose are hard to integrate). The optimum capacitance can be selected for the specific application. Design curves of performance vs. capacitance, given on the IC data sheets (AD582 and AD583) facilitate this process. In some types, the gain connections are external, like those of an op amp (AD582, AD583, SHA-5), permitting gains other than +1.

PERFORMANCE

In the *sample* mode, it is useful to consider that a SHA's performance can be characterized by specifications similar to those of a closed-loop operational amplifier (offset, drift, nonlinearity, gain error, bias current, etc.), but with somewhat slower response (gain-bandwidth, slewing rate, settling time) because of the need to charge the storage capacitor.

However, during the *sample-to-hold, hold,* and *hold-to-sample* states, the dynamic nature of the mode-switching introduces a number of specifications that are peculiar to SHAs. The most-important of these are defined below and illustrated in the adjoining figure. They include the *aperture time* and its *uncertainty*, the *sample-to-hold step, feedthrough* and *droop* (in hold), and *acquisition time.*



DEFINITIONS

Acquisition Time is the time required by the output of the device to reach its final value, within a specified error band, after the *sample* command has been given. Included are switch-delay time, the slewing interval, and settling time for a specified output-voltage change.

Aperture (Delay) Time is the time required after the *hold* command for the switch to open fully. The sample is, in effect, delayed by this interval, and the *hold* command would have to be advanced by this amount for precise timing.

Aperture Uncertainty–or *Aperture (Delay) Jitter*–is the range of variation in the *aperture time*. If the *aperture time* is "tuned

out" by advancing the *hold* command a suitable amount, this spec establishes the ultimate timing error, hence, the maximum sampling frequency to a given resolution. For example, the SHA-2A's specs are 10ns and 0.25ns; the corresponding specs of the AD583 are 150ns and 15ns.

Charge Transfer (or *offset step*), the principal component of *sample-to-hold* offset, is the charge transferred to the storage capacitor via stray capacitance when switching to the *hold* mode. It can sometimes be reduced by lightly coupling an appropriate-polarity version of the *hold* signal to the capacitor for cancellation. The associated voltage error (ΔQ/C) can be reduced by using greater capacitance for storage; but this increases response time.

Droop is the change of the output voltage during *hold* as a result of leakage or bias currents flowing through the storage capacitor. Its polarity depends on the sources of leakage current within a given device. In ICs, it is specified as a (*droop* or *drift*) current, in modules, a dV/dt.

Feedthrough is the fraction of the input signal variation or ac input waveform that appears at the output in *hold*. It is caused by stray capacitive coupling from the input to the storage capacitor, principally across the open switch.

Sample-to-Hold Offset, a shift in level between the last value in *sample* and the value settled-to in *hold*, is the residual step error after the *charge transfer* is accounted for and/or cancelled. Since it is unpredictable in magnitude and may be a function of the signal, it is also known as *offset nonlinearity*.

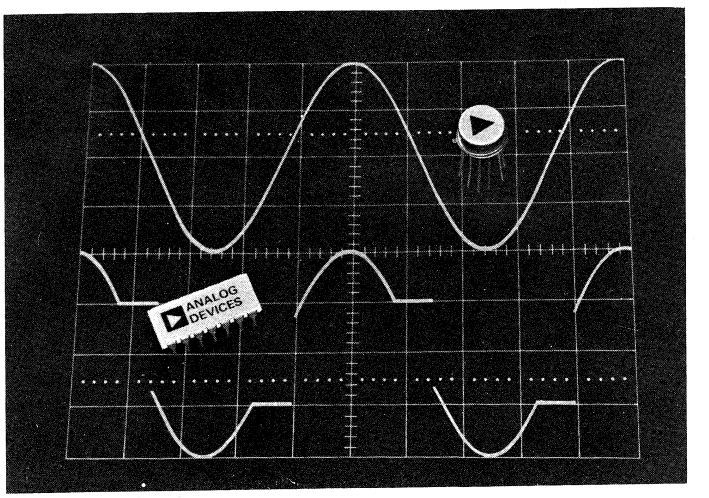
Selection Guide
Sample-Hold Amplifiers

Description	Model	Acquisition Time	Other	See Page
General Purpose	SHA-1A	5μs to ±0.01%	Module, aperture jitter 5ns max.	517
	AD582	6μs to ±0.1%	IC, aperture time 150ns	509
	AD583	4μs to ±0.1%	IC, aperture time 50ns	513
	SHA1134	3.4μs to ±0.01%	Module, aperture jitter 5ns max.	529
	SHA-5	15μs to ±0.01%	Module, aperture jitter 4ns	523
High Speed	SHA-2A	500ns to ±0.01%	Module, aperture jitter 0.25ns	519
Low Droop	SHA-3	75μs to ±0.01%	Module, aperture jitter 5ns, 10μV/ms droop, settling time 100μs to ±1mV, sample-to-hold	523
	SHA-4	20μs to ±0.01%	Module, aperture jitter 5ns, 10μV/ms droop, settling time 20μs to ±1mV, sample-to-hold	523
High Resolution	SHA-6	5ms to ±0.00075%	Module, use with ADC-16Q	525

Low Cost Sample/Hold Amplifier

AD582

FEATURES
Low Cost
Suitable for 12-Bit Applications
High Sample/Hold Current Ratio: 10^7
Low Acquisition Time: 6μs to 0.1%
Low Charge Transfer: <2pC
High Input Impedance in Sample and Hold Modes
Connect in Any Op Amp Configuration
Differential Logic Inputs



PRODUCT DESCRIPTION

The AD582 is a low cost integrated circuit sample and hold amplifier consisting of a high performance operational amplifier, a low leakage analog switch and a JFET integrating amplifier – all fabricated on a single monolithic chip. An external holding capacitor, connected to the device, completes the sample and hold function.

With the analog switch closed, the AD582 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open, the capacitor holds the output at its last level, regardless of input voltage.

Typical applications for the AD582 include sampled data systems, D/A deglitchers, analog de-multiplexers, auto null systems, strobed measurement systems and A/D speed enhancement.

The device is available in two versions: the "K" specified for operation over the 0 to +70°C commercial temperature range and the "S" specified over the full military temperature range, −55°C to +125°C. Both versions may be obtained in either the hermetically sealed, TO-100 can or the TO-116 DIP.

PRODUCT HIGHLIGHTS

1. The monolithic AD582 is the lowest cost sample and hold amplifier available. Until recently, quality sample and hold circuits could only be fabricated with costly discrete or hybrid components.
2. The specially designed input stage presents a high impedance to the signal source in both sample and hold modes (up to ±12V). Even with signal levels up to $\pm V_S$, no undesirable signal inversion, peaking or loss of hold voltage occurs.
3. The AD582 may be connected in any standard op amp configuration to control gain or frequency response and provide signal inversion, etc.
4. The AD582 offers a high, sample-to-hold current ratio: 10^7. The ratio of the available charging current to the holding leakage current is often used as a figure of merit for a sample and hold circuit.
5. The AD582 has a typical charge transfer less than 2pC. A low charge transfer produces less offset error and permits the use of smaller hold capacitors for faster signal acquisition.
6. The AD582 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.

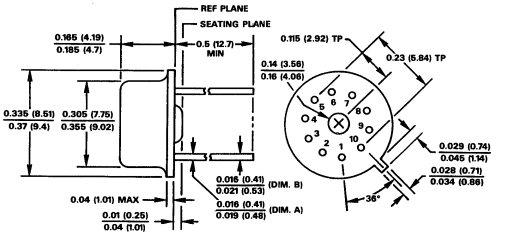
SPECIFICATIONS (typical @ +25°C, V_S = ±15V and C_H = 1000pF, A = +1 unless otherwise specified)

MODEL	AD582K	AD582S
SAMPLE/HOLD CHARACTERISTICS		
Acquisition Time, 10V Step to 0.1%, C_H = 100pF	6μs	*
Acquisition Time, 10V Step to 0.01%, C_H = 1000pF	25μs	*
Aperture Time, 20V p-p Input, Hold 0V	150ns	*
Aperture Jitter, 20V p-p Input, Hold 0V	15ns	*
Settling Time, 20V p-p Input, Hold 0V, to 0.01%	0.5μs	*
Droop Current, Steady State, ±10V_{OUT}	50pA max	*
Droop Current, T_{min} to T_{max}	1nA	50nA max
Charge Transfer	5pC max (1.5pC typ)	*
Sample to Hold Offset	0.5mV	*
Feedthrough Capacitance 20V p-p, 10kHz Input	0.05pF	*
TRANSFER CHARACTERISTICS		
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k	25k min (50k typ)	*
Common Mode Rejection V_{CM} = 20V p-p, F = 50Hz	60dB min (70dB typ)	*
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p, C_H = 200pF	1.5MHz	*
Full Power Bandwidth V_{OUT} = 20V p-p, C_H = 200pF	70kHz	*
Slew Rate V_{OUT} = 20V p-p, C_H = 200pF	3V/μs	*
Output Resistance Hold Mode, I_{OUT} = ±5mA	12Ω	*
Linearity V_{OUT} = 20V p-p, R_L = 2k	±0.01%	*
Output Short Circuit Current	±25mA	*
ANALOG INPUT CHARACTERISTICS		
Offset Voltage	6mV max (2mV typ)	*
Offset Voltage, T_{min} to T_{max}	4mV	8mV max (5mV typ)
Bias Current	3μA max (1.5μA typ)	*
Offset Current	300nA max (75nA typ)	*
Offset Current, T_{min} to T_{max}	100nA	400nA max (100nA typ)
Input Capacitance, f = 1MHz	2pF	*
Input Resistance, Sample or Hold 20V p-p Input, A = +1	30MΩ	*
Absolute Max Diff Input Voltage	30V	*
Absolute Max Input Voltage, Either Input	±V_S	*
DIGITAL INPUT CHARACTERISTICS		
+Logic Input Voltage Hold Mode, T_{min} to T_{max}, -Logic @ 0V	+2V min	*
Sample Mode, T_{min} to T_{max}, -Logic @ 0V	+0.8V max	*
+Logic Input Current Hold Mode, +Logic @ +5V, -Logic @ 0V	1.5μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	1nA	*
-Logic Input Current Hold Mode, +Logic @ +5V, -Logic @ 0V	24μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	4μA	*
Absolute Max Diff Input Voltage, +L to -L	+15V/-6V	*
Absolute Max Input Voltage, Either Input	±V_S	*
POWER SUPPLY CHARACTERISTICS		
Operating Voltage Range	±9V to ±18V	±9V to ±22V
Supply Current, R_L = ∞	4.5mA max (3mA typ)	*
Power Supply Rejection, ΔV_S = 5V, Sample Mode (see next page)	60dB min (75dB typ)	*
TEMPERATURE RANGE		
Specified Performance	0 to +70°C	-55°C to +125°C
Operating	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C	*
Lead Temperature (Soldering, 15 sec)	+300°C	*

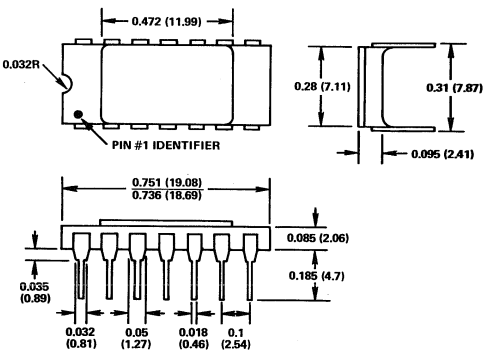
*Specifications same as AD582K.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



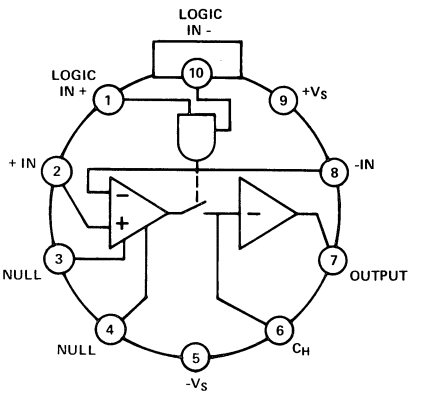
TO-100 "H"



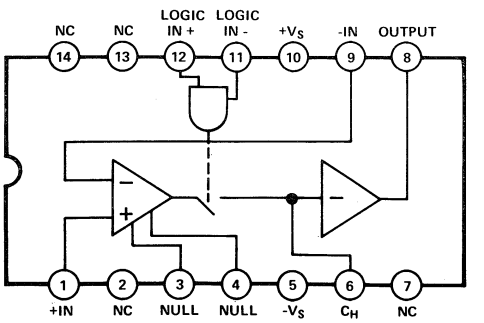
TO-116 "D"

PIN CONFIGURATIONS

TOP VIEW



10 PIN TO-100



14 PIN DIP

APPLYING THE AD582

Both the inverting and non-inverting inputs are brought out to allow op amp type versatility in connecting and using the AD582. Figure 1 shows the basic non-inverting unity gain connection requiring only an external hold capacitor and the usual power supply bypass capacitors. An offset null pot can be added for more critical applications.

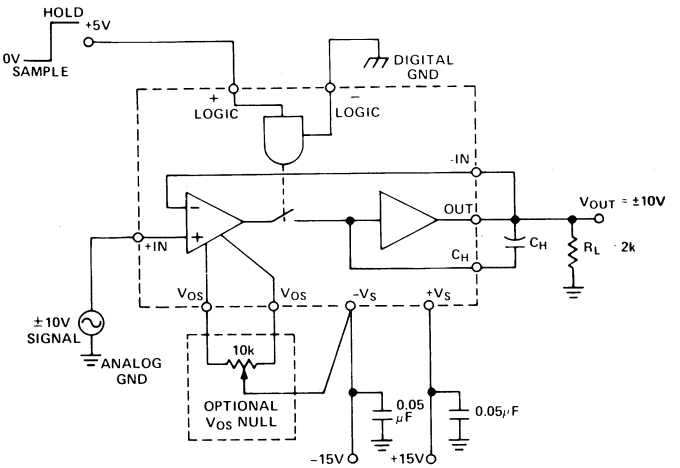


Figure 1. Sample and Hold with A = +1

Figure 2 shows a non-inverting configuration where voltage gain, A_V, is set by a pair of external resistors. Frequency shaping or non-linear networks can also be used for special applications.

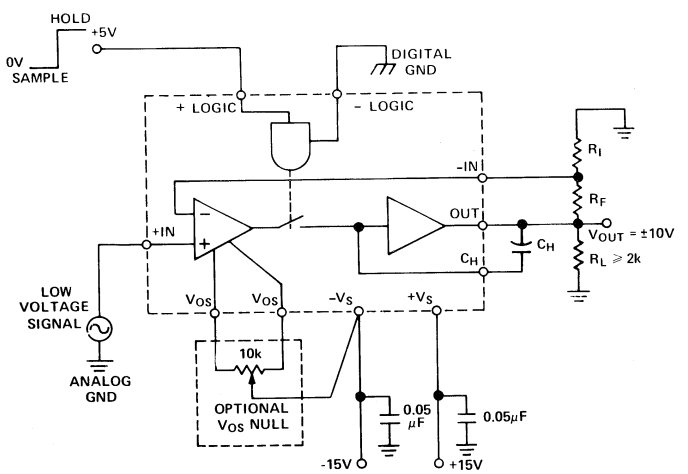


Figure 2. Sample and Hold with A = (1 + R_F/R_I)

The hold capacitor, C_H, should be a high quality polystyrene (for temperatures below +85°C) or Teflon type with low dielectric absorption. For high speed, limited accuracy applications, capacitors as small as 100pF may be used. Larger values are required for accuracies of 12 bits and above in order to minimize feedthrough, sample to hold offset and droop errors (see Figure 6). Care should be taken in the circuit layout to minimize coupling between the hold capacitor and the digital or signal inputs.

In the hold mode, the output voltage will follow any change in the $-V_S$ supply. Consequently, this supply should be well regulated and filtered.

Biasing the +Logic Input anywhere between -6V to +0.8V with respect to the -Logic will set the sample mode. The hold mode will result from any bias between +2.0V and ($+V_S$ - 3V). The sample and hold modes will be controlled differentially with the absolute voltage at either logic input ranging from $-V_S$ to within 3V of $+V_S$ (V_S - 3V). Figure 3 illustrates some examples of the flexibility of this feature.

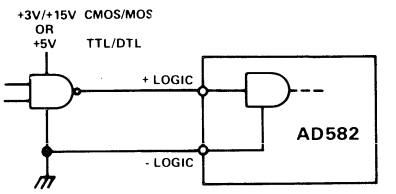


Figure 3A. Standard Logic Connection

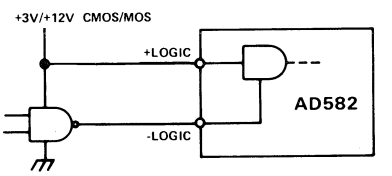


Figure 3B. Inverted Logic Sense Connection

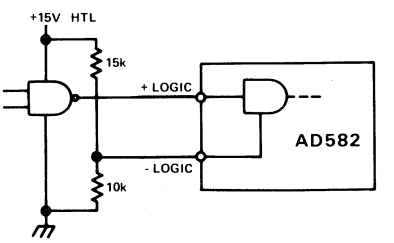


Figure 3C. High Threshold Logic Connection

DEFINITION OF TERMS

Figure 4 illustrates various dynamic characteristics of the AD582.

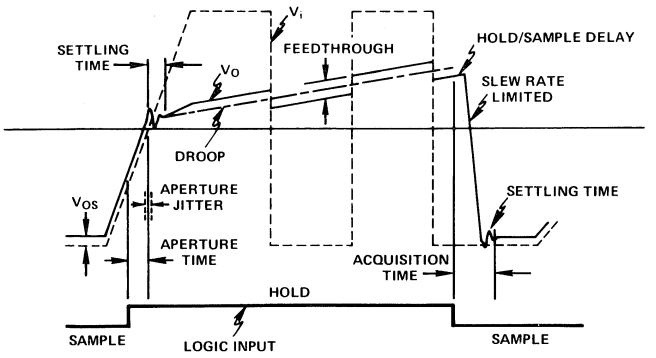


Figure 4. Pictorial Showing Various S/H Characteristics

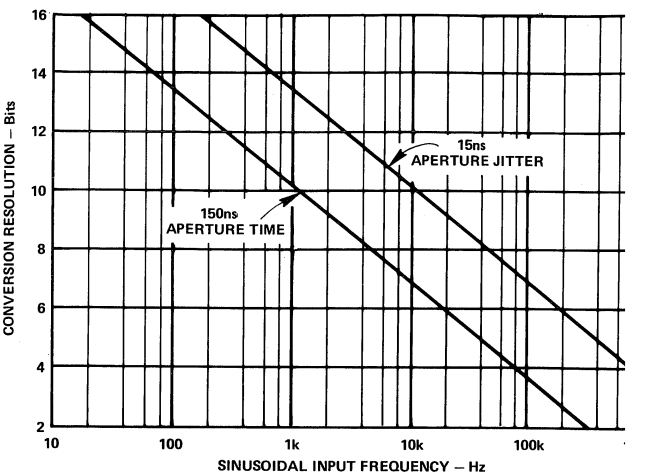


Figure 5. Maximum Frequency of Input Signal for ½L. Sampling Accuracy

Aperture Time is the time required after the "hold" command until the switch is fully open and produces a delay in the effective sample timing. Figure 5 is a plot giving the maximum frequency at which the AD582 can sample an input with a given accuracy (lower curve).

Aperture Jitter is the uncertainty in Aperture Time. If the Aperture Time is "tuned out" by advancing the sample-to-hold command 150ns with respect to the input signal, the Aperture Jitter now determines the maximum sampling frequency (upper curve of Figure 5).

Acquisition Time is the time required by the device to reach its final value within a given error band after the sample command has been given. This includes switch delay time, slewing time and settling time for a given output voltage change.

Droop is the change in the output voltage from the "held" value as a result of device leakage. In the AD582, droop can be in either the positive or negative direction. Droop rate may be calculated from droop current using the following formula:

$$\frac{\Delta V}{\Delta T}\ (\text{Volts/sec}) = \frac{I(pA)}{C_H(pF)}$$

(See also Figure 6.)

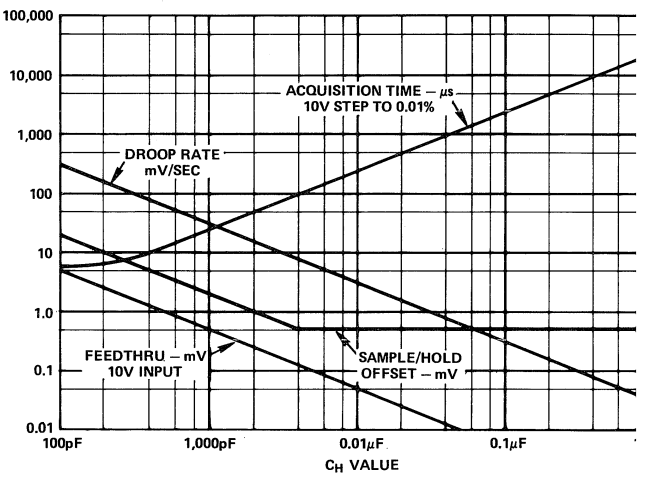


Figure 6. Sample and Hold Performance as a Function Hold Capacitance

Feedthrough is that component of the output which follows the input signal *after* the switch is open. As a percentage of the input, feedthrough is determined as the ratio of the feedthrough capacitance to the hold capacitance (C_F/C_H).

Charge Transfer is the charge transferred to the holding capacitor from the interelectrode capacitance of the switch when the unit is switched to the hold mode. The charge transfer generates a sample-to-hold offset where:

$$\text{S/H Offset (V)} = \frac{\text{Charge (pC)}}{C_H(pF)}$$

(See also Figure 6.)

Sample to Hold Offset is that component of D.C. offset independent of C_H (see Figure 6). This offset may be nulled using a null pot, however, the offset will then appear during the sampling mode.

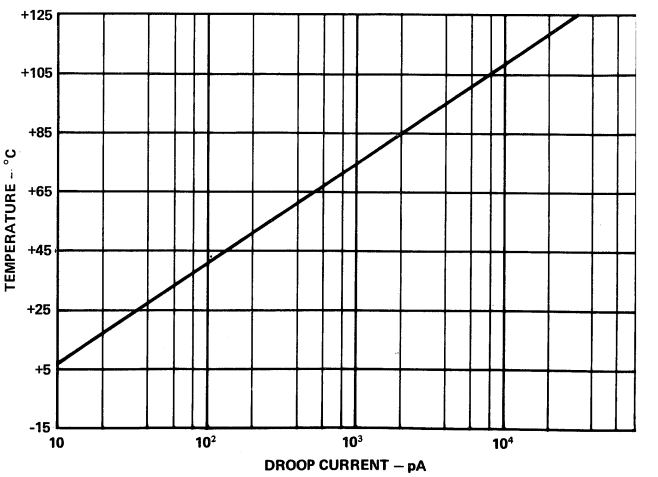


Figure 7. Droop Current Vs. Temperature

IC Sample and Hold Gated Op Amp

AD583

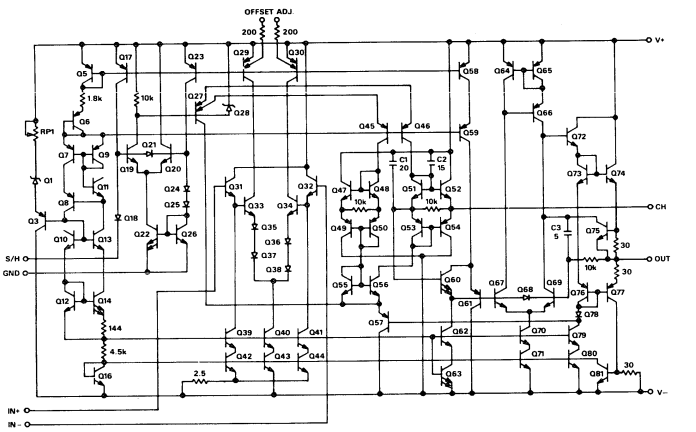
FEATURES
High Sample-to-Hold Current Ratio: 10^6
High Slew Rate: 5V/μs
High Bandwidth: 2MHz
Low Aperture Time: 50ns
Low Charge Transfer: 10pC
DTL/TTL Compatible
May Be Used as Gated Op Amp

PRODUCT DESCRIPTION

The AD583 is a monolithic sample and hold circuit consisting of a high performance operational amplifier in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier. An external holding capacitor, connected to the switch output, completes the sample-and-hold or track-and-hold function.

With the analog switch closed, the AD583 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open the capacitor holds the output at its previous level.

The AD583 may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.



Schematic Diagram

PRODUCT HIGHLIGHTS

1. Sample-and-hold operation is obtained with the addition of one external capacitor.
2. Low charge transfer (10pC) and high sample-to-hold current ratio insure accurate tracking.
3. Any gain or frequency response is available using standard op amp feedback networks.
4. High slew rate and low aperature time permit sampling of rapidly changing signals.
5. Output, gated through a low leakage analog switch, also makes the AD583 useful for applications such as analog switches, peak holding circuits, etc.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise specified)

MODEL	AD583K
OPEN LOOP GAIN R_L = 2kΩ, T_{min} to T_{max}	25k min (50k typ)
OUTPUT VOLTAGE SWING R_L = 2kΩ, T_{min} to T_{max}	±10V min
OUTPUT CURRENT	±10mA min
OUTPUT RESISTANCE	5Ω
OFFSET VOLTAGE T_{min} to T_{max}	6mV max (3mV typ) 8mV max (4mV typ)
BIAS CURRENT T_{min} to T_{max}	200nA max (50nA typ) 400nA max
OFFSET CURRENT T_{min} to T_{max}	50nA max (10nA typ) 100nA max
INPUT RESISTANCE	5MΩ min (10MΩ typ)
COMMON MODE RANGE	±10V min
COMMON MODE REJECTION T_{min} to T_{max}	74dB min (90dB typ)
GAIN BANDWIDTH PRODUCT	2MHz
SLEW RATE Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = ±10V p-p	5V/μs
RISE TIME Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = 400mV p-p	100ns
OVERSHOOT Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = 400mV p-p	20%
DIGITAL INPUT CURRENT V_{in} = 0, T_{min} to T_{max} V_{in} = +5.0V, T_{min} to T_{max}	 0.8V max (Logic "Sample") 2.0V min (Logic "Hold")
DIGITAL INPUT VOLTAGE Low T_{min} to T_{max} High T_{min} to T_{max}	 0.8V max 2.0V min
ACQUISITION TIME Av = +1, R_L = 2kΩ, C_L = 50pF to 0.1% of final value	4μs
APERTURE TIME	50ns
DRIFT CURRENT T_{min} to T_{max}	50pA max (5pA typ) 1.0nA max (0.05nA typ)
CHARGE TRANSFER	20pC max (10pC typ)
SUPPLY CURRENT	5.0mA max (2.5mA typ)
POWER SUPPLY REJECTION	74dB min (90dB typ)
OPERATING TEMP	0 to +70°C
STORAGE TEMP	-65 to +150°C

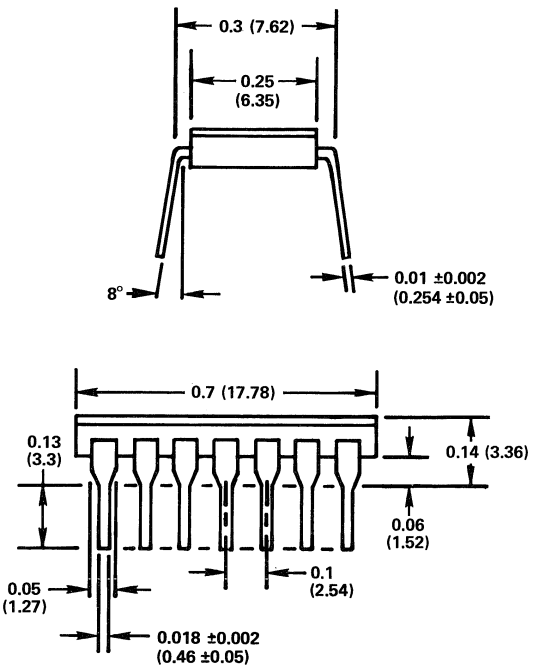
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Voltage between V+ and V- Terminals	40V
Differential Input Voltage	±30V
Digital Voltage (Pin 14)	+8V, -15V
Output Current	Short Circuit Protected
Internal Power Dissipation	30mW (Derate power dissipation by 4.3mW/°C above +150°C ambient temperature)

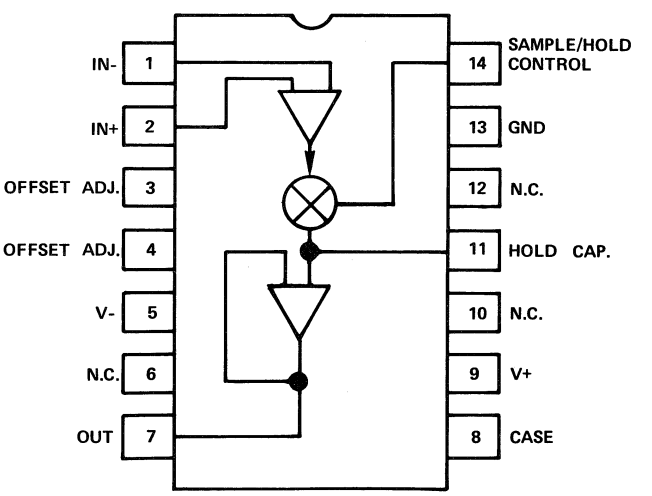
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



ALL DIMENSIONS ±0.010 UNLESS OTHERWISE SHOWN

PIN CONFIGURATION



APPLYING THE AD583

Figure 1 shows the AD583 connected in a simple sample and hold configuration with unity gain and offset nulling. Any other standard op amp gain and frequency response configuration may also be used. Note that the holding capacitor, C_H, should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), teflon or Mica types are recommended.

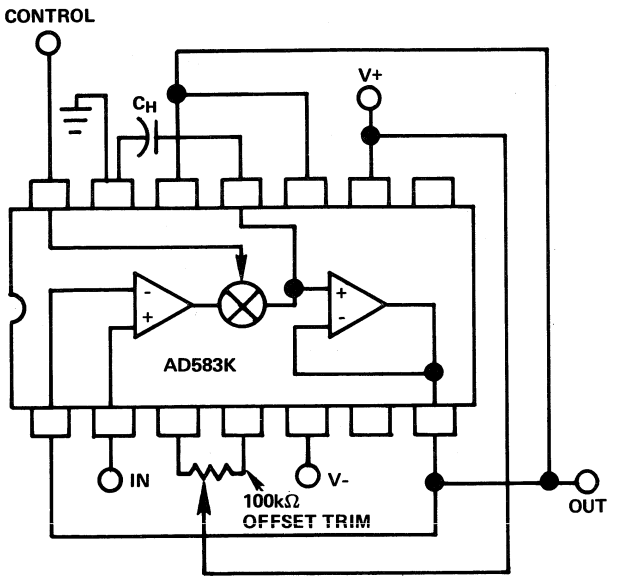


Figure 1. Basic Track-and-Hold/Sample-and-Hold

Figure 2 shows the guard ring used to reduce leakage paths between the pc board and the package. This minimizes drift during the hold command.

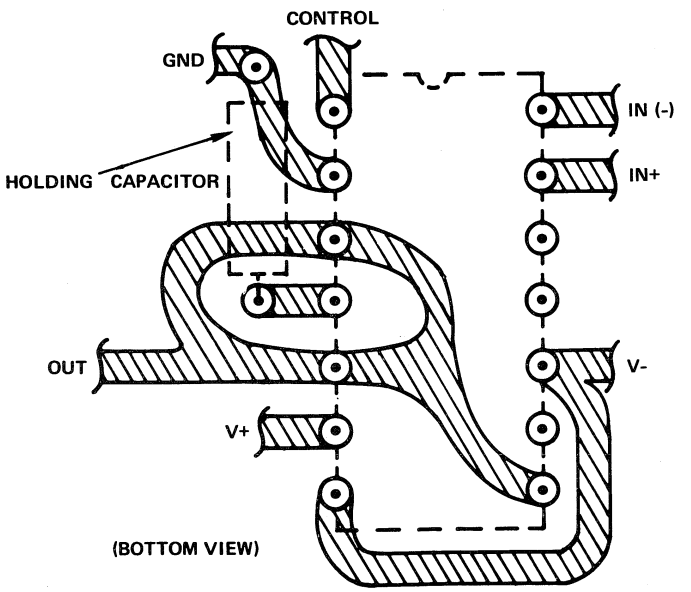


Figure 2. Guard Ring Layout

Also note that the input amplifier of the AD583 may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.

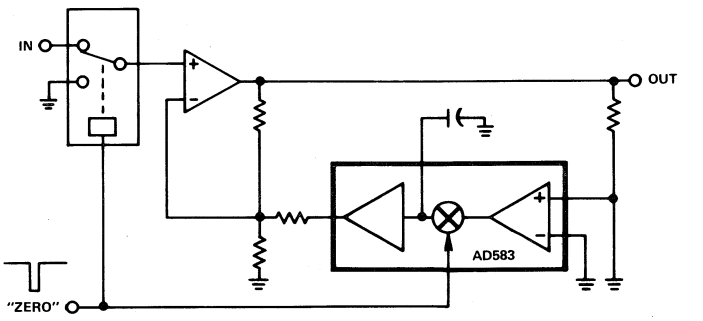


Figure 3. Automatic Offset Zeroing

The circuit of Figure 3 illustrates how the AD583 may be used to automatically zero a high gain amplifier. Basically, the input is periodically grounded and the output offset is then sampled and fed back to cancel the error. This technique is useful in A/D conversion, instrumentation, DVM's to eliminate offset drift errors by periodically rezeroing the system.

Care should be taken to assure that the zeroing loop is dynamically stable. A second sample-and-hold could be added in series with the output to remove the output discontinuity.

DEFINITION OF TERMS

Acquisition Time:

Acquisition Time is the time required by the device to reach its final value within ±0.1% after the sample command has been given. This includes switch delay time, slewing time, and settling time and is the minimum sample time required to obtain a given accuracy.

Charge Transfer:

Charge Transfer is the small charge transferred to the holding capacitor from the interelectrode capacitance of the switch when the unit is switched to the sample mode. Sample-to-hold offset error is directly proportional to this charge, where:

$$\text{Offset Error (V)} = \frac{\text{Charge (pC)}}{C_H\text{(pF)}}$$

Aperture Time:

The time required after the "hold" command until the switch is fully open. This delays the effective sample timing with rapidly changing input signals.

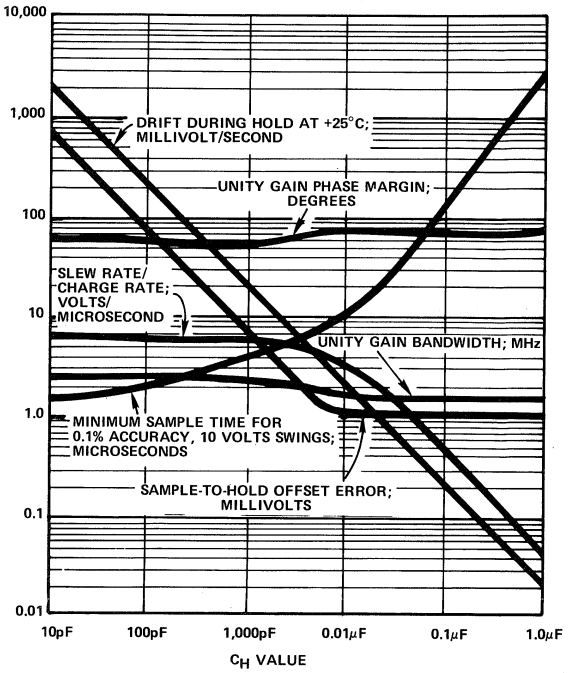
Drift Current:

Leakage currents from the holding capacitor during the sample mode cause the output voltage to drift. Drift rate (or droop rate) is calculated from drift current values using the formula:

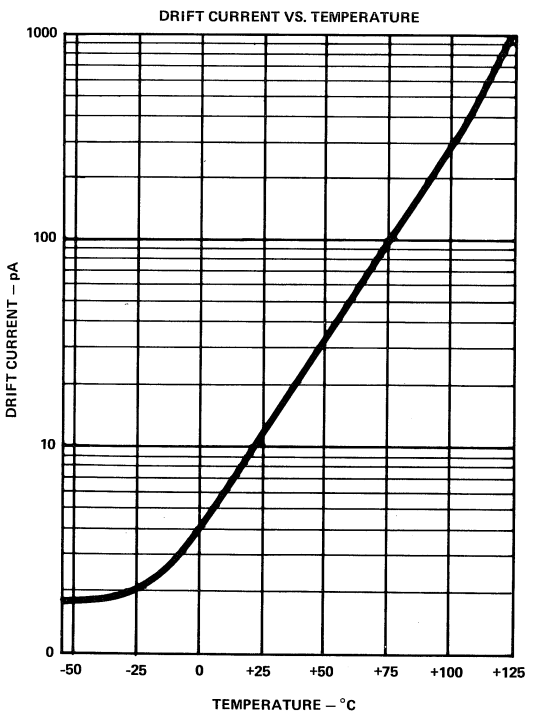
$$\frac{\Delta V}{\Delta T}\ \text{(Volts/sec)} = \frac{I\text{(pA)}}{C_H\text{(pF)}}$$

Performance Curves

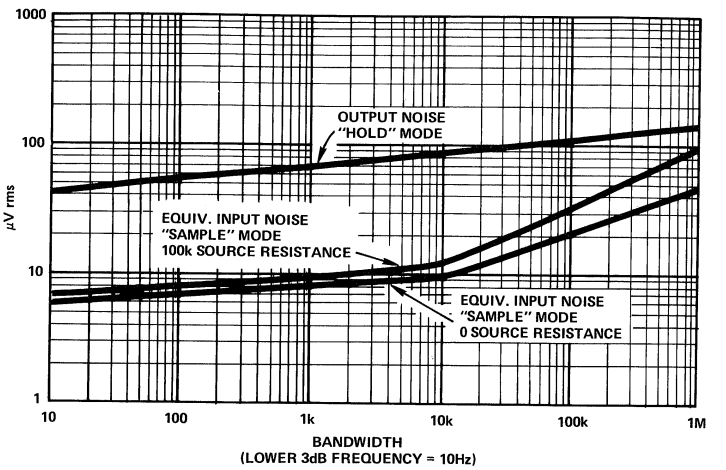
V_{SUPPLY} = ±15V dc, T_A = +25°C, C_H = 1,000pF unless otherwise specified)



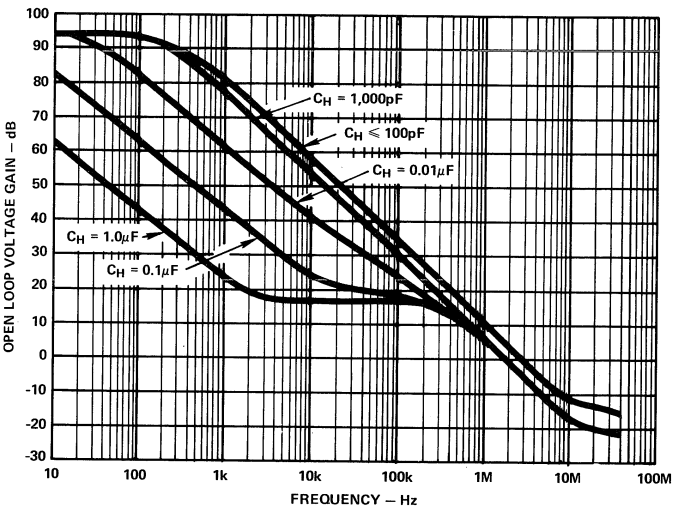
Typical Sample-and-Hold Performance as a Function of Holding Capacitance



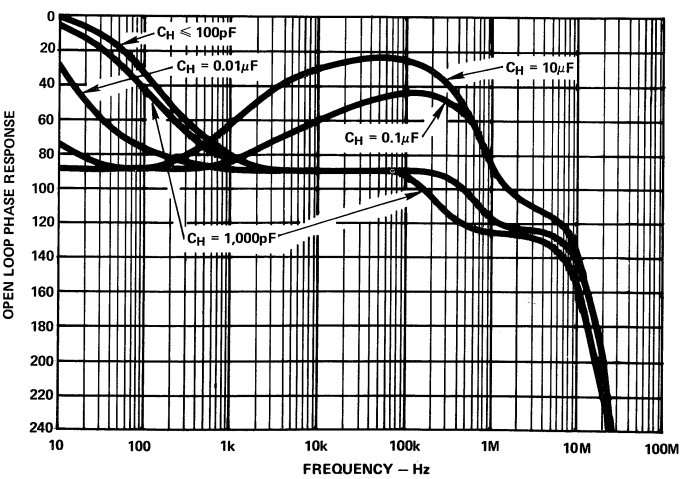
Drift Current vs. Temperature



Broadband Noise Characteristics



Open Loop Frequency Response



Open Loop Phase Response

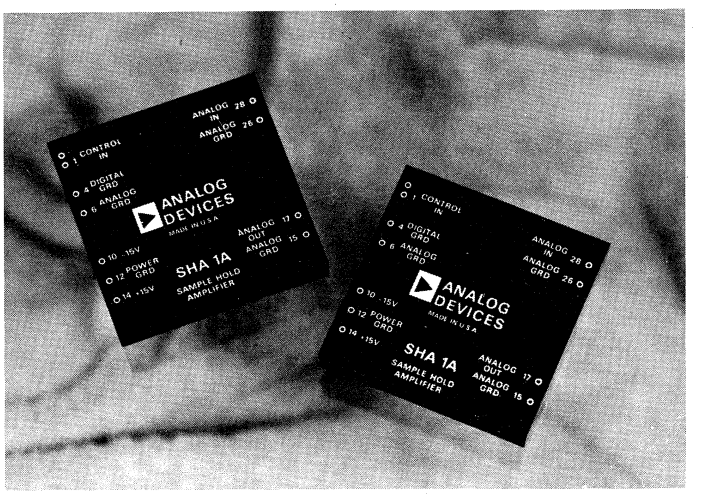
ANALOG DEVICES

Sample and Hold Module

SHA-1A

FEATURES
- 12-Bit System Compatible
- Throughput Nonlinearity 2mV max Over ±10V Input Range
- Acquisition Time 5μs max
- Input Buffer, $10^{12}\Omega$ R_{IN}
- Independent Digital, Analog, and Power Grounds
- Modular 0.4" High Construction
- Standard ±15V dc Power
- No External Adjustments Required

APPLICATIONS
- Data Acquisition Systems
- Data Distribution Systems
- Track and Hold
- Sample and Hold
- Peak Measurement Systems



GENERAL DESCRIPTION

The SHA-1A is a fast sample-and-hold module with low droop rate and overall accuracy compatible with 12-bit A/D conversion systems operating to ½LSB accuracy. When in the "sample" mode, the module appears as a fast amplifier with 5μs settling time of 0.01%, 1nA input current, 25μV/°C drift, and unity gain with ±10V at ±20mA output current capability. When in the "hold" mode, the droop rate is 50μV/ms max, so the SHA-1A will hold an input signal to 0.01% of full scale (20V p-p) for 40ms, sufficient for 12-bit A/D conversion.

SAMPLE TO HOLD CHARACTERISTICS

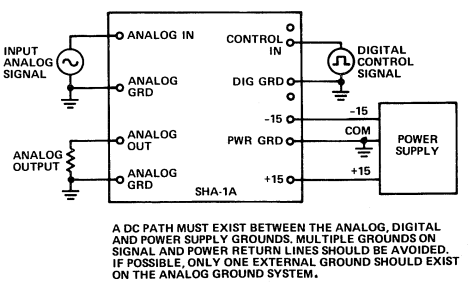
Of prime importance in selecting Sample-and-Hold amplifiers is the transition characteristics when the module is commanded into hold by the digital control line. A finite delay will occur between initiation of the hold command, and actual disconnection of the hold capacitor from the input buffer amplifier. In the SHA-1A, this delay time is 40ns maximum. The uncertainty, or jitter over which this delay time will vary from cycle to cycle, as the module is repeatedly commanded into hold, is ±5ns. In most systems, the jitter specification is the limiting factor on overall system speed for a given accuracy, since fixed delays can be removed by adjusting the system timing. The 5ns jitter specification means the SHA-1A can track a signal slewing up to 0.2V/μs, and "capture" that signal to within a 1mV accuracy for A/D conversion.

OVERALL ACCURACY

The SHA-1A is guaranteed to have an overall throughput nonlinearity of 2mV max over a ±10V input range, or 1mV max over 0 to +10V inputs. This specification combines the effects of common mode errors, gain nonlinearity and sample to hold offset nonlinearity. It is no longer necessary to guess at the combined effects of individual errors since the SHA-1A specification guarantees that its total nonlinearity errors are sufficiently low to insure ½LSB accuracy in 12-bit systems.

GROUNDING

Many data acquisition systems suffer from digital ground induced noise appearing in the analog system. To counteract this problem, the SHA-1A has three separate ground systems. The digital ground is actually one side of a differential amplifier, with the Sample/Hold digital control input being the other input of this amplifier. This effectively prevents digital ground noise from being impressed into the analog signal channel. The power ground and analog input/output grounds are also separate, so that power supply ground noise is reduced by the rejection coefficients of the amplifiers, normally well over 90dB. Ground connection instructions are given in Figure 1.



A DC PATH MUST EXIST BETWEEN THE ANALOG, DIGITAL AND POWER SUPPLY GROUNDS. MULTIPLE GROUNDS ON SIGNAL AND POWER RETURN LINES SHOULD BE AVOIDED. IF POSSIBLE, ONLY ONE EXTERNAL GROUND SHOULD EXIST ON THE ANALOG GROUND SYSTEM.

Figure 1. SHA-1A Connections and Grounding

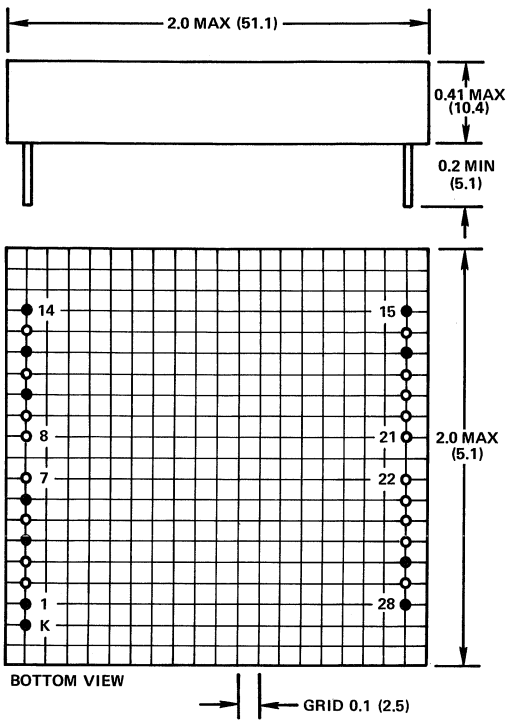
SPECIFICATIONS (typical @ +25°C and nominal supply voltages, unless otherwise noted)

ACCURACY	
Gain	+1
Gain Error	+0.0, -0.05% max
Total Throughput Nonlinearity	2mV max Over ±10V Input Range
(Includes Gain and Sample to Hold Nonlinearities)	1mV max Over 0 to +10V or 0 to -10V Input Range
FREQUENCY RESPONSE IN SAMPLE MODE	
Small Signal -3dB	500kHz min
Slew Rate	4V/μs
Settling Time to 0.01% for 20 Volt Input Step	5μs max
SAMPLE TO HOLD SWITCHING	
Aperture Delay Time	40ns max
Jitter (Cycle to Cycle Variance in Delay)	5ns Peak
Switching Transient Settling Time (to ±1mV)	300ns
HOLDING CHARACTERISTICS	
Droop Rate	50μV/ms max
Droop Rate vs. Temp.	X2/10°C
Feedthrough (10kHz, 20V p-p Input)	0.005% max
HOLD TO SAMPLE SWITCHING	
Acquisition Time to 0.01% of Full Scale	5μs max
INPUT CHARACTERISTICS	
Input Resistance	$10^{12}\Omega$
Input Capacitance	5pF max
Input Bias Current	10nA max, 1nA typ
Initial Input Offset	1mV max
Offset vs. Supply	100μV/%
Offset vs. Temp.	25μV/°C max
Input Voltage, max Safe	±15V
Input Voltage, Normal Operation	±10V
OUTPUT CHARACTERISTICS	
Output Voltage, Current	±10V min at ±20mA min
Maximum Load Capacitance at Output	500pF
DIGITAL CONTROL	
Logic Levels (DTL/TTL Comp)	
("1") Sample	+2V to +5.5V @ 40nA
("0") Hold	-0.5V to +0.8V @ 20μA
POWER REQUIREMENTS	±15V dc @ +10mA, -15mA (±3% Tolerance on Voltage)
TEMPERATURE RANGE	
Rated Accuracy	0 to +70°C
Storage	-55°C to +85°C

Specifications subject to change without notice.

OUTLINE DIMENSIONS AND PIN CONNECTIONS

Dimensions shown in inches and (mm).



Pins: 0.019 ±0.001 (0.48 ±0.03) dia. half-hard brass, gold plated per MIL-G-45204 Class 1, Type 2

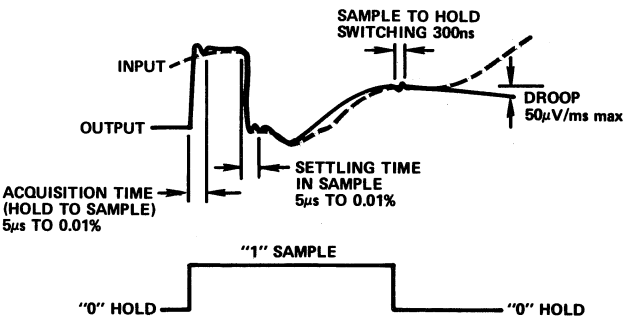


Figure 2. Illustration of Dynamic Specifications (not to scale)

OTHER PRODUCTS

Multiplexer MPX-8A

Available with 8 channels, digital addressing, expandable to 64 channels. Input range ±10V with standard ±15V dc supplies. MOSFET design prevents burn out due to power failure, -80dB cross-talk, 2μs max switching time. Accuracy to 0.01%.

Analog to Digital Converter ADC-QM, ADC1133

The QM is available in 8-, 10-, or 12-bit resolution and accuracy. Extremely low TCs, 3ppm differential linearity.

The new ADC1133 is 12 bits A/D with a conversion time of 25μs. TCs are also a low 3ppm.

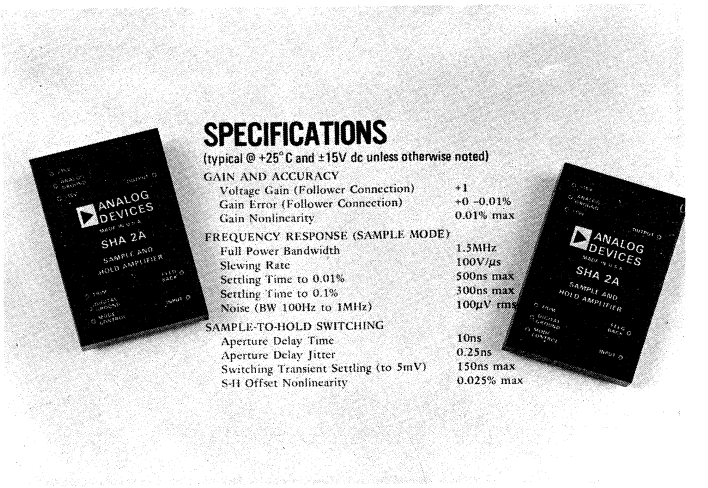
ANALOG DEVICES

Very High Speed 12 Bit Sample-and-Hold Amplifier

SHA-2A

FEATURES
±10V Range
10ns Aperture Delay
¼ns Aperture Jitter
300ns Settling Time
0.01% Linearity Error
Complete with Input Buffer

APPLICATIONS
Track and Hold
Peak Measurement Systems
Data Acquisition Systems
Simultaneous Sample-and-Hold



SPECIFICATIONS
(typical @ +25°C and ±15V dc unless otherwise noted)

GAIN AND ACCURACY	
Voltage Gain (Follower Connection)	+1
Gain Error (Follower Connection)	+0 -0.01%
Gain Nonlinearity	0.01% max
FREQUENCY RESPONSE (SAMPLE MODE)	
Full Power Bandwidth	1.5MHz
Slewing Rate	100V/μs
Settling Time to 0.01%	500ns max
Settling Time to 0.1%	300ns max
Noise (BW 100Hz to 1MHz)	100μV rms
SAMPLE-TO-HOLD SWITCHING	
Aperture Delay Time	10ns
Aperture Delay Jitter	0.25ns
Switching Transient Settling (to 5mV)	150ns max
S-H Offset Nonlinearity	0.025% max

GENERAL DESCRIPTION

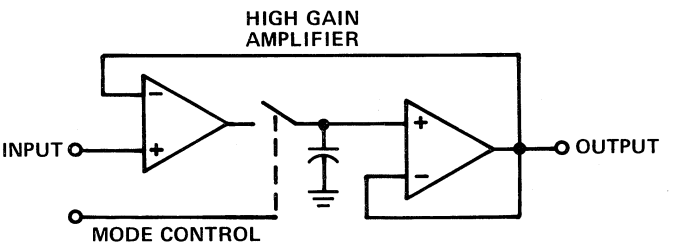
The SHA-2A is a very fast sample-and-hold module with accuracy and dynamic performance appropriate for application with very fast 12-bit A/D converters. In the "sample" mode, it acts as a fast amplifier, tracking the input signal. When switched to the "hold" mode, the output is held at a level corresponding to the input signal voltage at the instant of switching. The droop rate in "hold" mode is appropriate to allow 12-bit accurate conversion by very fast A/D converters, e.g. those having total conversion times of up to several microseconds.

DYNAMIC PERFORMANCE

The SHA-2A was designed for use with very fast A/D converters such as the Analog Devices' ADC1103 series, which convert 12 bits in less than 4μs. Since such converters will often be used to acquire data for fast slewing signal sources, the dynamic parameters were designed with this in mind. Slewing rate is 100V/μs, and settling time to 0.01% is <500ns. The aperture time of <10ns, and aperture jitter of 0.25ns, means that an input signal slewing at 200mV/μs (3kHz) will be acquired to appreciably better than one LSB uncertainty for a 12-bit converter. The maximum droop rate of 100μV/μs means that when the SHA-2A is in "hold," its output is holding constant for the ADC input, changing <0.1LSB per conversion time for a 1μs 12-bit ADC. The fast settling of the sample-hold transient allows the following A/D converter to make an accurate MSB decision only 150ns after the "hold" command is applied.

UNIQUE CIRCUIT ARRANGEMENT

Most sample-and-hold amplifier modules have input terminals connected either to a unity gain buffer, or directly to the hold capacitor through a switch. In the SHA-2A an input buffer is used, but the feedback connection has been omitted in order to allow the user to connect the SHA-2A as a follower, for unity gain, or to provide gain in order to simplify signal conditioning in his system. We call the user's attention to the fact that the input buffer bandwidth will go down as gain is increased, as it does for all op amps. Performance data is given for the unity gain buffer connection.



Typical Block Diagram

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

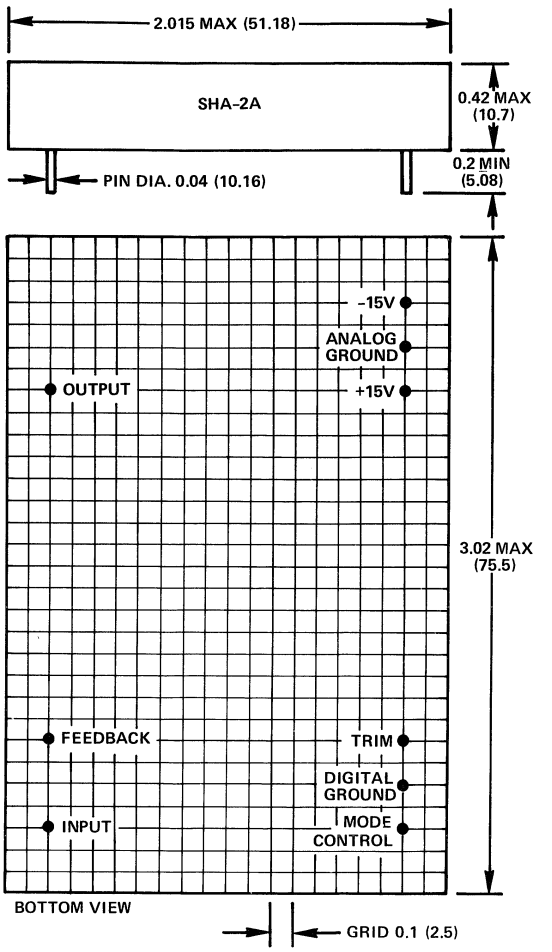
GAIN AND ACCURACY	
Voltage Gain (Follower Connection)	+1
Gain Error (Follower Connection)	+0 –0.01%
Gain Nonlinearity	0.01% max
INPUT CHARACTERISTICS	
Input Impedance	$10^{11}\Omega$ and 7pF
Input Bias Current	100pA max
Input Range	±10V min
Initial Offset Voltage	Adjustable to 0
Offset vs Temp	100μV/°C max
Offset vs Supply	500μV/%
FREQUENCY RESPONSE (SAMPLE MODE)	
Full Power Bandwidth	1.5MHz
Slewing Rate	100V/μs
Settling Time to 0.01%	500ns max
Settling Time to 0.1%	300ns max
Noise (BW 100Hz to 1MHz)	100μV rms
SAMPLE-TO-HOLD SWITCHING	
Aperture Delay Time	10ns
Aperture Delay Jitter	0.25ns
Switching Transient Settling (to 5mV)	150ns max
S-H Offset Nonlinearity	0.025% max
HOLDING CHARACTERISTICS	
Droop Rate	100μV/μs max
Feedthrough (10kHz, 20V p-p Input)	5mV p-p max
OUTPUT CHARACTERISTICS	
Output Voltage	±10V min
Output Current	±20mA min
Short Circuit Current	±70mA
Maximum Capacitive Load	200pF
DIGITAL CONTROL	
Logic Levels[1]	
Sample ("1")	>+2V @ 1μA to 3.7V @ 1mA
Hold ("0")	<0.8V 0 to 0.8V @ –7mA
POWER REQUIREMENTS	±15V ±2% @ 100mA
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	–25°C to +85°C
MATING SOCKET	AC1035

NOTE
[1] To achieve rated specifications, logic driving digital control input should be Schottky TTL.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



Pins are half hard brass, gold plated per MIL-G-45204B, Class I, Type II - Pin Diameter is 0.040" (0.483mm) ±0.001" (0.025mm).

MATING SOCKET AC1035

The AC1035 is a simple socket assembly, 2" x 3", for mounting the SHA-2A.

MOUNTING BOARD AC1503

The AC1503 is a 2¼" x 4½" PC board with edge connector. It contains a trimmer pot for adjustment of offset, as well as a logic chip, needed to simulate terminal characteristics of the SHA-2. When the SHA-2A is mounted on the AC1503, the assembly is a pin-compatible replacement for the SHA-2.

CIRCUIT DESCRIPTION

The SHA-2A is a typical sample-and-hold module in that it consists of an input isolator, a fast switch, the storage element, and an output buffer. It differs from typical designs in two particular respects:

1. Speed – since it was designed to be compatible with very fast A/D converters of the 1μs total conversion time class, aperture delay time was reduced to 10ns, aperture jitter to 0.25ns, and settling time to 300ns for 10-bit performance.

2. Application versatility – the user completes the feedback circuit for the SHA-2A external to the module. Therefore, the module may be used in various input configurations and can easily be arranged to provide circuit gain of more than unity, to simplify signal conditioning in a subsystem.

FEEDBACK CONNECTIONS

A block diagram of the SHA-2A is shown in Figure 1. The input section acts as a voltage-to-current converter, providing the current needed to charge the "HOLD" capacitor. The output amplifier isolates the "HOLD" capacitor, and provides low output impedance for driving the load. Since feedback is not hardwired in the module, both inverting and noninverting input terminals are available, and the SHA-2A can be connected as a follower with unity gain or potentiometric gain, as well as an inverter or even a differential amplifier. Since the unity gain follower mode will be the most frequent application, performance data in the specifications is based on this operating mode.

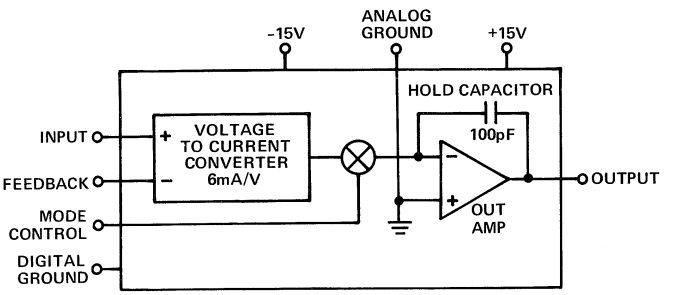


Figure 1. Block Diagram

1. Figure 2 shows feedback connections to the SHA-2A for the unity gain follower mode. Output (pin #3) is connected to feedback (or – input, pin #2). Input signal is applied to pin #1.

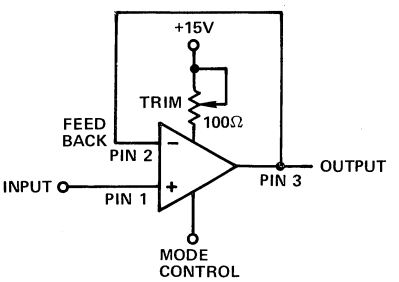


Figure 2.

2. Figure 3 shows feedback connections for noninverting operation with potentiometric gain. When the indicated values are installed, gain will be +5. As in all operational amplifiers, gain-bandwidth product is a constant for a given sample-and-hold. Effective 3dB bandwidth will be inversely proportional to gain.

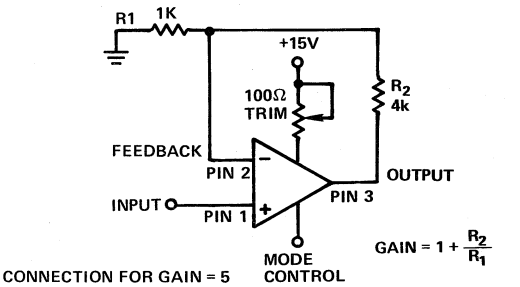


Figure 3.

3. By using conventional operational amplifier feedback connections, the SHA-2A can be connected for use as an inverter, with various gains (as determined by the R_F/R_I ratio), or as a differential amplifier.

CHARACTERISTICS OF REAL SAMPLE-HOLDS

In the ideal Sample-Hold of Figure 4a, tracking is error-free, acquisition and release occur instantaneously, settling times are zero, and hold is infinite. Commercially-available units are specified in terms of the extent to which they depart from the ideal. Here are some of the commonly-occuring deviations.

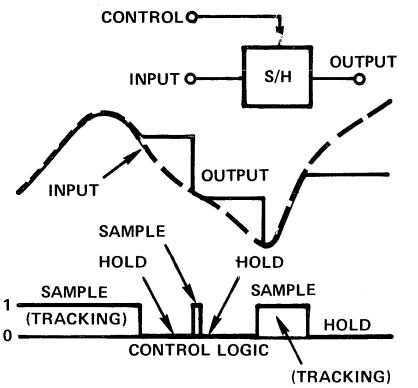


Figure 4a.

<u>During Sample (Figure 4b):</u>

Settling Time: The time required for the output to attain its final value within a specified fraction of full-scale when a full-scale input step is applied (0 to ±FS or -FS to +FS). See also *Acquisition Time* (Figure 4e).

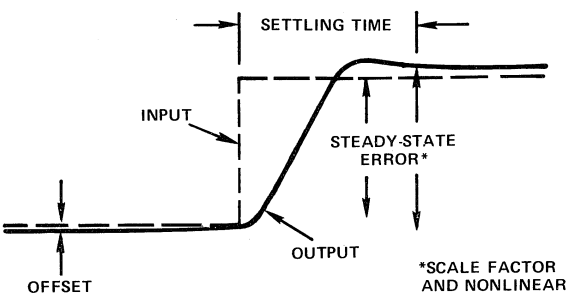


Figure 4b.

Sample to Hold (Figure 4c):

Aperture Time: The time elapsing between the command to *Hold* and the actual opening of the *Hold* switch. It has two components: a nominal time delay, and an uncertainty caused by jitter or variation from time-to-time or unit-to-unit. If a signal changing at a rate of 1V/μs must be resolved to within 0.1% of 10V (FS), the aperture *uncertainty* must be <10ns, provided that it is possible to anticipate the nominal delay and advance the command by an appropriate interval. In some sampled-data system applications, such as spectrum analyzers, auto- and cross-correlation function generators, the delay is unimportant, but the uncertainty directly affects uniformity of the sampling rate.

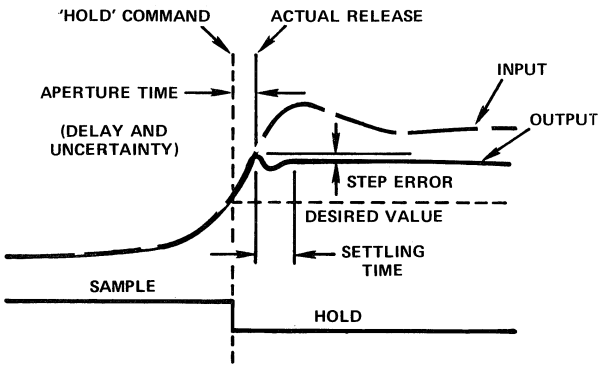


Figure 4c.

Switching Transients: At the time the switch opens, the circuit may not be in equilibrium — especially if the signal is changing rapidly — because of amplifier delay error, etc. This will cause transients at the time the switch opens.

Settling Time: The interval required for the output to attain its final value within a specified fraction of full scale, following the opening of the switch.

Sample-to-Hold Offset: A step error occurring at the initiation of the *Hold* mode caused by "dumping" of charge into the storage capacitor via the capacitance between the control circuit and the capacitor side of the switch (e.g., the gate-to-drain capacitance of a field-effect transistor).

During Hold (Figure 4d):

"DROOP": A drift of the output at an approximately constant rate caused by the flow of current through the storage capacitor (dV/dt = I/C). The current is the sum of the leakage across the switch and the amplifier's bias current.

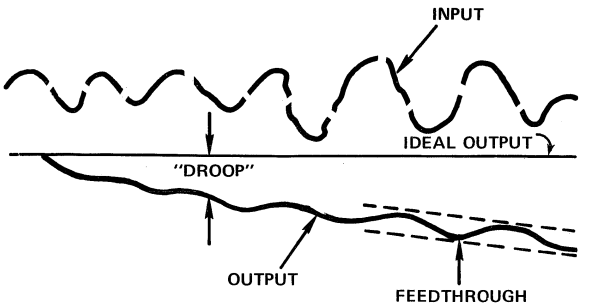


Figure 4d.

Feedthrough: The fraction of input signal that appears at the output in *Hold,* caused primarily by capacitance across the switch. Usually measured by applying a full-scale sinusoidal input at a fixed frequency (e.g., 20V p-p at 10kHz), and observing the output.

Dielectric Absorption: The tendency of charges within a capacitor to redistribute themselves over a period of time, resulting in "creep" to a new level when allowed to rest after large, fast changes. <0.01% for good polystyrene and teflon capacitors, as large as several percent for ceramic and mylar capacitors.

Hold to Sample (Figure 4e):

Acquisition Time: The time duration for which an input must be applied for sampling to the desired accuracy. Essentially the same as *Settling Time* for feedback types.

Hold-to-Sample Transients: Transients (e.g., spikes) occurring between the *Sample* command and final settling.

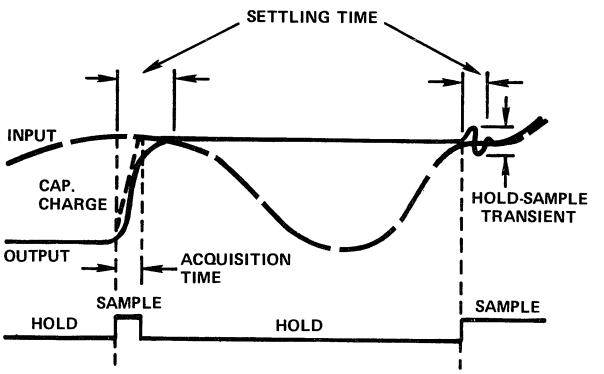


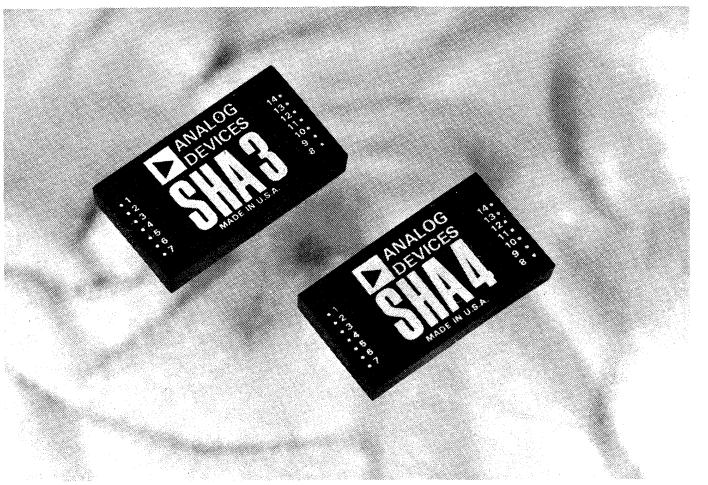
Figure 4e.

Low Cost, Low Droop, Sample-and-Hold

SHA-3, -4, -5

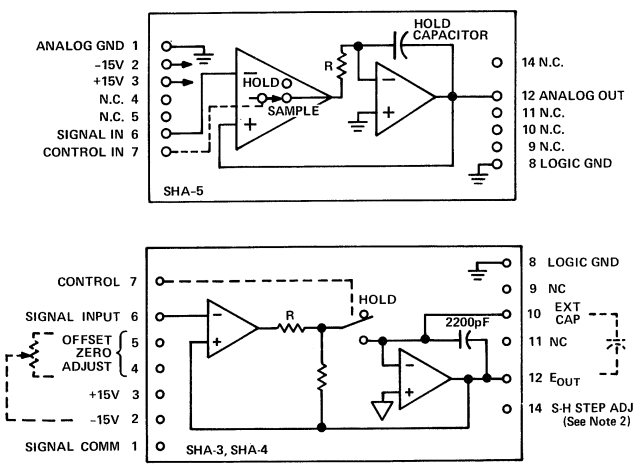
FEATURES
Low Tracking Error: 0.01% at Low Frequency
Low Drift: 10μV/°C (SHA-3, 4)
Low Droop Rate: 10μV/ms (SHA-3, 4)
Short Aperture: 40ns
High Input Impedance in Sample Mode: 4×10^9 ohms
DTL/TTL Compatible
Compact Module: 1 1/8" x 2" x 0.4"

APPLICATIONS
Data Acquisition
Data Distribution
Peak and Valley Measurement
Simultaneous Sample and Hold



GENERAL DESCRIPTION

The SHA-3 to -5 are a family of general purpose sample and hold amplifiers built in a very compact module package. When DTL or TTL Logic "1" is applied at the control input, the operating mode is "Sample", and the output tracks the input at unity gain, without polarity inversion. When Logic "0" is applied, the operating mode is "Hold", and the output remains at the value just prior to the opening of the switch. See Figure 1.



Notes: (SHA-3, -4)
1. Offset zero adjustment: (optional)
   a. Sample mode, signal input grounded, adjust for output zero.
2. Sample-to-Hold offset step trim (optional) 100Ω max; Adjust for minimum offset step when external capacitor is used.

Figure 1. Simplified Block Diagrams

TRACKING LOOP

Charge proportional to the instantaneous value of input signal voltage is stored in the hold capacitor (see Figure 1). Since this capacitor is connected in a high gain feedback loop, its charging current is provided by an amplifier. Thus, the SHA's are relatively easy to apply, since capacitor charging current does not have to be supplied by the signal source.

DYNAMIC PERFORMANCE

Of prime importance in selecting sample and hold amplifiers is the transition characteristic when the module is commanded into "Hold" by the application of a logic "0" to the control input. A finite delay occurs between the application of the hold command and the response of the internal switching circuit. In the SHA-5, this "aperture delay" time is 40ns. The aperture jitter, or the cycle to cycle repeatability of aperture delay, is approximately 4ns. In most systems and for most applications, the jitter specification is the limiting factor on overall system speed for a given accuracy, since the essentially fixed aperture delay can be compensated by adjusting the system timing.

The SHA-5 settles to 0.01% in 15μs or less after a 20 volt step input. When switched to "Hold", the switching transient settles to ±1mV within 2μs. Since aperture jitter is approximately 4ns, an input signal slewing at a rate of 12.5mV/μs will be acquired to appreciably better than one LSB uncertainty for a 12 bit A/D converter.

The SHA-3 and SHA-4 are characterized by low droop rate of 10μV/ms and are ideally suited for most data acquisition and data distribution applications.

APPLICATIONS

In the design of sample and hold amplifiers, the major tradeoff is usually in connection with speed of acquisition and droop in "Hold". As the size of the storage capacitor is increased, the droop rate improves and the acquisition time lengthens. The SHA-5, conceived as a general purpose product, has been designed with droop rate appropriate for use with almost all successive approximation A/D converters; it is also well suited for use in data distribution systems using D/A converters with up to 12 bit resolution, where the data update rate is not slower than approximately 10 per second. The 15μs settling time makes the SHA-5 appropriate for use with all but the fastest A/D converters.

SPECIFICATIONS (typical @ +25°C and nominal supply voltages, unless otherwise specified)

MODEL	SHA-3	SHA-4	SHA-5
ACCURACY			
Gain	+1	*	*
Gain Error	±0.01%	*	*
Gain Tempco	±1ppm/°C max	*	±0.3ppm/°C
SAMPLE MODE DYNAMICS			
Small Signal Frequency Response (-3dB)	50kHz	*	1.4MHz
Full Power Bandwidth	10kHz	*	30kHz
Settling Time to 0.01% (20V input step)	100μs max	20μs	15μs max
Overload Recovery (50% overload)	150μs	*	10μs
SAMPLE TO HOLD SWITCHING			
Aperture Delay Time	50ns	*	40ns
Aperture Jitter	5ns	*	~4ns
Switching Transient Settling Time (to ±1mV)	10μs	*	2μs
Sample-to-Hold Offset	1mV max	*	3mV (10mV max)
HOLDING CHARACTERISTICS			
Droop Rate	10μV/ms max	*	50μV/ms (250μV/ms max)
Feedthrough (20V p-p @ 1kHz in)	2mV p-p		1mV p-p
INPUT CHARACTERISTICS			
Resistance (Sample Mode) min	100MΩ	*	4 x 10^9Ω
Bias Current (Sample Mode)	200nA	*	25nA
Offset, Initial (Adj to 0)	±1.0mV	*	±1mV (±2mV max)
Offset vs Temp, max	±10μV/°C	*	±20μV/°C
Offset vs Supply, max	±0.015mV/%ΔV	*	±10μV/%ΔV
Input Voltage Range min	±10V	*	±10V
OUTPUT CHARACTERISTICS			
Output Voltage	±10V @ 10mA	*	*
Capacitance Load	1000pF	*	*
DIGITAL CONTROL LOGIC LEVELS (DTL/TTL Compatible)			
("1") Sample	+2 to +5.5V @ 15nA	*	*
("0") Hold	-0.5 to +0.8V @ 100μA	*	*
POWER REQUIREMENTS			
Supply Voltage	±15V ±2%	*	*
Quiescent Current	±15mA	±18mA	+30, -25mA
TEMPERATURE RANGE			
Operating	0 to +70°C	*	*
Storage	-55°C to +85°C	*	*
DIMENSIONS	1" x 2" x 0.4"	*	*
	(28.5mm x 50.8mm x 10mm)	*	*

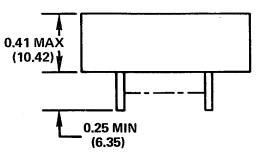
*Specifications same as SHA-3.

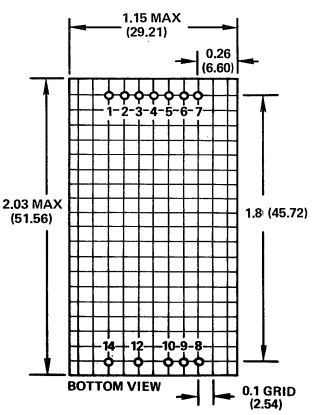
Specifications subject to change without notice.

NOTE: Switching the SHA-5 from SAMPLE to HOLD causes a 6mA decrease in the +15V supply current. This rapid change in current can induce voltage transients in certain types of power supplies which will couple directly onto the output terminal. To minimize this effect, a capacitor, such as a 100μF tantalum, should be connected between pins 1 and 3.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



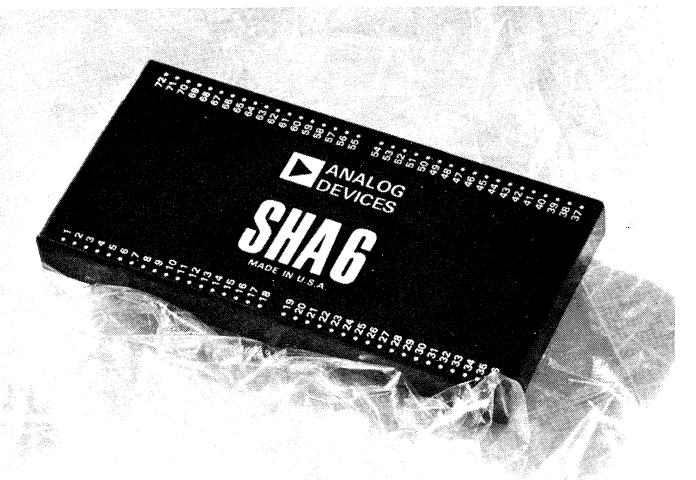


NOTES:
1. Pins: 0.019 ±0.001 (0.48mm ±0.02mm) dia. half-hard brass, gold plated per MIL-G-45204B, Class I, Type II.
2. Grid and markings next to pins are for reference only, and do not appear on unit.
3. Mating socket AC4102 or pin sockets P/N 2-330808-8 (7 required).

High Resolution Sample-and-Hold

SHA-6

FEATURES
Gain Range: 1 to 1000
Gain Stability: 2ppm/month (Gain = 1)
Linear Range: ±11V
CMR: 80dB min at any gain
Settling Time: 1ms to 0.00075%
(Gain = 100)
Offset Stability: ½ppm/°C
Aperture Uncertainty: ~10ns
Droop Rate in Hold: 10mV/sec max



GENERAL DESCRIPTION

The SHA-6 is a high accuracy wide dynamic range sample-and-hold module designed as a companion to the high resolution ADC-16Q A/D converter. It is designed to acquire an input signal to 16 bit accuracy, and to hold that signal fixed during the time that the following A/D is converting. Although sample and holds are most frequently used with unity gain, the gain of the SHA-6 is easily adjustable over the range 1 to 1000, by changing a single resistor in accordance with the specified gain formula. Since very high resolution A/D converters are likely to have moderate conversion speeds (because of the longer time needed by various amplifiers in the system to settle to 0.00075%), the SHA-6 has droop rate in "hold" of less than 10mV/sec.

PERFORMANCE CHARACTERISTICS

The SHA-6 was designed for use with A/D converters with resolution of up to 16 bits, consequently all operating parameters are defined in terms of high accuracy and stability, including effects of the instrumentation input buffer. Gain stability is 2ppm/°C and 2ppm/month. Offset stability (RTO) is ½ppm/°C and 2ppm/month. Settling time at unity gain is 5ms to 7.5ppm. Settling time decreases to 1ms to 7.5ppm for gain of 100. Recovery time from a 10 times overload is 150μs.

Signal processing characteristics unique to a sample and hold circuit were optimized to be truly appropriate for usage with 16 bit converters. Sample to hold offset is less than 75μV, while the switching transient is only 5mV (100kHzBW) and has decayed to 7.5ppm within 25μs. Aperture delay uncertainty is approximately 10ns, giving the SHA-6 the ability to acquire a signal slewing at 10V/ms to an uncertainty of 100μV, or two thirds of an LSB for the ADC-16Q.

HIGH PERFORMANCE INPUT BUFFER

It is next to impossible to supply any signal to a signal processing module completely free of common mode noise, and since 16 bit converter LSBs are only 152μV, it takes very little common mode noise to affect the accuracy of a reading. For this reason, the SHA-6 (as well as the ADC-16Q) has been provided with a true differential instrumentation amplifier as its input buffer. This buffer will allow the user to take full advantage of the high resolution and wide dynamic range capabilities of these fine system components.

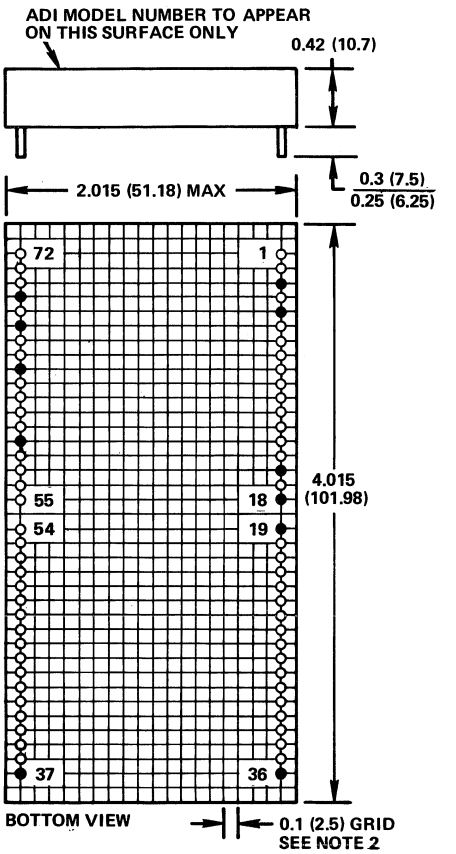
SPECIFICATIONS (typical @ +25°C and ±15V, unless otherwise noted)

GAIN AND STABILITY	
Gain Range (set by single resistor R_G)	1 to 1000
Gain Resistor Formula	$G = 1 + \frac{2x10^4}{R_G}$
Gain Error from Formula Value	0.2% max
Stability vs Time	±0.0002%/month
Stability vs Temp.	±0.0002%/°C
INPUT CHARACTERISTICS	
Impedance (Differential and Common Mode)	10^9 ohm (min) & 5pF (max)
Bias Current	80nA max
vs Temp.	250pA/°C max
Difference Current	40nA max
vs Temp.	100pA/°C max
Max Linear Differential and Common Mode	±11V
Max Safe Differential and Common Mode	$\pm V_S$
Common Mode Rejection (DC to 60Hz)	80dB min at any gain
DYNAMIC CHARACTERISTICS	
Unity Gain Small Signal BW	20kHz min
Full Power BW	2kHz min
Slew Rate	50V/ms
Settling Time to 0.00075%	
Gain = 1	5ms max
Gain = 10	3ms max
Gain = 100	1ms max
Recovery Time for x10 Overload	150μs max
SAMPLE-TO-HOLD SWITCHING	
Aperture Delay	-1.7μs
Aperture Uncertainty	10ns
Switching Transient Settling (to 75μV)	10μs max
Sample to Hold Offset	75μV max
HOLDING CHARACTERISTICS	
Feedthrough (DC to 10kHz)	-100dB min
Droop Rate	10mV/sec max
OUTPUT CHARACTERISTICS	
Output Voltage	±11V min @ 3mA min
Capacitive Load	1000pF min
Noise RTO (0.01Hz to 100kHz, 99.9% peak to peak, at any gain)	50μV max
Initial Offset	(1+G)mV max
Offset vs Temperature	5 (1+G)μV/°C max
Offset vs Supply	10 (1+G)μV/% max
Offset vs Time	20 (1+G)μV/mo max
DIGITAL CONTROL	
Logic Levels (TTL/DTL Compatible)	
Sample	0V to 0.8V @ 100μA max
Hold	+2.0V to +5.5V @ 10μA max
POWER SUPPLY	
Voltage, Rated Performance	±15V
Voltage, Operating	±(13-17)V
Current, Quiescent	±17mA max
TEMPERATURE	
Operating	0 to +70°C
Storage	-25°C to +100°C
MATING MOUNTING BOARD	AC1508

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES:
1. PINS: 0.040 ±0.001 (10.16 ±0.03) DIA BRASS, GOLD PLATED PER MIL-G-45204B CLASS I, TYPE II
2. GRID AND MARKINGS NEXT TO PINS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON UNIT
3. MOUNTING CARD: UNIT MATES WITH AC1508 (NOT SUPPLIED WITH UNIT)

CONNECTING THE SHA-6

The SHA-6 is easily interconnected for operation with the ADC-16Q or other high resolution converters, as shown in the diagram of Figure 1. The input divider (R_1, and R_2) will be required only if total differential input signal exceeds ±10 Volts. If the divider is used, it is extremely important to have resistors R_1 precisely equal, in order to avoid unbalance of the input system and degradation of the common mode performance.

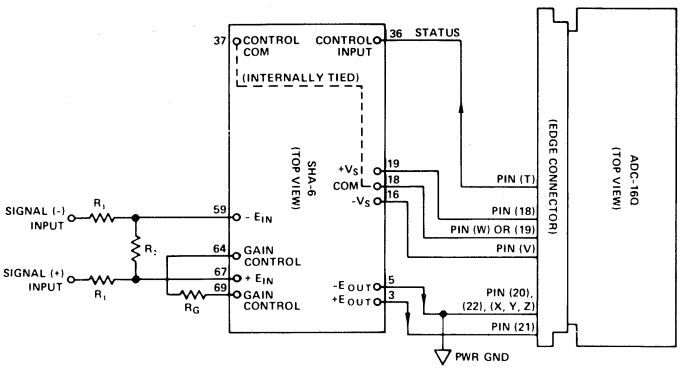


Figure 1. Interconnection of SHA-6 to an ADC-16Q

Because of its extreme stability, the SHA-6 is not provided with terminals for the adjustment of output offset. This adjustment can be made easily by a compensating adjustment of the offset in the following A/D converter, so long as the SHA-6 is operated at low gain, as is usually the case. If the SHA-6 is to be operated at high gain, the initial offset may be too great to allow compensation with the offset adjustment of the following converter. If that should be the case, we recommend the circuit of Figure 2 provide the needed adjustment. The SHA-6 linearity is not disturbed by the common mode signal appearing at its output, since the circuit has high CMR at both the input and the output.

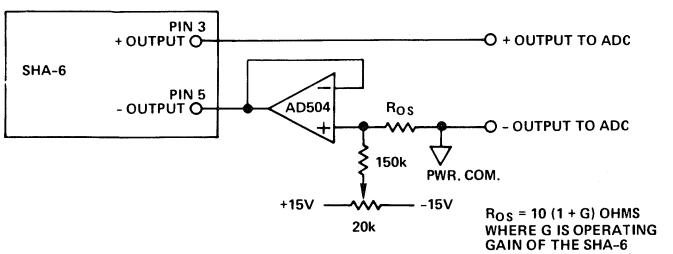


Figure 2. Offset Adjustment Circuit for High Gain Operation

ACCURACY AND INSTALLATION CONSIDERATIONS

The extremely high resolution and linearity of the SHA-6 demanded a systems approach to the design. Problems like common mode noise pickup in just a few feet of wire, or the thermocouple effect of connections of dissimilar materials, cannot be neglected in a 16-bit design. For these and other reasons, users of the SHA-6 should take exceptional care in planning installations, in order to minimize the effects of environmental conditions on system accuracy.

a. The unit and its connector and signal wiring should be located with an eye to optimum isolation from sources of RFI and EMI.
b. Special care must be observed in running input signal wiring to the buffer inputs, in order to avoid degrading the common mode rejection at ac.

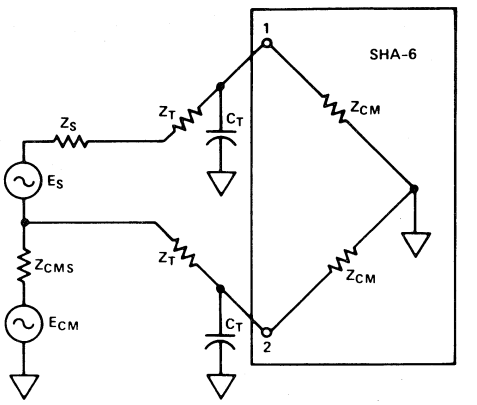
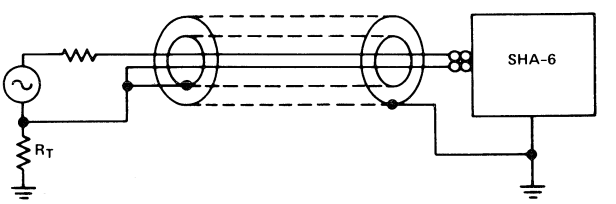


Figure 3. Simplified Equivalent Circuit-Differential Input System

Figure 3 shows a simplified equivalent circuit of the input system for common mode purposes, the points marked 1 and 2 being the input signal terminals, E_S and Z_S being the signal source and source resistance, and Z_T and C_T being the transmission line impedances. The circuit is a bridge, and if it is balanced there is no differential component of E_{CM} appearing across the input terminals.

It is clearly of great importance to maintain balance in Z_T and C_T when a signal source is wired to the converter input. Only a few pF of capacitance unbalance is enough to wipe out the common mode rejection at 60Hz.



Note: 2-wire double-shielded cable is Trompeter Electronics Inc. P/N QRC-78-2 or equivalent.

Figure 4. Shielding of Input Wiring

Figure 4 shows a recommended interconnection of a signal source to the SHA-6. Two-wire double-shielded cable should be used, with the inner shield connected to the "low" side of the signal, to act as a guard. Outer

shield is grounded, and a dc path from signal source to ground MUST be provided, if it is not inherent in the design. To optimize common mode rejection, the double-shielded cable should also be capacitance-balanced. (Such cables with a specification on maximum capacitance unbalance per unit length are available from several manufacturers.)

c. The unit, its connector and wiring should be located in a region of constant, stable temperature. Popular electronic wiring materials almost always involve use of more than one metal, and we must remember that junctions of two metals will act as thermocouples, and will generate error voltages proportional to temperature difference between junctions as well as to temperature gradients along wires. We cannot ignore these effects when the value of an LSB is 152μV!

There is still another dimension to the common-mode problem for high resolution products. Figure 5, the analog power distribution diagram, depicts the presence of a connector by showing its resistance. Typical edge connectors may have resistance of the order of 15 milliohms when mated. Note that the effect of 20mA of common circuit current flow would be the generation of 300μV across the connector! This 300μV appears as a common mode voltage between the SHA-6 *internal* power ground and its signal input terminals. It is therefore clear that, without a high common mode rejection input buffer, neither the SHA-6 nor the ADC-16Q would be able to operate to full linearity – the voltage drop in the connector causes 2LSB's of common mode!

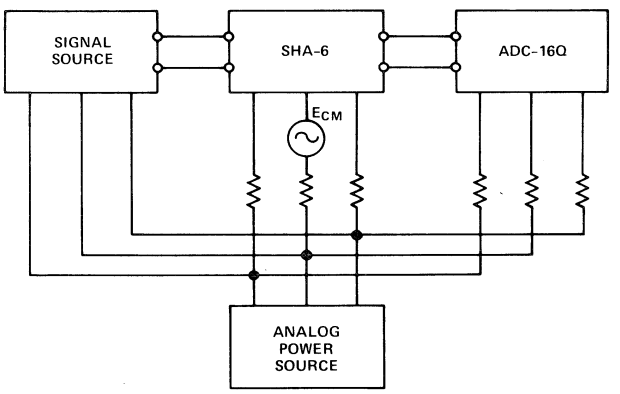


Figure 5. Analog Power Distribution Diagram for a High Resolution Converter Subsystem

With the high common mode rejection input buffers that are standard for both the SHA-6 and the ADC-16Q, not only are connector resistance problems avoided, but the user acquires practically complete flexibility in grounding the subsystem. In tests at our plant, we found no noticeable variation in subsystem performance as several possible grounding schemes were investigated.

THE AC1508 MOUNTING CARD

For the convenience of the SHA-6 user, the AC1508 mounting card is available. The 1508 is a simple edge-connector card with pin receptacles for plugging in the SHA-6. In addition, the AC1508 has provisions for connecting the gain control resistor and the offset adjustment components described in Figure 2. A mating receptacle for the edge connector is included in the price.

APERTURE DELAY DISCUSSION

In the SHA-6, the usual input buffer of the sample and hold is preceded by a high common mode instrumentation buffer. The signal phase delay through this buffer compensates for the aperture delay of the basic SHA circuit, resulting in a total aperture delay for the SHA-6 of –1.7μs. That is, the signal stored in the "hold" mode is that value that appeared at the input terminals 1.7μs *before* the hold command was applied.

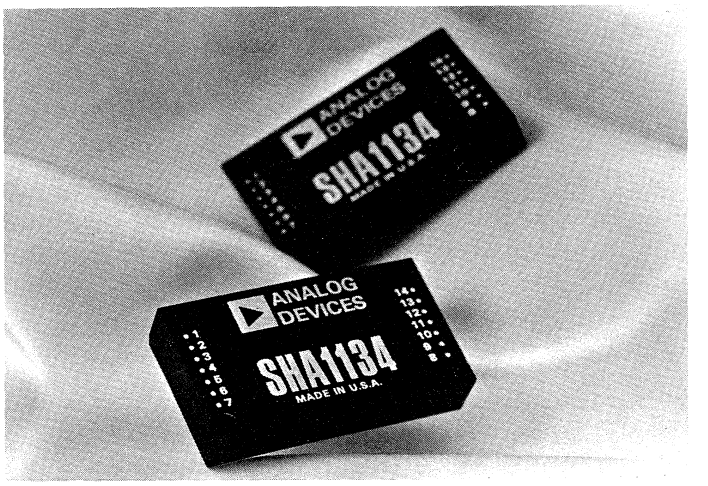
HOLD CAPACITOR STORAGE EFFECTS

All known capacitors have storage effects, and cannot be totally discharged instantaneously. The capacitor used in the SHA-6 was especially selected for optimum dielectric polarization effect for this application. When used to condition the input signal for an ADC-16Q, the effect of this polarization will usually be less than one third of an LSB change in the held value during the conversion time plus settling time of the ADC-16Q.

General Purpose Sample-and-Hold Amplifier

SHA1134

FEATURES
3.4μs Acquisition Time
Short 35ns Aperture Delay
±0.005% Maximum Linearity Error
High Input Impedance: $>10^7\Omega$
DTL/TTL Compatible
Compact Module: 1 1/8" x 2" x 0.4" (29 x 51 x 10mm)



GENERAL DESCRIPTION

The SHA1134 is a moderately fast, general purpose sample-and-hold amplifier which has been optimized for use in data acquisition applications with 12-bit analog-to-digital converters. When in the "sample" mode, the module appears as a fast amplifier with a 3.2μs settling time to ±0.01% accuracy. When switched to the "hold" mode, the output is held at a level corresponding to the input signal voltage at the instant of switching. The operating mode of the SHA1134 is controlled by a TTL/DTL compatible logic input.

The SHA1134 features an aperture delay time of 35ns and an aperture delay time uncertainty, or "jitter", of 2ns. The droop rate of 50mV/s makes it suitable for operation with virtually all successive approximation A/D converters. Package size for this compact module is 1.12" x 2" x 0.4" (29 x 51 x 10mm). It needs no adjustments and requires only ±15V external power for operation.

PRINCIPLE OF OPERATION

The SHA1134 consists basically of two high speed operational amplifiers, a storage capacitor, and a digitally controlled switch connected in a feedback loop as shown below.

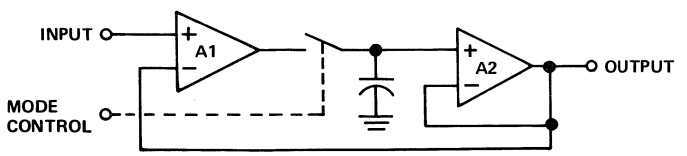


Figure 1. SHA1134 Basic Configuration

When the mode control inputs is shifted to Logic "1", the switch closes, causing the capacitor voltage and output voltage to match the input voltage. In addition to providing input buffering, amplifier A1 supplies the current needed to quickly charge the storage capacitor in this mode of operation. The high gain feedback loop contributes to high tracking accuracy.

When the mode control is shifted back to Logic "0", the switch opens and the output remains fixed at a voltage equal to the voltage "stored" across the capacitor. The low input current of amplifier A2 and the low "off" leakage current of the field-effect-transistor switch minimize the leakage of the capacitor's charge and, thus, the "droop" in the output voltage. Amplifier A2 provides the SHA1134 with low output impedance and good current drive capability.

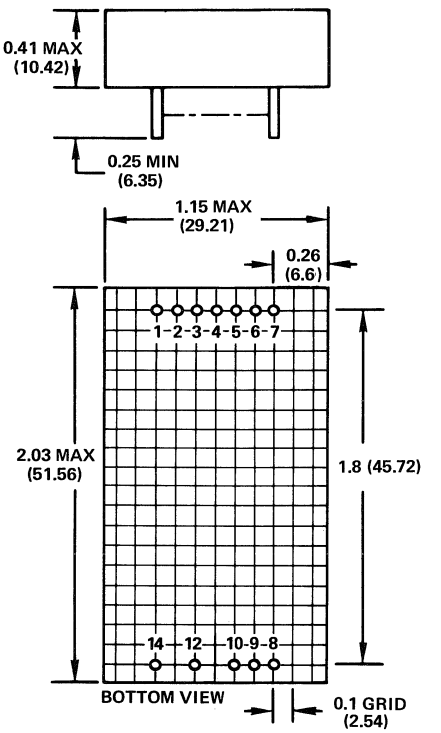
SPECIFICATIONS (typical @ +25°C and ±15V, unless otherwise noted)

MODEL	SHA1134
ACCURACY	
Gain	+1
Gain Error	±0.036% (0.04% max)
Gain Temperature Coefficient	6.5ppm/°C (10ppm/°C max)
Gain Nonlinearity	±0.001% (±0.005% max)
STATIC INPUT CHARACTERISTICS	
Voltage Range for Rated Accuracy	±10V max
Impedance	$>10^7\Omega$
Bias Current	0.5μA max
Input Offset Voltage	0.5mV (1.5mV max)
Temperature Coefficient	135μV/°C (200μV/°C max)
Supply Coefficient	$20\mu V/\%\Delta V_S$ ($30\mu V/\%\Delta V_S$)
OUTPUT CHARACTERISTICS	
Voltage	±10V
Current	±5mA max
Resistance	0.05Ω
Capacitive Load	100pF max
Noise @ 100kHz Bandwidth	0.3mV (0.5mV max)
@ 1MHz Bandwidth	1.8mV (2.2mV max)
SAMPLE MODE DYNAMICS	
Frequency Response	
Small Signal (-3dB)	800kHz
Full Power	600kHz
Slew Rate	15V/μs
Settling Time to ±0.01% (20V Step)	3.2μs (4.0μs max)
Overload Recovery (50% Overload)	0.6μs (1μs max)
SAMPLE-TO-HOLD SWITCHING	
Aperture Delay Time	35ns (50ns max)
Aperture Uncertainty	2ns (5ns max)
Offset Step	3.3mV (5.5mV max)
Offset Linearity	±3mV
Switching Transient	
Amplitude	±70mV
Settling Time to ±0.01%	1μs
HOLD MODE DYNAMICS	
Droop Rate	±50mV/s (±200mV/s max)
Variation with Temperature	Doubles Every 10°C
Feedthrough (for ±10V Input @ 1kHz)	1.0mV (2.0mV max)
HOLD-TO-SAMPLE SWITCHING	
Acquisition Time to ±0.01%	3.4μs (4.1μs max)
DIGITAL INPUT	
Sample Mode (Logic "1")	+2V ≤ LOGIC "1" ≤ +5.5V @ 15nA max
Hold Mode (Logic "0")	0V ≤ LOGIC "0" ≤ +0.8V @ 5μA (20μA max)
POWER REQUIRED	+15V ±3% @ +20mA -15V ±3% @ -17mA
TEMPERATURE RANGE	
Operating	0 to +70°C
Storage	-55 to +85°C

Specifications subject to change without notice.

OUTLINE DIMENSIONS and PIN CONNECTIONS

Dimensions shown in inches and (mm).



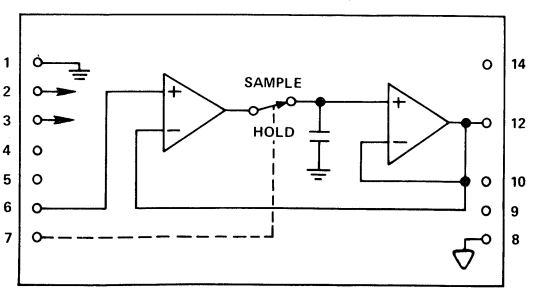
NOTES:

1. Pins: 0.019 ±0.001 (0.48mm ±0.02mm) dia. half-hard brass, gold plated per MIL-G-45204B, Class I, Type II.
2. Mating socket AC4102 or pin sockets P/N 2-330808-8 (7 required).

PIN DESIGNATIONS

1. ANALOG GROUND	8. LOGIC GROUND
2. -15V	9. N.C.
3. +15V	10. N.C.
4. N.C.	11. NO PIN
5. N.C.	12. ANALOG OUTPUT
6. SIGNAL IN	13. NO PIN
7. CONTROL IN	14. N.C.

BLOCK DIAGRAM



DATA ACQUISITION APPLICATION

Successive-approximation A/D converters can generate substantial linearity errors if the analog input varies during the period of conversion; even the fastest 12-bit models available cannot tolerate input signal frequencies of greater than 10Hz. For this reason, sample-and-hold amplifiers like the SHA1134 are often connected between the A/D and its signal source to hold the analog input constant during conversion.

When the SHA1134 is connected to an A/D, its aperture time uncertainty, rather than the A/D's conversion time, is the factor which limits the allowable input signal slew rate. The SHA1134, with a typical aperture delay time of 35ns and an uncertainty of 2ns, will change from the sample mode to the hold mode 33 to 35ns after the "1" to "0" transition of the mode control input. If the system timing is so arranged as to initiate the mode control signal 33ns early, then switching will actually occur within 2ns of the desired time as shown below.

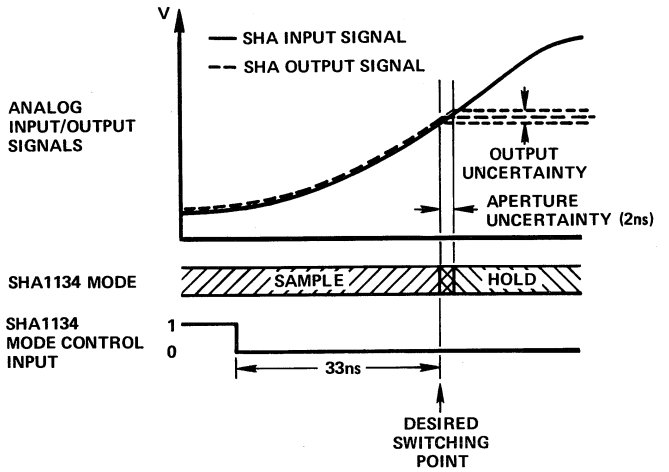


Figure 2. Aperture Uncertainty

The maximum allowable slew rate will thus equal the quotient of the maximum allowable voltage uncertainty and the 2ns aperture uncertainty. For sinewave inputs, the corresponding maximum frequency is expressed by:

$$f_{max} = \left(\frac{\Delta E}{E_{FS}}\right)\left(\frac{1}{2\pi\Delta t}\right) \cong 8 \times 10^7 \left(\frac{\Delta E}{E_{FS}}\right)$$

where: ΔE = the allowable voltage uncertainty

E_{FS} = the sinewave magnitude

For a system containing a SHA1134 and a 12-bit A/D with ±10V input signals and an allowable input uncertainty of ±½LSB (±2.44mV), the maximum allowable slew rate will be ±1.22V/μs. This corresponds to the maximum rate of change of a 19.5kHz sinewave signal.

OPERATION WITH AN A/D CONVERTER

Figure 3 below shows the appropriate connections between the SHA1134 and a successive approximation A/D converter in block diagram form.

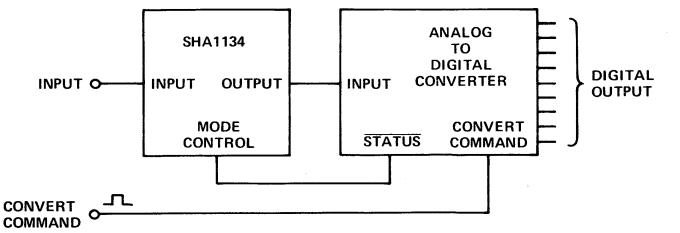


Figure 3. SHA1134 and A/D Connections

The resulting timing sequence at the start of conversion is illustrated in Figure 4.

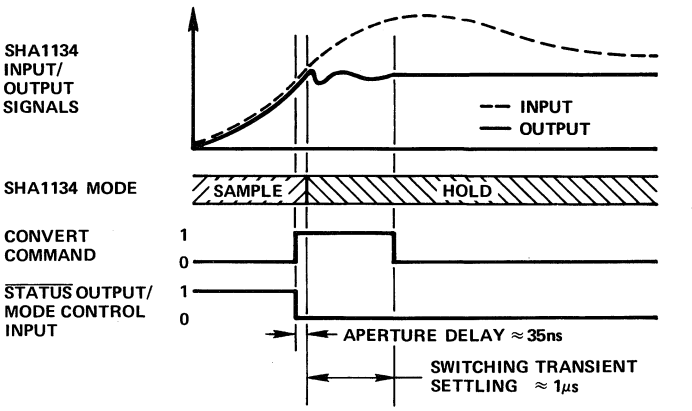


Figure 4. A/D and SHA Timing at Start of Conversion

Note that the leading edge of the convert command pulse causes the converter's $\overline{\text{STATUS}}$ output to go to Logic "0" which in turn switches the SHA1134 from sample to hold. As discussed previously, the typical SHA1134 actually changes modes 33 to 35ns after the "1" to "0" transition of the mode control input. This mode switching causes a transient on the output terminal which decays to within 0.01% of the final value in approximately 1μs. Once the transient has settled, the convert command input is returned to Logic "0" and the conversion proceeds. As shown in Figure 5, the $\overline{\text{STATUS}}$ signal returns to Logic "1" and the SHA1134 returns to the sample mode at the end of conversion. Within 3.4μs, it will have acquired the input signal to 0.01% accuracy and a new conversion cycle may be started.

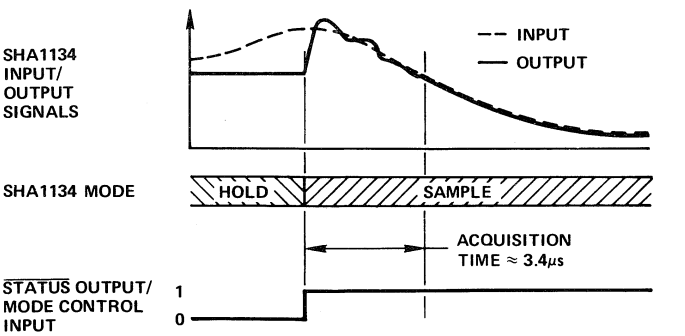


Figure 5. A/D and SHA Timing at End of Conversion

OPERATION WITH AN A/D AND MULTIPLEXER

The subsystem of Figure 3 may also be connected to a multiplexer like Analog Devices' model MPX-8A as shown below:

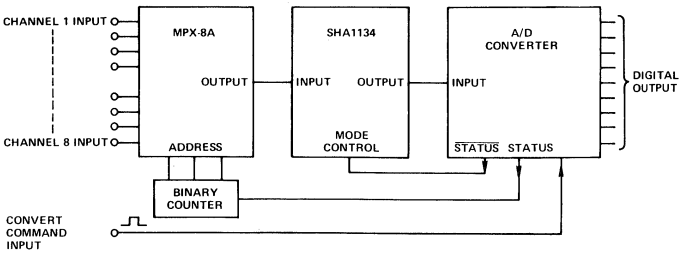


Figure 6. A/D, SHA, and MPX Connections

The leading edge of the convert command pulse sets the $\overline{\text{STATUS}}$ output to Logic "0" thereby switching the SHA1134 to "hold"; the corresponding change to Logic "1" of the STATUS output increments the binary counter and changes the multiplexer address. Since the SHA1134's aperture time is small with respect to the multiplexer switching time, it will have switched to the hold mode before the MPX-8A actually changes channels. The multiplexer switching transients will settle out long before the SHA returns to "sample" at the end of conversion. The timing sequence described above is illustrated in Figure 7.

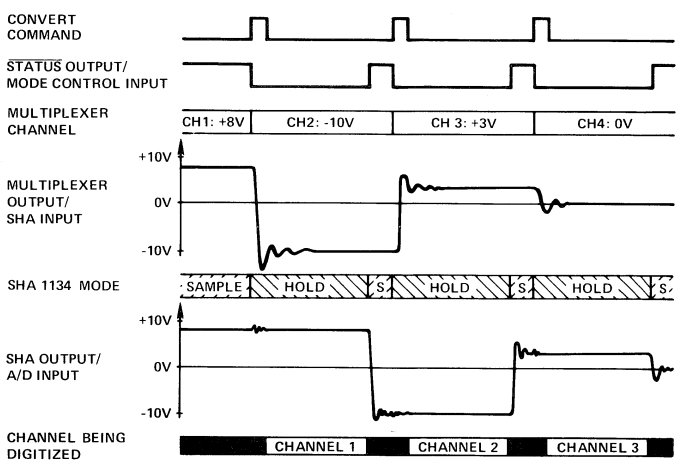


Figure 7. A/D, SHA, and MPX Timing

This method of sequencing the multiplexer may be altered to permit random addressing or addressing in a preset pattern. The timing of multiplexer address changes may also be altered but consideration should be given to the effects of feedthrough in the SHA1134. Feedthrough is the coupling of analog input signals to the output terminal while the SHA is in "hold". For the SHA1134, a 20V p-p input signal will typically produce a 1mV signal at the output. If large multiplexer switching transients occur while the A/D conversion is in progress, errors can be introduced.

THROUGHPUT RATE

The rate at which the systems of Figures 3 and 6 can perform conversions will, of course, depend on the conversion time of the A/D converter used. The table below lists the minimum system throughput rates achievable with several of Analog Devices' 12-bit successive approximation A/D converters.

A/D CONVERTER	MINIMUM SYSTEM THROUGHPUT RATE
ADC12QZ	22.1kHz
ADC12QM	33.1kHz
ADC1133	33.1kHz
ADC12QU	49.6kHz
ADC1102	74.0kHz
ADC1103-003	115.6kHz

POWER SUPPLY AND GROUNDING CONNECTIONS

The proper power supply and grounding connections are shown below in Figure 8.

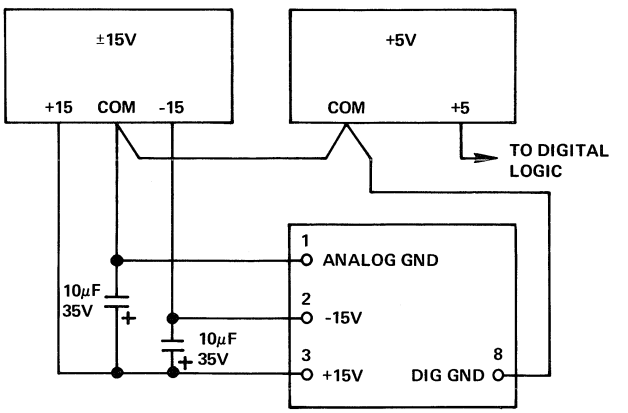


Figure 8. Power Supply and Grounding Connections

The ±15V power supplies must be externally bypassed as shown. The capacitors should be tantalum types and should be installed as close to the module pins as possible. The analog and digital ground lines should be run separately to their respective power supply commons to prevent coupling of digital switching noise to the sensitive analog circuit section.

Switches and Multiplexers

Orientation
Switches and Multiplexers

Analog Devices offers a complete line of monolithic CMOS analog multiplexers and switches, which utilize a high-breakdown CMOS process, in conjunction with a double-layer interconnect for high density. Both 8- and 16-channel multiplexers are available, in one-line and two-line (4- and 8-channel differential) versions. The switches are duals and quads, available in a variety of contact forms. Both direct and inverted logic options are available for the most-popular types. The popular AD7510/11/12DI (quad SPST/dual SPDT) utilize dielectric isolation, are latchup-proof, and can withstand overrange to ±25V beyond the supplies.

CMOS switches have extremely low quiescent power dissipation, require little drive or supply current while switching, and are low in cost. Their R_{ON} is low and is, to a first-order, independent of applied voltage; in the off condition, leakage is quite small, both across the gate and to the drive and supply circuits. Most types respond to TTL/DTL, as well as CMOS, logic.

Definitions for terminal nomenclature used in the data sheets are given below, and a summary of device functions appears on the following page. General information on the nature of CMOS, its advantages, its applications, and its protection, is to be found in the *Guide to CMOS Switches and Multiplexers*, available from Analog Devices upon request.

MULTIPLEXER TERMINOLOGY

R_{ON}:	Ohmic resistance between the output and an addressed input.
R_{ON} vs. Temperature:	R_{ON} drift over the temperature range.
ΔR_{ON} between Switches:	Difference between the R_{ON}'s of any two switches.
R_{ON} vs. Temperature between Switches:	Difference between the R_{ON} drifts of any two switches.
I_S:	Current at any switch input, S1 through SN. This is a leakage current when the switch is open.
I_{OUT}:	Current at the output. This is a leakage current when all switches are open.
$I_{OUT} - I_S$:	Difference between the current going into terminal "S" and the current going out of terminal "out" when terminal "S" is addressed.
V_{INL}:	Digital threshold voltage for the low state.
V_{INH}:	Digital threshold voltage for the high state.
C_S:	Capacitance between any open terminal "S" and ground.
C_{OUT}:	Capacitance between the output terminal and ground with all switches open.
C_{S-OUT}:	Capacitance between any open terminal "S" and the output terminal.
C_{SS}:	Capacitance between any two "S" terminals.
$t_{transition}$:	Delay time when switching from one address state to another.
t_{open}:	"OFF" time of both switches when switching from one address state to another.
t_{on} (En):	Delay time between the 50% points of the enable input and the switch "ON" condition.
t_{off} (En):	Delay time between the 50% points of the enable input and the switch "OFF" condition.
V_{DD}:	Most positive voltage supply.
V_{SS}:	Most negative voltage supply.
I_{DD}:	Positive supply current.
I_{SS}:	Negative supply current.

SWITCH TERMINOLOGY

R_{DS}:	Ohmic resistance between terminals D and S.
I_D (I_S):	Current at terminals D or S. This is a leakage current when the switch is OFF.
I_{DS}:	Current flowing through the closed switch.
$I_D - I_S$:	Leakage current that flows from the closed switch into the body. (This leakage will show up as the difference between the current I_D going into the switch and the outgoing current I_S.)
V_D (V_S):	Analog voltage on terminal D (S).
C_S (C_D):	Capacitance between terminal S (D) and ground. (This capacitance is specified for the switch open and closed.)
C_{DS}:	Capacitance between terminals D and S. (This will determine the switch isolation over frequency.)
C_{DD} (C_{SS}):	Capacitance between terminals D (S) of any 2 switches. (This will determine the cross coupling between switches vs. frequency.)
t_{ON}:	Delay time between the 50% points of the digital input and switch "ON" condition.
t_{OFF}:	Delay time between the 50% points of the digital input and switch "OFF" condition.
V_{INL}:	Threshold voltage for the low state.
V_{INH}:	Threshold voltage for the high state.
I_{INL} (I_{INH}):	Input current of the digital input.
C_{IN}:	Input capacitance to ground of the digital input.
V_{DD}:	Most positive voltage supply.
V_{SS}:	Most negative voltage supply.
I_{DD}:	Positive supply current.
I_{SS}:	Negative supply current.

Selection Guide
Switches and Multiplexers

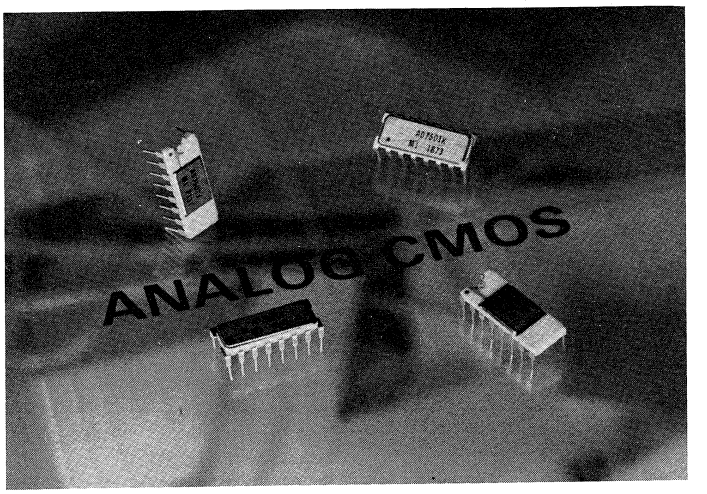
Description	Model	Diagram	See Page
CMOS IC Switches	AD7510DI	Dielectrically isolated QUAD SPST; Address high closes switch	545
	AD7511DI	Dielectrically isolated QUAD SPST; Address low closes switch	545
	AD7512DI	Dielectrically isolated QUAD SPDT	545
	AD7513	Dual SPST	553
	AD7516	Quad SPST replaces CD4016A/4066A	557
	AD7519	Quad SPDT current-steering switch	559
CMOS IC Multiplexers	AD7501	8-channel multiplexer, High enables	537
	AD7503	8-channel multiplexer, Low enables	537
	AD7502	4-channel differential multiplexer	537
	AD7506	16-channel multiplexer	541
	AD7507	8-channel differential multiplexer	541
Modular Multiplexer	MPX-8A	8-channel, expandable to 64	561

ANALOG DEVICES

CMOS 4/8 Channel Analog Multiplexers

AD7501, AD7502, AD7503

FEATURES
DTL/TTL/CMOS Direct Interface
Power Dissipation: 30μW
R_{ON}: 170Ω
Output "Enable" Control
AD7503 Replaces HI-1818



GENERAL DESCRIPTION

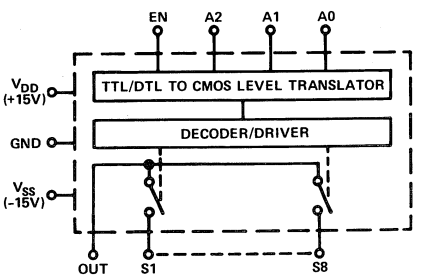
The AD7501 and AD7503 are monolithic CMOS, 8 channel analog multiplexers which switches one of 8 inputs to a common output depending on the state of three binary address lines and an "enable" input. The AD7503 is identical to the AD7501 except its "enable" logic is inverted. All digital inputs are TTL/DTL and CMOS logic compatible.

The AD7502 is a monolithic CMOS dual 4-channel analog multiplexer. Depending on the state of 2 binary address inputs and an "enable", it switches two output busses to two of 8 inputs.

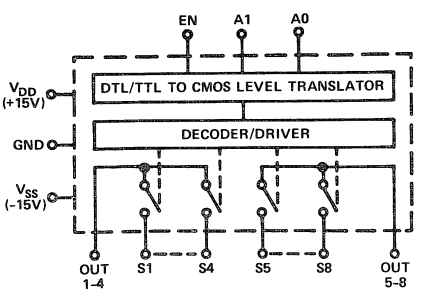
The AD7502 is an excellent example of a high breakdown CMOS process combined with a double layer interconnect for high density. Silicon nitride passivation ensures long term stability and reliability.

FUNCTIONAL DIAGRAMS

AD7501, AD7503



AD7502



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

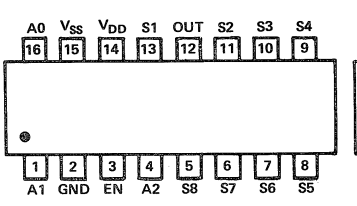
V_{DD} – GND . . . . . +17V
V_{SS} – GND . . . . . -17V
V Between Any Switch Terminals. 25V
Switch Current (I_S, Continuous) 35mA
Switch Current (I_S, Surge)
1ms duration, 10% duty cycle 50mA
Digital Input Voltage Range . . . . . V_{DD} to GND
Power Dissipation (package)
16 pin Ceramic DIP
Up to +75°C. 450mW
Derates above +75°C by . . . . . 6mW/°C
16 pin Plastic DIP
Up to +70°C. 670mW
Derates above +70°C by . . . . . 8.3mW/°C
Operating Temperature
Plastic. . . . . 0 to +75°C
Ceramic (J, K versions). . . . . -25°C to +85°C
Ceramic (S version) . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION:

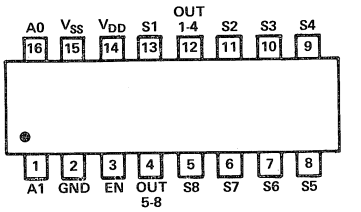
1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

PIN CONFIGURATIONS (Top View)

AD7501, AD7503



AD7502



SPECIFICATIONS (V_{DD} = +15V, V_{SS} = -15V unless otherwise noted)

PARAMETER	VERSION[1]	SWITCH CONDITION	@25°C AD7501, AD7503	@25°C AD7502	OVER SPECIFIED TEMP. RANGE AD7501, AD7503	OVER SPECIFIED TEMP. RANGE AD7502	TEST CONDITIONS
ANALOG SWITCH							
R_{ON}	All	ON	170Ω typ, 300Ω max	*			$-10V \leq V_S \leq +10V$
R_{ON} vs. V_S	All	ON	20% typ	*			I_S = 1.0mA
R_{ON} vs. Temperature	All	ON	0.5%/°C typ	*			V_S = 0V, I_S = 1.0mA
ΔR_{ON} Between Switches	All	ON	4% typ	*			
R_{ON} vs. Temperature Between Switches	All	ON	±0.01%/°C	*			
I_S	J, K	OFF	0.2nA typ, 2nA max	*	50nA max	*	V_S = -10V, V_{OUT} = +10V and
	S	OFF	0.5nA max	*	50nA max	*	V_S = +10V, V_{OUT} = -10V
I_{OUT}	J, K	OFF	1nA typ, 10nA max	0.6nA typ, 5nA max	250nA max	125nA max	V_S = -10V, V_{OUT} = +10V and
							V_S = +10V, V_{OUT}= -10V
	S	OFF	5nA max	3nA max	250nA max	125nA max	AD7501: Enable HIGH
							AD7502, 03: Enable LOW
$\lvert I_{OUT} - I_S \rvert$	J, K	ON	12nA max	7nA max	300nA max	175nA max	V_S = 0
	S	ON	5.5nA max	3.5nA max	300nA max	175nA max	
DIGITAL CONTROL							
V_{INL}	All				0.8V max	*	
V_{INH}	J				3.0V min	*	Note 2
	K, S				2.4V min	*	
I_{INL} or I_{INH}	All		10nA typ	*			
C_{IN}	All		3pF typ	*			
DYNAMIC CHARACTERISTICS[3]							
t_{ON}	All		0.8μs typ	*			V_{IN} = 0 to +5.0V
t_{OFF}	All		0.8μs typ	*			(See Test Circuit 2)
C_S	All	OFF	5pF typ	*			
C_{OUT}	All	OFF	30pF typ	15pF typ			
$C_{S\text{-}OUT}$	All	OFF	0.5pF typ	*			
C_{SS} Between Any Two Switches	All	OFF	0.5pF typ	*			
POWER SUPPLY							
I_{DD}	J, K		1μA typ, 100μA max	*			All Digital Inputs Low
I_{SS}	J, K		1μA typ, 100μA max	*			
I_{DD}	S		500μA max	*	500μA max	*	
I_{SS}	S		500μA max	*	500μA max	*	
I_{DD}	J, K		200μA typ, 500μA max	*			All Digital Inputs High
I_{SS}	J, K		1μA typ, 100μA max	*			
I_{DD}	S		800μA max	*	800μA max	*	
I_{SS}	S		800μA max	*	800μA max	*	

NOTES:
*Same specifications as AD7501 and AD7503.
[1] JN, KN versions specified for 0 to +75°C; JD, KD versions for -25°C to +85°C; and SD versions for -55°C to +125°C.
[2] A pullup resistor, typically 1-2kΩ is required to make the AD7501J, AD7502J and AD7503J compatible with TTL/DTL levels. The maximum value is determined by the output leakage current of the driver gate when in the high state.
[3] AC parameters are sample tested to ensure conformance to specifications.

Specifications subject to change without notice.

TRUTH TABLES

AD7501

A_2	A_1	A_0	E_N	"ON"
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8
X	X	X	0	None

AD7503

A_2	A_1	A_0	E_N	"ON"
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8
X	X	X	1	None

AD7502

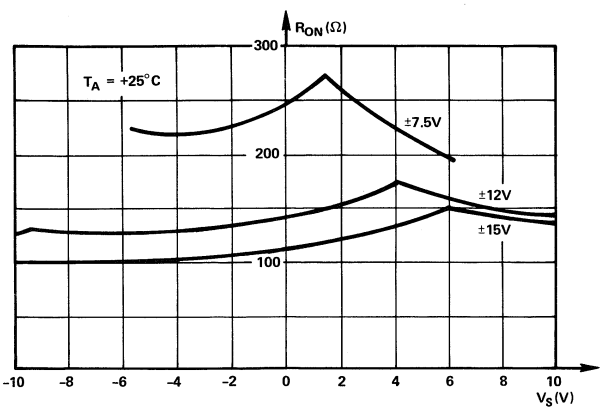
A_1	A_0	E_N	"ON"
0	0	1	1 & 5
0	1	1	2 & 6
1	0	1	3 & 7
1	1	1	4 & 8
X	X	0	None

ORDERING INFORMATION

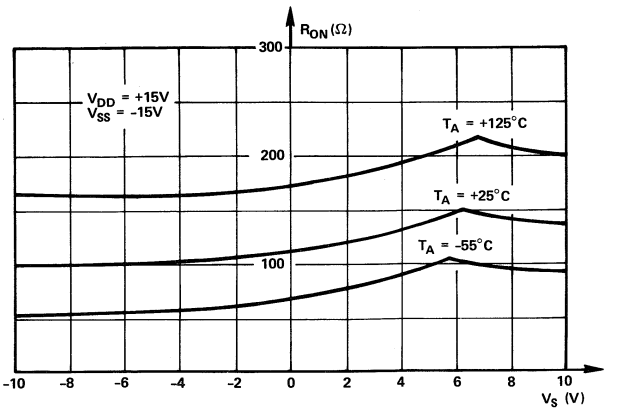
Plastic (Suffix N)	Ceramic (Suffix D)	Operating Temperature Range
AD7501JN AD7501KN AD7503JN AD7503KN		0 to +75°C
	AD7501JD AD7501KD AD7503JD AD7503KD	-25°C to +85°C
	AD7501SD AD7503SD	-55°C to +125°C
AD7502JN AD7502KN		0 to +75°C
	AD7502JD AD7502KD	-25°C to +85°C
	AD7502SD	-55°C to +125°C

Typical Performance Characteristics

1. R_{ON} As A Function Of Switch Voltage (V_S)

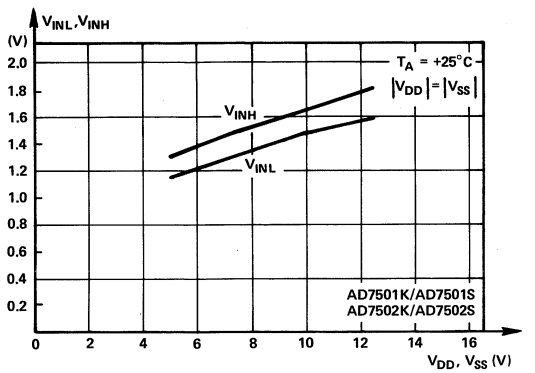


At Different Power Supplies

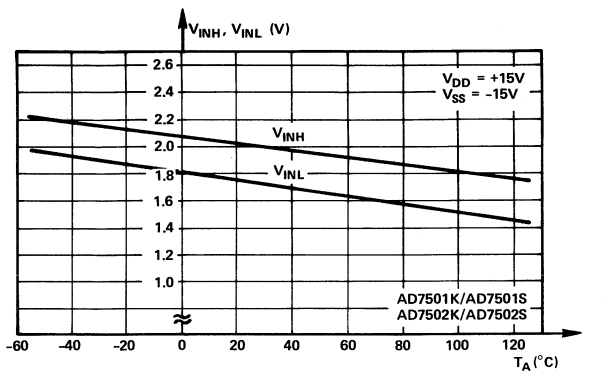


At Different Temperatures

2. Digital Threshold Voltage (V_{INH}, V_{INL})

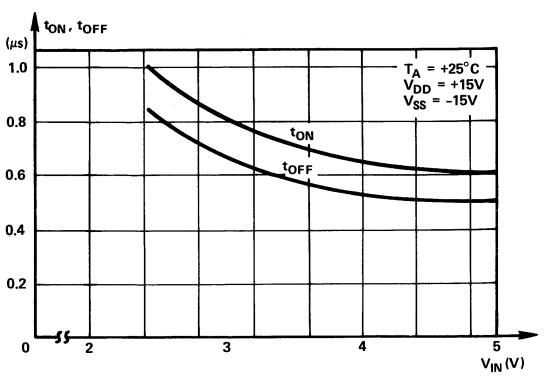


vs. Power Supply



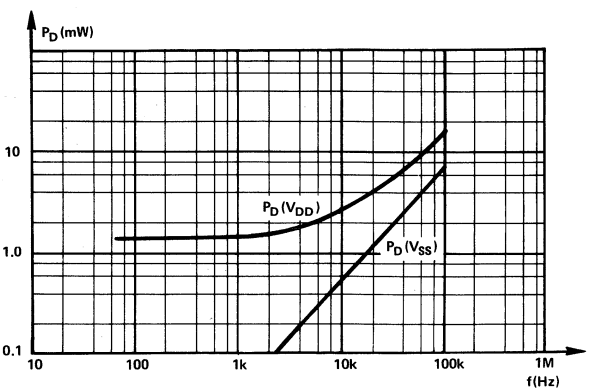
vs. Temperature

3. T_{ON}, T_{OFF}



vs. Digital Input Voltage

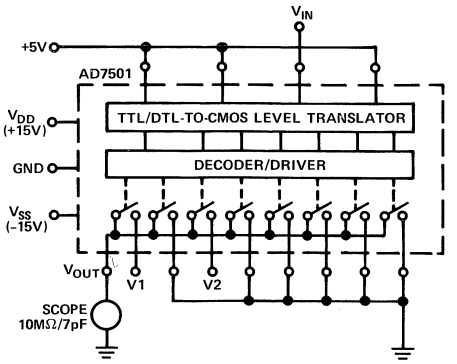
4. Power Dissipation

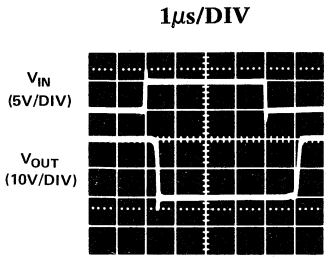


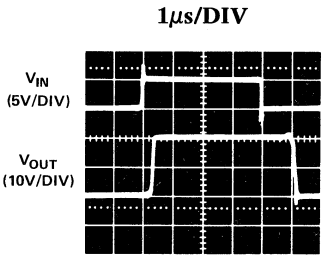
vs. Logic Frequency (50% Duty Cycle)

TYPICAL SWITCHING CHARACTERISTICS

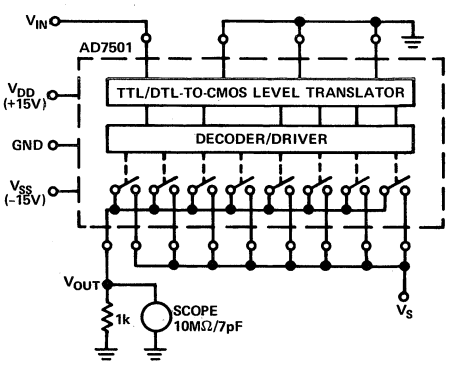
TEST CIRCUIT 1

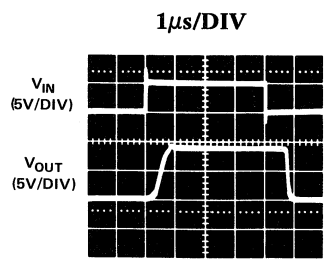


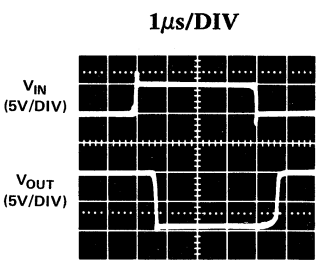


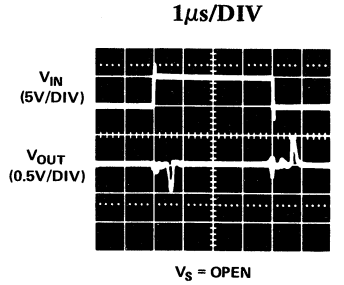


TEST CIRCUIT 2





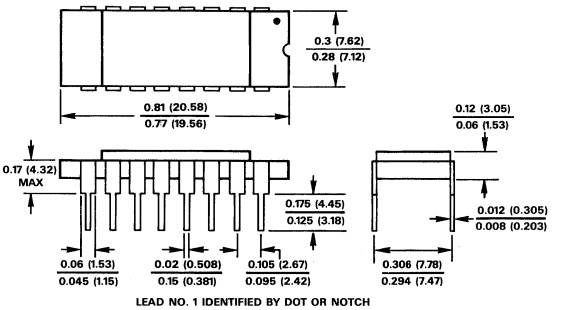




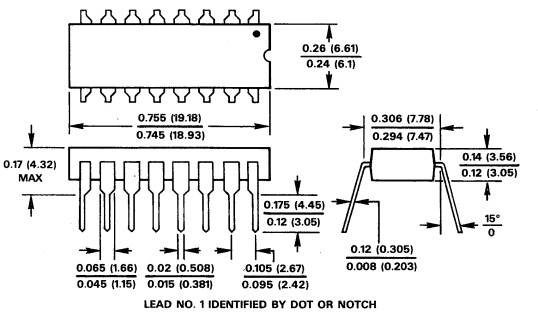
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-PIN CERAMIC DIP (SUFFIX D)

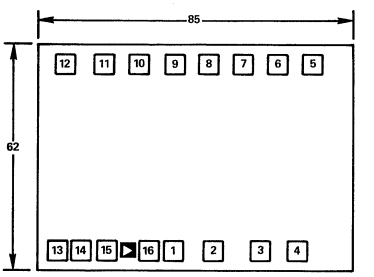


16-PIN PLASTIC DIP (SUFFIX N)

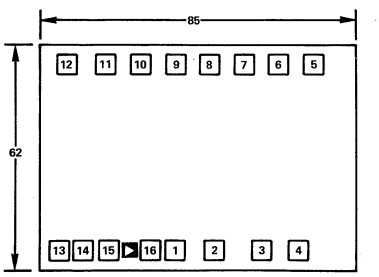


BONDING DIAGRAMS

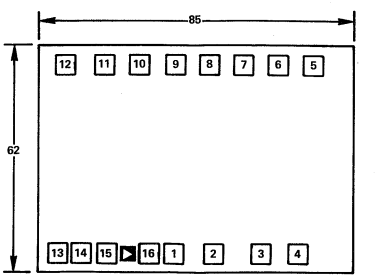
AD7501



AD7502



AD7503



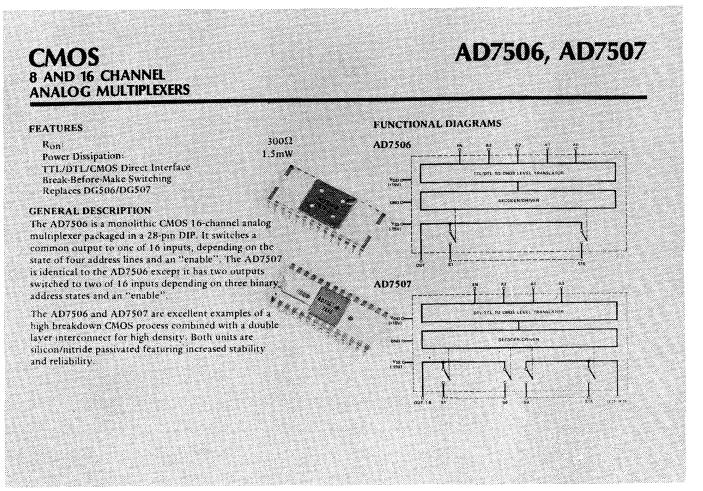
All bonding pads are 4 x 4 MIL.
All pad numbers correspond with DIP package pin configuration.

ANALOG DEVICES

CMOS 8 and 16 Channel Analog Multiplexers

AD7506, AD7507

FEATURES
R_{ON}: 300Ω
Power Dissipation: 1.5mW
TTL/DTL/CMOS Direct Interface
Break-Before-Make Switching
Replaces DG506/DG507


CMOS
8 AND 16 CHANNEL
ANALOG MULTIPLEXERS
AD7506, AD7507
FEATURES
R_{on} 300Ω
Power Dissipation: 1.5mW
TTL/DTL/CMOS Direct Interface
Break-Before-Make Switching
Replaces DG506/DG507
GENERAL DESCRIPTION
The AD7506 is a monolithic CMOS 16-channel analog multiplexer packaged in a 28-pin DIP. It switches a common output to one of 16 inputs, depending on the state of four address lines and an "enable". The AD7507 is identical to the AD7506 except it has two outputs switched to two of 16 inputs depending on three binary address states and an "enable".
The AD7506 and AD7507 are excellent examples of a high breakdown CMOS process combined with a double layer interconnect for high density. Both units are silicon/nitride passivated featuring increased stability and reliability.
FUNCTIONAL DIAGRAMS
AD7506
AD7507

GENERAL DESCRIPTION

The AD7506 is a monolithic CMOS 16-channel analog multiplexer packaged in a 28-pin DIP. It switches a common output to one of 16 inputs, depending on the state of four address lines and an "enable". The AD7507 is identical to the AD7506 except it has two outputs switched to two of 16 inputs depending on three binary address states and an "enable".

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

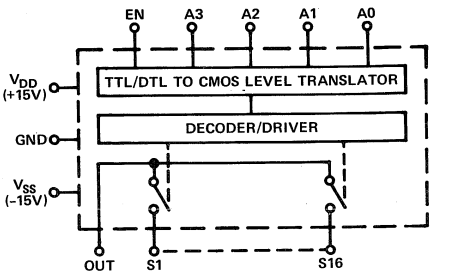
V_{DD} – GND . . . . . +17V
V_{SS} – GND . . . . . -17V
V Between Any Switch Terminals. 25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Switch Current (I_S, Continuous). 20mA
Switch Current (I_S, Surge)
  1ms duration, 10% duty cycle 35mA
Power Dissipation (Package)
28 pin Ceramic DIP
  Up to +50°C. 1000mW
  Derates above +50°C by . . . . . 10mW/°C
28 pin Plastic DIP
  Up to +50°C. 1200mW
  Derates above +50°C by . . . . . 12mW/°C
Operating Temperature
  Plastic (J, K versions). . . . . 0 to +75°C
  Ceramic (J, K versions). . . . . -25°C to +85°C
  Ceramic (S, T versions). . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION:

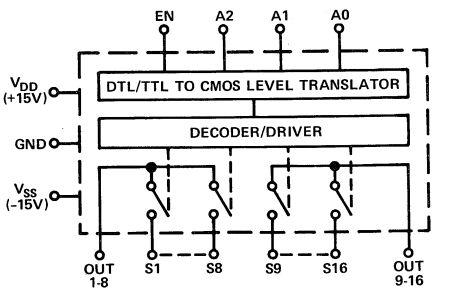
1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

FUNCTIONAL DIAGRAMS

AD7506

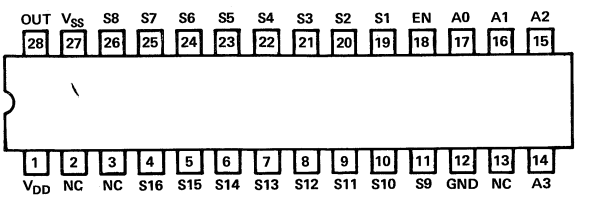


AD7507

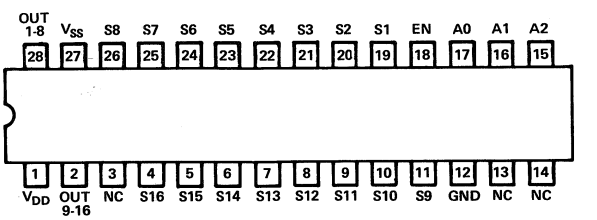


PIN CONFIGURATIONS (Top View)

AD7506



AD7507



SPECIFICATIONS (V_{DD} = +15V, V_{SS} = -15V unless otherwise noted)

PARAMETER		VERSION[1]	SWITCH CONDITION	@ +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
ANALOG SWITCH						
R_{ON}		J, K	ON	300Ω typ, 450Ω max	550Ω max	V_S = -10V to +10V, I_S = 1mA
		S, T	ON	400Ω max	500Ω max	
R_{ON} vs. V_S		All	ON	15% typ		
R_{ON} vs. Temperature		All	ON	0.5%/°C typ		V_S = 0V, I_S = 1mA
ΔR_{ON} Between Switches		All	ON	4% typ		
R_{ON} vs. Temperature Between Switches		All	ON	0.05%/°C typ		
I_S		J, K	OFF	0.05nA typ, 5nA max	50nA max	V_S = -10V, V_{OUT} = +10V and V_S = +10V, V_{OUT} = -10V "Enable" Low
		S, T	OFF	0.05nA typ, 1nA max	50nA max	
I_{OUT}	AD7506	J, K	OFF	0.3nA typ, 20nA max	500nA max	
		S, T	OFF	0.3nA typ, 10nA max	500nA max	
	AD7507	J, K	OFF	0.3nA typ, 10nA max	250nA max	
		S, T	OFF	0.3nA typ, 5nA max	250nA max	
$I_{OUT} - I_S$	AD7506	J, K	ON	0.3nA typ, 20nA max	500nA max	V_S = 0
		S, T	ON	0.3nA typ, 10nA max	500nA max	
	AD7507	J, K	ON	0.3nA typ, 10nA max	250nA max	
		S, T	ON	0.3nA typ, 5nA max	250nA max	
DIGITAL CONTROL						
V_{INL}		J, S			0.8V max	Note 2
V_{INH}		K, T			3.0V min 2.4V min	
I_{INL} or I_{INH}		All		10μA max	30μA max	
C_{IN}		All		3pF typ		
DYNAMIC CHARACTERISTICS[3]						
$t_{TRANSITION}$		J, S		700ns typ		V_{IN}: 0 to 3.0V
		K, T		700ns typ, 1000ns max		
t_{OPEN}		All		100ns typ		
t_{ON} (En)		J, S		0.8μs typ		V_{EN}: 0 to 3.0V
		K, T		1.5μs max		
t_{OFF} (En)		J, S		0.8μs typ		
		K, T		1μs max		
"OFF" Isolation		All		70dB typ		V_{EN} = 0, R_L = 200Ω, C_L = 3.0pF, V_S = 3.0V rms, f = 50kHz
C_S		All	OFF	5pF typ		
C_{OUT}	AD7506	All	OFF	40pF typ		
	AD7507	All	OFF	20pF typ		
C_{S-OUT}		All	OFF	0.5pF typ		
C_{SS} Between Any Two Switches		All	OFF	0.5pF typ		
POWER SUPPLY						
I_{DD}		J, K	OFF	0.05mA typ, 1mA max		All Digital Inputs Low
		S, T	OFF	0.05mA typ, 1mA max	2mA max	
I_{SS}		J, K	OFF	0.05mA typ, 1mA max		
		S, T	OFF	0.05mA typ, 1mA max	2mA max	
I_{DD}		J, K	ON	0.3mA typ, 1mA max		All Digital Inputs High
		S, T	ON	0.3mA typ, 1mA max	2mA max	
I_{SS}		J, K	ON	0.05mA typ, 1mA max		
		S, T	ON	0.05mA typ, 1mA max	2mA max	

NOTES:
[1] JN, KN versions specified for 0 to +75°C; JD, KD versions for -25°C to +85°C; and SD, TD versions for -55°C to +125°C.
[2] A pullup resistor, typically 1-2kΩ is required to make the J and S versions compatible with TTL/DTL. The maximum value is determined by the output leakage current of the driver gate when in the high state.
[3] AC parameters are sample tested to ensure conformance to specifications.
Specifications subject to change without notice.

TRUTH TABLES

AD7506

A_3	A_2	A_1	A_0	E_N	"ON"
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16
X	X	X	X	0	None

AD7507

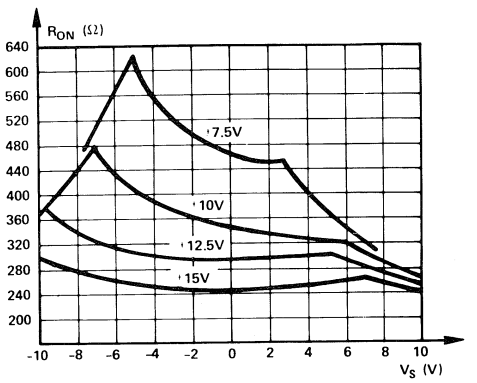
A_2	A_1	A_0	E_N	"ON"
0	0	0	1	1 & 9
0	0	1	1	2 & 10
0	1	0	1	3 & 11
0	1	1	1	4 & 12
1	0	0	1	5 & 13
1	0	1	1	6 & 14
1	1	0	1	7 & 15
1	1	1	1	8 & 16
X	X	X	0	None

ORDERING INFORMATION

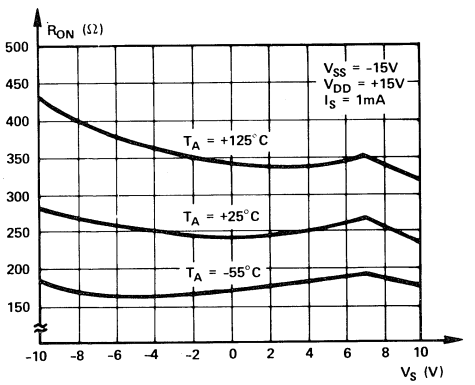
Plastic (Suffix N)	Ceramic (Suffix D)	Operating Temperature Range
AD7506JN AD7506KN AD7507JN AD7507KN		0 to +75°C
	AD7506JD AD7506KD AD7507JD AD7507KD	-25°C to +85°C
	AD7506SD AD7506TD AD7507SD AD7507TD	-55°C to +125°C

Typical Performance Characteristics

1. R_{ON} vs. V_S

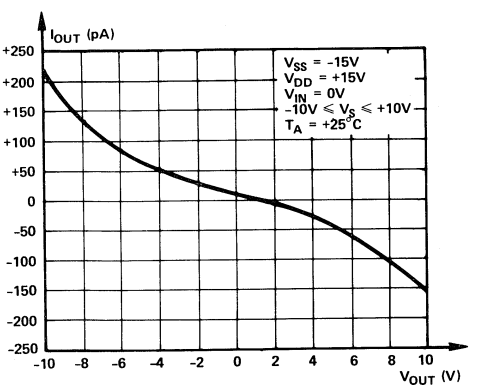


At Different Power Supplies

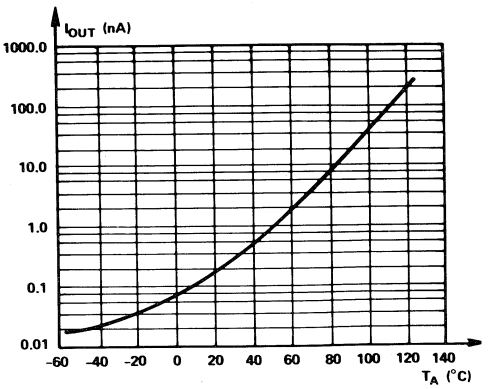


At Different Temperatures

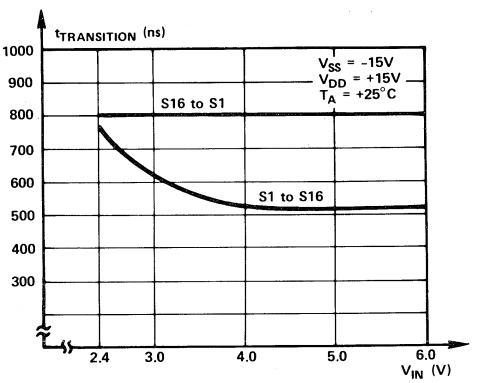
2. I_{OUT} vs. V_{OUT}



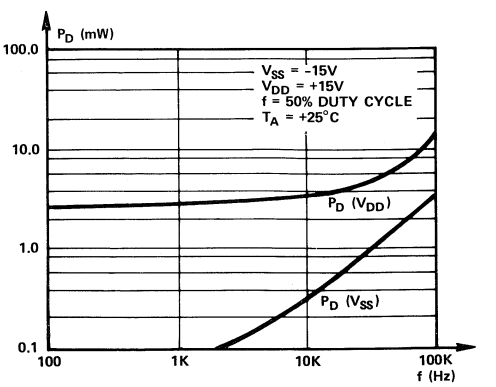
3. I_{OUT} vs. T_A



4. $t_{TRANSITION}$ vs. V_{IN}

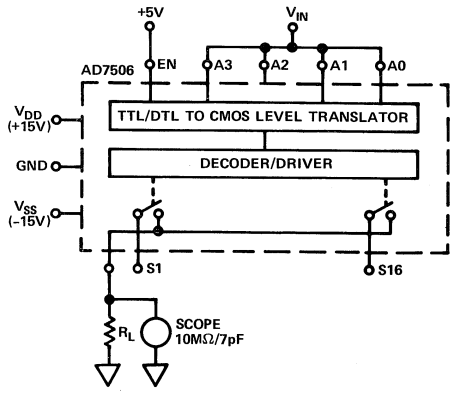


5. P_D vs. Logic Frequency

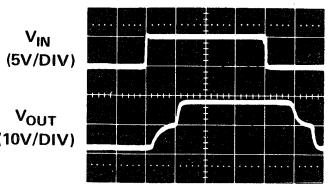


TYPICAL SWITCHING CHARACTERISTICS

TEST CIRCUIT 1

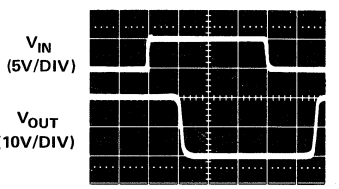


0.5μs/DIV



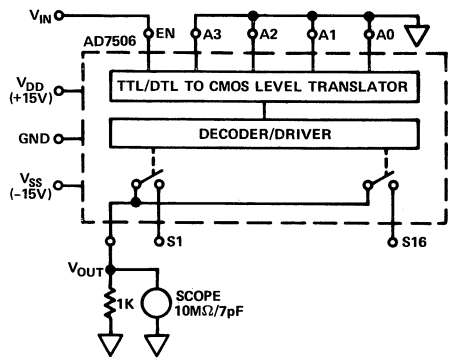
S_1 = -10V, S_{16} = +10V,
$S_2 - S_{15}$ = 0V, R_L = 1K

0.5μs/DIV

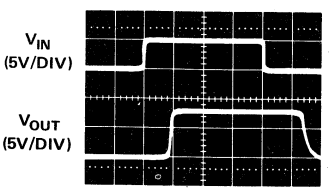


S_1 = +10V, S_2 = -10V,
$S_2 - S_{15}$ = 0V, R_L = ∞

TEST CIRCUIT 2

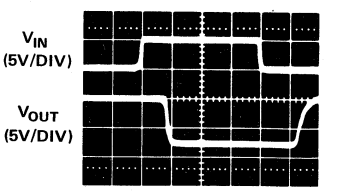


0.5μs/DIV



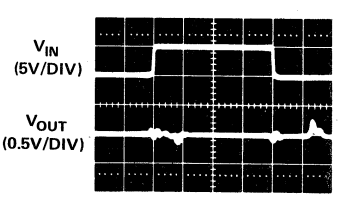
S_1 through S_{16} = +10V

0.5μs/DIV



S_1 through S_{16} = -10V

0.5μs/DIV

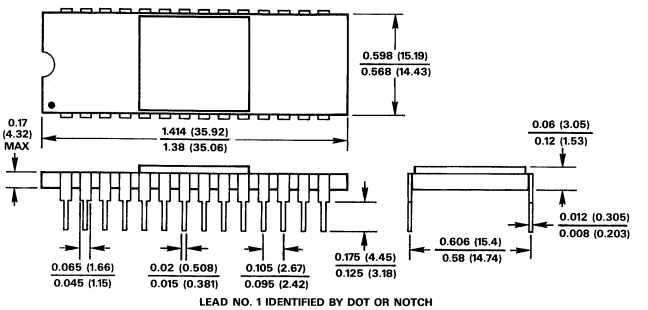


S_1 through S_{16} = 0V

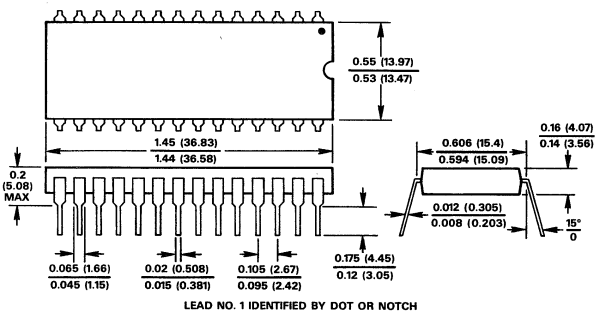
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-PIN CERAMIC DIP (SUFFIX D)

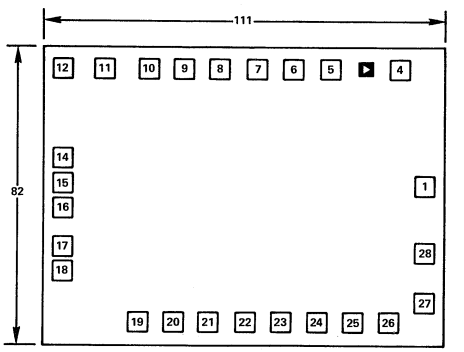


28-PIN PLASTIC DIP (SUFFIX N)

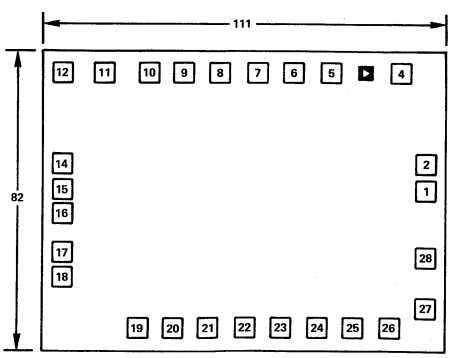


BONDING DIAGRAMS

AD7506



AD7507



All bonding pads are 4 x 4 MIL.
All pad numbers correspond with DIP package pin configuration.

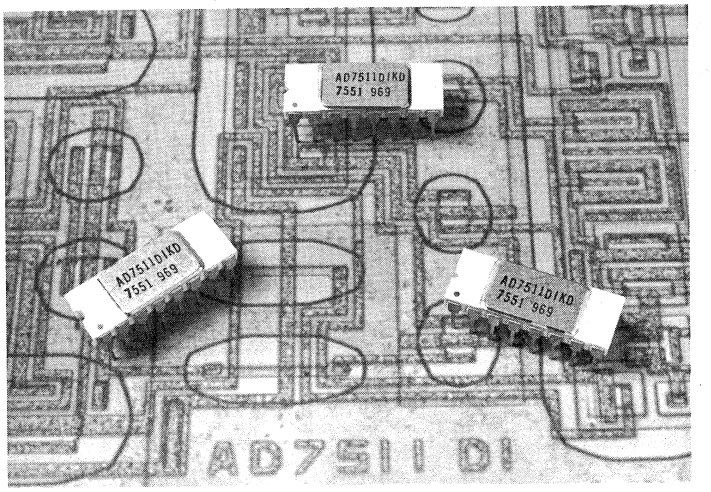
ANALOG DEVICES

DI CMOS Protected Analog Switches

AD7510DI, AD7511DI, AD7512DI

FEATURES

- Latch-Proof
- Overvoltage-Proof: ±25V
- Low R_{ON}: 75Ω
- Low Dissipation: 3mW
- TTL/CMOS Direct Interface
- Silicon-Nitride Passivated
- Monolithic Dielectrically-Isolated CMOS



GENERAL DESCRIPTION

The AD7510DI, AD7511DI and AD7512DI are a family of latch proof dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance (75Ω) or low leakage current (400pA), the main features of an analog switch.

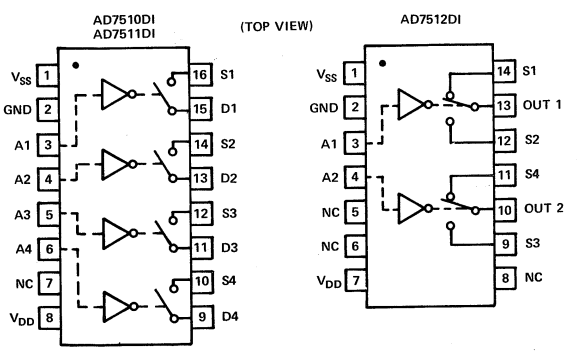
The AD7510DI and AD7511DI consist of four independent SPST analog switches packaged in a 16-pin DIP. They differ only in that the digital control logic is inverted. The AD7512DI has two independent SPDT switches packaged in a 14-pin DIP.

Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

ORDERING INFORMATION

Plastic (Suffix N)	Ceramic (Suffix D)	Operating Temperature Range
AD7510DIJN AD7510DIKN AD7511DIJN AD7511DIKN AD7512DIJN AD7512DIKN		0 to +70°C
	AD7510DIJD AD7510DIKD AD7511DIJD AD7511DIKD AD7512DIJD AD7512DIKD	−25°C to +85°C
	AD7510DISD AD7511DISD AD7511DITD AD7512DISD AD7512DITD	−55°C to +125°C

PIN CONFIGURATIONS



CONTROL LOGIC

AD7510DI: Switch "ON" for Address "HIGH"

AD7511DI: Switch "ON" for Address "LOW"

AD7512DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = –15V unless otherwise noted)

COMMERCIAL VERSIONS (J, K)

PARAMETER	MODEL	VERSION	+25°C	0 to +70°C (N) –25°C to +85°C (D)	TEST CONDITIONS
ANALOG SWITCH					
R_{ON} [1]	All	J, K	75Ω typ, 100Ω max	175Ω max	$-10V \leqslant V_D \leqslant +10V$
R_{ON} vs V_D (V_S)	All	J, K	20% typ		I_{DS} = 1.0mA
R_{ON} Drift	All	J, K	+0.5%/°C typ		
R_{ON} Match	All	J, K	1% typ		V_D = 0, I_{DS} = 1.0mA
R_{ON} Drift Match	All	J, K	0.01%/°C typ		
I_D (I_S) OFF[1]	All	J, K	0.5nA typ, 5nA max	500nA max	V_D = –10V, V_S = +10V and V_D = +10V, V_S = –10V
I_D $(I_S)_{ON}$ [2]	All	J, K	10nA max		$V_S = V_D$ = +10V $V_S = V_D$ = –10V
I_{OUT} [1]	AD7512DI	J, K	15nA max	1500nA max	$V_{S1} = V_{OUT} = \pm 10V$, $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$, $V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL} [1]	All	J, K		0.8V max	
V_{INH} [1]	All	J		3.0V min	
	All	K		2.4V min	
C_{IN}	All	J, K	3pF typ		
I_{INH} [1]	All	J, K	10nA max		$V_{IN} = V_{DD}$
I_{INL} [1]	All	J, K	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON}	AD7510DI	J, K	180ns typ		
	AD7511DI	J, K	350ns typ		V_{IN} = 0 to +3.0V
t_{OFF}	AD7510DI	J, K	350ns typ		
	AD7511DI	J, K	180ns typ		
$t_{TRANSITION}$	AD7512DI	J, K	300ns typ		
C_S (C_D)OFF	All	J, K	8pF typ		
C_S (C_D)ON	All	J, K	17pF typ		
C_{DS} (C_{S-OUT})	All	J, K	1pF typ		V_D (V_S) = 0V
C_{DD} (C_{SS})	All	J, K	0.5pF typ		
C_{OUT}	AD7512DI	J, K	17pF typ		
Q_{INJ}	All	J, K	30pC typ		Measured at S or D terminal. C_L = 1000pF, V_{IN} = 0 to 3V, V_D (V_S) = +10V to –10V
POWER SUPPLY					
I_{DD} [1]	All	J, K	500μA max		All digital inputs = V_{INH}
I_{SS} [1]	All	J, K	100μA max		
I_{DD} [1]	All	J, K	100μA max		All digital inputs = V_{INL}
I_{SS} [1]	All	J, K	100μA max		

NOTES:
[1] 100% tested.
[2] Guaranteed, not production tested.
[3] A pullup resistor, typically 1-2kΩ is required to make "J" versions TTL compatible.

Specifications subject to change without notice.

MILITARY VERSIONS (S, T)

PARAMETER	MODEL	VERSION	+25°C	-55°C to +125°C	TEST CONDITIONS
ANALOG SWITCH					
R_{ON} [1]	All	S, T	100Ω max	175Ω max	$-10V \leq V_D \leq +10V$ I_{DS} = 1mA
I_D $(I_S)_{OFF}$ [1]	All	S, T	3nA max	200nA max	V_D = -10V, V_S = +10V and V_D = +10V, V_S = -10V
I_D $(I_S)_{ON}$ [2]	All	S, T	10		$V_S = V_D$ = +10V and $V_S = V_D$ = -10V
I_{OUT} [1]	AD7512DI	S, T	9nA max	600nA max	$V_{S1} = V_{OUT} = \pm 10V$ $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$ $V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL} [1]	All	S, T		0.8V max	
V_{INH} [1,3]	AD7510DI	S		2.4V min	
	AD7511DI	T		2.4V min	
	AD7512DI	T		2.4V min	
	AD7511DI	S		3.0V min	
	AD7512DI	S		3.0V min	
I_{INH} [1]	All	S, T	10nA max		$V_{IN} = V_{DD}$
I_{INL} [1]	All	S, T	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON} [2]	AD7510DI	S, T	1.0μs max		V_{IN} = 0 to +3V
	AD7511DI	S, T	1.0μs max		
t_{OFF} [2]	AD7510DI	S, T	1.0μs max		
	AD7511DI	S, T	1.0μs max		
$t_{TRANSITION}$ [2]	AD7512DI	S, T	1.0μs max		
POWER SUPPLY					
I_{DD} [1]	All	S, T		800μA max	All digital inputs = V_{INH}
I_{SS} [1]	All	S, T		800μA max	
I_{DD} [1]	All	S, T		500μA max	All digital inputs = V_{INL}
I_{SS} [1]	All	S, T		500μA max	

NOTES:

[1] 100% tested.
[2] Guaranteed, not production tested.
[3] A pullup resistor, typically 1-2kΩ is required to make AD7511DISD and AD7512DISD TTL compatible.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND . . . . . +17V
V_{SS} to GND . . . . . -17V
Overvoltage at V_D (V_S)
(1 second surge) . . . . . V_{DD} +25V
or V_{SS} -25V
(Continuous) . . . . . V_{DD} +20V
or V_{SS} -20V
Switch Current (I_{DS}, Continuous) 50mA
Switch Current (I_{DS}, Surge)
1ms Duration, 10% Duty Cycle 150mA
Digital Input Voltage Range . . . . . 0V to V_{DD}
Power Dissipation (Package)
14 & 16 pin Ceramic Dip
Up to +75°C. 450mW
Derates above +75°C by . . . . . .6mW/°C
14 & 16 pin Plastic Dip
Up to +70°C. 670mW
Derates above +75°C by . . . . . .8.3mW/°C
Storage Temperature . . . . . -65°C to +150°C
Operating Temperature
Plastic (J, K Versions) . . . . . 0 to +70°C
Ceramic (J, K Versions) . . . . . -25°C to +85°C
Ceramic (S, T Versions) . . . . . -55°C to +125°C

CAUTION: The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high electrostatic fields. Keep unused units in conductive foam at all times. Prior to pulling the devices from the conductive foam, ground the foam to deplete any accumulated charge.

CIRCUIT DESCRIPTION

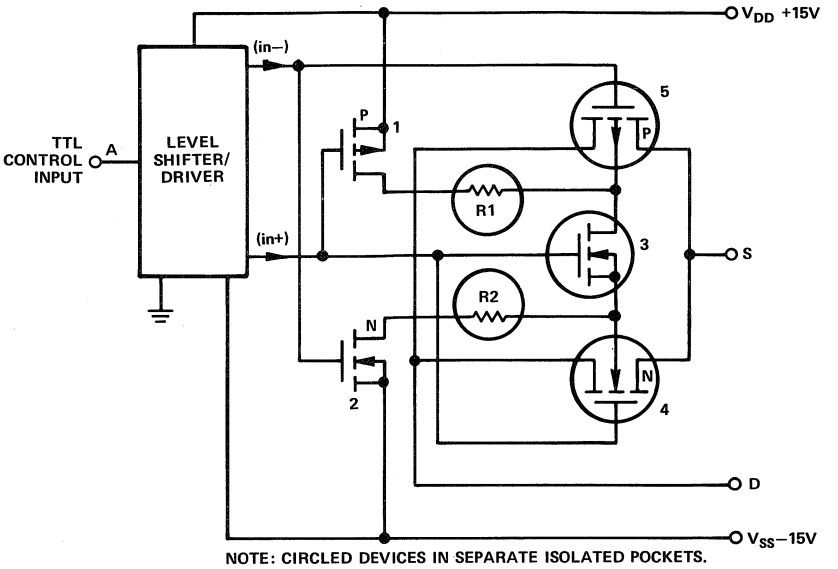


Figure 1. Typical Output Switch Circuitry of AD7510DI Series

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenum necessitated protection circuitry. These protection circuits, however, either caused degradation of important switch parameters such as R_{ON} or leakage, or provided only limited protection in the event of overvoltage.

The AD7510DI series switches utilize a dielectrically-isolated CMOS fabrication process to eliminate the four-layer substrate found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 1. The output switching element is comprised of device numbers 4 and 5. Operation is as follows: for an "ON" switch, (in+) is V_{DD} and (in—) is V_{SS} from the driver circuits. Device numbers 1 and 2 are "OFF" and number 3 is "ON." Hence, the back-gates of the P- and N-channel output devices (numbers 4 and 5) are tied together and floating. (The circled devices are located in separate dielectrically isolated pockets.) Floating the output switch back-gates with the signal input increases the effective threshold voltage for an applied analog signal, thus providing a flatter R_{ON} versus V_S response.

For an "OFF" switch, device number 3 is "OFF," and the back-gates of devices 4 and 5 are tied through 1kΩ resistors (R1 and R2) to the respective supply voltages through the "ON" devices 1 and 2.

If a voltage is applied to the S or D terminal which exceeds V_{DD} or V_{SS}, the S- or D-to-back-gate diode is forward biased; however, R1 and R2 provide current limiting action.

Consequently, without external current limiting resistance (or increased R_{ON}), the AD7510DI series switches provide:

1. Latch-proof operation
2. Overvoltage protection 25V beyond the V_{SS} and V_{DD} supply voltage

An equivalent circuit of the output switch element in Figure 2 shows that, indeed, the 1kΩ limiting resistors are in series with the back-gates of the P- and N-channel output devices—*not* in series with the signal path between the S and D terminals.

In some applications it is possible to turn on a parasitic NPN (drain to back-gate to source of the N-channel) transistor, causing device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors (200Ω) or current limiting devices (output of op amps) will prevent damage to the device.

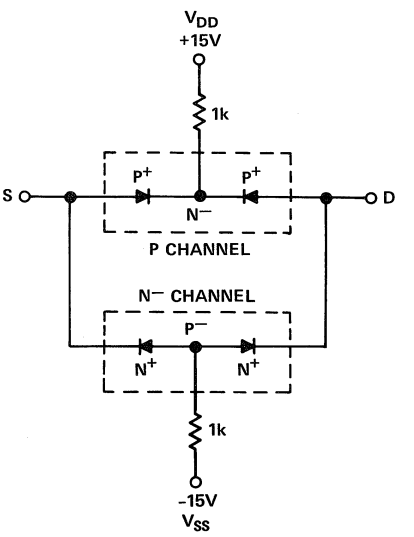
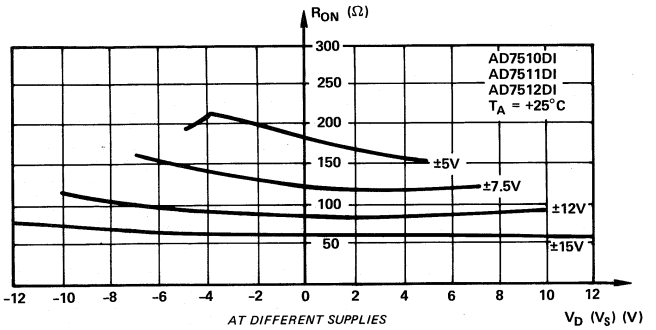
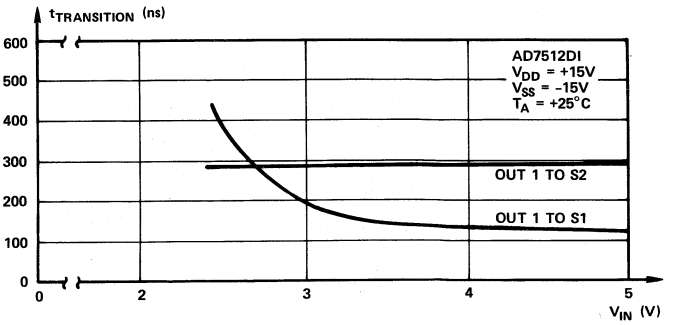


Figure 2. AD7510DI Series Output Switch Diode Equivalent Circuit

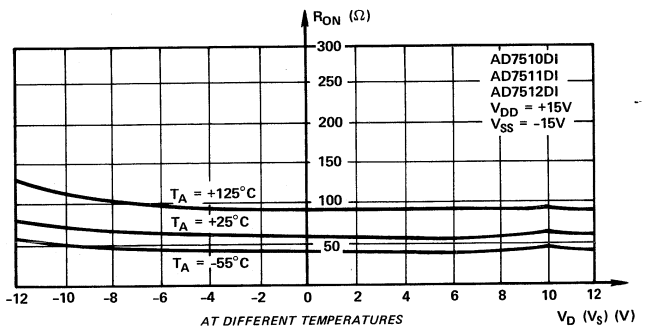
TYPICAL PERFORMANCE CHARACTERISTICS



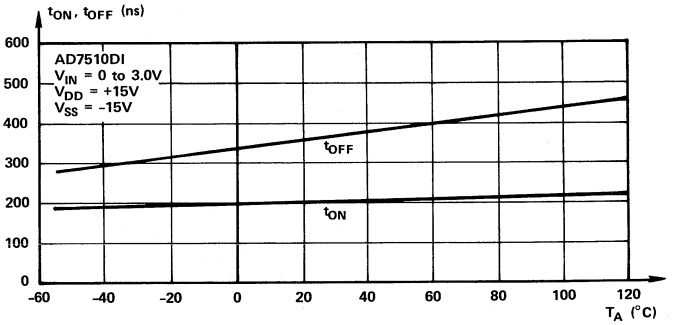
R_{ON} as a Function of V_D (V_S)



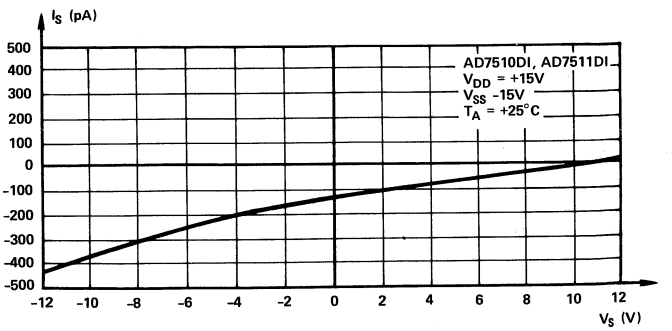
$t_{TRANSITION}$ as a Function of Digital Input Voltage



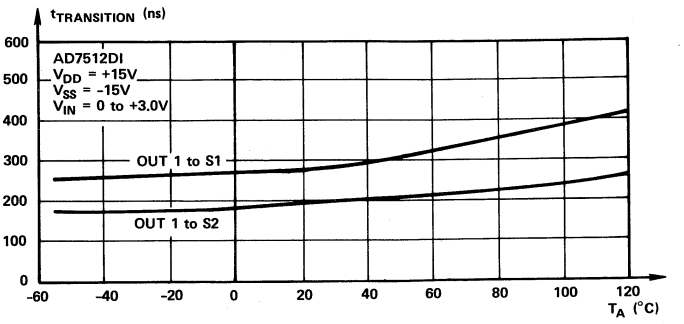
R_{ON} as a Function of V_D (V_S)



t_{ON}, t_{OFF} as a Function of Temperature

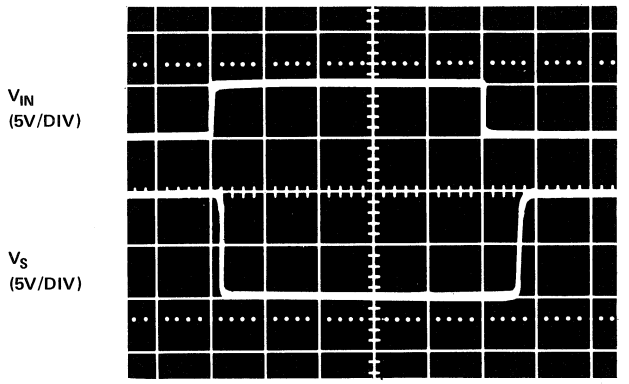


I_S, $(I_D)_{OFF}$ vs V_S



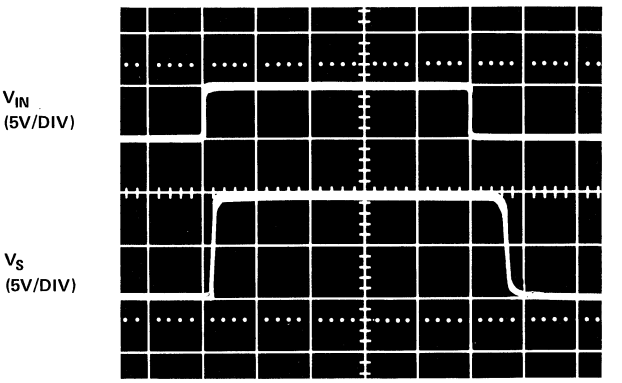
$t_{TRANSITION}$ as a Function of Temperature

0.5μs/DIV



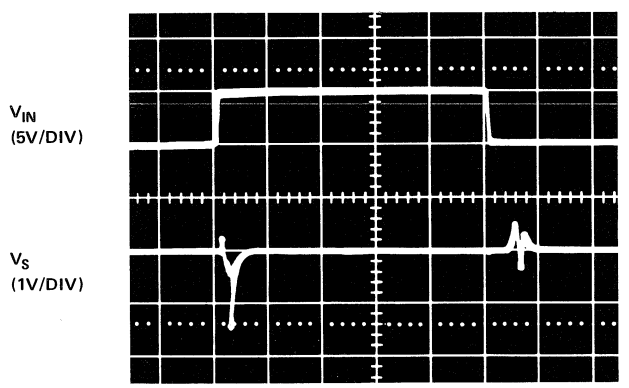
Switching Waveforms for V_D = -10V

0.5μs/DIV



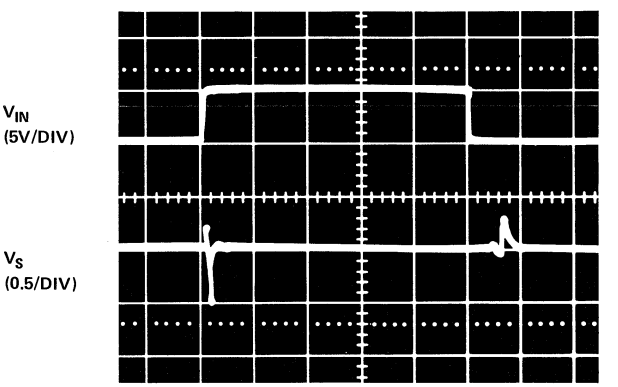
Switching Waveforms for V_D = +10V

0.5μs/DIV



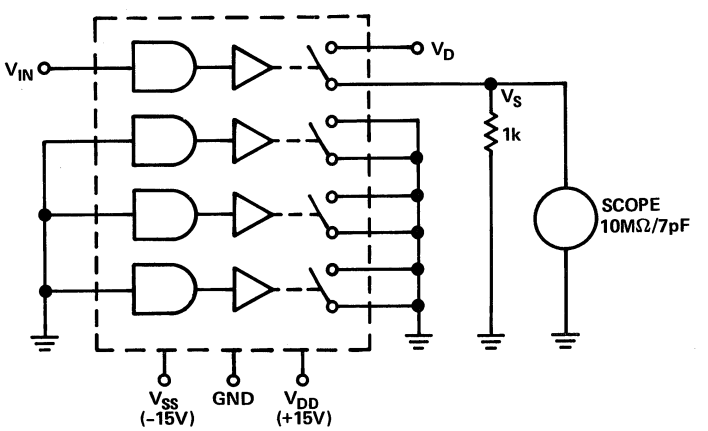
Switching Waveforms for V_D = Open

0.5μs/DIV



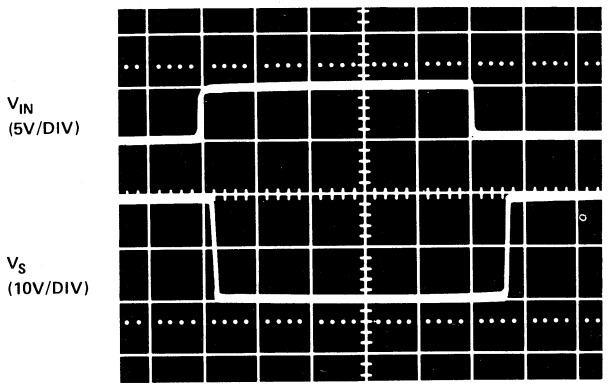
Switching Waveforms for V_D = 0V

AD7510DI, AD7511DI TEST CIRCUIT



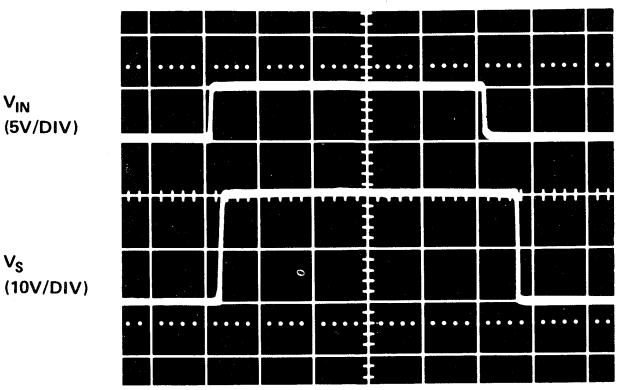
TYPICAL SWITCHING CHARACTERISTICS AD7512DI

0.5μs/DIV



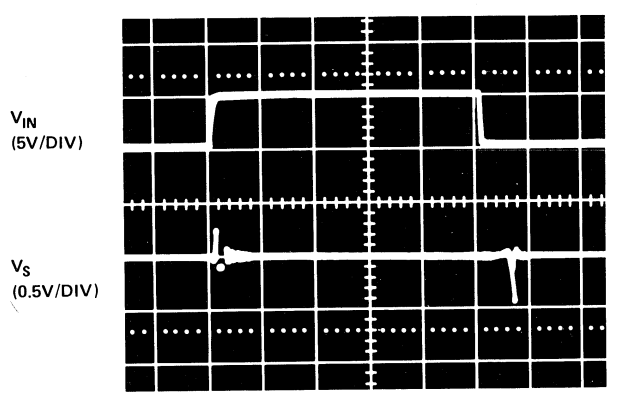
Switching Waveforms for
V_{S1} = -10V, V_{S2} = +10V, R_L = 1k

0.5μs/DIV



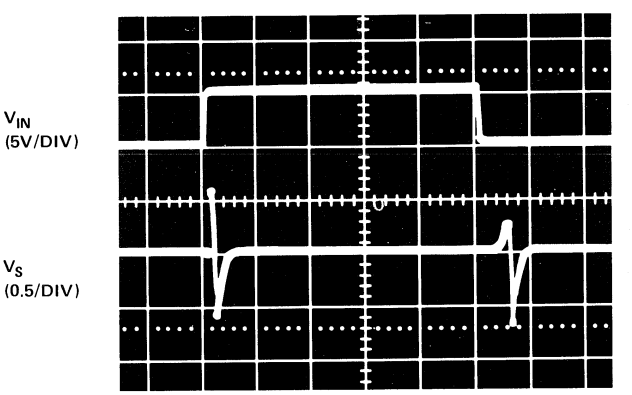
Switching Waveforms for
V_{S1} = +10V, V_{S2} = -10V, R_L = ∞

0.5μs/DIV



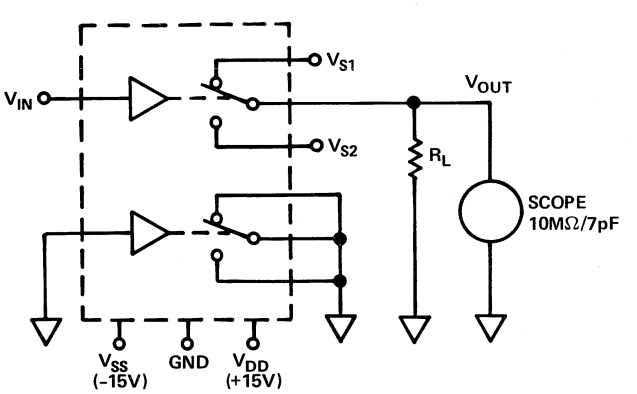
Switching Waveforms for
V_{S1} and V_{S2} = 0V, R_L = ∞

0.5μs/DIV



Switching Waveforms for
V_{S1} and V_{S2} = Open, R_L = 1k

AD7512DI TEST CIRCUIT

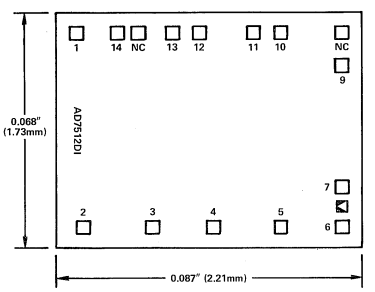


TERMINOLOGY

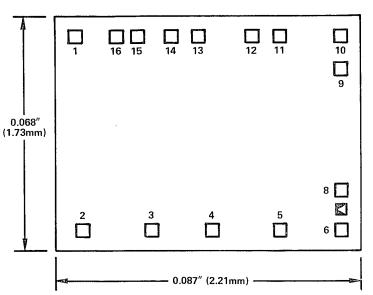
R_{ON}:	Ohmic resistance between terminals D and S.
R_{ON} Drift Match:	Difference between the R_{ON} drift of any two switches.
R_{ON} Match:	Difference between the R_{ON} of any two switches.
I_D (I_S)$_{OFF}$:	Current at terminals D or S. This is a leakage current when the switch is "OFF."
I_D (I_S)$_{ON}$:	Leakage current that flows from the closed switch into the body. (This leakage will show up as the difference between the current I_D going into the switch and the outgoing current I_S.)
V_D (V_S):	Analog voltage on terminal D (S).
C_S (CD):	Capacitance between terminal S (D) and ground. (This capacitance is specified for the switch open and closed.)
C_{DS}:	Capacitance between terminals D and S. (This will determine the switch isolation over frequency.)
C_{DD} (C_{SS}):	Capacitance between terminals D (S) of any two switches. (This will determine the cross coupling between switches vs. frequency.)
t_{ON}:	Delay time between the 50% points of the digital input and switch "ON" condition.
t_{OFF}:	Delay time between the 50% points of the digital input and switch "OFF" condition.
$t_{transition}$:	Delay time when switching from one address state to another.
V_{INL}:	Threshold voltage for the low state.
V_{INH}:	Threshold voltage for the high state.
I_{INL} (I_{INH}):	Input current of the digital input.
C_{IN}:	Input capacitance to ground of the digital input.
V_{DD}:	Most positive voltage supply.
V_{SS}:	Most negative voltage supply.
I_{DD}:	Positive supply current.
I_{SS}:	Negative supply current.

BONDING DIAGRAMS (TOP VIEW)

AD7512DI



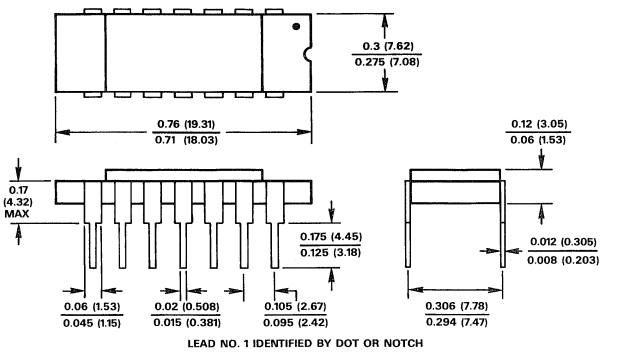
AD7510DI, AD7511DI



OUTLINE DIMENSIONS

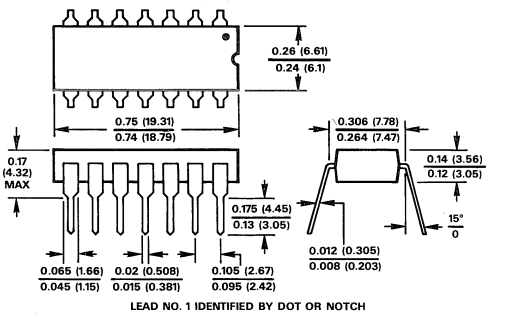
Dimensions shown in inches and (mm).

14-PIN CERAMIC DIP



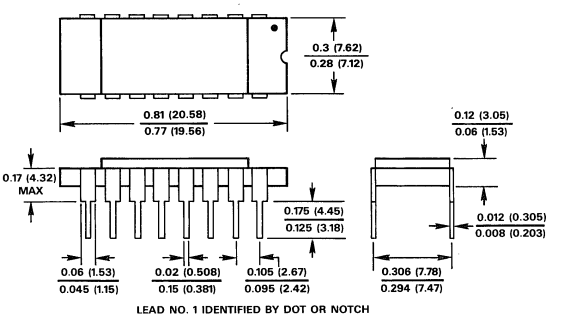
AD7512DI

14-PIN PLASTIC DIP



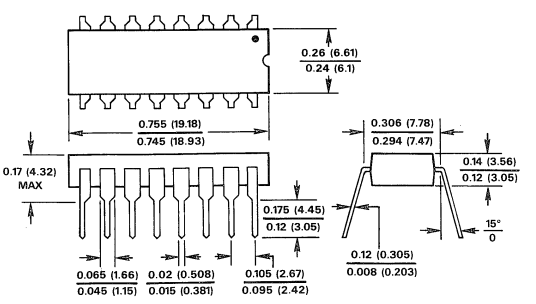
AD7512DI

16-PIN CERAMIC DIP



AD7510DI, AD7511DI

16-PIN PLASTIC DIP



AD7510DI, AD7511DI

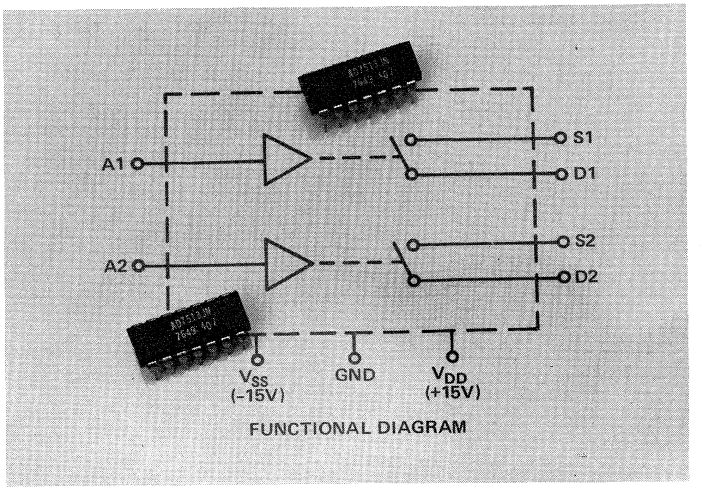
ANALOG DEVICES

CMOS Dual SPST Analog Switch

AD7513

FEATURES

"ON" Resistance: 55Ω
Break-Before-Make Switching Power Dissipation: 3mW
DTL/TTLCMOS Compatible
Switch Current: 50mA
Replaces DG-200



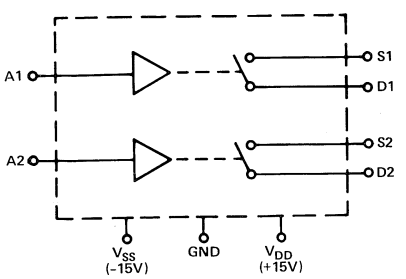
FUNCTIONAL DIAGRAM

GENERAL DESCRIPTION

The AD7513 is composed of two independent single-pole-single-throw switches on a CMOS chip. State-of-the-art design provides TTL/DTL/CMOS compatibility and a low power dissipation of 3mW.

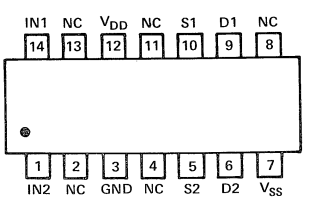
The AD7513 is an excellent replacement for reed relays and FET switches due to its low power dissipation, direct logic interface capability and low price. Its high surge current capability makes it ideal for use in integrator or sample/hold circuits.

FUNCTIONAL DIAGRAM

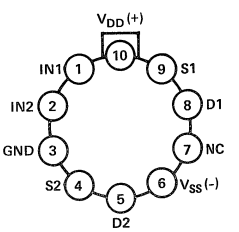


PIN CONFIGURATIONS (Top View)

PLASTIC DIP



TO-100



ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . +17V
V_{SS} to GND . . . . . -17V
V Between any Switch Terminals . . . . . +25V
Switch Current (I_{DS}, Continuous). 50mA
Switch Current (I_{DS}, Surge) –
1ms duration, 10% duty cycle 150mA
Digital Input Voltage Range . . . . . GND to V_{DD}
Power Dissipation (Package)
14 pin Plastic DIP
Up to +70°C 670mW
Derates above +70°C by . . . . . 8.3mW/°C
10 lead TO-100
Up to +25°C 680mW
Derates above +25°C by . . . . . 5.4mW/°C
Operating Temperature
Plastic. . . . . 0 to +75°C
TO-100 (J, K versions) . . . . . -25°C to +85°C
TO-100 (S, T versions) . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION:

1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

LOGIC

Switch "ON" For Address "LOW".

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = -15V unless otherwise noted)

PARAMETER	VERSION[1]	SWITCH	@ +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
ANALOG SWITCH					
R_{DS}	J, K	ON	55Ω typ, 80Ω max	100Ω max	-10V ≤ V_D ≤ +10V,
	S, T	ON	55Ω typ, 70Ω max	100Ω max	I_{DS} = 1mA
R_{DS} vs. V_D	All	ON	20% typ		
R_{DS} vs. Temperature	All	ON	+0.5%/°C typ		V_D = 0, I_{DS} = 1mA
ΔR_{DS} Between Switches	All	ON	1% typ		
R_{DS} vs. Temperature Between Switches	All	ON	0.01%/°C typ		
I_D or I_S	J, K	OFF	0.1nA typ, 5nA max	500nA max	V_S = 10V, V_D = -10V and
	S, T	OFF	0.1nA typ, 2nA max	1000nA max	V_S = -10V, V_D = 10V
$I_D - I_S$	J, K	ON	0.1nA typ	500nA max	V_S = V_D = -10V and
	S, T	ON	0.1nA typ	1000nA max	V_S = V_D = +10V
DIGITAL CONTROL					
V_{INL}	All		0.8V max	0.8V max	Note 2
V_{INH}	J, S		3V min	3V min	
	K, T		2.4V min	2.4V min	
I_{INL} or I_{INH}	All		0.01μA max	10μA max	
C_{IN}	All		5pF typ		
DYNAMIC CHARACTERISTICS[3]					
t_{ON}	J, S		700ns typ		V_{IN} = 0 to +3.0V
	K, T		700ns typ, 1000ns max		
t_{OFF}	J, S		400ns typ		
	K, T		400ns typ, 500ns max		
C_S or C_D	All	OFF	8pF typ		V_D (V_S) = 0V
C_S or C_D	All	ON	22pF typ		
C_{DS}	All	OFF	1pF typ		
C_{DD} or C_{SS}	All	ON	0.5pF typ		
"OFF" Isolation	All	OFF	65dB typ		V_{IN} = 5V, R_1 = 1kΩ, C_L = 10pF
					V_S = 3V rms, f = 100kHz
POWER SUPPLY					
I_{DD}	All	OFF	0.15mA typ, 1mA max		V_{IN} = 5V, Both Channels
I_{SS}	All	OFF	0.1mA typ, 1mA max		
I_{DD}	All	ON	0.1mA typ, 1mA max		V_{IN} = 0V, Both Channels
I_{SS}	All	ON	0.1mA typ, 1mA max		
Operating Voltage Range	All		±7.5V typ to ±15V typ		

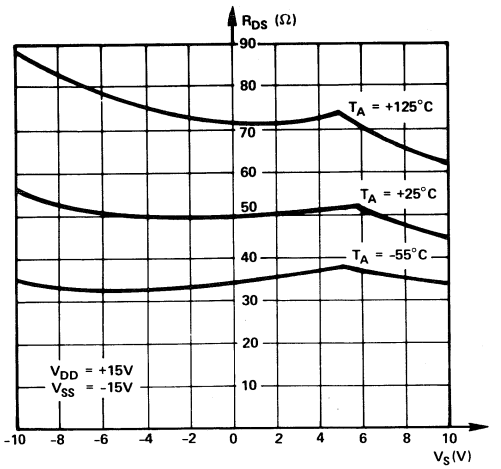
NOTES:
[1] JN, KN versions specified to 0 to +75°C; JH, KH versions for -25°C to +85°C and SH, TH versions for -55°C to +125°C.
[2] A pullup resistor, typically 1-2kΩ, is required to make J and S versions TTL/DTL compatible. The maximum value is determined by the output leakage current of the driver gate when in the high state.
[3] AC parameters are sample tested to assure conformance to specification limits.
Specifications subject to change without notice.

ORDERING INFORMATION

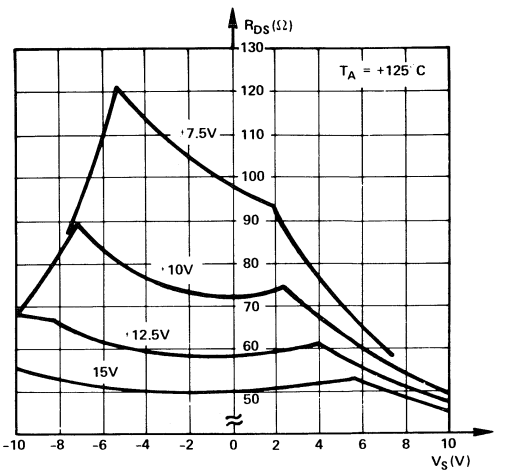
Plastic Dip (Suffix N)	TO-100 (Suffix H)	Operating Temperature Range
AD7513JN AD7513KN		0 to +75°C
	AD7513JH AD7513KH	-25°C to +85°C
	AD7513SH AD7513TH	-55°C to +125°C

Typical Performance Characteristics

1. R_{DS} vs. V_S

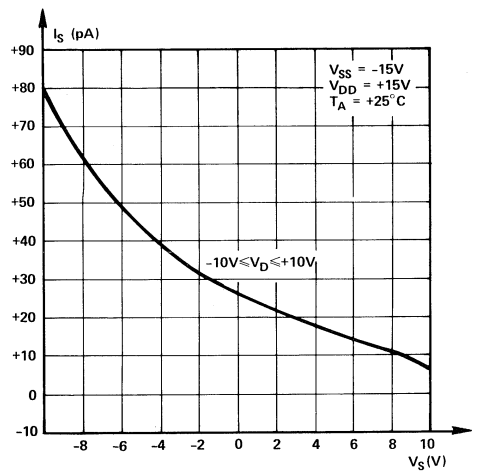


At Different Temperatures

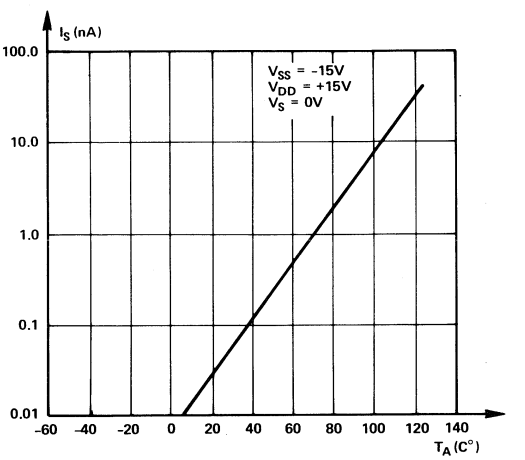


At Different Power Supplies

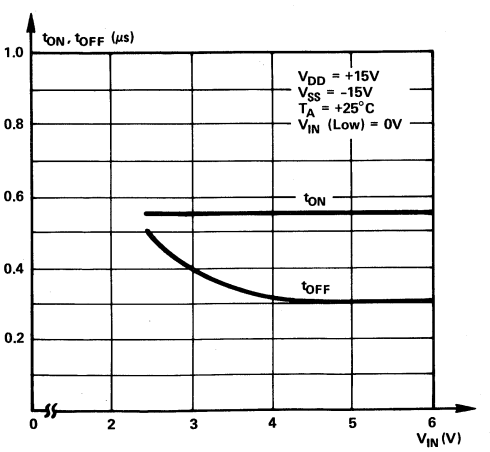
2. I_S vs. V_S



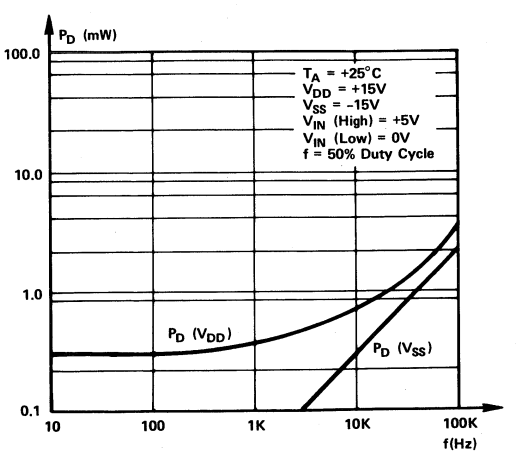
3. I_S vs. T_A



4. t_{ON}, t_{OFF} vs. V_{IN}

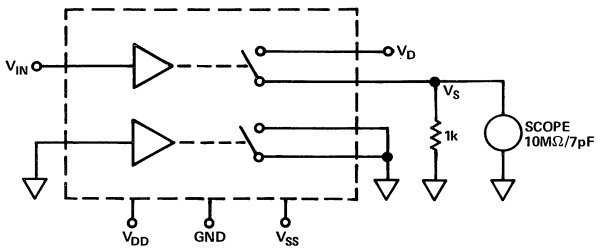


5. P_D vs. Logic Frequency

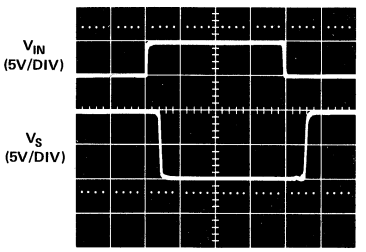


TYPICAL SWITCHING CHARACTERISTICS

TEST CIRCUIT

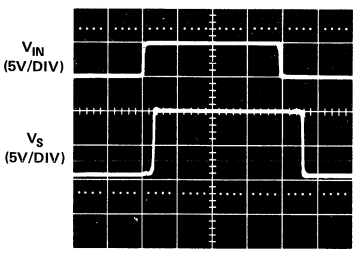


1μs/DIV



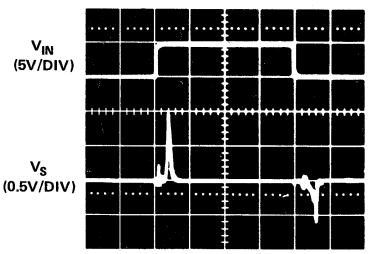
Switching Waveforms for V_D = +10V

1μs/DIV



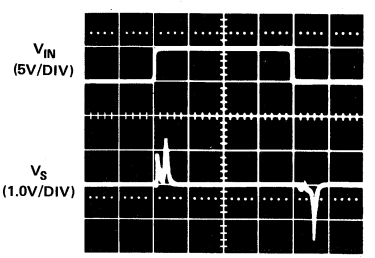
Switching Waveforms for V_D = -10V

1μs/DIV



Switching Waveforms for V_D = 0V

1μs/DIV

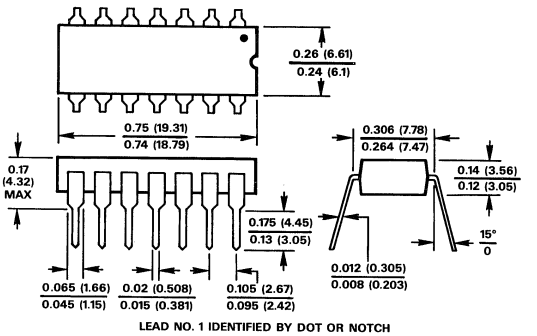


Switching Waveforms for V_D = Open

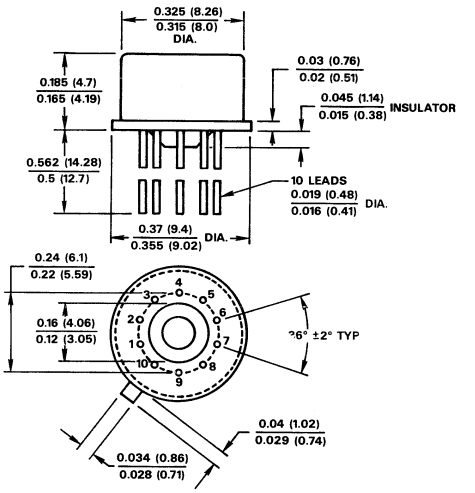
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

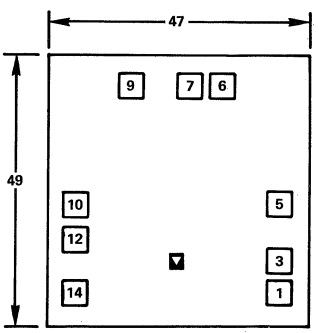
14-PIN PLASTIC DIP (SUFFIX N)



TO-100 (SUFFIX H)



BONDING DIAGRAM



All bonding pads are 4 x 4 MIL.
All pad numbers correspond with DIP package pin configuration.

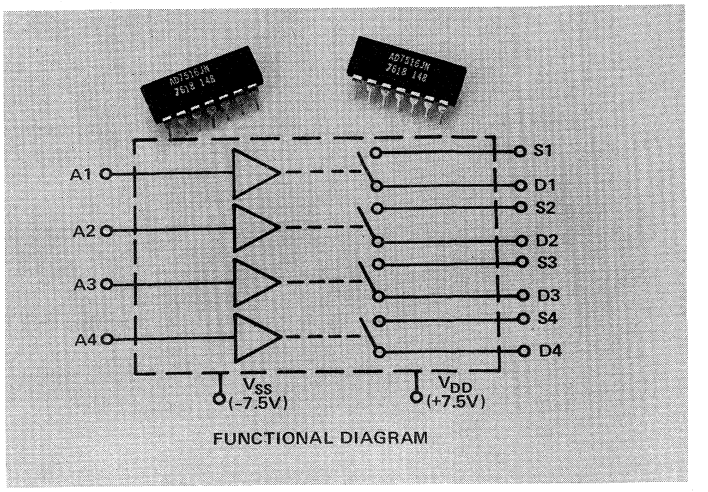
ANALOG DEVICES

CMOS Quad SPST Analog Switch

AD7516

FEATURES

- Low "ON" Resistance: 100Ω
- R_{ON} Mismatch Between Switches: 1%
- Fast Switching: 20ns
- Low Power Dissipation: 10μW, max
- Superior Replacement for:
  - CD4016A (AD7516J, S)
  - CD4066A (AD7516K, T)

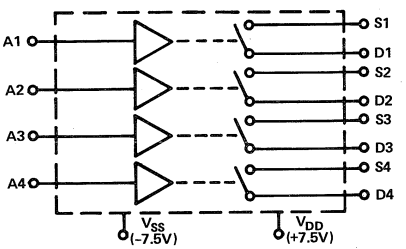


FUNCTIONAL DIAGRAM

GENERAL DESCRIPTION

The AD7516 consists of four SPST switches on a monolithic CMOS chip. It is intended as a superior replacement for the CD4016A, and CD4066A offering improved R_{ON} characteristics. It is useful for fast switching of a wide range of digital or analog signal levels – digital or analog signals to 15V peak and analog signals to ±7.5V peak. It can be operated from balanced or unbalanced power supplies.

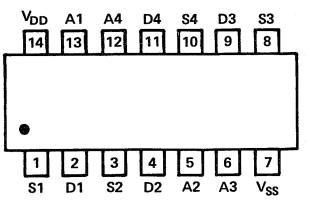
FUNCTIONAL DIAGRAM



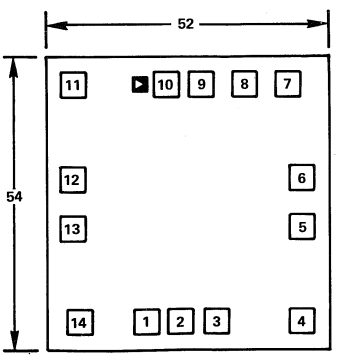
LOGIC

Switch "ON" For Address "HIGH".

PIN CONFIGURATION (Top View)



BONDING DIAGRAM



All bonding pads are 4 x 4 MIL.
All padnumbers correspond with DIP package pin configuration.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

$V_{DD} - V_{SS}$	17V
Switch Voltage	V_{SS} to V_{DD}
Switch Current (I_{DS}, Continuous)	10mA
Switch Current (I_{DS}, Surge)	
1ms duration, 10% duty cycle	15mA
Digital Input Voltage Range	V_{SS} to V_{DD}
Power Dissipation (Package)	
14 pin Ceramic DIP	
Up to +75°C	450mW
Derates above +75°C by	6mW/°C
14 pin Plastic DIP	
Up to +70°C	670mW
Derates above +70°C by	8.3mW/°C
Operating Temperature	
Plastic	0 to +75°C
Ceramic (S, T versions)	-55°C to +125°C
Storage Temperature	-65°C to +150°C

CAUTION:

1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when $V_{SS} = V_{DD} = 0V$ all other pins should be at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

ORDERING INFORMATION

Plastic Dip (Suffix N)	Ceramic Dip (Suffix D)	Operating Temperature Range
AD7516JN		0 to +75°C
AD7516KN		0 to +75°C
	AD7516SD	-55°C to +125°C
	AD7516TD	-55°C to +125°C

SPECIFICATIONS (V_{DD} = +7.5V, V_{SS} = -7.5V unless otherwise noted)

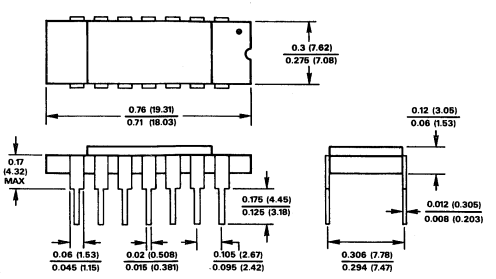
PARAMETER	VERSION[1]	SWITCH	@ +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
ANALOG SWITCH					
R_{DS}	J	ON	400Ω max	520Ω max	$V_{DD} - V_{SS}$ = 15V, $V_{IN} = V_{DD}$, $V_D = V_{SS}$ to V_{DD}, R_L = 10kΩ
	K	ON	280Ω max	300Ω max	
	S	ON	400Ω max	600Ω max	
	T	ON	280Ω max	320Ω max	
	J	ON	150Ω typ, 660Ω max	840Ω max	$V_{DD} - V_{SS}$ = 10V, R_L = 10kΩ, $V_{IN} = V_{DD}$, $V_D = V_{SS}$ to V_{DD}
	K	ON	500Ω max	520Ω max	
	S	ON	150Ω typ, 660Ω max	960Ω max	
	T	ON	500Ω max	850Ω max	
R_{DS} vs. V_D	All	ON	50% typ		$V_{DD} - V_{SS}$ = 15V, $V_D = V_{SS}$ to V_{DD}, $V_{IN} = V_{DD}$
R_{DS} vs. Temperature	All	ON	0.5%/°C typ		$V_{DD} - V_{SS}$ = 15V, $V_{IN} = V_{DD}$, I_{DS} = 1mA, $V_D = \frac{V_{DD} - V_{SS}}{2}$
ΔR_{DS} Between Switches	All	ON	1% typ		$V_{DD} - V_{SS}$ = 15V; $V_{IN} = V_{DD}$, $V_D = V_{SS}$ to V_{DD}, R_L = 10kΩ
	All	ON	1% typ		$V_{DD} - V_{SS}$ = 10V; $V_{IN} = V_{DD}$, $V_D = V_{SS}$ to V_{DD}, R_L = 10kΩ
I_S (I_D)	All	OFF	100pA typ		V_{DD} = +7.5V, V_{SS} = -7.5V; $V_{IN} = V_{SS}$, $V_D(V_S) = V_{SS}$ to V_{DD}, $V_S(V_D)$ = 0V
	All	OFF	125nA max		V_{DD} = +5V, V_{SS} = -5V; $V_{IN} = V_{SS}$, $V_D(V_S) = V_{SS}$ to V_{DD}, $V_S(V_D)$ = 0V
DIGITAL CONTROL					
V_{TH}	All	OFF	0.5V min, 1.5V typ, 2.7V max		V_{SS} = 0V, V_{DD} = +15V, V_D = +15V, I_S = 10μA, V_S = 0V
I_{INL} or I_{INH}	All		10pA typ		$V_{DD} - V_{SS}$ = 10V
C_{IN}	All		5pF typ		
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	All		20ns typ		$V_{DD} - V_{SS}$ = 10V, $V_D \leq$ 10V, $V_{INL} = V_S$, C_L = 15pF, $V_{INH} = V_{DD}$
t_{OFF}	All		20ns typ		
t_{PD}[3]	All	ON	10ns typ		V_{DD} = 10V, V_{SS} = 0V, V_D = 10V (Square Wave), $V_{IN} = V_{DD}$, C_L = 15pF
f_{3dB}	All	ON	40MHz typ		V_{IN} = +5V; V_{DD} = +5V, V_{SS} = -5V, R_L = 1kΩ, V_D = 5V p-p sinewave, f = 1.25MHz
"OFF" Isolation	All	OFF	-50dB typ		V_{IN} = -5V; V_{DD} = +5V, V_{SS} = -5V, R_L = 1kΩ, V_D = 5V p-p sinewave, f = 1.25MHz
Crosstalk – Digital Input to Signal Output	All		50mV typ		$V_{DD} - V_{SS}$ = 10V, $V_{INH} = V_{DD}$, $V_{INL} = V_{SS}$, R_L = 10kΩ, C_L = 15pF
Maximum Control Repetition Rate	All		10MHz typ		V_{DD} = 10V, R_L = 1kΩ, V_{SS} = 0V, V_{INH} = 10V, C_L = 15pF, V_{INH} = 0V
C_S or C_D (OFF)	All	OFF	6pF typ		
C_S or C_D (ON)	All	ON	20pF typ		
C_{SD}	All	OFF	1pF typ		
C_{SS} or C_{DD} Between Any Two Switches	All	ON	0.5pF typ		
POWER SUPPLY					
I_{DD}	All	ON	0.5μA max	8μA max	V_{DD} = +10V, V_{SS} = 0V, V_{IN} = +10V
I_{SS}	All	ON	0.5μA max	8μA max	
I_{DD}	All	OFF	0.5μA max	8μA max	V_{DD} = +10V, V_{SS} = 0V, V_{IN} = 0V
I_{SS}	All	OFF	0.5μA max	8μA max	

NOTES:
[1] J version specified for 0 to +75°C; S version specified for -55°C to +125°C.
[2] AC parameters are sample tested to ensure conformance to specifications.
[3] "t_{PD}" is analog input to output propagation delay.
Specifications subject to change without notice.

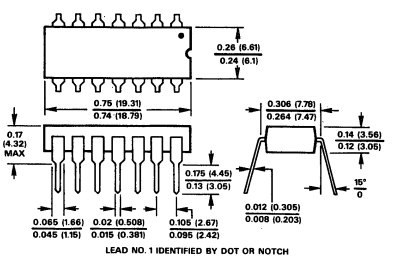
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

14-PIN CERAMIC DIP (SUFFIX D)



14-PIN PLASTIC DIP (SUFFIX N)

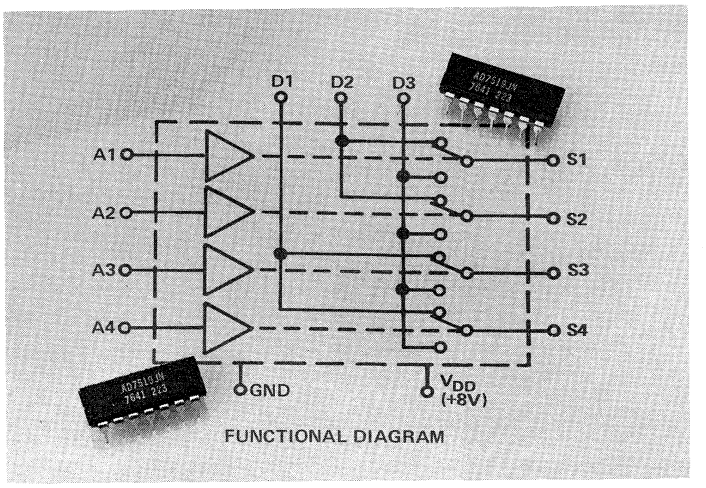


ANALOG DEVICES

CMOS Quad SPDT Steering Switch

AD7519

FEATURES
Low R_{ON}: 65Ω
Low Power Dissipation: 8.0μW
Fast Switching: 20ns
CMOS Compatible

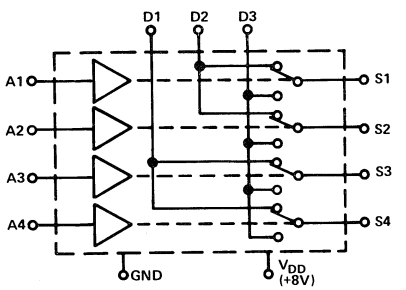


FUNCTIONAL DIAGRAM

GENERAL DESCRIPTION
The AD7519 consists of four SPDT switches which steer current to one of two buss lines that normally should be terminated at ground or the virtual ground of an operational amplifier. It operates from a single +7.5 to +10V supply with a quiescent power dissipation of only 8.0μW.

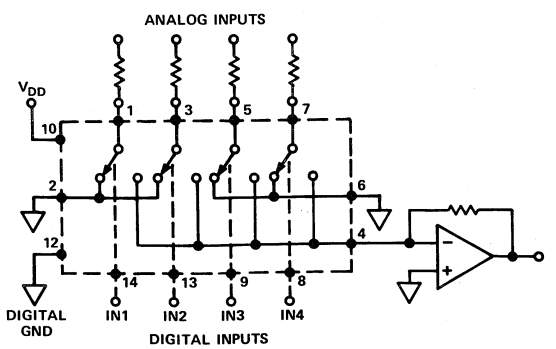
Typical AD7519 applications include fast settling D/A converters, variable gain amplifiers, and digitally controlled summing amplifiers.

FUNCTIONAL DIAGRAM



LOGIC
Switch "Makes" Terminal D-3 for Address "HIGH"

TYPICAL APPLICATION (SUMMING AMPLIFIER)

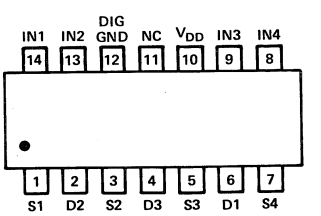


ABSOLUTE MAXIMUM RATINGS
(T_A = +25°C unless otherwise noted)

V_{DD} − GND . . . . . +12V
Digital Input Voltage . . . . . 0V to V_{DD}
Switch Current 5.0mA
Power Dissipation (Package)
14 pin Ceramic DIP
Up to +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C
14 pin Plastic DIP
Up to +70°C 670mW
Derates above +70°C by . . . . . 8.3mW/°C
Operating Temperature . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Switch Voltage
(pins 1, 3, 4, 5, 7) . . . . . -100mV to V_{DD}

CAUTION:
1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

PIN CONFIGURATION (Top View)



ORDERING INFORMATION

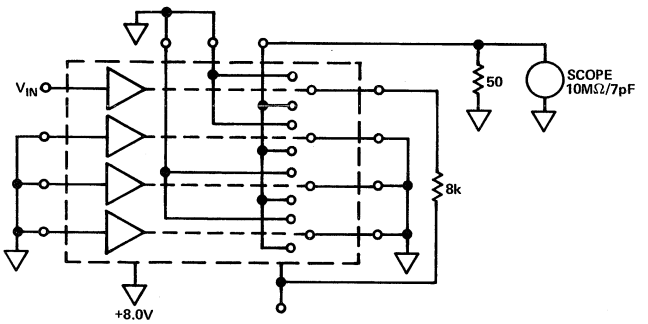
AD7519JN	0 to +75°C

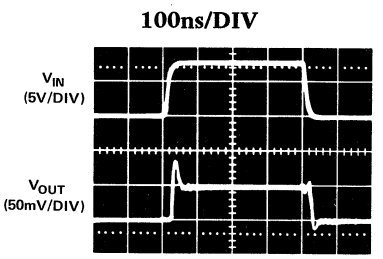
SPECIFICATIONS (V_{DD} = +8.0V, T_A = +25°C unless otherwise noted)

PARAMETER	SWITCH CONDITION	@ +25°C	TEST CONDITIONS
ANALOG SWITCH			
R_{ON}	ON	65Ω typ, 100Ω max	V_D 0V, I_{DS} = 1.0mA
R_{ON} vs. Temperature	ON	+0.5%/°C typ	I_{DS} = 1.0mA
ΔR_{ON} Between Switches	ON	5% typ	I_{DS} = 1.0mA
$I_{LEAKAGE}$ (Pin 4)	OFF	50nA typ	V_{IN} = 0V
DIGITAL CONTROL			
V_{INL}		0.4V max	
V_{INH}		7V min	
I_{INL} or I_{INH}		10nA typ	
C_{IN}		3pF typ	
DYNAMIC CHARACTERISTICS[1]			
t_{ON}		20ns typ	V_{IN} = 0 to V_{DD} & V_{DD} to 0
t_{OFF}		30ns typ	
C_{OUT}[2]	ON	55pF typ	V_{IN} = V_{DD}
	OFF	15pF typ	V_{IN} = 0V
POWER SUPPLY			
I_{DD}		1μA typ	V_{IN} = 0 or V_{DD}

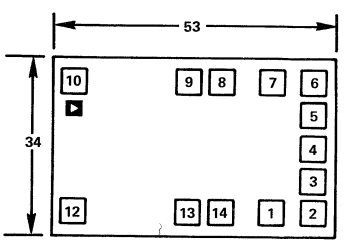
NOTES:
[1] AC parameters are sample tested to ensure conformance to specifications.
[2] Pin 4 to GND.
Specifications subject to change without notice.

TYPICAL SWITCHING CHARACTERISTICS





BONDING DIAGRAM



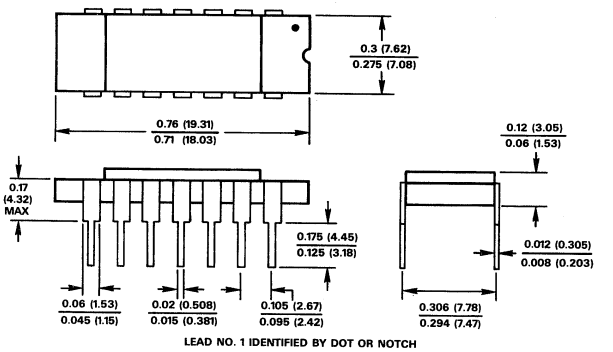
All bonding pads are 4 x 4 MIL.
All pad numbers correspond with DIP package pin configuration.

MECHANICAL INFORMATION

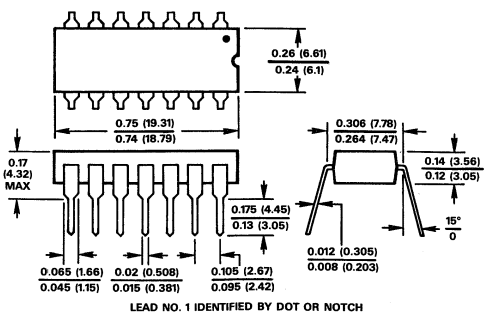
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-PIN CERAMIC DIP (SUFFIX D)



14-PIN PLASTIC DIP (SUFFIX N)



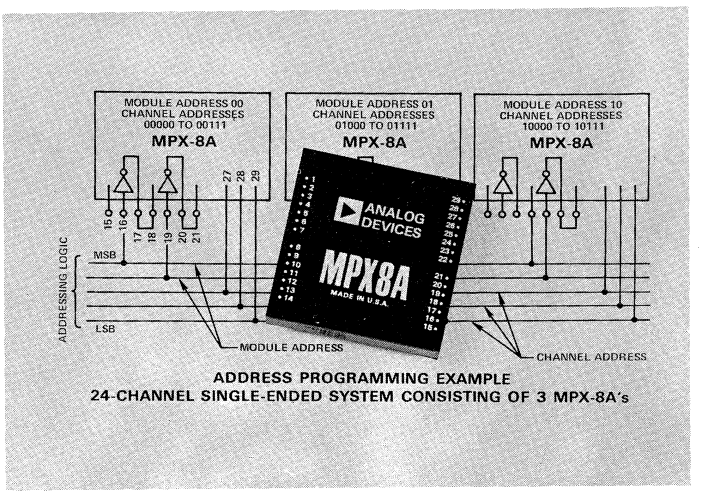
ANALOG DEVICES

High Speed 8 Channel Multiplexer

MPX-8A

FEATURES
8-Channel Single-Ended or 4-Channel Differential
MOSFET Switches
DTL/TTL Compatible
Binary Address Selection
±10V Range with ±15V Power
±15V Max Allowable Input
Crosstalk -80dB
Settling Time $< 2\mu s$ to 0.01%

APPLICATIONS
Data Acquisition
Data Distribution
Independent Switching



ADDRESS PROGRAMMING EXAMPLE
24-CHANNEL SINGLE-ENDED SYSTEM CONSISTING OF 3 MPX-8A's

GENERAL DESCRIPTION

The MPX-8A is a complete 8-channel high-speed MOSFET multiplexer packaged in a small encapsulated module; it is compatible both in package and electrical input/output characteristics with other Analog Devices hybrid interface products such as sample-and-hold, and analog-to-digital and digital-to-analog converters. The MPX-8A was designed for applications requiring high accuracy, high throughput rates, and minimal crosstalk.

ADDRESS SELECTION LOGIC

The TTL compatible binary address selection logic has all the needed logic elements required to expand the multiplexer to 64 signal channels, whether each channel is single-ended or differential. Mode control, programmed by the user with a jumper at the module terminals, determines whether each MPX-8A module operates as an 8-channel single-ended switch or a 4-channel differential switch.

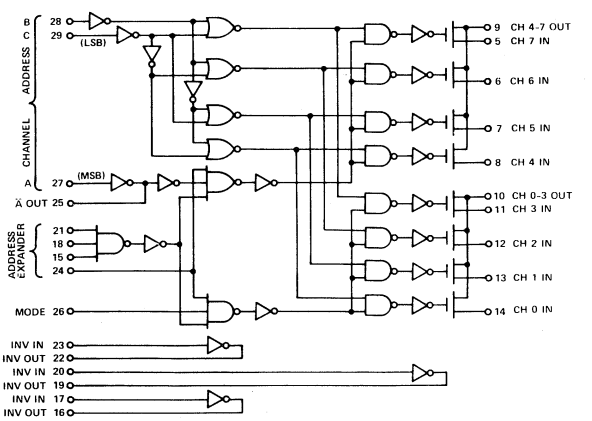
Unlike many other MOSFET multiplexers currently available, the MPX-8A settles at very high speed regardless of the input slewing direction. In most cases, system throughput rate will be limited by associated equipment, since the "worst case" switching time is $2\mu s$. Optimum case switching time is 300–400ns.

BENEFITS OF ADVANCED DESIGN

The MPX-8A is unique in providing the advantages of MOSFET switching over a signal range of ±10V with power supply of only ±15V. Being a unipolar device, the MOSFET switch contributes no offset voltage to the signal being processed. Advanced guarding techniques minimize switch capacitance, minimize crosstalk, and optimize switching speed. Since the MOSFET requires gate excitation to turn on, the MPX-8A turns off all switches upon removal of power, thus guarding active signal sources against damage by inadvertent turn on of more than one channel. The binary address control guards against inadvertent turn-on of more than one channel at a time, further protecting active signal sources from damage.

IMPEDANCE AND ACCURACY CONSIDERATIONS

Since the MPX-8A is a switch with ultra-high insulation resistance, the resistive component of input impedance and the effective transfer error are really determined by the characteristics of the following buffer amplifier. When followed by a high quality fast buffer, such as Analog Devices model 45, input impedance will be on the order of $10^{10}\Omega$ and transfer accuracy will be better than 0.01%.

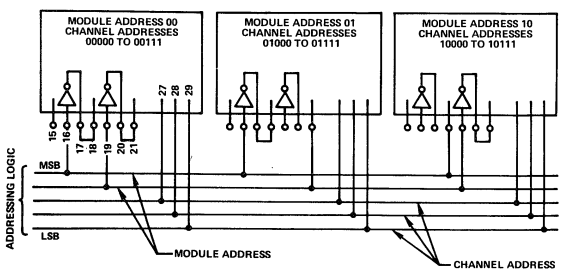


Block Diagram – MPX-8A

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODEL	MPX-8A
CHANNELS	8 Single-Ended, or 4 Differential (programmable by user)
VOLTAGE RANGE	
Normal Operating	−10V to +10V
Overvoltage Protection	−15V to +15V
CROSSTALK	<−80dB
TRANSFER ACCURACY	Determined by following amplifier Values to <0.01% readily attainable
INPUT IMPEDANCE	Determined by following amplifier Values to $10^{10}\Omega$ readily attainable
COMMON MODE REJECTION	Determined by following amplifier Values to 120dB available
ANALOG SWITCHES	MOSFET transistors
SWITCH CHARACTERISTICS (Each Channel)	
ON Resistance	1000Ω
OFF Resistance	1000MΩ, min
Input Capacitance	10pF
Leakage Capacitance (OFF Channels)	<3pF
ON Input Leakage Current	
@ +25°C	10nA, max
@ +70°C	100nA, max
Settling Time to 0.01% +10V to −10V	<2μs
THROUGHPUT RATE	Rates to 500kHz. Practical high limit is determined by accessory equipment, as well as nature of signals
FAULT PROTECTION	1. Binary address selection makes it impossible to select more than one channel at a time 2. MOSFET switches return to "OFF" state whenever power is lost or removed
ADDRESS CONTROL	
Code	Binary
Logic	TTL/DTL Compatible
"1"	E>+2.4V @ +40μA, or Open Circuit
"0"	E<+0.8V @ −1.6mA
Channel Address	3-bit Binary Code turns on one of 8 Switches
Mode Control	Jumper at module terminals determines whether module operates as 8-channel single-ended, or 4-channel differential switch
Address Extender (4 input AND gate)	All Inputs at Logic "1" enable module addressing. Provides for system expansion to 64 channels, either single-ended or differential
Logic Inverters (3, uncommitted)	Provide all logic elements required for full expansion of system
Module Disable	A Logic "0" at any input of extender gate opens all switches in module
POWER	+15V ±1V @ 6.2mA +0V @ 4mA +5V ±10% @ 102mA
TEMPERATURE	
Operating	0 to +70°C
Storage	−65°C to +150°C
SIZE	2" x 2" x 0.4" Module

Specifications subject to change without notice.



ADDRESS PROGRAMMING EXAMPLE
24-Channel Single-Ended System
Consisting of 3 MPX-8A's

INSTRUCTIONS FOR ADDRESSING

SWITCH ADDRESS SELECTION IN A MODULE

Desired switch address is the switch channel number (0–7); the 3 bit binary code is applied to module pins 27, 28 and 29. Pin 27 is the MSB.

SINGLE-ENDED OR DIFFERENTIAL OPERATION

Jumpering to pin 26 (MODE or "pairing" control determines the operating mode.)

a) For 8-channel single-ended operation, jumper pin 26 to pin 25. ("$\overline{A}$" connects to mode control)
b) For 4-channel differential operation, jumper pin 26 to pin 27. ("A" connects to mode control)

SYSTEM EXPANSION

All logic elements are provided in each MPX-8A module to allow system expansion to 64 channels (each channel either differential or single-ended), which would involve use of 8 MPX-8A modules (for 64-channel single-ended) or 16 MPX-8A modules (for 64-channel differential).

On each module, pins 15, 18, 21 and 24 are effectively 4 inputs to an AND gate, and Logic "1" must be presented to each in order to enable the module for switch opening. Since open circuit at each input acts as a Logic "1", unneeded gate inputs need only be left unconnected to allow use of the module. Thus, a single module used as an 8-channel single-ended switch needs no connections to the expander gate. Note, however, that any one of the expander gate inputs can be used to open ALL switches in a module, by applying a Logic "0".

EXAMPLE OF EXPANDED SYSTEM WIRING

In the figure entitled "Address Programming Example," we see the address wiring for a 24-channel single-ended system, consisting of 3 MPX-8As. A 5-bit addressing code is required, and would actually suffice for further expansion to 32-channels.

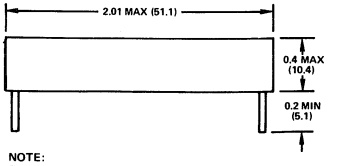
The 3 bits of channel address logic are wired to all 3 MPX-8As in parallel, to pins 27, 28 and 29 (MSB to pin 27, LSB to pin 29). The proper addressing of one of the three MPX-8As via connections to the extender AND gate (via inverters, where necessary) is required to determine which of the 3 modules is enabled.

When module address code is 00, module 00 must be enabled. Since "1" must be presented to the expander gate inputs, the 2 bits of module address code must be fed to the gate inputs through inverters. Note that the inverters are conveniently connected to pin numbers between the extender gate inputs, to simplify the locating of jumpers.

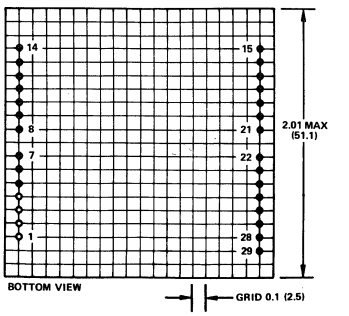
In like manner, the module address code lines going to modules 01 and 10 require use of one inverter each for addressing 01, the inverter is located in the MSB line; for addressing 10, the inverter is located in the 2nd MSB line.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hole locations.
All pins are gold plated half-hard brass, (MIL-G-45 204), 0.019" ±0.001" (0.48 ±0.03mm) dia.



Computer Interface Products

Selection Guide
Computer Interface Products

Type	Model	Description	Page
Data Acquisition Subsystem	DAS1128	General-purpose 12-bit data-acquisition module. Accepts 8 differential or 16-single-ended inputs, performs multiplexing, sample-hold, and A/D conversion, with maximum throughput rate of 35kHz. Can be readily interfaced with microcomputer systems, via 8255 or PIA.	565
Real-Time Interface	RTI-1200	Analog/Microcomputer Interface System. A complete ready-to-use analog I/O subsystem designed for physical, electrical, and software compatibility with the SBC-80/10 Single-Board Computer — and easy interfacing with any other 8080-based microcomputer having accessible address-, data-, and control buses. Interfaces as a block of memory addresses.	573
	RTI-1201	Analog Output Subsystem with four 12-bit DAC's. Compatible with Intel SBC-80, MDS — and the RTI-1200. Includes many of the same features as the RTI-1200, and also includes DAC readback capability.	577
	RTI-1220	Analog/Microcomputer Input Subsystem for Pro-Log microcomputers. Many of the same features as the RTI-1200.	581
	RTI-1221	Analog Output Subsystem with up to four 12-bit DAC's for Pro-Log and other 8080 or 6800 based microcomputers.	581
	RTI-1240	12-Bit Analog Input Subsystem. A complete ready-to-use analog input subsystem designed for physical, electrical, and software compatibility with TM-990/100M 16-bit microcomputers. Interfaces as a block of memory addresses.	585
	RTI-1241	12-Bit Analog Input/Output Subsystem. Similar to RTI-1240, but includes two 12-bit digital-to-analog converters.	585
	RTI-1242	Analog Output Subsystem with four 12-bit DAC's, designed for full compatibility with TM-990/100M 16-bit microcomputers. Includes eight channels of software-controlled high-power one-bit *digital* output for on-off control functions.	585
	RTI-1243	Analog Output Subsystem with eight 12-bit DAC's. Otherwise similar to the RTI-1242.	585
SERial Data-EXchange (SERDEX)	STX2603 Card STX1003 Module	Serial Transmitter Card/Module. Translates parallel digital data to asynchronous serial to permit communication between ADC's or other analog- or digital-input devices and systems employing two-wire ASCII communication. Incoming control signal can initiate conversion and ASCII-coded readback, and/or other on-off control functions STX2603 complete card STX1003 basic module	599 599
	SRX2605 Card SRX1005 Module	Serial Receiver Card/Module. Translates ASCII digital data to parallel digital output to permit communication with remote DAC's or other analog- or digital-output devices. Incoming control signals can strobe digital readout and/or other on-off control functions. SRX2605 complete card SRX1005 basic module	599 599
	SMX2607 Card SMX1004—SMC1007 Modules	Serial Multiplexer Card/Modules. Stackable multiplexers route ASCII data and control signals to remote transmitters, receivers, and multiplexers in 8-channel increments. SMX2607 complete card SMX1004-SMC1007 basic module-pair	599 599

Low Cost, High Speed Data Acquisition Module

DAS1128

FEATURES

- Complete Data Acquisition System
- 12 Bit Digital Output
- 16 Single or 8 Differential Analog Inputs
- High Throughput Rate
- Selectable Analog Input Ranges
- Versatile Input/Output/Control Format
- Low 3 Watt Power Dissipation
- Small 3" x 4.6" x 0.375" Module

GENERAL DESCRIPTION

The DAS1128 is a complete self-contained miniature high speed data acquisition system. The compact 3" x 4.6" x 0.375" module provides the designer with an easily implemented solution to the data acquisition problem. It contains an analog input signal multiplexer, a sample-and-hold amplifier, a 12 bit A/D converter, and all of the programming, timing and control circuitry needed to perform the complete data acquisition function.

The DAS1128 is a high performance device which can digitize an analog signal to an accuracy of ±½LSB out of 12 bits, relative to full scale. It has ±8ppm/°C gain temperature coefficient, and the maximum throughput rate can be varied from 50,000 conversions/second for a 12 bit conversion from different analog input channels, to 200,000 conversions/second for a successive 4 bit conversion made on a single channel.

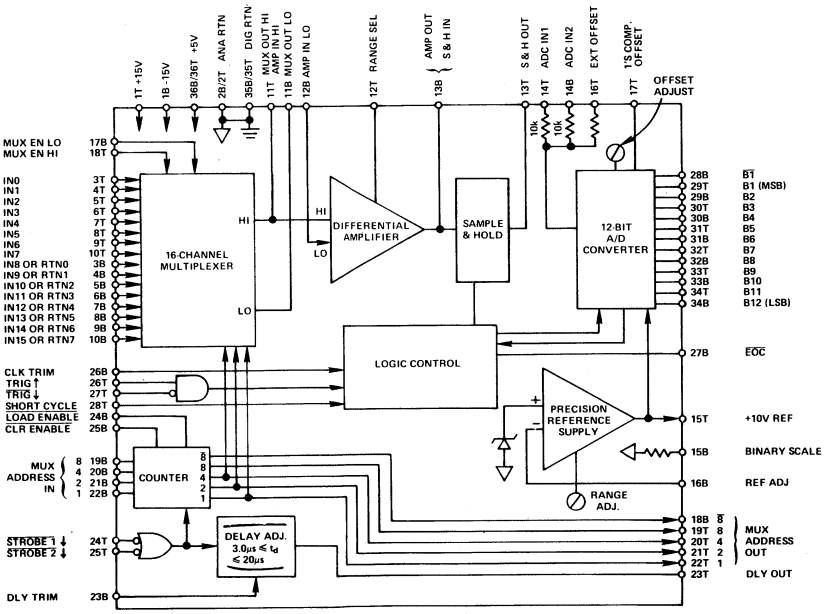


Figure 1. Functional Block Diagram

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

ANALOG INPUTS

Number of Inputs to Multiplexer	16 Single Ended, 8 True-Differential, 16 Pseudo-Differential
Input Voltage (Full Scale Range)	-10V to +10V, 0V to +10V, -5V to +5V, 0V to +5V, -10.24V to +10.24V, 0V to +10.24V, -5.12V to +5.12V, or 0V to +5.12V.
Maximum Input Voltage	±15V
Input Current (per channel)	5nA max
Input Impedance	$>10^{10}$ ohms
Input Capacitance	10pF for "OFF" channel 100pF for "ON" channel
Input Fault Current (power off or MUX failure)	Internally limited to 20mA
Direct ADC Input Impedance	10kΩ for each input line

ACCURACY[1]

Resolution	12 Bits
Error Relative to F.S.	±½LSB
Quantization Error	±½LSB
Differential Nonlinearity Error	
@ 33kHz throughput rate	±½LSB, 1LSB max
@ 50kHz throughput rate	±1LSB
Noise Error	±¼LSB
-FS to +FS Error Between Successive Channel Transitions	±1LSB

TEMP. COEFFICIENTS

Gain	8ppm/°C, 20ppm/°C max
Offset	5ppm/°C, 15ppm/°C max
Differential Nonlinearity	2.5ppm/°C, 6ppm/°C max

SIGNAL DYNAMICS

Throughput Rate (12 Bits)	50kHz (max) (includes 5μs for MUX and SHA settling time plus 15μs for ADC)
MUX Crosstalk ("OFF" channels to "ON" channel)	>80dB down @ 1kHz
Differential Amplifier CMRR	70dB to 1kHz
SHA Acquisition Time to 0.01%	4.5μs max
SHA Aperture Uncertainty	10ns
SHA Feedthrough	70dB down @ 1kHz

DIGITAL INPUT SIGNALS

Compatibility	Standard DTL/TTL logic levels, 1 unit load/line
MUX Address Inputs (8, 4, 2, 1; Pins 19B through 22B)	Positive true natural binary coding selects channel for random addressing mode. Must be stable for 100ns after $\overline{\text{STROBE}}$.
MUX ENABLE HI (Pin 18T)	High (Logic "1") input enables MUX "HI" output (for inputs 0 through 7)
MUX ENABLE LO (Pin 17B)	High (Logic "1") input enables MUX "LO" output (for inputs 8 through 15)
$\overline{\text{STROBE}}$ (Pin 24T or 25T)	Negative going transition (Logic "1" to Logic "0") updates MUX address register. $\overline{\text{STROBE}}$ 1 must be a Logic "1" to enable $\overline{\text{STROBE}}$ 2. $\overline{\text{STROBE}}$ 2 must be at Logic "1" to enable $\overline{\text{STROBE}}$ 1.
$\overline{\text{LOAD ENABLE}}$ (Pin 24B)	High (Logic "1") input allows next $\overline{\text{STROBE}}$ command to sequentially advance MUX address register. Low (Logic "0") input allows next $\overline{\text{STROBE}}$ command to update MUX address register according to external address inputs.
$\overline{\text{CLEAR ENABLE}}$ (Pin 25B)	Low (Logic "0") input allows next $\overline{\text{STROBE}}$ command to reset MUX address to channel "0" overriding $\overline{\text{LOAD ENABLE}}$.
TRIGGER (Pin 26T)	Positive going transition (Logic "0" to Logic "1") initiates A/D conversion (even during conversion); $\overline{\text{TRIGGER}}$ (Pin 27T) must be at Logic "0" to allow TRIGGER function.
$\overline{\text{TRIGGER}}$ (Pin 27T)	Negative going transition (Logic "1" to Logic "0") initiates A/D conversion; Pin 26T (TRIGGER) must be at Logic "1" to allow $\overline{\text{TRIGGER}}$ function.

DIGITAL OUTPUT SIGNALS

Compatibility	Standard DTL/TTL logic levels; 5 unit loads/line.
Parallel Outputs	$\overline{\text{B1}}$, B1 through B12
Coding	Natural binary, two's complement, offset binary, or one's complement. Pin selectable.
MUX Address Outputs ($\overline{8}$, 8, 4, 2, $\overline{1}$; pins 18B, 19T through 22T)	Positive true natural binary coding indicates channel selected.
DELAY OUT (Pin 23T)	Negative going transition (Logic "1" to Logic "0") occurring normally 5μs (adjustable from 3.0μs to 20μs) after $\overline{\text{STROBE}}$ command initiates A/D conversion automatically when connected to the $\overline{\text{TRIGGER}}$.
$\overline{\text{EOC}}$ (Pin 27B)	High (Logic "1") output during A/D conversion.

ADJUSTMENTS & TRIMS

Offset Adjust	
Internal Adjustment (Externally Accessible)	±10LSB's (min)
Remote External Adjustment (Pin 16T)	±10LSB's (min)
Range Adjust	
Internal Adjustment (Externally Accessible)	±10LSB's (min)
Remote External Adjustment (Pin 16B)	±10LSB's (min)
Clock Trim (Pin 26B)	
Factory Setting (Pin 26B "OPEN")	1.25μs/Bit
External Adjustment Range	1.25μs/Bit to 2.08μs/Bit
Delay Trim (Pin 23B)	
Factory Setting (Pin 23B "OPEN")	3.0μs
External Adjustment Range	3.0μs to 20μs

CONTROLS

SHORT CYCLE (Pin 28T)	Connect to ground for full 12 bit resolution. Connect to B_n output for resolution to B_{n-1} bits.
Channel Selection Mode (MUX Address Loading Mode)	Random, sequential continuous, and sequential triggered. Pin selectable.
A-D Conversion/Channel-Select Sequences	Normal (input channel remains selected during its A/D conversion) and overlap (next channel selected during A/D conversion). Pin selectable.
Range Select (Pin 12T)	Differential Amplifier gain control: connect to ANA RTN (Pin 2T) for X1 gain; connect to AMP OUT (Pin 13B) for X2 gain. This control is used in FSR selection procedure.
BINARY SCALE (Pin 15B)	Connect to REF ADJ (Pin 16B) to set reference to 10.24V. This control is used in FSR selection procedure, see Table II.
OUTPUT CODING (Pin 17T)	Ground for 1's complement output code; connect to -15V dc for other available codes.

POWER REQUIREMENTS

+15V ±3%	40mA, 50mA max
-15V ±3%	70mA, 100mA max
+5V ±5%	250mA, 500mA max
Power Supply Sensitivity[2]:	
Gain	±2.0mV/V
Offset	±4.0mV/V
Ref	±0.5mV/V

ENVIRONMENT & PHYSICAL

Operating Temperature	0 to +70°C
Storage Temperature	-25°C to +85°C
Relative Humidity	Up to 95% non-condensing
Electrical Shielding	RFI & EMI 6 sides (except connector area)
Packaging	Insulated steel cased module 3.00" x 4.60" x 0.375"

[1] Warmup time to rated accuracy is 5 minutes.
[2] Specification applies only when tracking +15V and -15V supplies are used, and for slowly occuring variations in power supply voltages.

Specifications subject to change without notice.

THEORY OF OPERATION

A block diagram of the DAS1128 is shown in Figure 1. Analog input signals are applied to the various inputs of the 16 channel CMOS multiplexer. This multiplexer in conjunction with the differential amplifier that follows it, can be configured by the user to accept 16 single ended analog inputs, or 8 fully differential analog inputs. It can also be connected as a 16 channel "pseudo-differential" input device, which permits some of the benefits of differential operation while maintaining a 16 channel input capability.

The differential buffer amplifier is gain programmable by the user via jumpers at the module pins. This feature, along with the selectable reference voltages, permits the user to set up the DAS1128 to operate on any of 8 input voltage ranges. The differential amplifier drives a sample-and-hold amplifier, whose function it is to hold the selected analog input signal at a constant level while the A/D converter is making a conversion.

The A/D converter is a high speed 12 bit successive approximation device that has been designed using the Analog Devices' AD562, 12 bit integrated circuit D/A. The reference voltage for the conversion is supplied by an adjustable precision reference circuit that has a temperature coefficient of 5ppm/°C.

In addition to these basic functional blocks, the DAS1128 also contains all of the clock circuitry necessary to perform the complete data acquisition function. The internal clock can be externally adjusted to provide various throughput rates at different accuracies. Input channel addressing logic is provided, as is the capability to short cycle the A/D converter (i.e. perform conversions of less than 12 bits resolution). It is also possible for the user to adjust the time interval between input channel selection and the commencement of a conversion. The user can thus trade off speed vs. accuracy in the settling time of the multiplexer and sample-and-hold amplifier, as well as speed versus accuracy of the A/D converter.

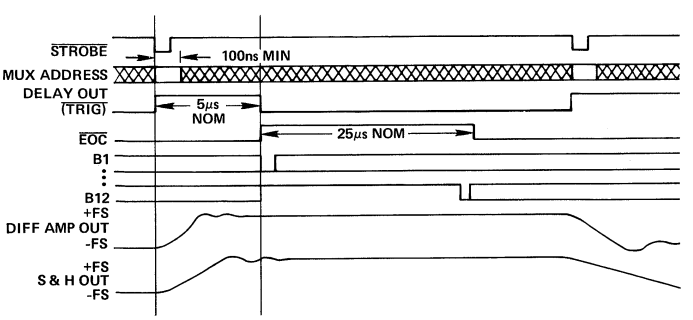


Figure 2. Simplified Timing Diagram, Showing Time-Interval Assignments and Constants

INPUT CONNECTIONS

As shown in Figure 3, three input configurations can be used. 16 single-ended inputs (3a) can be connected to the multiplexer, all referenced to analog gnd. In the second configuration (3b), the inputs are connected individually as 8 true differential pairs. In this case the differential amplifier is connected "Differentially" with the output of the MUX. Finally, a "Quasi-Differential" connection (3c) can be realized under favorable ground path conditions. In this configuration the differential amplifier Lo terminal is used as the ground return for all sensors. In each of these input schemes, it should be noted that the input multiplexer has been designed to protect itself and signal sources from both overvoltage failure and from fault currents due to power-off loading or MUX failure.

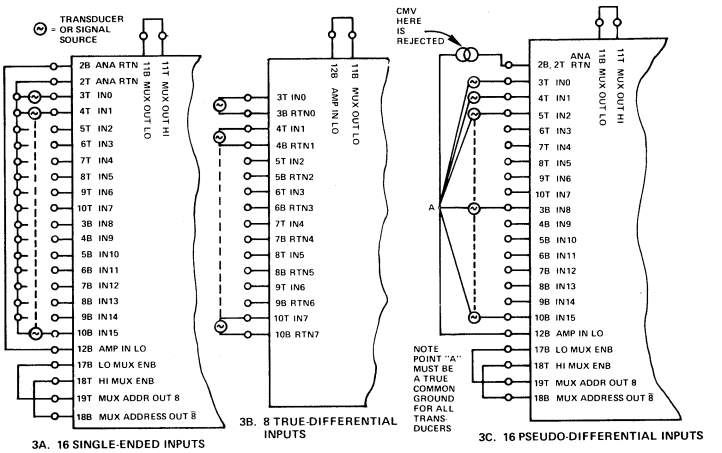


Figure 3. Signal Input Connections for Three Different Configurations

Full scale range of the DAS1128 may be set by appropriate jumper connections for 8 different ranges: 0 to +10V; 0 to +5V; 0 to +10.24V; 0 to +5.12V; -10 to +10V; -5 to +5V; -10.24 to +10.24V; -5.12 to +5.12V.

Note that 10.24 and 5.12 ranges are commonly used since conversion increments become 5mV/bit, 2.5mV/bit, and 1.25mV/bit.

MUX AND S/H DYNAMICS – OVERLAP MODE

The overlap mode is defined as the ability of MUX to accept a new channel address thereby selecting the next channel to be sampled while the previously acquired sample is being held by the S/H for conversion. The dynamic characteristics of the S/H circuit are shown in Figure 4. Maximum throughput rates are obtainable when a single channel is held at a single address and the channel is sampled repeatedly. In a dynamic condition, data-throughput rates obtainable are shown in Figure 5.

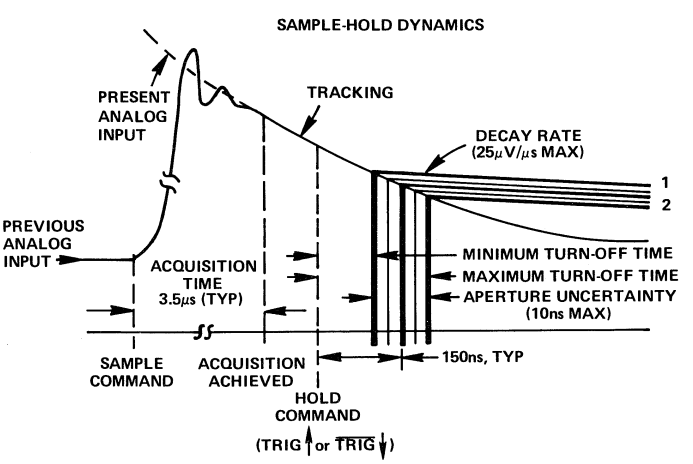


Figure 4. Sample-Hold Parameters Defined and Specified

SHORT CYCLE

It is possible to short cycle the DAC1128, i.e., stop the conversion after less than 12 bits. This can be done by connecting an external jumper between short cycle terminal and one of the output terminals. With shorter cycles the attainable throughput rate increases, see Figure 5. In short cycle operation the $\overline{EOC}$ will decrease proportionately to the number of bits selected. Note the short cycle terminal *must* be grounded for full 12-bit operation.

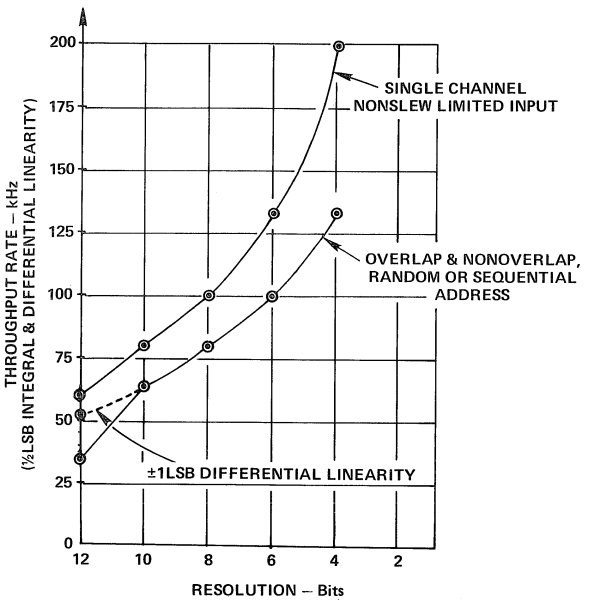
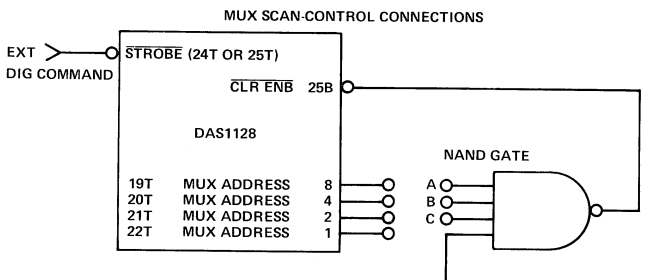


Figure 5. DAS1128 Throughput Rates

MUX ADDRESSING

External terminals have been provided for the address counter. Thus the address counter can be configured to produce the following modes: Continuous sequential scanning (free running), sequential scanning with external step command, abbreviated scan continuously, random channel selection. See Figure 6 and set up procedure for details.



LAST CHANNEL	MUX ADDRESS 8	4	2	1	DIG. GROUND
1	X	X	X	A	X
2	X	X	B	X	X
3	X	X	B	A	X
4	X	C	X	X	X
5	X	C	X	A	X
6	X	C	B	X	X
7	X	C	B	A	X
8	C	X	X	X	X
9	C	X	X	A	X
10	C	X	B	X	X
11	C	X	B	A	X
12	B	C	X	X	X
13	B	C	X	A	X
14	A	C	B	X	X
15	X	X	X	X	A

X = NO CONNECTION

IF $\overline{LOAD\ ENB}$ IS ALSO USED, CONNECT THIS INPUT TO IT (TO 24B). THIS GIVES LOADING PREFERENCE OVER CLEARING.

NOTE: FOR INITIAL CHANNEL = M, CONNECT GATE OUTPUT TO $\overline{LOAD\ ENB}$ (24B) AND CODE CHANNEL IN 8, 4, 2, 1 TO ADDRESS M. HOWEVER, THIS PRECLUDES RANDOM ADDRESSING.

Figure 6. To shorten scanning sequency of multiplexer channels, make the appropriate connections, (as shown in the chart) between an external NAND gate and MUX ADDRESS terminals 19T to 21T

GROUNDING CONSIDERATIONS

Attention should be given to the methods of connection for electrical returns and voltage reference points. Analog return (ANA RTN) and digital return (DIG RTN) are provided. The following rules should be applied when integrating the DAS112[illegible] into the system.

1. If the ±15V power supply is floating (for optimum analog accuracy), connect its return to ANA RTN (Pin 2B or 2T). If the ±15V power supply is *not* floating, connect its return to DIG RTN (Pin 35T or 35B).
2. Connect the +5V supply return to DIG RTN (Pin 35T or 35B). If this supply also powers additional equipment, run separate, parallel returns to the equipment ground and to DIG RTN (Pin 35T or 35B).
3. To minimize signal grounding problems, single-ended input signals should only be returned to ANA RTN (Pin 2B or 2T). If this is not possible, then connect the input signals in either the "true differential" or "pseudo-differential" configurations (see Figure 3).
4. Connect computer ground to DIG RTN (Pin 35T or 35B). Use heavy wire or ground planes.
5. The computer chassis should be connected to the computer and power supply grounds at only one point.
6. Connect the third-wire ground from main ac power input to the computer power supply return.

GAIN AND OFFSET ADJUSTMENTS

The DAS1128 is calibrated with external gain and offset adjustment potentiometers connected as shown in Figure 7 and 8. The offset adjustment potentiometer has an adjustment range of at least ±10LSB's, and the gain range adjustment potentiometer has an adjustment range of at least ±10LSB's.

Offset calibration is not affected by changes in gain calibration, and should therefore be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable. It should be capable of being set to within ±1/10LSB of the desired value at any point within its range.

These adjustments are not made with zero and full scale input signals, and it may be helpful to understand why. An A/D converter will produce a given digital word output for a small range of input signals, the nominal width of the range being one LSB. If the input test signal is set to a value which should cause the converter to be on the verge of switching between two adjacent digital outputs, the unit can be calibrated so that it does switch at just that point. With a high speed convert command rate and a visual display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices *Analog-Digital Conversion Notes* gives more detailed information on testing and calibrating A/D converters.

OFFSET CALIBRATION

For unipolar +10V operation set the input voltage precisely to +0.0012V and adjust the offset potentiometer until the converter is just on the verge of switching from 000000000000 to 000000000001.

For ±5V bipolar operation set the input voltage precisely to -4.9988V; for ±10V units set it to -9.9976V. Adjust the offset

potentiometer, Figure 7, until Offset Binary coded units are just on the verge of switching from 000000000000 to 000000000001 and Two's Complement coded units are just on the verge of switching 100000000000 to 100000000001.

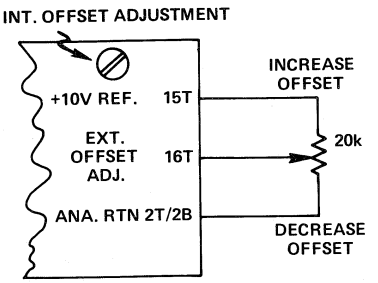


Figure 7. Ext. Offset Adjustment

GAIN CALIBRATION

Set the input voltage precisely to +9.9963V for unipolar operation, +4.9963V for inputs of ±5V or +9.9926V for inputs of ±10V. Note that these values are 1½LSB's less than nominal full scale. Adjust the 20k variable gain resistor, Figure 8, until Binary and Offset Binary coded units are just on the verge of switching from 111111111110 to 111111111111 and Two's Complement coded units are just on the verge of switching from 011111111110 to 011111111111.

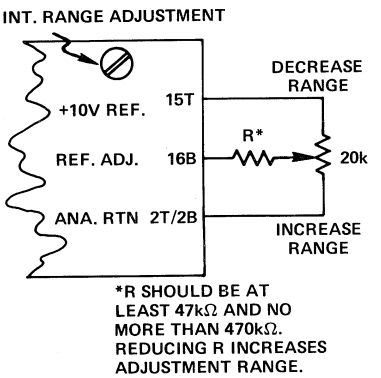


Figure 8. Ext. Ref. Adjustment

CLOCK RATE ADJUSTMENT

The clock rate may be adjusted for best conversion time/accuracy trade-off. The conversion time is varied by means of the external circuitry shown in Figure 9. An open CLK TRIM terminal (Pin 26B) results in 1.25μs/bit nominal conversion time. A grounded CLK TRIM terminal (for highest accuracy) results in 2.08μs/bit conversion.

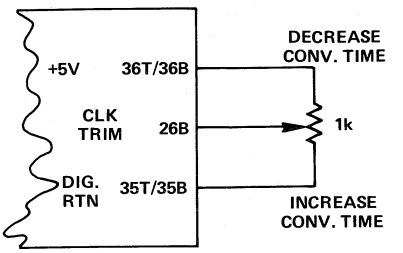


Figure 9. Clock Trim

DELAY TIME ADJUSTMENT

The DLY OUT signal may be adjusted to vary the A/D converter triggering time by means of the external circuitry shown in Figure 10. An open DLY TRIM terminal (Pin 23B) results in a nominal delay time of 3.0μs. A grounded DLY TRIM terminal (for highest-accuracy) results in 20μs delay time nominal.

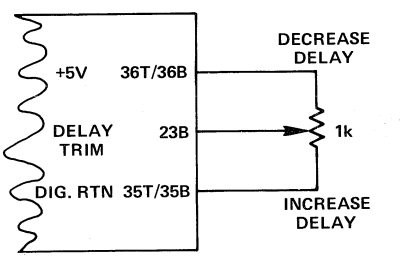


Figure 10. Delay Trim

TABLE I

INPUT CONFIGURATION	ANALOG INPUT CONNECTIONS	ANALOG INPUT RETURN	JUMPER CONNECTIONS
16 Single-Ended Inputs (Figure 3a)	3T thru 10T and 3B thru 10B	All input returns to 2B or 2T	11B to 11T 12B to 2B or 2T 17B to 19T 18T to 18B
8 Differential Inputs (Figure 3b)	3T thru 10T	3B thru 10B	11B to 12B 17B to 18T to "1"
16 Pseudo-Differential Inputs (Figure 3c)	3T thru 10T and 3B thru 10B	Common Input return to 12B	11B to 11T 17B to 19T 18T to 18B

RECOMMENDED SET-UP PROCEDURE

1. Select input configuration, see Table I.
2. Select MUX address mode.
   The method of addressing the multiplexer can be selected by connecting the unit as follows:

   RANDOM. Set Pin 24B ($\overline{\text{LOAD ENB}}$) to Logic "0". The next falling edge of $\overline{\text{STROBE}}$ will load the address presented to Pins 19B through 22B (8, 4, 2, 1). The code on these lines must be stable during the falling edge of $\overline{\text{STROBE}}$ plus 100ns.

   SEQUENTIAL FREE RUNNING. Set to Logic "1", Pin 24B ($\overline{\text{LOAD ENB}}$) and 25B ($\overline{\text{CLR ENB}}$). Connect Pin 27B ($\overline{\text{EOC}}$) to Pin 24T ($\overline{\text{STROBE 1}}$). Connect Pin 23T (DLY OUT) to Pin 27T ($\overline{\text{TRIG}}$). Use Pin 26T ($\overline{\text{TRIG}}$) as a run/stop control (i.e., A/D conversion will continue while TRIG is high and will stop while TRIG is low).

   SEQUENTIAL TRIGGERED. Set to Logic "1", Pins 24B ($\overline{\text{LOAD ENB}}$) and 25B ($\overline{\text{CLR ENB}}$). Connect Pin 24T ($\overline{\text{STROBE}}$) to external triggering source. The multiplexer address register will automatically advance by one channel whenever a $\overline{\text{STROBE}}$ command is received. The initial channel can be selected by setting Pin 24B ($\overline{\text{LOAD ENB}}$) to Logic "0" during only one $\overline{\text{STROBE}}$ command. The multiplexer address will then be determined by the logic levels on Pins 19B through 22B (the external MUX address lines). Channel "0" can be selected as the initial channel by setting Pin 25B ($\overline{\text{CLR ENB}}$) to Logic "0" during only one $\overline{\text{STROBE}}$ command. The final channel can be selected by following the procedure presented in Figure 6.
3. Select A-D conversion/channel select sequence (see Figure 5).
   (1) NORMAL (input channel remains selected during its A/D conversion). Connect Pin 23T (DLY OUT) to Pin 27T ($\overline{\text{TRIG}}$).
   (2) OVERLAP (next channel is selected during A/D conversion). Connect Pin 27B ($\overline{\text{EOC}}$) to TTL compatible inverter input. Connect inverter output to Pin 24T ($\overline{\text{STROBE}}$). Connect Pin 23T (DLY OUT) to Pin 27T ($\overline{\text{TRIG}}$). Adjust the delay to at least 4μs greater than $\overline{\text{EOC}}$, 20μs max (see Figure 10). The signal on Pin 26T (TRIG) serves as RUN/STOP control.
   (3) REPETITIVE SINGLE CHANNEL. After selecting the input channel to be repetitively sampled (see MUX ADDRESS MODE, above), set Pin 27T ($\overline{\text{TRIG}}$) to Logic "0". Connect Pin 26T (TRIG) to a triggering source. Conversion process is initiated by positive edge of TRIG command.
4. Select output resolution.
   a. Full 12 bit resolution: connect Pin 28T (SHT CYC) to Pin 35B (DIG RTN).
   b. Bn (Bn $<$ 12) bit resolution: connect Pin 28T to the output pin for Bn + 1.
5. Select optimum throughput rate.
   The system clock frequency and the STROBE to TRIG delay (if used) can be trimmed to optimize the accuracy/throughput rate trade-off. See Figures 9 and 10.
6. Select input voltage full scale range. See Table II.
7. Select output digital coding. See Table III.

TABLE II

FOR FULL SCALE RANGE OF:	MAKE THE FOLLOWING CONNECTIONS
0 to +10V	12T to 2T; 14T to 14B to ADC Source*.
0 to +10.24V	same as 0 to +10V, *plus* 15B to 16B.
0 to +5V	12T to 13B; 14T and 14B to ADC Source
0 to +5.12V	same as 0 to +5V, *plus* 15B to 16B
-10V to +10V	12T to 2T; 14T to 15T; and 14B to ADC Source*.
-10.24V to +10.24V	same as -10V to +10V, *plus* 15B to 16B
-5V to +5V	12T to 13B; 14T to 15T and 14B to ADC Source*.
-5.12V to +5.12V	same as -5V to +5V, *plus* 15B to 16B.

*ADC Source is usually Sample and Hold Output (13T), but may be any signal source including Diff. Amp. Output (13B) if Sample and Hold is not desired.

TABLE III

OUTPUT CODE	CONNECTIONS
Unipolar Binary	Connect 17T to -15V Use 29T (B1) for MSB
2's Complement	Connect 17T to -15V Use 28B ($\overline{\text{B1}}$) for MSB
Offset Binary	Connect 17T to -15V Use 29T (B1) for MSB
1's Complement	Connect 17T to 2B Use 28B ($\overline{\text{B1}}$) for MSB

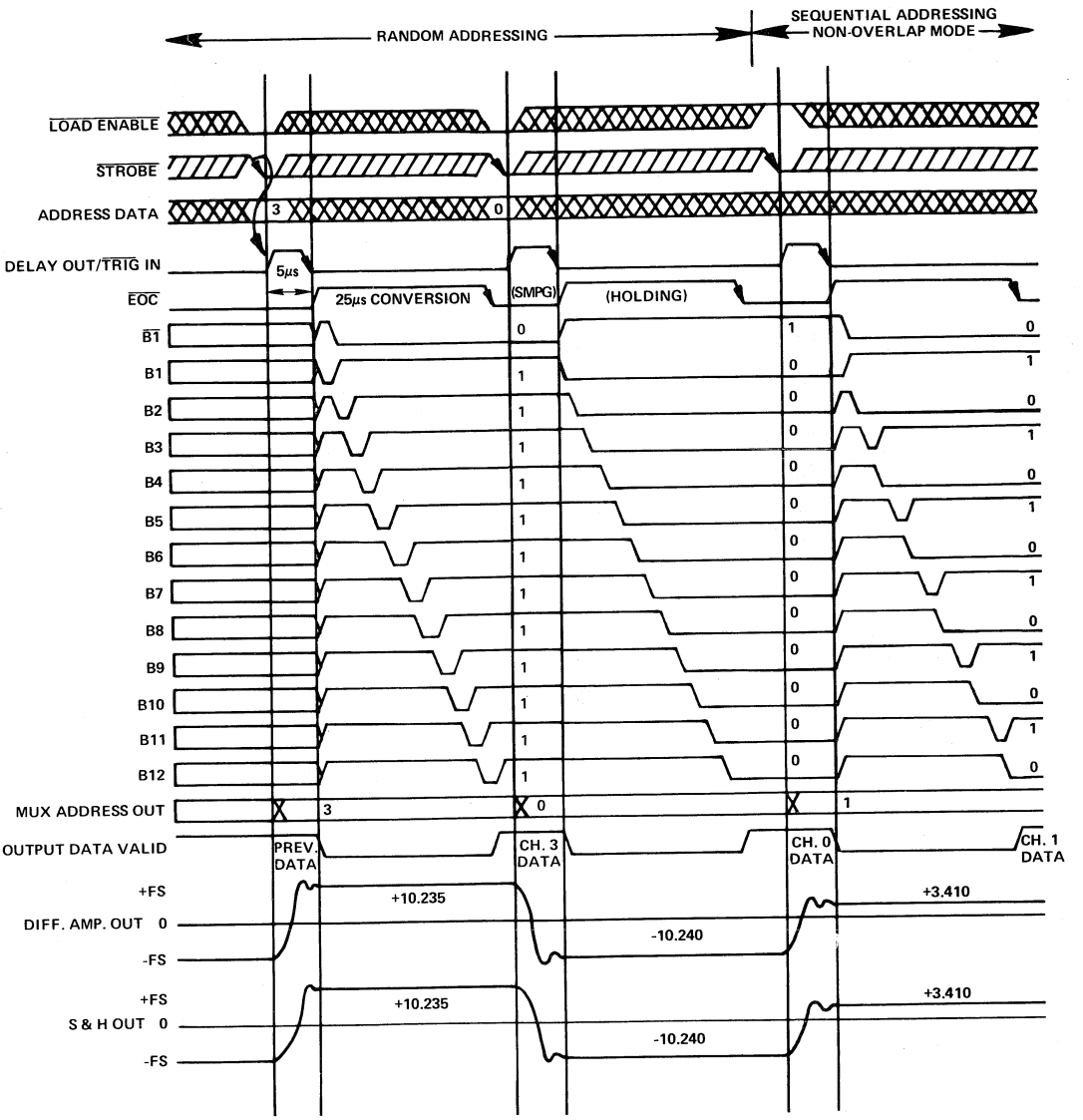


Figure 11. Timing for Non-Overlap Operation in Both Random and Sequential Addressing Modes. For Status Keys and Signal Condition Data, Refer to Box Below.

SIGNAL CONDITIONS AND STATUS KEYS FOR FIGURES 11 AND 12.

CH. 2 = -3.415V CODE 010 101 010 101
CH. 3 = +10.235V CODE 111 111 111 111
CH. 0 = -10.240V CODE 000 000 000 000
CH. 1 = +3.410V CODE 101 010 101 010

ADC SET UP FOR ±10.24V. INPUT, OFFSET BINARY. (FOR TWO'S COMPLEMENT, USE $\overline{B1}$ FOR M.S.B.)

KEY	INPUTS	OUTPUTS
XXX	May change	Don't know
ZZZ	May change 0 to 1	Changes 0 to 1
SSS	May change 1 to 0	Changes 1 to 0
$\overline{OR}$	Must be stable	Will be stable

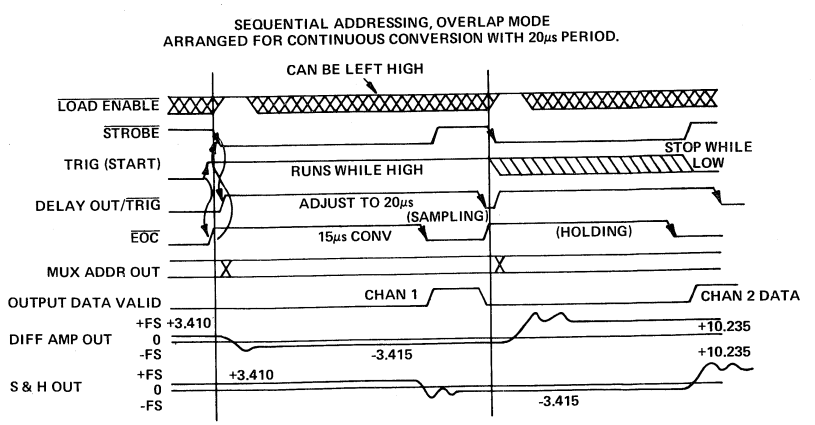


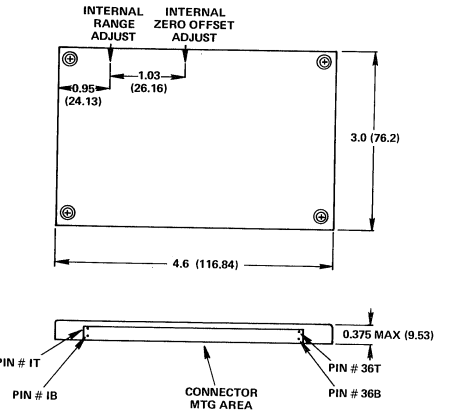
Figure 12. Timing Diagram for Overlap Operation in the Sequential Addressing Mode. For Status Keys and Signal Condition Data, See Box at Right.

Outline Drawings and Pin Designations

DAS1128 Connector Pin Diagram

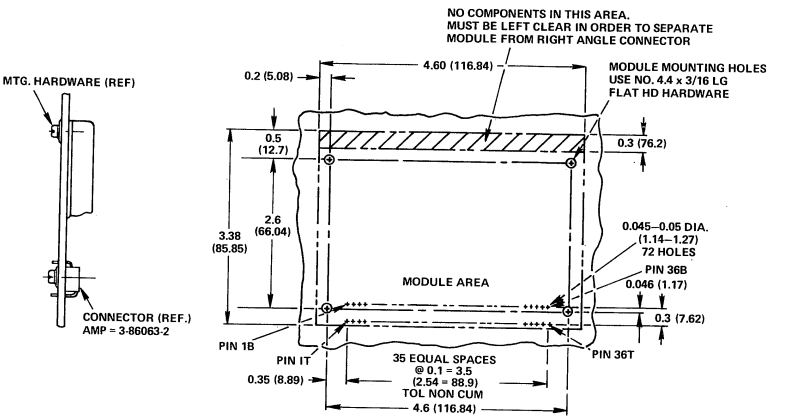
+15V	1T	1B	-15V	
ANA RTN	2T	2B	ANA RTN	
CH 0 IN	3T	3B	CH 8 IN	(CH 0 RTN)
CH 1 IN	4T	4B	CH 9 IN	(CH 1 RTN)
CH 2 IN	5T	5B	CH 10 IN	(CH 2 RTN)
CH 3 IN	6T	6B	CH 11 IN	(CH 3 RTN)
CH 4 IN	7T	7B	CH 12 IN	(CH 4 RTN)
CH 5 IN	8T	8B	CH 13 IN	(CH 5 RTN)
CH 6 IN	9T	9B	CH 14 IN	(CH 6 RTN)
CH 7 IN	10T	10B	CH 15 IN	(CH 7 RTN)
MUX HI OUT	11T	11B	MUX LO OUT	
RANGE SEL	12T	12B	AMP IN LO	
S & H OUT	13T	13B	AMP OUT	
ADC IN 1	14T	14B	ADC IN 2	
+10V REF	15T	15B	BINARY SCALE	
EXT OFFSET	16T	16B	REF ADJ	
OUTPUT CODING	17T	17B	ENABLE LO	
ENABLE HI	18T	18B	$\overline{8}$ OUT	
8 OUT / 4 OUT / 2 OUT / 1 OUT — MUX ADDRESS LINES	19T	19B	8 IN / 4 IN / 2 IN / 1 IN — MUX ADDRESS LINES	
	20T	20B		
	21T	21B		
	22T	22B		
DLY OUT	23T	23B	DLY TRIM	
$\overline{\text{STROBE 1}}$	24T	24B	$\overline{\text{LOAD ENB}}$	
$\overline{\text{STROBE 2}}$	25T	25B	CLR ENB	
TRIG	26T	26B	CLK TRIM	
$\overline{\text{TRIG}}$	27T	27B	$\overline{\text{EOC}}$	
SHT CYC	28T	28B	$\overline{\text{B1}}$ OUT	
B1 OUT	29T	29B	B2 OUT	
B3 OUT	30T	30B	B4 OUT	
B5 OUT	31T	31B	B6 OUT	
B7 OUT	32T	32B	B8 OUT	
B9 OUT	33T	33B	B10 OUT	
B11 OUT	34T	34B	B12 LSB OUT	
DIG RTN	35T	35B	DIG RTN	
+5V	36T	36B	+5V	

TOP VIEW



BASIC MODULE CONFIGURATION

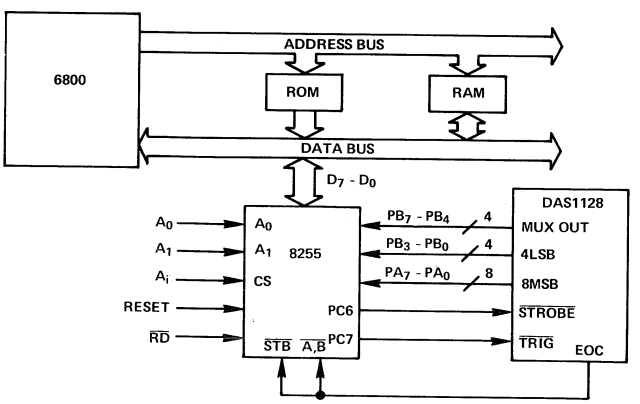
Dimensions shown in inches and (mm).



P.C. BOARD LAYOUT

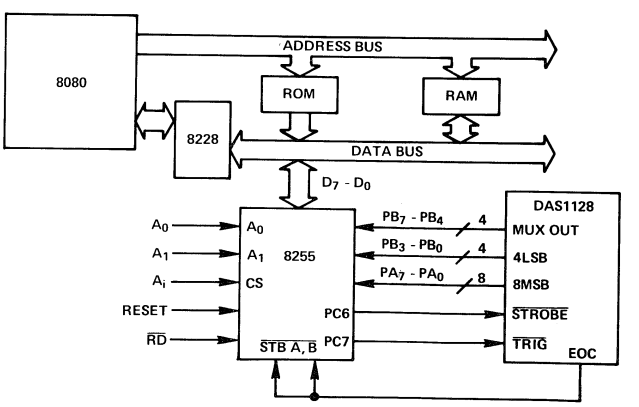
Typical Applications

DAS1128 WITH MOTOROLA 6800



NOTE:
1. 8255 USED IN MODE 1 (STROBED I/O)
2. PC6 INDEXES MUX TO DESIRED CHANNEL
3. CS TO A_i (WHERE, A_i IS AN ADDRESS BIT OTHER THAN A_0 OR A_1)
4. PC7 INITIATES CONVERSION
5. EOC STROBES IN DATA AND MUX INFO
6. 8255 SHOWN, HOWEVER 6820 CAN ALSO BE USED

DAS1128 WITH INTEL 8080



NOTE:
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3. PC6 INDEXES MUX TO DESIRED CHANNEL
4. PC7 INITIATES CONVERSION
5. EOC STROBES IN DATA AND MUX INFO

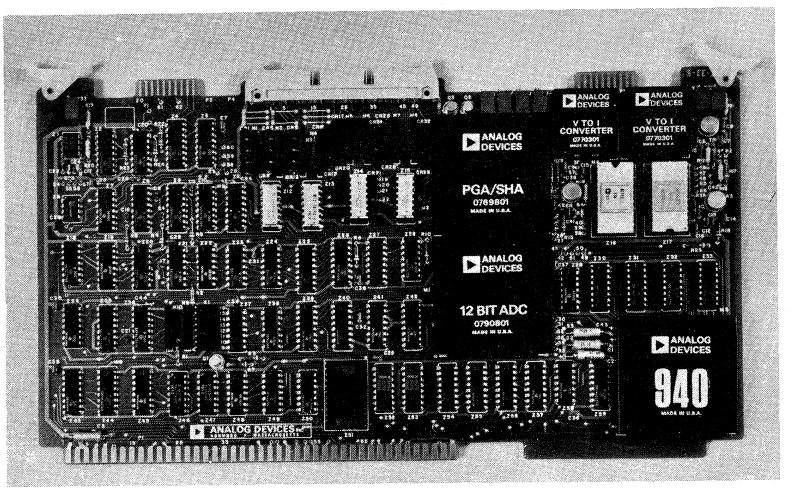
ANALOG DEVICES

Real-Time Analog I/O Interface

MODEL RTI-1200

FEATURES

- **Complete Analog I/O Subsystem**
- **Intel SBC-80/10, 80/20, and MDS Compatible**
- **Memory Mapped I/O Interface**
- **Data Acquisition:**
  - **Up to 32 Input Channels**
  - **Sample and Hold Amplifier**
  - **Programmable Gain Amplifier**
  - **12 Bit A/D Converter**
  - **Input Fault Protection**
- **Real-Time Pacer Clock System**
- **On-Board PROM Socket**
- **Two Optional 12 Bit DAC's**
- **Optional 4–20mA Current Outputs**
- **Optional Single +5V Power**
- **Memory Overlay — RAM and ROM Inhibit**



GENERAL DESCRIPTION

The RTI-1200 is a complete analog input/output subsystem that greatly simplifies the task of interfacing analog signals to Intel SBC-80 Single Board Computers, or other 8080-based microcomputers. It is functionally, electrically, and mechanically compatible with the SBC-80, and all connections to it are made simply by plugging the RTI-1200 into a slot in a card cage that also contains an SBC-80. The RTI-1200 can also be readily interfaced to other 8080-based microcomputers whose address, data, and control busses are accessible.

The RTI-1200 is interfaced to an SBC-80 or other 8080 based microcomputer as a block of contiguous memory locations. It combines on a single printed circuit card many features and capabilities which reduce the hardware required to interface analog signals to a microcomputer, and significantly ease the programming effort associated with inputting and outputting analog signals.

DATA ACQUISITION

The RTI-1200's most basic function is data acquisition. This is accomplished with an analog input multiplexer, a programmable gain amplifier, a sample-and-hold amplifier, and a 12 bit A/D converter. These components are shown in the block diagram (Figure 1). The standard RTI-1200 offers either 16 single ended or 8 differential input channels (user selected). An optional multiplexer expander allows for up to 32 single ended or 16 differential input channels. All of the analog inputs are fully protected up to ±28 volts, and additional protection against larger, potentially destructive overloads is afforded by fusing resistors located at the inputs.

The RTI-1200's A/D Converter can be configured by the user to accept 0 to +10V, ±5V, or ±10V full scale input signals. A programmable gain amplifier preceding the A/D converter has software selectable gains of 1, 2, 4 and 8. This expands the dynamic range of the A/D converter to 15 bits, and results in greater input sensitivity. For example, when operating on the 0 to +10V input range with a programmable gain amplifier gain of 8, the actual input range is 0 to +1.25V. The programmable gain amplifier allows the user to program different gains for different input channels, or to have different gains for varying input levels on the same channel. It is even possible to write software to implement automatic gain ranging operation.

Eight of the input channels have provisions for resistors provided by the user that allow the inputs to accept 4-20mA current loop signals. Output data from the A/D converter is in natural binary code for unipolar input ranges, and at the user's option can be either offset binary or two's complement coding when using bipolar input ranges. A special feature of the RTI-1200's data acquisition operation is that the controlling microcomputer's CPU (i.e., the 8080) is not tied up while a conversion is taking place. This significantly enhances system throughput capability and flexibility, as the CPU is free to pursue other tasks while an A/D conversion is in progress.

SPECIFICATIONS (typical @ +25°C and with +5V and ±15V, unless otherwise noted)

DATA ACQUISITION

Number of Analog Inputs	
Standard	16 Single-Ended or 8 Diff.
With Multiplexer Expander[1]	32 Single-Ended or 16 Diff.
Multiplexer Switching Characteristics	Break-Before-Make. All Switches Open When Power is Off.
Input Voltage Ranges[2]	0 to +10V, ±5V, ±10V
Programmable Gains[3]	1, 2, 4, 8 Software Selectable
Input Impedance	$>10^9$ Ohms
Input Bias Current	
at +25°C	5nA
over 0 to +70°C	50nA
Diff. Input Bias Current	
at +25°C	3nA
over 0 to +70°C	3.5nA
Input Overvoltage Protection	
Continuous Overvoltage	±28 Volts maximum
Overvoltage >±28V	Fusing Resistors
Accuracy	
Resolution	12 Bits
Nonlinearity Error[4]	±1/2LSB typ, ±1LSB max
Diff. Nonlinearity Error	±1/2LSB typ, ±1LSB max
Quantization Error	±1/2LSB max
Input Offset Voltage[5]	Adjustable to Zero
Gain Error[5]	Adjustable to Zero
CMRR	75dB min
CMV	±10V
Noise Error[6]	±1/2LSB max
Temperature Coefficients	
Gain	±15ppm/°C typ, ±25ppm/°C max
Offset	±25μV/°C Referred to Input
Diff. Nonlinearity	±3ppm/°C max
Settling Time to ±0.01%[7]	10μs max at any Gain
SHA Aperture Time	90ns
SHA Aperture Width	20ns
SHA Aperture Uncertainty	±5ns
Conversion Time	25μs max
Maximum Throughput Rate[8]	28kHz

ANALOG OUTPUTS

Number of DAC Channels[9]	2
Accuracy	
Resolution	12 Bits
Nonlinearity Error[4]	±1/2LSB
Diff. Nonlinearity Error	±1/2LSB
Voltage Output Characteristics	
Voltage Output Ranges[2]	±2.5V, 0 to +5V, ±5V, 0 to +10V, ±10V
Output Current	5mA min @ ±10V
Settling Time[10]	10μs max
Gain TC	±8ppm/°C typ, ±15ppm/°C max
Offset TC	±5μV/°C typ, ±20μV/°C max
Current Loop Characteristics[11]	
Current Output Range	4 to 20mA
Load Resistance Range	0 to 500Ω
Loop Supply Voltage	+15V to +30V
Settling Time[12]	50μs max
Gain TC	±10ppm/°C typ, ±25ppm/°C max
Offset TC	±0.4μA/°C
Reference Voltage Output	+5.00V ±0.02% @ 5mA max

REAL-TIME PACER CLOCK SYSTEM

Modes of Operation	Pacer-Timed Conversion Trigger, Pacer-Timed Interrupt, Pacer Off
Types of Clocks	Variable Frequency R-C, Fixed Frequency Crystal, External
Crystal Clock Freq.[13]	Determined by User Supplied Crystal
Variable Freq. Clock Range	30Hz to 30kHz, User Adjustable

LOGIC DRIVER OUTPUTS

Number Available	2
Characteristics	Open Collector, 30V max, 300mA max Continuous Sink Current per Output

MICROCOMPUTER INTERFACE

Compatibility	Completely Compatible with Intel SBC-80/10, SBC-80/20, and MDS Bus System
Type of Interface	Interfaces as a Block of Memory Locations, Using Address, Data and Control Busses.
Position in Memory[14]	User Selectable Among any of 14 Possible Locations.
On-Board PROM	Socket for Intel 2708 or Equivalent 1024 Byte x 8 Bit PROM, of which 1008 Bytes are Usable.
Memory Overlay (Inhibit)	RAM or ROM

POWER REQUIREMENTS[15, 17]

Without DC/DC Option[16]	+15V ±3% @ 40mA -15V ±3% @ 40mA +5V ±5% @ 1.2A
With DC/DC Option	+5V ±5% @ 1.7A

TEMPERATURE RANGE

Operating	0 to +70°C
Storage	-55°C to +85°C

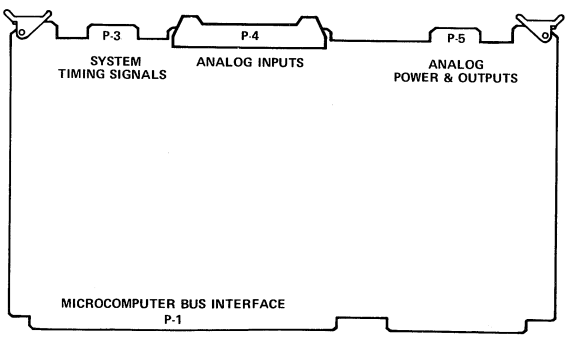
MECHANICAL 6.75" x 12.00" with 0.6" Board-to-Board Sp (171.5 x 304.8 x 15.24mm)

RTI-1200 ORDERING GUIDE

MODEL NUMBER	OPTIONS			
	DC/DC	MUX EXP	DACS	CURRENT LOOPS
RTI-1200-001			X	
-004			X	X
-006				
-011		X		
-014		X	X	
-016		X	X	X
-101	X			
-104	X		X	
-106	X		X	X
-111	X	X		
-114	X	X	X	
-116	X	X	X	X

X DENOTES OPTIONS INCLUDED WITH THE CORRESPONDING MODEL NUMBER. THE OPTIONS ARE DESCRIBED IN NOTES 1, 9, AND 16.

RTI-1200 MECHANICAL OUTLINE



MATING CONNECTORS FOR RTI-1200

PART NO.	MATES TO	DESCRIPTION
AC1551	P3 or P5	Flat Cable Connector 20 Pin, 0.1" Center
AC1552	P4	Flat Cable Connector 50 Pin, 0.1" Center
AC1553	P4	Flat Cable Connector 50 Pin, 0.1" Center with 2' Color Coded Assembly Attached

NOTES

[1] The multiplexer expander is an option, and is shown in the ordering guide as MUX EXP.

[2] The desired range is user selectable with straps.

[3] The input gain of a channel is multiplied by the gain setting of the programmable gain amplifier (e.g., the input range of the 0 to +10V range when using a gain of 8 is 0 to +1.25V).

[4] Defined as deviation from a straight line passing through the end points of the range.

[5] For any one software programmable gain setting. Maximum offset shift of ±1LSB or gain shift of ±0.02% when using a programmable gain setting other than the one used during calibration.

[6] When using a programmable gain setting of 1. It is ±1.5LSB max when using a programmable gain setting of 8.

[7] For a 20V step. This specification is valid for a step change on one input, or following a channel change, or following a programmable gain change, or simultaneous changes involving any combination of these changes.

[8] Based on a 10μs settling time, followed by a 25μs A/D conversion time. Overall system throughput rate is enhanced because the CPU is not held up during conversions.

[9] Two channels of D/A converters and two channels of current loops are available on an option basis. See Ordering Guide.

[10] To ±0.01% of full scale range following a 20V step.

[11] The current loop characteristics include the effects of the driving D/A converter.

[12] To ±0.02% of full scale current following a full scale step.

[13] Space provided for HC-18/U crystal cut for a frequency of up to 50MHz. User can select to divide crystal frequency by 10^3 or 10^4 on-board the RTI-1200.

[14] The memory map shows in detail where the data and control functions appear in memory.

[15] Power requirements shown are for an RTI-1200 with no DAC or current loop options.

[16] The dc/dc power converter is an option that converts +5V dc power to ±15V. It is shown in the ordering guide as dc/dc.

[17] +12V and -5V power is required only if optional PROM is used. This power is supplied by the SBC bus.

Specificatons subject to change without notice.

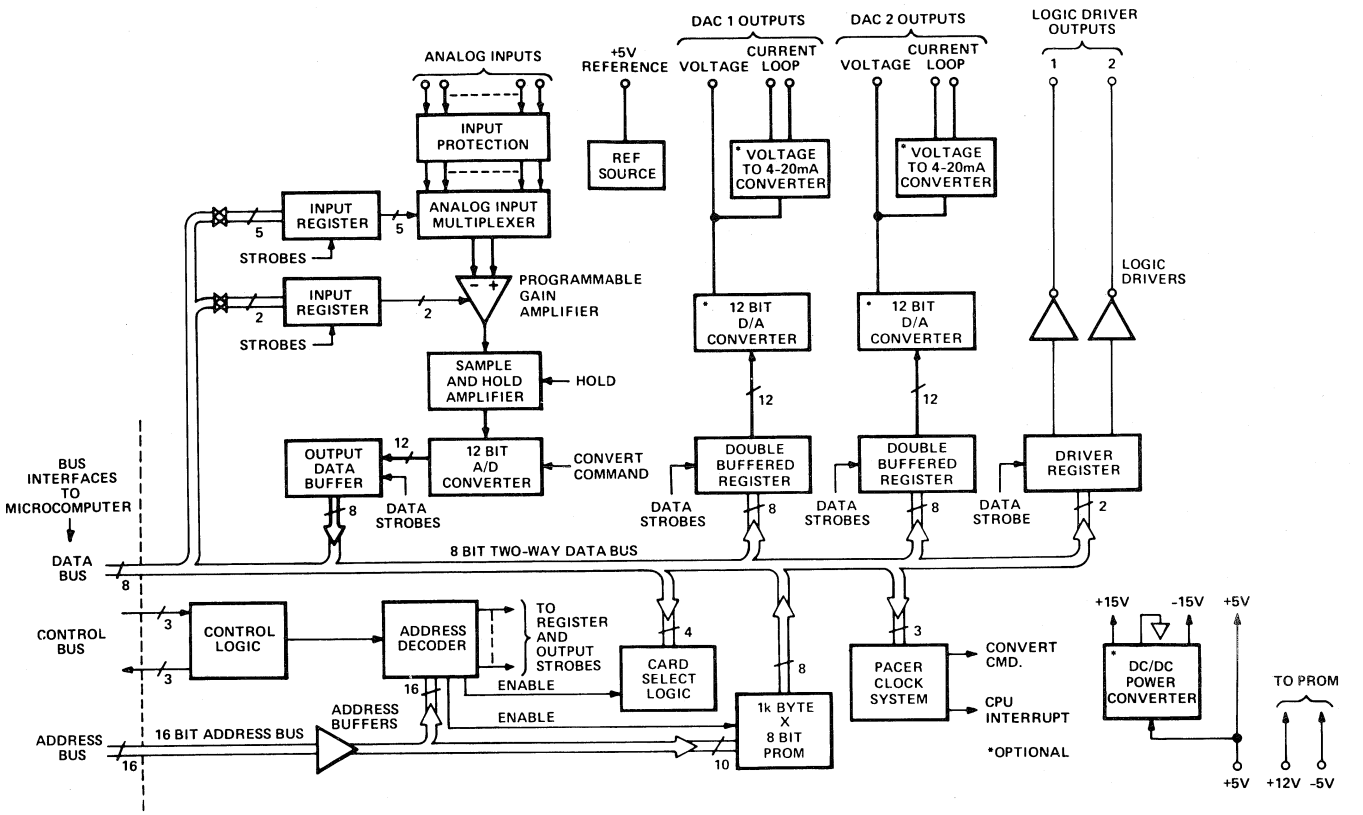


Figure 1. RTI-1200 Functional Block Diagram

ANALOG OUTPUTS

The RTI-1200 has provisions for two optional 12 bit D/A converters which are software driven via double buffered registers. They can be used for such functions as driving an analog recorder, or generating analog control signals. Both D/A converters can be user set to any of five voltage output ranges. The D/A input data is natural binary for unipolar output ranges, and at the user's choice can be offset binary or two's complement for bipolar output ranges. Both analog output channels can also be optionally equipped with 4-20mA current loop outputs. This permits them to drive directly the 4-20mA control loops often used in process and industrial controls.

ON-BOARD MEMORY

The RTI-1200 contains a socket which can accommodate a 1024 byte x 8 bit PROM, such as the Intel 2708. The user can store programs in such a PROM that would establish setpoints, perform data linearization, execute testing subroutines, or perform other RTI-1200 related tasks. This can be of significance in easing programming effort, particularly when more than one RTI-1200 is used with a single SBC-80. Alternatively, the PROM socket can act simply as an extension of the PROM space available on the microcomputer.

REAL TIME PACER CLOCK SYSTEM

Most real world microcomputer applications requiring interfacing to analog data also require that many operations be referenced to real time. The RTI-1200 is equipped with a highly versatile real time pacer clock system that can provide real time operation without resorting to cumbersome and grossly inefficient software timing loops. Two pacer clocks are provided. One clock is of the R-C variety, and can be set by the user to any frequency between approximately 30Hz and 30kHz. The other is a crystal controlled clock, in which a user supplied crystal generates very precisely timed pulses. These pulses can be used to generate accurately spaced A/D conversions, as is required in Fourier transform analysis, or in generating a highly accurate time-of-day clock. A pulse from either of the clocks, or an externally supplied pacer signal, can either trigger A/D conversions directly, or signal interrupts to the controlling microcomputer. The Time Mark bit in the status word is set each time a pacer tick occurs.

OTHER FEATURES

Two software driven open-collector logic driver outputs are available for system control functions, such as providing pen lift commands in an analog data recording application. In addition, a precision 5 volt reference is a standard feature of every RTI-1200 for use in calibration and testing (e.g., as a test input on one of the anlaog input channels). Finally, the RTI-1200 can be ordered with an optional dc/dc power converter. In those instances where +15V and -15V power is not readily available, this option allows the RTI-1200 to be operated solely from the same +5V supply that powers the microcomputer used with the RTI-1200.

MEMORY MAP INTERFACE

The RTI-1200 interfaces to the SBC-80 as a 1K block (1024 bytes) of memory. The SBC-80 can address 65,536 bytes of memory, which can be envisioned as 64 blocks of 1024 bytes each. The RTI-1200 can be configured by the user to occupy one of 14 selected blocks. The 14 possible blocks are spread throughout the 65K address space, so the user should have no trouble positioning the RTI-1200 in a block that does not interfere with already committed address space.

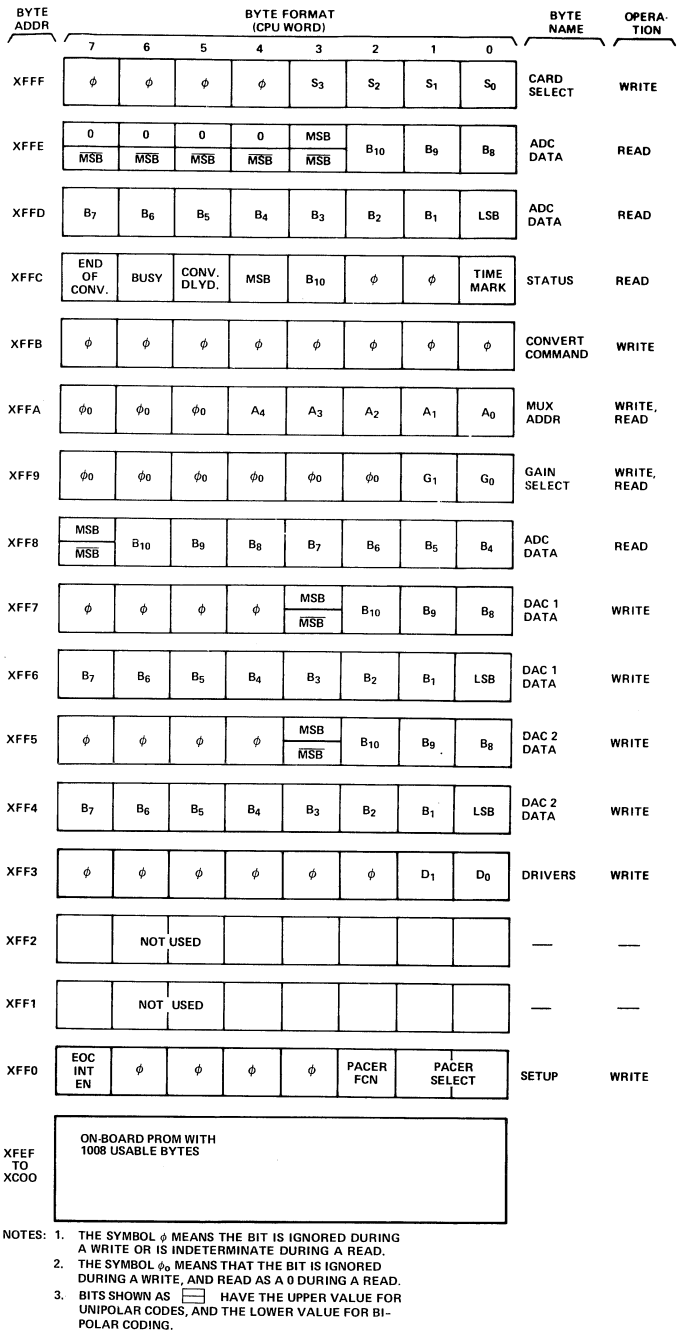
The top 16 addresses (i.e., highest numbered) in the 1K block occupied by the RTI-1200 are devoted to the data and control functions of the RTI-1200. The bottom 1008 addresses are reserved for the on-board PROM. This structure can be seen by referring to Figure 2, the memory map. The byte addresses are shown in hexadecimal notation, with the most significant digit on the left. The addresses from XFFO to XFFF are those associated with the RTI-1200 operation itself (the actual value of hexadecimal digit X is determined by where in the 8080's memory address space the user wishes to have the RTI-1200 appear. All of the memory bytes associated with a particular RTI-1200 will have the same value for X.) The bottom 1008 memory addresses, from XCOO to XFEF, are reserved for the use of an on-board PROM.

Since the RTI-1200 interfaces as memory, any of the 8080's memory reference instructions can be used. The memory map has been carefully thought out so as to make programming as easy as possible. A complete discussion of the memory map is included in the RTI-1200's User's Guide, and only a summary is included here.

When acquiring data, the desired channel is written into address XFFA. The number of the selected channel can also be read back, allowing the use of an increment memory instruction to advance the input multiplexer to the next channel. The desired gain of the programmable gain amplifier is written into address XFF9. A conversion is commanded either by a pulse from one of the pacer clocks, or by writing a convert command into address XFFB. The end of a conversion can be determined either by checking the EOC bit in the status word, or by directing the A/D converter's EOC signal to trigger an interrupt. The A/D converter's output data can be read as 12 bit data in two byte format at addresses XFFD and XFFE. This can be performed with a single LHLD instruction. If only 8 bit data is required, the 8 most significant bits can be read as a single byte at address XFF8.

Analog output data is loaded into the two 12 bit D/A converters at addresses XFF4 through XFF7. The data is in two byte form, and the data for a single D/A converter can be loaded with a single SHLD instruction. The use of double buffers on the RTI-1200 permits the two data bytes to be loaded simultaneously into the D/A converter. This allows the D/A converter's analog output to move directly from an old analog value to a new analog value without first going to an intermediate value.

Address XFFF is the address of the byte used to select one RTI-1200 from among two or more when multiple RTI-1200's time share the same 1k block of memory. Address XFF3 contains the two bits that control the two logic driver outputs. The exact nature and use of the status and setup bytes, as well as hints on maximizing program efficiency when using the RTI-1200, are covered in the RTI-1200 User's Guide.



NOTES:
1. THE SYMBOL ϕ MEANS THE BIT IS IGNORED DURING A WRITE OR IS INDETERMINATE DURING A READ.
2. THE SYMBOL ϕ_0 MEANS THAT THE BIT IS IGNORED DURING A WRITE, AND READ AS A 0 DURING A READ.
3. BITS SHOWN AS ⊟ HAVE THE UPPER VALUE FOR UNIPOLAR CODES, AND THE LOWER VALUE FOR BIPOLAR CODING.

Figure 2. RTI-1200 Memory Map

CARD SELECT FEATURE

The RTI-1200 contains a card select feature, which if enabled by the user, allows up to 15 RTI-1200's to share a single 1k block of memory locations in the SBC-80. This feature (which is somewhat analogous to memory paging, or memory bank selection) allows one RTI-1200 to be active while the others are in a standby or wait state. This feature can be very useful in simplifying software when it is desirable to use the same subroutines with more than one RTI-1200 in a given system. It also conserves the use of memory space.

RTI-1200 USER'S GUIDE

Detailed installation and operating information, along with programming hints and a technical explanation of the operation of the RTI-1200 are contained within the RTI-1200 User's Guide. A copy of this manual is shipped with each RTI-1200. It is also available separately from Analog Devices.

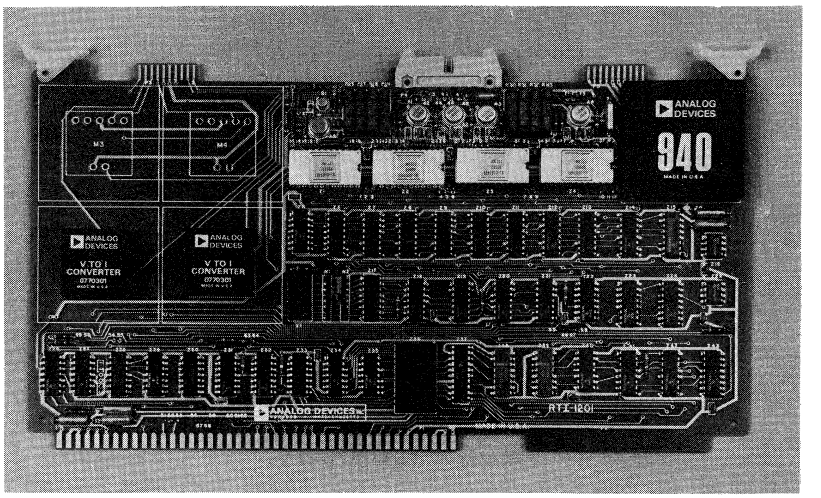
ANALOG DEVICES

Intel Compatible Output Subsystem

RTI-1201

FEATURES

- Complete Output Subsystem
- SBC-80, SYSTEM-80, MDS, BLC-80, & RTI-1200 Compatible
- Memory Mapped I/O Interface
- Wire Wrap Feature Selection
- Four Software Controlled Logic Driver Outputs
- Two or Four Channels of 12 Bit Analog Output
- DAC Data Read Back
- DAC Reset Function
- Optional 4-20mA Current Loop Outputs
- Precision +10V Reference
- Optional Single +5V Power
- Memory Overlay – RAM and ROM Inhibit
- Multiple Card Select Function
- On-Board PROM Socket



GENERAL DESCRIPTION

The RTI-1201 is a complete 8 channel output subsystem comprised of 4 digital and 4 analog channels. This subsystem is electrically and mechanically compatible with the Intel SBC-80 series of single board computers. It is also compatible with the Analog Devices RTI-1200 Analog I/O Interface board, the Intel System-80 microcomputer series, the MDS-800 microcomputer development system and the National Semiconductor BLC-80/10 board level computer.

The RTI-1201 combines on a single printed circuit board many features and capabilities which reduce both the hardware and software effort required to interface a microcomputer to the real world. The RTI-1201 was designed to be extremely versatile, efficient and easy to use in the end user's application. All connections to the microcomputer are made by simply plugging the RTI-1201 into the digital bus connector in the user's card cage. The analog interface is made through a high quality pin connector mounted at the opposite board edge from the digital bus connection. Digital outputs are made at a card edge connector.

DIGITAL OUTPUTS

The RTI-1201 contains four digital output channels. These digital outputs are comprised of high-current logic drivers which can be used for simple "on/off" control of various system functions. These open collector driver outputs are software controlled and have a 30V, 300mA capability.

ANALOG OUTPUTS

The RTI-1201 is configured with either two or four 12 bit D/A converters which are software driven via double buffered registers. They can be used for such functions as driving an analog recorder or generating analog control signals. By using the +10V on-board reference, each of the D/A converters can be individually set by the user to any of five output ranges. The D/A input code for each channel can also be individually set for natural binary, offset binary, or two's complement. The desired configuration is user selectable at convenient wire-wrap posts.

REFERENCE

The RTI-1201 inherently guarantees superb tracking capability of all analog output channels since they all share a single on-board reference. This reference is also buffered and brought out for user convenience. The user may also choose to disconnect the internal reference and use the provision for an external reference.

REMOTE SENSING

Sense inputs of the D/A converter are present at the output connector for applications where the load is to be located a considerable distance from the RTI-1201. Without this feature, IR drops in the output line could rapidly degrade overall accuracy. The board is shipped with jumpers connecting the D/A converter sense inputs to local sense points.

DAC DATA REGISTERS

The D/A converters are software driven via double buffered registers. The buffers allow two data bytes to be loaded simultaneously into the D/A converter so that the output changes directly from one 12 bit value to another. The RTI-1201 also has a provision for writing the 8 MSB's in a single byte word to each D/A converter. This allows fast, highly accurate, eight bit operation.

SPECIFICATIONS (typical at +25°C and with nominal voltages, unless otherwise noted)

RTI-1201 ANALOG/DIGITAL OUTPUT BOARD

Digital Outputs	
Number	4 Logic Drivers
Characteristics	Open Collector, 30V max, 300mA max Continuous Sink Current per Output.
Analog Outputs[1]	
Number Available	2 or 4 DAC's
Accuracy[2]	
Resolution	12 Bits
Overall Error	±1/2LSB (0.0125% FSR)
Voltage Output Characteristics	
Ranges[3]	0 to 5V, 0 to 10V, ±2.5V, ±5V, ±10V
Output Current	5mA min @ ±10V
Settling Time (to 0.02% FS for 10V Step)	5μs
Offset T.C.	±10μV/°C
Gain T.C.	±10ppm/°C
Current Loop Characteristics[1, 4]	
Number	0, 2, or 4
Range	4–20mA Nonisolated
Compliance Voltage[5]	10V @ 20mA with 15V Supply
Loop Supply Voltage Range	+15V to +30V
Settling Time (to ±0.01% for Full Scale Step)	50μs max
Offset T.C.	±0.4μA/°C
Gain T.C.	±15ppm/°C
Load Resistance Range	0 to 500 ohms
Digital Input Coding[3]	BIN, OBN, 2SC
On-Board Reference[6]	
Voltage Output	+10.00V ±0.02% @ 2mA
T.C.	±10ppm/°C
External Reference Input[6]	
Range	0V to +10V
Input Impedance	20kΩ ±15%

LOGIC DRIVER OUTPUTS

Number	4
Characteristics	Open Collector, 30V max, 300mA max Continuous Sink Current per Output

MICROCOMPUTER INTERFACE

Compatibility	Completely Compatible with Intel SBC-80/10, SBC-80/20, and MDS Bus System, RTI-1200; BLC-80/10
Type of Interface	Interfaces as a Block of Memory Locations, Using Address, Data and Control Busses.
Position in Memory[7]	User Selectable Among any of 16 Possible Locations.
Card Select Feature[7]	16 Cards per 1K Memory Position
On-Board PROM Socket	Socket for Intel 2708 or Equivalent 1024 Byte x 8 Bit PROM, of which 1008 Bytes are Usable. +12V and -5V are supplied from the Digital Bus.
Memory Overlay (Inhibit)[3]	RAM or ROM
DAC Load Sense	Provision is made for Local (on-board) or External Load Sensing for each DAC.
Reset[3]	All DAC's can be Reset to 0V Output with a Single Write Instruction or upon System Reset. All logic drivers can be turned "off" upon system reset.
DAC Readback	DAC Data can be Read Back

POWER REQUIREMENTS[8]

Without DC/DC Options	
RTI-1201-020	+15V ±3% @ 45mA -15V ±3% @ 95mA +5V ±5% @ 1100mA
Per DAC Pair	+15V ±3% @ 20mA -15V ±3% @ 25mA
Per V/I Pair	+15V ±3% @ 20mA -15V ±3% @ 20mA
With DC/DC Option[9]	
RTI-1201-144	+5V ±5% @ 1700mA max

TEMPERATURE RANGE

Operations	0 to +70°C
Storage	-55°C to +85°C

MECHANICAL

Size	6.75" x 12.00" with 0.6" min Board Spacing (171.5 x 304.8 x 15.2mm)
Connectors	See Ordering Guide Below

NOTES

[1] See ordering guide for information on allowable combinations.

[2] Overall error is specified with gain and offset trimmed and is defined as the deviation from a straight line passing through the end points of the range. It is expressed in terms of bits and in terms of the deviation as a percent of the full scale range. (i.e., 2.5mV is 0.0125% FSR of a -10V to 10V range).

[3] User selectable with wire-wrap jumpers.

[4] The current loop specifications include the effects of the driving D/A converter.

[5] Up to 11V compliance is possible @ 20mA with a +18V minimum loop supply.

[6] The reference is trimmed to within 0.02% accuracy at no load. Long term drift is less than 1/2LSB/1000 Hours operation. DAC accuracy is reduced with lower reference levels. Overall error is 0.1% with a 1V external reference input.

[7] The memory map shows in detail where the data and control functions appear in memory.

[8] Power requirements shown are for RTI-1201-020 with 2 DAC's and no Current Loop options. Power requirements for each additional pair of DAC's and V/I converters are also shown.

[9] The DC/DC converter option provides ±15V for the analog circuits from the SBC system's +5V bus.

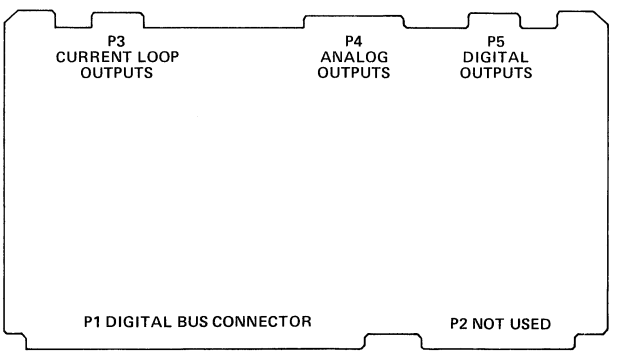
Specifications subject to change without notice.

RTI-1201 ORDERING GUIDE

MODEL NUMBER	DC/DC	DACs	V/Is
RTI-1201-020	0	2	0
-022	0	2	2
-040	0	4	0
-042	0	4	2
-044	0	4	4
-120	1	2	0
-122	1	2	2
-140	1	4	0
-142	1	4	2
-144	1	4	4

NOTE: ALL OPTIONS HAVE 4 LOGIC DRIVER OUTPUTS

MECHANICAL OUTLINE



MATING CONNECTIONS

	Mates to	Description
AC1551	P3 or P5 (Card Edge Connector)	Solder Tail Connector 20 pin, 0.1" centers w/o connecting cable
AC1555	P4 (Analog Pin Connector)	Flat Cable Connector 20 pin, 0.1" centers with 2' color coded cable attached.
AC1556	P3 or P5 (Card Edge Connector)	Flat Cable Connector 20 pin, 0.1" centers with 3' color coded cable attached.

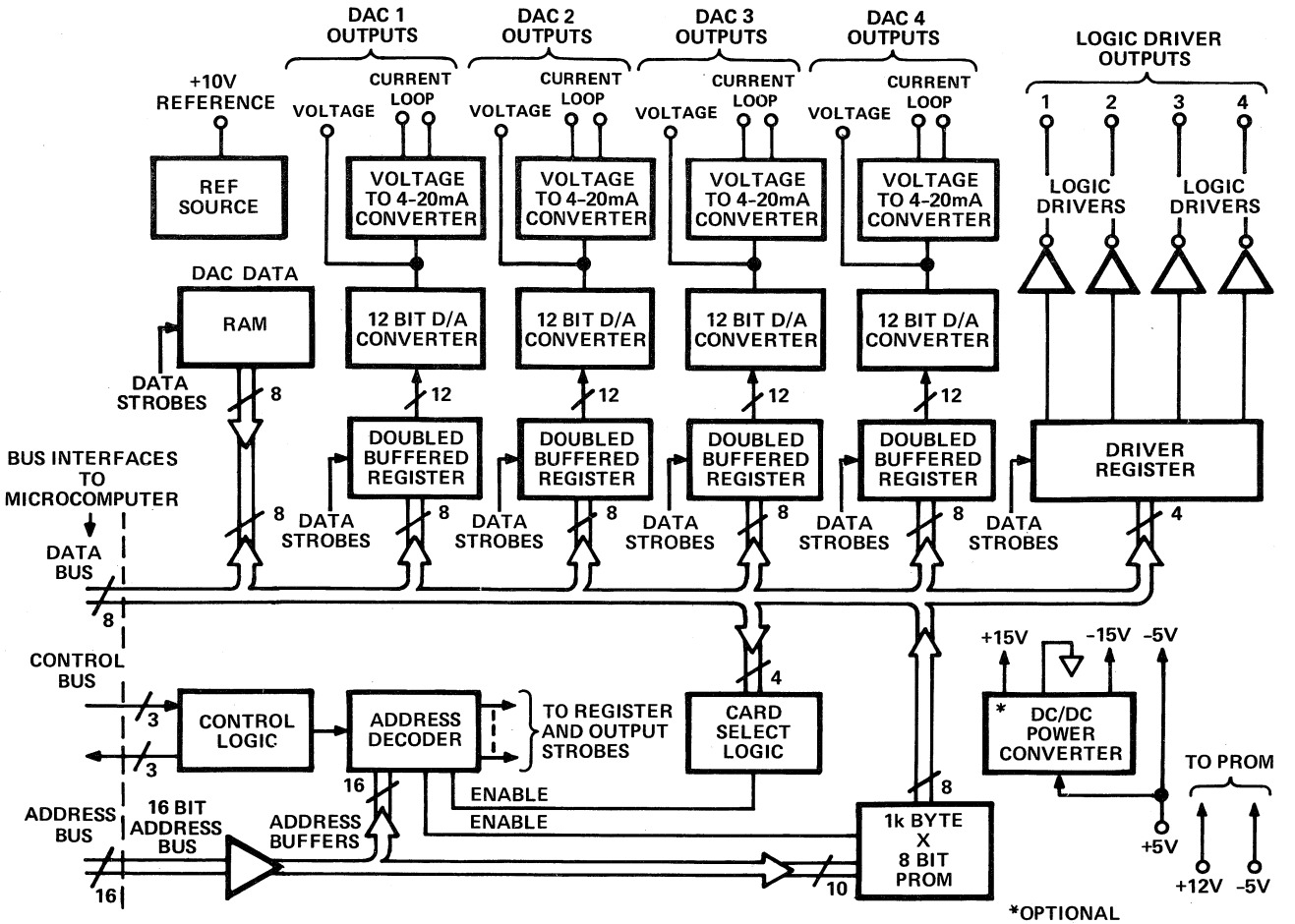


Figure 1. RTI-1201 Functional Block Diagram

DAC READBACK

The RTI-1201 has the capability of reading back DAC input data. This feature offers additional software flexibility and convenience since it eliminates the need for scratch pad memories or software overhead to store data written into the DAC's.

RESET FEATURE

A flash reset feature is also incorporated in the RTI-1201 that allows resetting any or all D/A converters by a single byte instruction. The user can also connect jumpers to allow the DAC's and/or the logic drivers to reset on a system reset.

CURRENT LOOP OUTPUTS

Each of the four analog output channels can be optionally equipped with a voltage to current converter. With this option, a 4-20mA current loop signal is available for process and industrial control applications.

POWER OPTION

The RTI-1201 can be powered from ±15V where available or, as an option, a dc/dc converter can be provided that will allow the RTI-1201 to be operated solely from the same +5V supply that powers the microcomputer.

MEMORY MAP INTERFACE

The RTI-1201 interfaces to the microcomputer as a 1K block (1024 bytes) of memory. The RTI-1201 can be configured by the user to occupy any one of 16 selected blocks of memory spread throughout the SBC's 65K address space so that it does not interfere with already committed address space. The RTI-1201 is jumpered for a 1K address offset relative to the RTI-1200 analog input board. This technique allows complete versatility and efficiency when using the boards individually or together. (Removing this jumper eliminates the offset.)

By using the RTI-1201 as a memory mapped interface the designer has the opportunity to use all of the 8080 memory reference instructions. An I/O port interface only allows for data transfer between the accumulator and the ports. Therefore, software for the RTI-1201 can be as sophisticated as the user desires or as simple as that allowed by I/O port interfacing.

MEMORY OVERLAY

The RTI-1201 has the capability of "memory overlay" (also referred to as "memory inhibit"). Only the RAM or ROM memory occupying the same 1K memory block as the RTI-1201 is inhibited. The on-board PROM is not inhibited by enabling this feature.

CARD SELECT FEATURE

The RTI-1201 contains a card select feature, which if enabled by the user, allows up to 16 RTI-1201's to share the same 1K block of memory locations. This feature (which is somewhat analogous to memory paging), allows one RTI-1201 at a time to be active on the system bus. The feature can be very useful in simplifying software when it is desirable to use the same subroutines with more than one RTI-1201 in a given system. It also conserves memory space. The card select feature may also be used for efficient multiple use of a combination of RTI-1200's and RTI-1201's.

ON BOARD MEMORY

The RTI-1201 contains a PROM socket that maps with the card address and with the card select feature. It can accommodate a 2708 compatible 1024 byte x 8 bit PROM. The user can store programs on board to perform data linearization, execute testing subroutines, store waveform values, or perform other RTI-1201 related tasks. This can significantly ease programming effort. Alternatively, the PROM socket can act simply as an extension of the PROM space available on the SBC-80 or other microcomputer.

RTI-1201 USER'S GUIDE

Detailed installation and operating information, along with programming hints and a technical explanation of the operation of the RTI-1201 are contained within the RTI-1200/1201 User's Guide. A copy of this manual is shipped with each RTI-1201.

MEMORY INTERFACE

Address Selection: The RTI-1201 occupies 1024 consecutive memory addresses (X800 to XBFF). Their location is selectable at an on-board memory address/card select socket using either a DIP switch or jumper plugs to program the value of the most significant hex digit.

Card Select: Up to 16 cards may share the same memory space and subroutine programming. The 4 LSBs of the data word written into the card select memory address (XBFF) determine which card is activated. The card code is user determined by inserting a DIP switch or jumper plugs into the memory address/card select socket. The card select feature can be enabled by removing a jumper installed at the factory.

DAC Data: Analog output data can be written into memory in either single 8 bit byte format or in 12 bit resolution two byte format (e.g., for DAC 2 data, 12 bit data is written into XBF6 and XBF7. For 8 bit data the user would write a single byte into address XBF1). When using single byte data, the four LSB's of the DAC are set to zero.

DAC Reset: Each DAC may be reset to zero voltage output by writing a "1" into the corresponding bit location in address XBFD.

Digital Outputs: Each of the four logic drivers may be turned "on" (logic low output @ 300mA max) by writing a "1" into the corresponding bit location of address XBFC.

PROM Addresses: The on-board PROM socket is allocated the lower 1008 locations (X800 to XBEF) of the 1K memory block in which the RTI-1201 resides. The upper 16 PROM locations are allocated to the RTI-1201 control and data functions and will not read back PROM data if they are addressed.

SAMPLE PROGRAM FOR ANALOG OUTPUT (8080 LANGUAGE)

LXI H, OFFFH	H and L register pair loaded with all "1"s in the 12 LSB's.
SHLD XBFC	Reset all DAC's and Driver outputs to zero volts.
SHLD XBF6	Contents of H and L registers are loaded into DAC 2 (12 bit data).
JMP X800	Jump to lowest address of on-board PROM for next instructions.

RTI-1201 MEMORY IMAGE AND WORD FORMATS

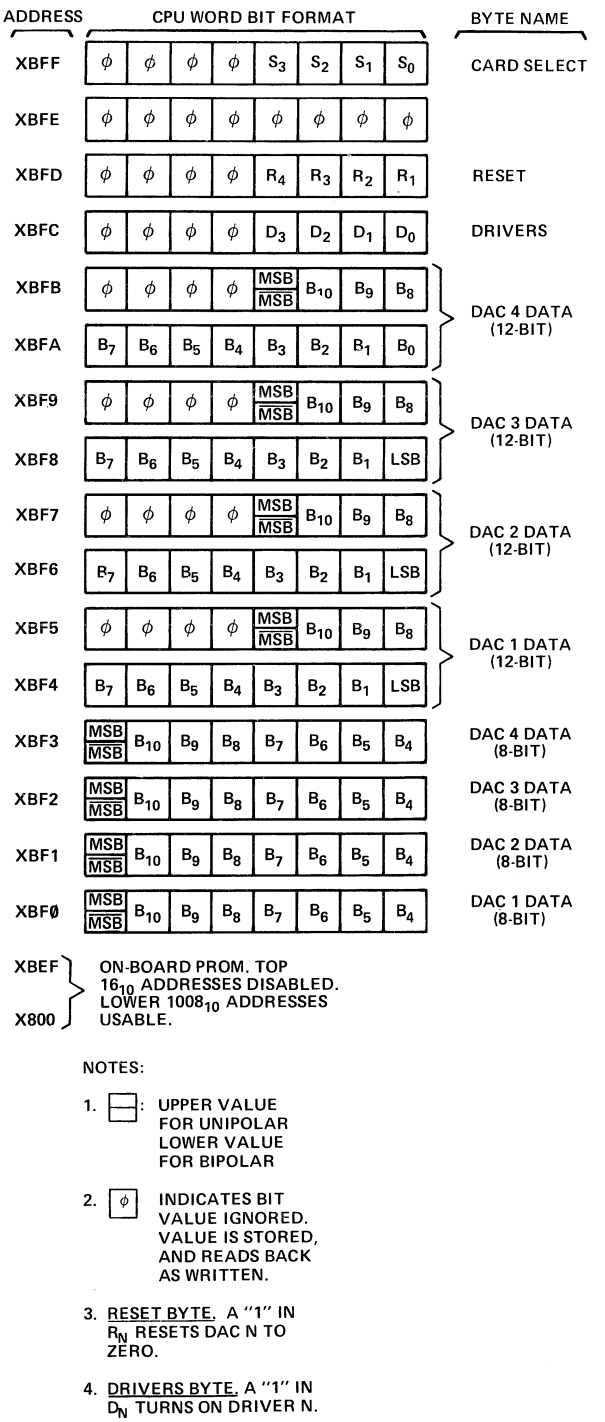


Figure 2.

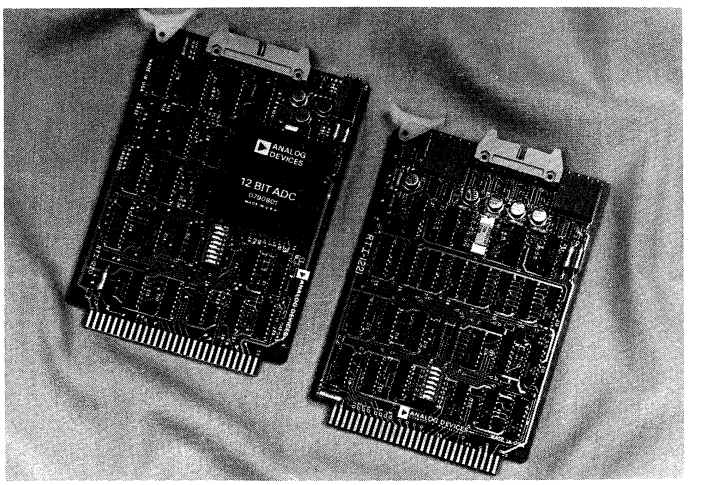
ANALOG DEVICES

Pro-Log Compatible Real-Time Analog I/O Interface

MODELS RTI-1220, RTI-1221

FEATURES

- **Directly Compatible with Pro-Log 8 Bit and 4 Bit Microcomputers**
- **Complete Analog Input and Output Subsystems**
- **Memory Mapped or I/O Port Interface**
- **Card Select Feature**
- **Wire Wrap Feature Selection**
- **Data Acquisition (Model RTI-1220)**
  - **16 Input Channels**
  - **4-20mA Current Input Capability**
  - **Sample and Hold Amplifier**
  - **Adjustable Gain Instrumentation Amp.**
  - **8 Bit or 12 Bit A/D Converter Option**
  - **Input Fault Protection**
- **Analog Output (Model RTI-1221)**
  - **4 Channel Output**
  - **Full 4-Quadrant Multiplying DAC's**
  - **-5V and -10V Precision References Available at Pin Connector**



GENERAL DESCRIPTION

The RTI-1220, Analog Data Acquisition Board and the RTI-1221, Analog Output Board comprise complete analog I/O subsystems. They simplify system development between real-timc analog signals and Pro-Log microcomputers or other 8080 and 6800 based systems. The RTI-1220 and RTI-1221 are functionally, mechanically, and electrically compatible with the Pro-Log series of microcomputers. All address, control, and data bus connections are made by simply plugging these cards into a user wired Pro-Log card cage. The analog interface to each card is made through a high quality pin connector mounted at the opposite board edge from the digital bus.

Each board can be configured as a block of contiguous memory locations (memory mapped interface) or as an I/O device. Each analog subsystem combines on a single printed circuit board a number of features and capabilities designed to reduce the hardware required to interface analog signals to the microcomputer. These features simplify programming for analog I/O interface between the microcomputer and the real world.

DATA ACQUISITION – RTI-1220

The basic functions of the RTI-1220 are analog signal data acquisition, and conversion into digital information acceptable to a microcomputer. This is accomplished with a protected analog multiplexer, an adjustable gain instrumentation amplifier, a sample and hold amplifier, and either a 12 bit or an 8 bit A/D converter. These functions are shown in the block diagram of the RTI-1220.

The input of model RTI-1220 may be configured for either 16 channel single-ended, or pseudo-differential operation, or for 8 channel full differential operation. The desired configuration is user selectable at convenient wire wrap posts. All analog input signals are fully protected to $\pm V_{CC}$ ±20V. This condition applies for all values of V_{CC} within the range of $-15.5V \leqslant 0 \leqslant +15.5V$. In addition, four of the input channels have provisions for resistors provided by the user that allow the inputs to accept 4-20mA current loop signals.

The RTI-1220 has a special feature that prevents erroneous data acquisition. Each time an input channel is switched an automatic convert command delay is enabled. This delay allows for signal settling at the front end before initiation of conversion. The controlling microcomputer is not held up during either the delay time or the conversion time. For high gain applications, the convert command delay time may be increased through software or by addition of a capacitor.

An adjustable gain instrumentation amplifier precedes the SHA. Its gain is user selectable by a single metal film or wire-wound resistor for any gain in the range of 1 to 1000V/V. This feature allows increased sensitivity resulting in the capability of accurately processing low level signals.

A special feature of the RTI-1220's data acquisition operation is that the controlling microcomputer does not have to wait while an A/D conversion is taking place. This significantly enhances system throughput capability, as the CPU is free to pursue other tasks such as manipulating data while

SPECIFICATIONS (typical @ +25°C with +5V and ±15V unless otherwise noted)

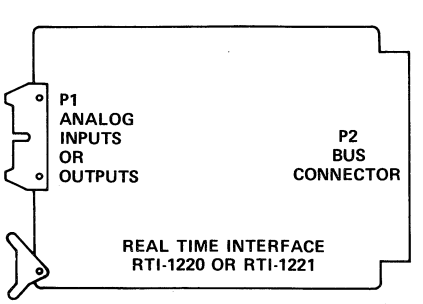
MODEL	RTI-1220
ANALOG INPUT	
Number of Analog Inputs	16 Single-Ended, 8 Differential, or 16 Pseudo-Differential
Multiplexer Switching Characteristics	Break-Before-Make. All Channels Open When Power is Off.
Input Voltage Ranges[1]	±10mV to ±10V
Input Current Loop Ranges (Resistor Programmable)	4-20mA, 10-50mA, etc.
ADC Input Ranges[2]	0V to +10V, 0V to -10V, ±5V, ±10V
Amplifier Gain Range (Resistor Programmable)	1 to 1000V/V
Amplifier Gain Equation	$G = (1 + \frac{10K}{R})$
Input Impedance	$>10^8\Omega$
Settling Time[3]	30µs max @ G = 1
Input Bias Current (0 to +70°C)	300nA
Amplifier Input Offset Voltage	±0.3mV max
Amplifier Input Offset Voltage Drift	±25µV/°C
CMRR	75dB min
CMV	±10V
Noise Error[4]	±1/2LSB max
Input Overvoltage Protection	
Continuous Overvoltage	$\pm V_{CC}$ ±20V
CONVERSION CHARACTERISTICS	
Accuracy	8 BIT ADC / 12 BIT ADC
Resolution	8 Bits / 12 Bits
Overall Error[5], G = 1	±0.2% max / ±0.025% max
G = 10	±0.3% / ±0.03%
G = 200	±0.4% / ±0.2%
T.C. of Overall Error, G = 1	±0.02%/°C max / ±0.005%/°C
Conversion Time[6]	2µs / 25µs
Delay Time[6]	35µs / 35µs
Throughput Rate[7]	27.0kHz / 16.7kHz
SHA Aperture Time	150ns / 150ns
SHA Aperture Uncertainty	±15ns / ±15ns
Gain Error	Adjustable to Zero
Input Offset Voltage	Adjustable to Zero
Digital Output Coding	Binary, Offset Binary, Two's Complement
MICROCOMPUTER INTERFACE	
Compatibility	All Pro-Log 4 or 8 Bit Bus or I/O Port-Oriented Microcomputer Cards
TYPE OF INTERFACE[8]	Memory Mapped or I/O Port-Interface
Address[9]	User Selectable
Power Requirements	+15V ±3% @ 9mA
	-15V ±3% @ 9mA
	+5V ±5% @ 420mA
Mechanical Size	4.5" x 6" with 0.5" min Board Spacing (114.3mm x 152.4mm x 12.7 mm)
Temperature Range	
Operating	0 to +70°C
Storage	-55°C to +85°C
Mating Connectors	AC1554
Analog Connector (P-1) with 2' Color Coded Flat Cable Attached.	

MODEL	RTI-1221
ANALOG OUTPUT	
Number of DAC Channels	4
Accuracy	8 Bit Option / 10 Bit Option
Resolution	10 Bits / 10 Bits
Overall Error	±0.4% max / ±0.1% max
Offset Error	Adjustable to Zero
Gain Error	Adjustable to Zero
Voltage Output Characteristics	
Voltage Output Range[2, 10]	0 to +5V, ±5V, 0 to +10V, ±10V
Output Current	5mA min @ ±10V
Settling Time to 0.05% (20V Step)	30µs max
Gain T.C.	±30ppm/°C max
Offset T.C.	±25µV/°C max
Reference Voltage Outputs	-10.00V @ 2mA (±0.02%)
	-5.00V @ 2mA (±0.07%)
External Reference Input[11]	
Voltage Range	-10V to +10V
Input Resistance	10kΩ Nominal
Digital Input Coding[2]	Binary, Offset Binary, Two's Complement (All digital inputs are double buffered)
Address[9]	User Selectable
Power Requirements	
+15V	35mA
-15V	25mA
+5V	265mA
Temperature Range	
Operating	0 to +70°C
Storage	-55°C to +85°C
Mating Connector	AC1555
Analog Connector (P-1) with 2' Color Coded Flat Cable Attached.	

NOTES
[1] The input signal range is the A/D converter range divided by the gain of the instrumentation amplifier.
[2] User selectable with wire wrap jumpers.
[3] Settling time is a function of gain and increases to 1.5 milliseconds at G = 200.
[4] Typically 1/2LSB for G = 1 to 200 with an 8 bit ADC and 1/2 LSB for G = 1 to 50 with the 12 bit ADC.
[5] When offset and gain error are trimmed to zero. Noise error is specified separately.
[6] Neither delay time nor conversion time will hold up the CPU (see paragraph on Data Acquisition).
[7] The throughput rate is based on a 35µs delay time followed by a 25µs conversion time for the 12 bit ADC or 2µs conversion time for the 8 bit ADC.
[8] The memory map shows in detail where the data and control functions appear in memory.
[9] The address is selected at an on board socket by a user provided DIP switch (or shorting plugs).
[10] These ranges are possible by using the on board reference voltages. Other ranges may be obtained with an external reference.
[11] Each DAC used on model RTI-1221 is a true four quadrant multiplying DAC which can be used with an independent reference voltage or ac signal for programmable attenuation.

Specifications subject to change without notice.

RTI-1220/1221 MECHANICAL OUTLINE



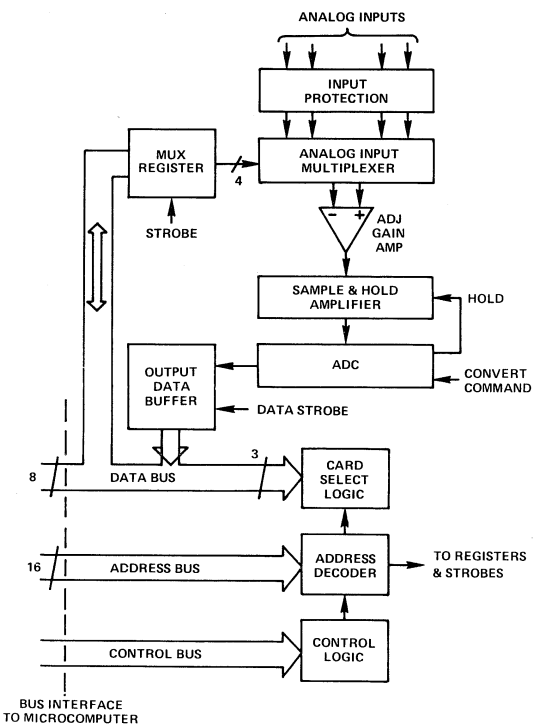
RTI-1220 AND RTI-1221 ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
RTI-1220-8	Analog Input Board with 8 Bit ADC
RTI-1220-12	Analog Input Board with 12 Bit ADC
RTI-1221-8	Analog Output Board with Four 10 Bit DACs Having 8 Bit Accuracy.
RTI-1221-10	Analog Output Board with Four 10 Bit DACs Having 10 Bit Accuracy.

an A/D conversion is in progress. A sample and hold amplifier that is automatically switched to the hold mode when a convert command is issued also allows acquisition of signals that are 100 times faster than could be acquired without a sample and hold.

The RTI-1220 can be easily configured by wire wrap jumpers at the ADC to accept 0 to +10V, -10V to 0V, ±5V, or ±10V full scale ADC input signals. Output data from the A/D converter is natural binary code for unipolar input ranges and at the user's option, can be either offset binary or two's complement coding when using bipolar input ranges. Another feature of the RTI-1220 is that all of the resulting ADC data appears in both single and double byte format.

ANALOG INPUT BOARD FOR PROLOG MICROCOMPUTERS
16 ANALOG INPUT CHANNELS



RTI-1220 Block Diagram

ANALOG OUTPUTS – RTI-1221

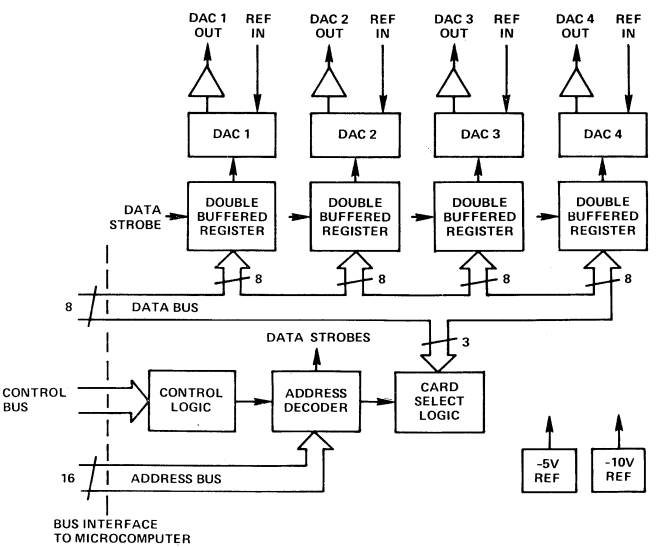
The basic function of the RTI-1221 is to provide Analog outputs corresponding to digital information available from the microcomputer. The RTI-1221 is a complete four channel analog output system that consists of double-buffered registers, 10 bit resolution DACs, and output amplifiers. Two precision voltage references are also available for on-board or external system utilization. These functions are shown in the RTI-1221 block diagram.

Double-buffered input registers are used so that digital data from the microcomputer may be presented in two byte format for 10 bit resolution or in single byte format for a highly accurate 8 bit output. The D/A input data is natural Binary for unipolar output ranges and can be user configured for Offset Binary or Two's Complement for bipolar output ranges.

All four D/A converters can be set to virtually any voltage range desired. By using the on-board references, 4 output ranges may be selected by wire wrap jumpers (±10V, 0 to 10V, ±5V, 0 to 5V). If an external reference is used, the user has complete freedom to set the full scale output to any value from a few millivolts to ±10 volts. This feature is made possible by the utilization of true four quadrant multiplying DACs. If a varying reference signal is used, the DAC becomes a programmable attenuator. For more sophisticated applications flexibility, the output of one D/A channel can be used as a reference for a second D/A channel. The resulting Analog output is then directly proportional to the product of two variables and is completely under software control.

The RTI-1221 provides precision -5V and -10V references as a standard feature for use in calibration and testing. Either of these references may be used as a test input for one of the Analog input channels on the RTI-1220 data acquisition board.

ANALOG OUTPUT BOARD FOR PROLOG MICROCOMPUTERS



RTI-1221 Block Diagram

MEMORY INTERFACE

RTI-1220 – Analog Input Board

Address Selection – The RTI-1220 occupies 8 consecutive memory addresses (FXF8 to FXFF). Their location is user selectable at the on-board memory address/card select socket with either a DIP switch or jumper plug.

Card Select – Up to eight cards may share the same memory space and subrouting programming. The 3 LSBs of the data word written into the card select memory address (FXFF) determine which card is activated. The card code is user determined by inserting a DIP switch or jumper plug into the memory address/card select socket.

Multiplexer Address – The 4 LSB's of the data word written into the multiplexer memory address (FXF9) determine which channel is selected. The channel address may be incremented by using a memory increment instruction. The active channel number may also be read back.

Convert Command – Conversion can be initiated either by writing any data word into the convert command memory address (FXFA) or by external circuitry.

Status – End of conversion is indicated by a Logic "1" MSB in the status memory address (FXFB). Reading a Logic "0" indicates that conversion is either still in progress or never was initiated.

ADC Data – 12 bit ADC right justified data can be read in two byte format at a pair of ADC data memory addresses (FXFC & FXFD). The highest order 8 bits are also available at another address (FXFE) and may be read with a single byte read instruction.

MEMORY ADDR.	DATA: 8-BIT BYTE FORMAT	DATA: 4-BIT	BYTE NAME	OPER.
FXFF	ϕ ϕ ϕ ϕ ϕ S_2 S_1 S_0	ϕ S_2 S_1 S_0	CARD SELECT	WRITE
FXFE	MSB/MSB B_{10} B_9 B_8 B_7 B_6 B_5 B_4	MSB/MSB B_{10} B_9 B_8	ADC DATA	READ
FXFD	0/MSB 0/MSB 0/MSB 0/MSB MSB/MSB B_{10} B_9 B_8	B_7 B_6 B_5 B_4	ADC DATA	READ
FXFC	B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0	B_3 B_2 B_1 B_0	ADC DATA	READ
FXFB	EOC ϕ ϕ ϕ ϕ ϕ ϕ ϕ	EOC ϕ ϕ ϕ	STATUS	READ
FXFA	ϕ ϕ ϕ ϕ ϕ ϕ ϕ ϕ	ϕ ϕ ϕ ϕ	CONV. COM'D.	WRITE
FXF9	ϕ_0 ϕ_0 ϕ_0 ϕ_0 A_3 A_2 A_1 A_0	A_3 A_2 A_1 A_0	MPX ADDR.	WRITE, READ
FXF8			UNUSED	—

UPPER ENTRY UNIPOLAR / LOWER ENTRY BIPOLAR

X : USER SELECTED (SEE ADDRESS SELECTION)

ϕ : BIT IGNORED ON WRITES; UNDEFINED ON READS

ϕ_0 : BIT IGNORED, READS AS "0"

RTI-1220 Memory Image Format

Sample Program for Data Acquisition (8080 Language)

	MVI	A,02H	Accumulator set to 2
	STA	FXF9H	Channel 2 selected
	STA	FXFAH	Convert command issued
LOOP:	LDA	FXFBH	Status word read
	RLC		
	JNC	LOOP	EOC bit checked
	LHLD	FXFCH	12 bit ADC data read into register pair H and L
	SHLD	EFF0	Contents of H and L stored in memory address EFF0 and EFF1.
	HLT		Halt Command

RTI-1221 – Analog Output Board

Address Selection – The RTI-1221 occupies 16 consecutive memory addresses (FXF0 to FXFF). Their location is selectable at an on-board memory address/card select socket with either a DIP switch or jumper plugs.

Card Select – This feature is the same as that on RTI-1220.

DAC Data – Analog output data can be written into memory in either single 8 bit byte format or in 10 bit resolution two byte format (e.g. – for DAC1 data, 10 bit data is written into FXF6 and FXF7. 8 bit data would be written into FXFB). When using single byte data, the two LSB's of the DAC are set to zero.

DAC Reset – All DACs may be simultaneously reset to zero voltage output by writing any data word into the DAC reset memory address (FXFC).

Sample Program for Analog Output (8080 Language)

LXI	H,OFFFH	H and L pair loaded with all 1's.
SHLD	FXF4	Contents of H and L are loaded into DAC2 (10 bit data)
HLT		

MEMORY ADDR.	8-BIT BYTE FORMAT	BYTE NAME	4-BIT	BYTE NAME
FXFF	ϕ ϕ ϕ ϕ ϕ S_2 S_1 S_0	CARD SELECT	ϕ S_2 S_1 S_0	CARD SELECT
FXFE		NOT USED		NOT USED
FXFD		NOT USED		NOT USED
FXFC	ϕ ϕ ϕ ϕ ϕ ϕ ϕ ϕ	DAC'S RESET	ϕ ϕ ϕ ϕ	DAC'S RESET
FXFB	MSB B_8 B_7 B_6 B_5 B_4 B_3 B_2	DAC 1 DATA	ϕ ϕ MSB B_8	DAC 1 DATA
FXFA	MSB B_8 B_7 B_6 B_5 B_4 B_3 B_2	DAC 2 DATA	B_7 B_6 B_5 B_4	DAC 1 DATA
FXF9	MSB B_8 B_7 B_6 B_5 B_4 B_3 B_2	DAC 3 DATA	B_3 B_2 B_1 LSB	DAC 1 DATA
FXF8	MSB B_8 B_7 B_6 B_5 B_4 B_3 B_2	DAC 4 DATA	ϕ ϕ MSB B_8	DAC 2 DATA
FXF7	ϕ ϕ ϕ ϕ ϕ ϕ MSB B_8	DAC 1 DATA	B_7 B_6 B_5 B_4	DAC 2 DATA
FXF6	B_7 B_6 B_5 B_4 B_3 B_2 B_1 LSB	DAC 1 DATA	B_3 B_2 B_1 LSB	DAC 2 DATA
FXF5	ϕ ϕ ϕ ϕ ϕ ϕ MSB B_8	DAC 2 DATA	ϕ ϕ MSB B_8	DAC 3 DATA
FXF4	B_7 B_6 B_5 B_4 B_3 B_2 B_1 LSB	DAC 2 DATA	B_7 B_6 B_5 B_4	DAC 3 DATA
FXF3	ϕ ϕ ϕ ϕ ϕ ϕ MSB B_8	DAC 3 DATA	B_3 B_2 B_1 LSB	DAC 3 DATA
FXF2	B_7 B_6 B_5 B_4 B_3 B_2 B_1 LSB	DAC 3 DATA	ϕ ϕ MSB B_8	DAC 4 DATA
FXF1	ϕ ϕ ϕ ϕ ϕ ϕ MSB B_8	DAC 4 DATA	B_7 B_6 B_5 B_4	DAC 4 DATA
FXF0	B_7 B_6 B_5 B_4 B_3 B_2 B_1 LSB	DAC 4 DATA	B_3 B_2 B_1 LSB	DAC 4 DATA

ALL OPERATIONS ARE MEMORY WRITES

X: USER SELECTED

ϕ: BIT IGNORED

RTI-1221 Memory Image Format

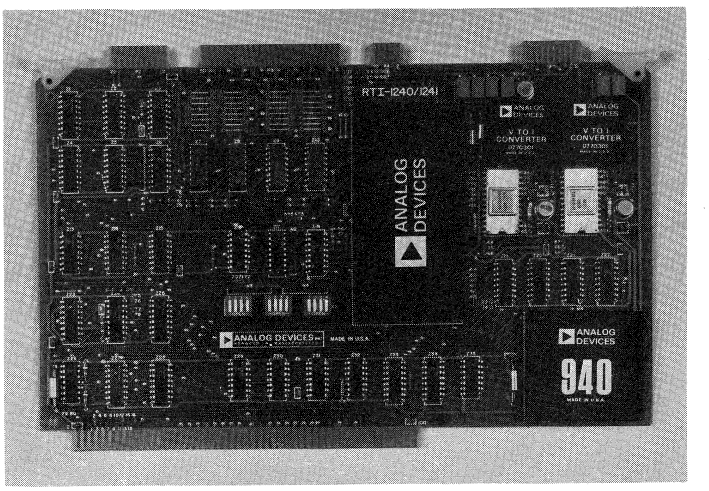
T.I. TM-990/100M Compatible Analog I/O Subsystems

MODELS RTI-1240, 1241, 1242, 1243

FEATURES
Complete Analog I/O Subsystems
T.I. 16 Bit TM-990/100M Compatibility
Memory Mapped I/O Interface
12 Bit Resolution and Accuracy
Optional Single +5V Power
Wire Wrap Feature Selection

INPUT SUBSYSTEMS
256 Channel Expansion Capability
Input Overvoltage Protection
Software or Resistor Programmable Gain
Interrupt Operation Capability
Optional Analog Output Channels

OUTPUT SUBSYSTEMS
8 High Current Logic Driver Outputs
4 or 8 Analog Output Channels
Detailed User's Guide



SERIES DESCRIPTION

The RTI-1240 Series are complete, 12 bit resolution, analog I/O subsystems which are electrically and mechanically compatible with the Texas Instruments 16 bit TM-990/100M single board microcomputer. The series is comprised of an input only board, an output only board, and a combination I/O board; each of which interfaces to the microcomputer as a block of 8 or 16 address locations (memory mapped interface). All data bus, control bus and address bus connections to the microcomputer are made by simply plugging the board into the computer card cage. The analog signals connect at the opposite board edge from the digital bus connector.

Many additional capabilities, features and options are included to reduce both the hardware and the software effort required in interfacing analog signals to the microcomputer. The designer is then free to spend more time and effort on the particular application instead of on designing basic building block functions.

RTI-1240 ANALOG INPUT SUBSYSTEM —

GENERAL DESCRIPTION

The basic function of the RTI-1240 is to acquire signals and present them to the microcomputer in digital form. The design is comprised of a protected input multiplexer, either a resistor or a software programmble gain instrumentation amplifier, a sample and hold amplifier, a 12 bit A/D converter and the associated digital interface logic as shown in the block diagram.

INPUT MULTIPLEXER

The RTI-1240 is available with up to 32 single-ended/16 differential protected input channels on-board, and has the capability of off-board expansion to 256 channels using on-board control logic. The multiplexer (MUX) channel can be randomly selected at the MUX word in the memory map as shown further. The MUX can also be incremented to the next channel upon receipt of a convert command. This auto increment feature is enabled by a software command to the setup word which allows scanning and random channel addressing to be mixed under software control.

INSTRUMENTATION AMPLIFIER/SAMPLE AND HOLD AMPLIFIER

The RTI-1240 is available with two types of instrumentation amplifiers (IA) which provide 12 bit compatible CMRR and CMV specifications. The software-programmable-gain (1-2-4-8) IA provides dynamic range expansion through subranging as well as the flexibility of using different gain settings for each input channel to accommodate different signal levels. The resistor-programmable gain IA may be used for input ranges from 10mV F.S. to ±10V F.S. There is very little loss of speed and no degradation of linearity at high gains.

The sample and hold amplifier (SHA) allows sampling of high slew rate signals and is automatically switched to the hold mode upon receipt of a convert command. The RTI-1240 also has a built-in provision which delays the convert command to allow for input section settling following a gain change or channel change. For very high gain applications, the convert command delay can be increased either through software or by addition of a single resistor.

SPECIFICATIONS (typical @ +25°C and nominal supply voltage)

ANALOG INPUT	COMBINATION I/O BOARDS		INPUT ONLY BOARDS	
Model Numbers	RTI-1241-R	RTI-1241-S	RTI-1240-R	RTI-1240-S
Input Channels				
Basic Board	16 SE, 16 PD, 8 Diff.[1]	*	*	*
Expansion: On-Board	32 SE, 32 PD, 16 Diff.[1]	*	*	*
Off-Board	256 Total	*	*	*
Input Range at Card Edge[2]	10mVFS to ±10VFS	0.625 to ±10VFS	*	**
Current Loop Inputs[3]	0 to 50mA, 0 to 20mA, etc.	*	*	*
Input Protection	±(V_{CC} +20V)	*	*	*
Switching	Break-Before-Make	*	*	*
Input Impedance	$>10^8\Omega$	*	*	*
Input Bias Current	±50nA max	±5nA max	*	**
0 to +70°C	±70nA	±50nA	*	**
Instrumentation Amplifier	Resistor Programmable Gain	Software Programmable Gain	*	**
Gain Range	1 to 1000 V/V	1, 2, 4, 8 V/V	*	**
CMV	±10V min	*	*	*
CMRR (dc–500Hz)	76dB min	*	*	*
Input Settling Time[4]	15µs max (G = 1)	10µs max (G = 1 to 8)	*	**
ADC Input Ranges[1]	±5V, ±5.12V, ±10V, ±10.24V, +10V, +10.24V	*	*	*
Resolution	12 Bits	*	*	*
Conversion Time	25µs max	*	*	*
Throughput Rate[5]	40,000 Channels/sec	*	*	*
Output Codes[1]	Binary, Offset Binary, Two's Complement	*	*	*
Nonlinearity Error	±1/2LSB typ (±1LSB max)	*	*	*
Offset Error[6]	Adj. to Zero	*	*	**
Gain Error[6]	Adj. to Zero	*	*	*
Offset TC	$\pm(1 + \frac{20}{G})\mu V/^\circ C$ (RTI)	±30µV/°C (RTI)	*	**
Gain TC	±20ppm of rdg/°C (RTI)	±25ppm of rdg/°C (RTI)	*	**
Noise Error[7]	±1/4LSB max	*	*	*
Overall Error @ G = 1[8]	±1LSB max	*	*	*
SHA Aperture Delay	90ns	*	*	*
SHA Aperture Width	20ns	*	*	*
SHA Aperture Uncertainty	5ns	*	*	*

ANALOG OUTPUT			OUTPUT ONLY BOARDS	
Model Number	RTI-1241-R	RTI-1241-S	RTI-1242	RTI-1243
Output Channels	2	2	4	8
Resolution	12 Bits	*	*	*
Output Ranges[1] (with on board Ref)	+5V, +10V, ±2.5V, +5V, +10V	*	*	*
Output Current	±5mA min @ ±10V	*	*	*
Nonlinearity Error @ +10V Ref	±0.01% max	*	*	*
Offset Error	Adj. to Zero	*	*	*
Gain Error	Adj. to Zero	*	*	*
Offset TC	±15µV/°C	*	*	*
Gain TC	±15ppm/°C	*	*	*
Settling Time[8] (for 20V step to ±0.01%)	10µs	*	*	*
Reference Range External[9]	1V to +10V	*	*	*
Input Codes	Binary, Two's Complement, or Offset Binary	*	*	*
OTHER OUTPUTS	2 Optional Current Loops	*	8 Logic Drivers	***
Type	ISA-S50.1, Type 3, Class 6	*	Open Collector	***
Output Current Range[10]	4-20mA	*	300mA sink @ 0.7V	***
Supply Voltage Range	+15V to +30V	*	+30V max	***
Input Voltage Range	0V to +10V	*		
Offset Error	Adj. to Zero	*		
Gain Error	Adj. to Zero	*		
Offset TC	±0.4µA/°C	*		
Gain TC	±30ppm/°C	*		
Nonlinearity Error	±0.01% max	*		
Settling Time	50µs max to 0.02%	*		

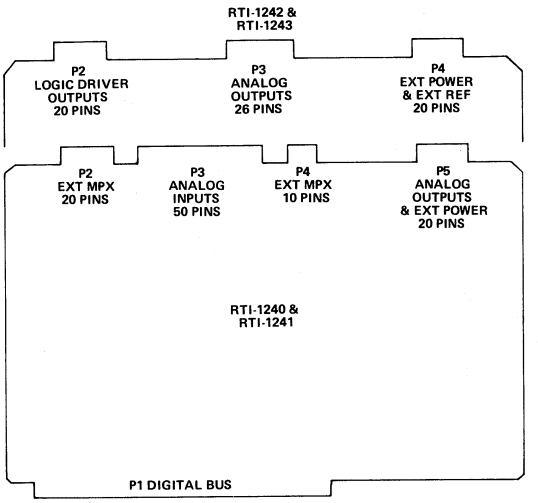
POWER REQUIREMENTS					
Model Number	RTI-1240	RTI-1241	RTI-1242	RTI-1243	V/I
Without Optional dc-dc					
+15V ±3%	40mA	50mA	45mA	50mA	10mA
–15V ±3%	40mA	80mA	80mA	150mA	2mA
+5V ±5%	1100mA	1100mA	900mA	1000mA	0mA
With dc-dc Option					
+5V ±5%	1.4A	1.5A	1.3A	1.6A	mA

MECHANICAL (All Models)	
Size	7.5" x 11.0" (190.5mm x 279.4mm)
Card Outline	Conforms to Texas Instruments Drawing SK922321
Card Spacing	0.6" min (15.2mm)

*Same as for RTI-1241-R
**Same as for RTI-1241-S
***Same as for RTI-1242
Specifications subject to change without notice.

NOTES
[1] User selectable by wire wrap jumpers.
[2] The full scale input signal range is the A/D converter range divided by the gain of the instrumentation amplifier.
[3] The user may install one resistor per channel (SE or Diff) to convert the input current to the proper voltage range. Any input current span can therefore be accommodated.
[4] Input settling time applies to either a multiplexer channel change or a software controlled gain change. The settling time increases to 50µs @ G = 1000.
[5] The effective throughput rate is determined by the user's software data handling capability. The max throughput rate listed is exclusive of the CPU interface operations which may or may not be completed during the subsystem's conversion time. In CPU hold mode, the user's software and interface time obviously must be added to the conversion time to determine the maximum effective throughput rate.
[6] For any one programmable gain setting. Maximum offset shift of ±1LSB or gain shift of ±0.02% when using a programmable gain setting other than the one used during calibration.
[7] Noise error increases to ±1/2LSB max @ G = 8 for the SPG models and to ±1LSB @ G = 100 for the RPG models.
[8] Overall error increased to ±2LSB max @ G = 8 for the SPG models and 2LSB max @ G = 1000 for the RPG models.
[9] Overall error increases to 0.1% @ 1V external reference.
[10] The current loop load resistance range is 0Ω to 450Ω with a +15V supply. A load resistance of 500Ω may be used with a +18V supply.

MECHANICAL OUTLINE AND CONNECTOR DIAGRAM



ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
RTI-1240-R	Input Board with Resistor Programmable Gain Amplifier
RTI-1240-S	Input Board with Software PGA
RTI-1241-R	I/O Board with Resistor PGA
RTI-1241-S	I/O Board with Software PGA
RTI-1242	Output Board with Four DACs
RTI-1243	Output Board with Eight DACs
ACCESSORIES	
0A08	4-20mA V/I Module
0A09	DC-DC Converter
0A10	Multiplexer Expansion Kit (2 ea. HI-508A)
CONNECTORS	
AC1556	20 pin, Card Edge*
AC1557	50 pin, Card Edge*
AC1558	10 pin, Card Edge*
AC1559	26 pin, Card Edge*

*ALL CONNECTORS HAVE 3' OF COLOR CODED CABLE ATTACHED

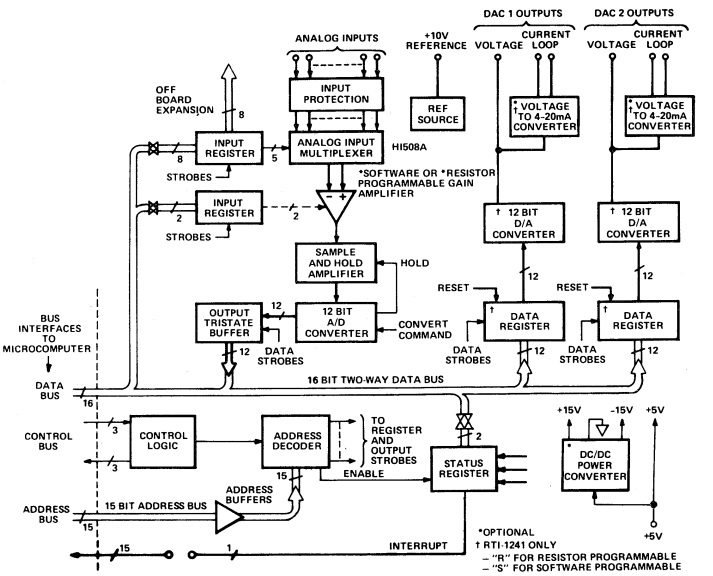


Figure 1. RTI-1240 & RTI-1241 Functional Block Diagram

ANALOG/DIGITAL CONVERTER

The RTI-1240 provides the user the choice of selecting either single instruction programming for software simplicity or variations of polled status programming for the highest data throughput rates.

The RTI-1240 contains a fast, 12 bit, successive approximation converter. The user can select one of six ADC input ranges and one of three output codes with wire-wrap jumpers.

The subsystem can be used in any of three operation modes:

1. The *CPU Hold Mode* allows the user to initiate conversions and read or operate upon ADC data with a single instruction. This results in the simplest software programs for acquisition of data.
2. In the *Interrupt Mode*, the setting of the end of conversion bit in the status word can be made to create a CPU interrupt. Reading the status word clears both the EOC bit and the associated interrupt, and is the only acknowledgement required. This results in very efficient polling.
3. In the normal *Polled Status Mode*, the CPU reads the EOC bit in the status word to determine if the ADC data is valid. This allows the most software flexibility and can be mixed with the software controlled EOC Interrupt Mode for truly versatile data acquisition system operation.

MICROCOMPUTER INTERFACE

The digital hardware interface to the microcomputer is made through the T.I. 100 pin digital bus. Each board's base address is selected at the on-board address sockets while the least significant bits of any memory reference instruction address determine which word is addressed in the memory maps (shown further).

The optional status words allow the user some flexibility during polling to read either ADC data or gain and multiplexer data at the same time that the status word is read. An under-range bit for gain ranging applications is available in the status word to indicate when the signal just converted is small enough to permit a higher gain and that a higher gain is still available.

Several timing and control signal lines are available at the board edge for signal and converter synchronization (converter status, external convert command, internal convert commands and the convert command delay gate). With software control over the EOC Interrupt, External Convert Command, and Auto Increment features, and with the converter signals readily available, the user has complete control over the analog input function.

POWER SUPPLY

In addition to the +5V logic power required for the digital interface circuits, the RTI-1240 series require ±15V power for its analog circuitry. These voltages can be supplied by the user at a card edge connector or the ±15V can be supplied from an optional card mounted dc-dc converter (P/N0A09).

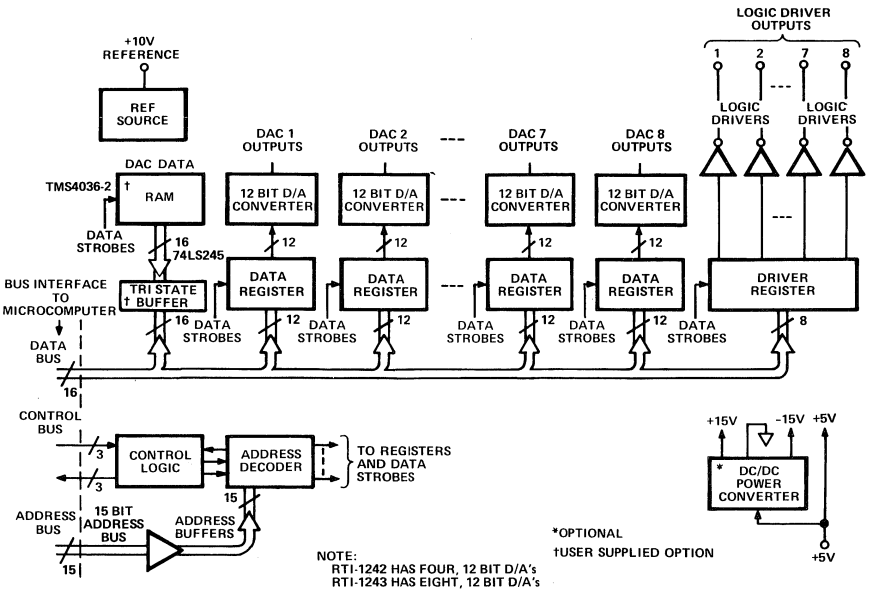


Figure 2. RTI-1242 & RTI-1243 Functional Block Diagram

RTI-1241 COMBINATION ANALOG I/O INTERFACE

The RTI-1241 provides the same analog input functions as the RTI-1240 and in addition has two channels of 12 bit analog output.

ANALOG OUTPUTS

The RTI-1241 has two 12 bit resolution D/A converters (DAC's) providing up to ±10V analog output in several ranges. The input coding and output range of each DAC are independently selectable by wire-wrap jumpers.

REFERENCE

The +10V reference for the DAC's is located on-board. However, should the user desire, an external reference between +1V and +10V may be used.

RESET

By installing optional jumpers, the DAC's will reset to zero volts upon system reset. This feature can be used to reduce output transients when system power is applied.

CURRENT LOOP OUTPUTS

The two analog output channels can also be ordered with optional 4-20mA current loop outputs for use in process and industrial control applications. These voltage to current (V/I) converter modules (P/N 0A08) meet all the requirements of ISA-S50.1 for Type 3, Class L, non-isolated 4-20mA current loop transmitters.

RTI-1242 AND RTI-1243 OUTPUT SUBSYSTEMS

The RTI-1242 and 1243 output subsystems provide 4 or 8 channels of analog output and 8 high current, logic driver outputs. The block diagram above shows the basic output functions and optional features.

LOGIC OUTPUTS

The eight digital outputs are software controlled, open collector, drivers capable of 300mA maximum sink current and voltages up to +30V. They can be used to provide "on/off" system functions for relay, solenoid, and valve control.

ANALOG OUTPUTS

The RTI-1242 and RTI-1243 have four or eight 12 bit DAC's respectively. Each DAC's input code and output range is independently selectable.

REFERENCE

The RTI-1242 and RTI-1243 each have a single on-board +10V precision reference to provide excellent tracking between channels. Each board also provides inputs for external references. The user can select an external reference between +1V and +10V to provide tracking between several boards or for scaling or multiplying functions.

REMOTE LOAD SENSING

Each DAC has an external load sensing capability for applications where the load is to be located a considerable distance from the DAC output. Without this feature, IR voltage losses in the output line could degrade overall accuracy.

READBACK

Both output subsystems provide sockets for RAM's and buffers (T.I. P/N TMS4036-2 and 74LS245) to allow DAC and driver data to be read back to the microcomputer. This feature offers additional software flexibility and convenience since it eliminates the need for scratch pad memory or software overhead to store data written to the RTI-1242 or RTI-1243 DAC's and drivers.

RESET

When enabled by wire-wrap jumpers, the DAC's and/or logic drivers, will reset upon occurrence of a system reset. The DAC's will reset to 0V and the logic drivers reset to the "off" (High level) state. This feature will allow the system to start from a known state after initially applying power to the system or after a momentary loss of power.

INPUT BOARD MEMORY INTERFACE
RTI-1240 AND RTI-1241

The RTI-1240 and RTI-1241 have the same basic memory image format. The sole difference is that the RTI-1241 I/O board had two DAC words corresponding to the two on-board DAC's. These two addresses are not used on the RTI-1240.

BASE ADDRESS SELECTION

The RTI-1240 and RTI-1241 subsystems occupy 8 consecutive 16 bit word addresses. To determine the most significant hexadecimal digits of the base address, the user installs switches or shorting plugs at three on-board sockets.

DAC DATA WORDS (BASE + 0 AND + 2, RTI-1241 ONLY)

DAC outputs are set by writing the digital data to the corresponding DAC address. Data can be in either binary, offset binary or two's complement coding.

SETUP WORD (BASE + 4)

By loading the three most significant bits of the setup word, any of three software controlled features may be enabled. The MSB is the End of Conversion (EOC) Interrupt enable bit. By enabling this feature the EOC signal from the ADC will create an interrupt on the interrupt line previously selected by a wire wrap jumper. When bit 2 is set, the multiplexer will increment to the next sequential channel just after the SHA holds for each conversion in the Auto Scan Mode. Writing a one to bit 3 enables external convert command signals to be applied to the converter. These three software enabled features allow the user flexibility in creating system software for each particular application.

GAIN WORD (BASE + 6, "S" MODELS ONLY)

By writing the appropriate code into this word, the gain of the software programmable instrumentation amplifier is set. Auto-gain-ranging for a dynamic range of 15 bits is possible through the use of this feature.

MULTIPLEXER CHANNEL WORD (BASE + 8)

Any random input channel can be selected by writing the channel address code into this word. The beginning channel of a scan using the auto-scan feature is also selected in this manner. Up to 256 channels can be addressed at this location using on-board logic.

CONVERT COMMAND WORD (BASE + A)

By writing any data into this word a convert command is issued to the ADC. This is the standard mode of operation but other means of creating this command exists. Externally generated convert commands can be connected via the P-2 edge connector. Convert commands can also be generated by ADC data read instructions in CPU Hold Mode operation.

STATUS WORD (BASE + C)

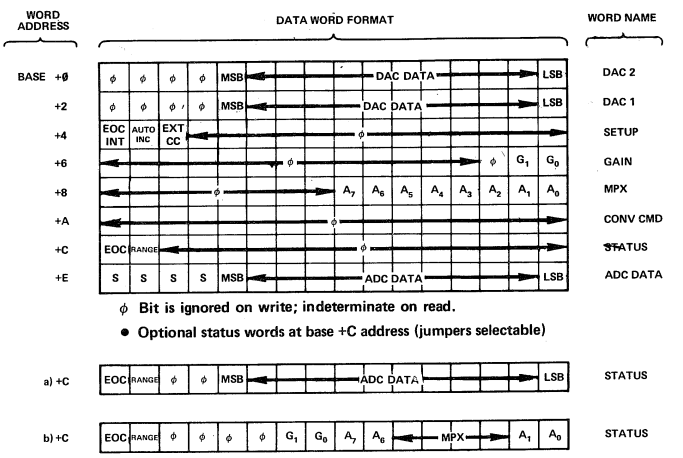
The end of conversion (EOC) bit in the status word is set when the conversion is complete. Reading the status word resets the EOC bit and any associated interrupt.

The status word also contains an underrange bit for gain ranging applications on models equipped with a software programmable gain amplifier. This bit is set whenever a higher gain range is still available and when the signal being measured is small enough to permit the use of a higher gain.

Additional information can be provided in the status word by selecting wire-wrap jumpers. Gain and MUX channel data are made available with one jumper and the ADC data is available with the other jumper selection. These status word variations allow very efficient programs and high operating speeds.

ADC DATA WORD (BASE + E)

ADC data is available at this address (and, if enabled by jumper option, in the status word). It remains valid until the next conversion begins. When using two's complement code and a bipolar input range, the most significant four bits of the ADC Data word are sign extension bits.



RTI-1240, 1241 Address Map

SAMPLE PROGRAM FOR NORMAL MODE

```
NXT   SETO  *R1      Send conv. comm.        ]
      INCT  R2       Update data store addr. |
      DEC   R3       Decr. sample counter    | Conv.
      JLE   OUT      Out if done             | in
CK    INV   *R5      Status (Data Ready)     | Process
      JLT   CK       Check Loop              |
      MOV   *R4,*R2  Store Data Sample       |
      JMP   NXT      Next Sample             ]
OUT
```

This program takes N samples on one channel and stores them in successive memory locations.

Registers: R1 – Conv. Comm. Address
R2 – Data Storage Address Pointer
R3 – Sample Counter: Initialize to No. of Samples
R4 – ADC Data Address
R5 – Status Word Address

SAMPLE PROGRAM FOR WAIT MODE

```
NXT   MOV   *R4,*R2 +  ]  Start Conversion; Read Resulting
                       |  Data; Store in Memory; Update
                       ]  Data Store Address
      DEC   R3         Decr. Sample Counter
      JH    NXT        Out if Done. Otherwise Next Sample
```

This program does the same job as the Normal Mode example above. In this case, but not in general, the speed is about the same.

OUTPUT BOARD MEMORY INTERFACE

BASE ADDRESS SELECTION

This is set in the same manner as for the RTI-1240 and RTI-1241 as shown on the previous page.

DRIVER DATA WORD (BASE + 10)

The logic drivers may be turned "on" (to sink up to 300mA of current) by writing ones at the appropriate driver data bits in the driver data word. When turned "off" by writing a zero to the corresponding bit each driver takes up to +30V at the collector. The logic drivers are capable of being reset to the "off" condition upon system reset by connecting a wire wrap jumper.

DAC DATA WORDS (BASE + 1A THROUGH 1E)

As with the RTI-1241 each DAC receives update information from the data written into the corresponding DAC data word. By wire wrap jumper the output subsystem DAC's may also be reset to 0 volts output upon receipt of a system reset.

OPTIONAL MEMORY IMAGES

If the logic drivers are not used, the user may select an optional address map for the RTI-1243 with only 8 words. Another 8 word address map is available for use with the RTI-1242.

SAMPLE PROGRAM FOR ANALOG OUTPUTS

```
NXT   MOV   *R2+, *R6
      DEC   R3
      JLE   OUT
      JMP   NXT
```

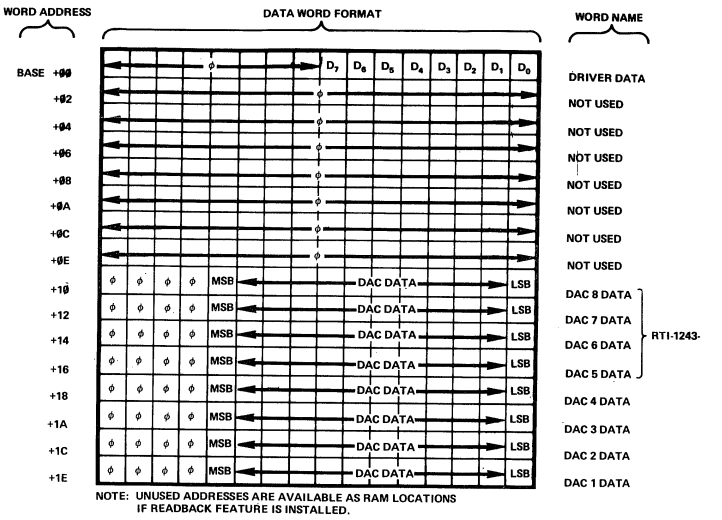
This program outputs a set of samples stored in memory to the DAC channel whose address is stored in R6. Transfer rate is approximately 1 sample/17 microseconds. If desired, a delay loop can be inserted to permit a slower update rate

Register usage:

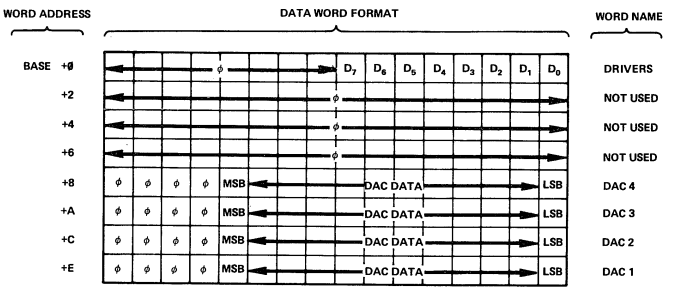
- R2: Memory address of data block
- R3: Sample counter
- R6: Address of DAC in use

DETAILED USER'S MANUAL

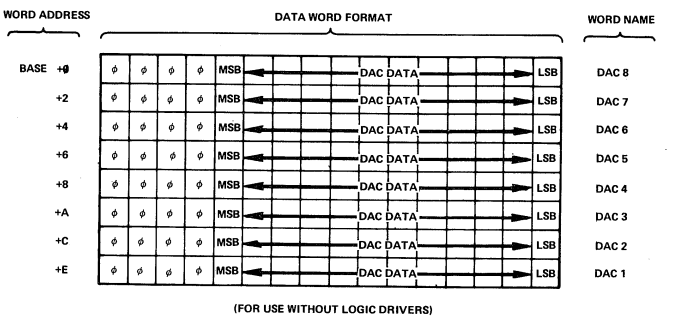
A detailed manual giving installation and operation instructions along with suggested software routines for calibration and operation is provided with each RTI-Subsystem. This manual also provides theory of operation as well as schematics and tables to enable the user to install, and start operating the system as easily and quickly as possible.



Standard RTI-1242 & RTI-1243 Address Map



Optional RTI-1242 Address Map



Optional RTI-1243 Address Map

Power Supplies

AC/DC Power Supplies

MODULAR AC/DC POWER SUPPLIES

Analog Devices ac/dc Power Supplies are designed to provide OEM's and circuit designers with a broad line of high reliability, regulated and short circuit protected power supplies at low overall cost. These modules are available with 5 volt to 24 volt output (single and dual), and current ratings from 25mA to 2 Amps. Most Analog Devices Power Supplies are available from stock in both large and small quantities. Substantial discounts apply on quantity orders.

ADVANTAGES

Packaged circuit modules have found wide acceptance. Engineers have discovered the convenience and economy of plug-in building blocks . . . op amps, logic cards, miniature A/D and D/A converters are now available in wide varieties. Now a complete line of modular power supplies is available from Analog Devices. These encapsulated units are shipped ready to use, at prices below the internal manufacturing cost of most OEM users. Further savings and reduced lead time are achieved by eliminating engineering start-up, documentation costs, and manufacturing delays. Designed by experts in linear and digital logic technology, these units offer features that you would expect to find only in considerably more expensive supplies.

ENCAPSULATED MODULES

This line of modular power supplies covers most popular applications. All designs employ the series pass technique for regulation, thereby achieving excellent line and load regulation with very low ripple on the output. The output is also free from spikes which are typical of switching supplies. Another advantage of the series pass design is the ease with which it may be applied. Since the return line carries no switching transients, ground loop problems are limited to the circuit being powered, and not the power supply. Still further advantages of the series pass design are the absence of two other problems reserved for switching supplies; beat frequency problems due to an internal chopper and reflected input ripple.

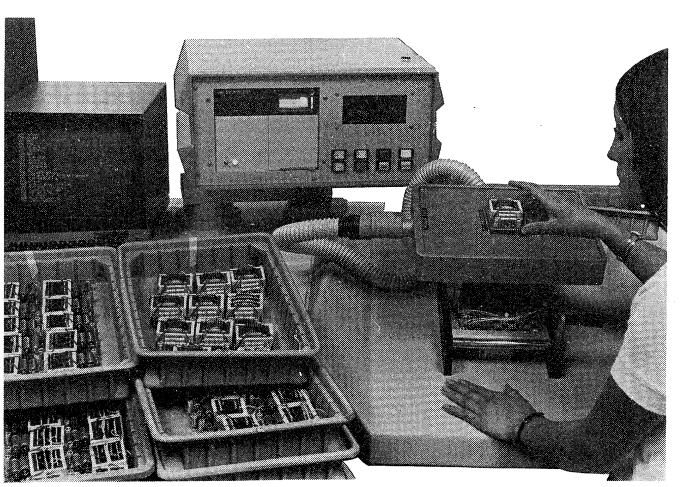
All modular supplies available from Analog Devices feature current limiting. This technique of overload and short circuit protection guarantees that the supply will not only be protected when overloaded, but it insures that the supply will be free from start up and latch up problems characteristic of "current fold-back" schemes.

CHASSIS MOUNT SUPPLIES

This series of supplies consists of the same reliable designs as described above but input and output connections are made by a terminal strip rather than pins. They are intended for use in designs where it is either undesirable or impractical to utilize printed circuit boards or sockets. Mounting is readily accomplished by four threaded inserts on the bottom of the unit.

AUTOMATIC TESTING

Automatic power supply testers are used for 100% testing of all modular supplies. Supplies are tested before encapsulation, after encapsulation and once again before being shipped. This stringent quality assurance guarantees customer satisfaction.



SPECIFICATIONS

Complete electrical performance specification for all ac/dc supplies are shown on pages 594 and 595. Complete mechanical specifications are shown on page 597.

DC/DC Converters

MODULAR DC/DC CONVERTERS

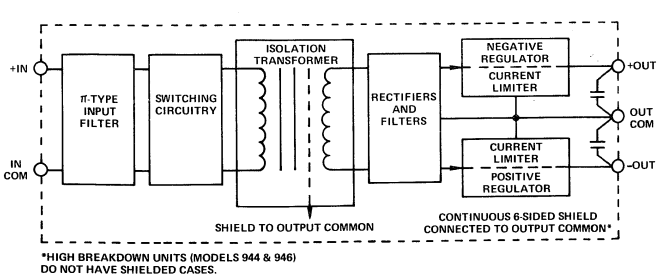
Analog Devices' 940 series comprises a full line of compact dc-to-dc converters which satisfy a wide variety of floating power requirements in analog (Function Modules, Op Amps, Instrumentation Amps) and digital (A-D/D-A) applications. All 940 series converters offer accurate (±0.05% max error), regulated outputs with very low noise (<50mV p-p in 20MHz B.W.). Models 940, 941, 942, 943, and 945 are high efficiency designs (typically over 60% at full-load) that feature complete 6-sided continuous shielding for EMI/RFI protection. All devices use π-type input filters to reduce reflected input ripple current.

SHORT CIRCUIT PROTECTION

Constant current limiting insures that the converters will resume normal operation after a short circuit condition is removed without having to turn off and restart the input power system. This trait is essential in applications where fault-induced system shutdowns are costly and inconvenient. All models will also turn on when reverse polarity current is injected into the output. This feature is required whenever power turn-on sequences can cause some system voltages to come up before the dc/dc power causing small currents to flow into the dc/dc output.

DUAL OUTPUT MODELS

Logic to analog power conversion is available with models 940, 941 and 944. These modules deliver floating analog power (±12V or ±15V) from logic power sources (5V). This permits analog networks to be separated from digital systems in order to avoid intersystem grounding problems.



Block Diagram — Dual Output Supplies

ISOLATION RATINGS

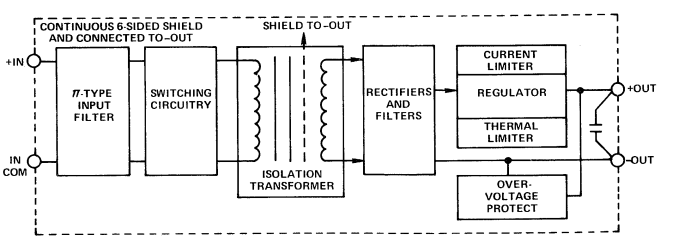
High input-to-output breakdown is the outstanding feature of models 944 and 946. These designs boast 8000V dc breakdowns with input-to-output impedance of $10^{11}\|5pF$. The 944 provides ±15V from a 5V input while 946 operates from 23 to 31 volt inputs. Both modules are packaged in 3″ x 2″ x 0.6″ non-metallic cases. In data acquisition systems, these converters can be used to power front-end circuitry in applications where high CMV may be encountered.

INPUT VOLTAGE VERSATILITY

A versatile input range is offered by models 945 and 946. They derive regulated floating ±15V outputs from any combination of inputs between 23 and 31 volts. The 945 and 946 converters can be powered from dual 12 volt (24V), dual 15 volt (30V), +24 volt or +28 volt power supplies, for compatibility with most analog systems.

SINGLE OUTPUT MODELS

Logic to logic power conversion is offered by models 942, and 943. These modules derive a high current 5V output from standard +5V logic supplies (600mA — model 942; 1000mA — model 943). This allows remote digital systems to be isolated from the central system in order to safeguard against shorts and overloads in remote system causing central system power interruption.



Block Diagram — Single Output Supplies

RELIABILITY

High reliability is assured by the conservative design techniques used in all converters. Capacitors operate with at least a 30% margin below their rated working voltage. Semiconductor junctions run at least +25°C below rated temperatures under full load at +71°C ambient. Additional reliability is imparted by a 100 hour factory burn-in at full load. Very low junction-to-case thermal resistance enables all units to operate without derating or heat sinks over the full temperature range and to withstand short circuits for at least 8 hours at +71°C. Specifications: Complete electrical performance specification for all dc/dc converters are shown on page 596. Complete mechanical specifications are shown on page 597.

Product Specifications

MODULAR AC/DC POWER SUPPLIES

900 SERIES AC/DC POWER SUPPLIES FEATURES

- Current limited short circuit protection.
- Options for international line voltages.
- Current outputs of 25mA to 350mA for dual output supplies, 250mA to 2A for single output supplies.
- Free-air convection cooling-no external heat sink required.

GENERAL SPECIFICATIONS FOR ALL MODELS

Input Voltage: 105V ac to 125V ac, 50 to 400Hz
Temperature Coefficient: 0.015%/°C
Input Isolation: 50 megohms
Breakdown Voltage: >500V
Operating Temperature: -25°C to +71°C
Operating at elevated temperatures may require derating. Consult factory.
Storage Temperature: -25°C to +85°C
Short Circuit Protection: All of the 900 Series Power Supplies employ current limiting. They can withstand substantial overload including direct shorts. Prolonged operation should be avoided since excessive temperature rises will occur.
Mechanical Specification: see page 597.
Options: "E" Option; 205-240V ac, 50 to 400Hz input
"F" Option; 90-110V ac, 50 to 400Hz input
"H" Option; 220-260V ac, 50 to 400Hz input
"I" Option; Units have interwinding shield with separate ground lead. Input to output capacitance is less than 10pF.

Order option desired as a suffix to model number. No additional additional charge for "E" option. Additional charge for "I" option.

DUAL POWER SUPPLIES

SPECIFICATIONS (typical @ +25°C and 115V ac 60Hz unless otherwise noted)

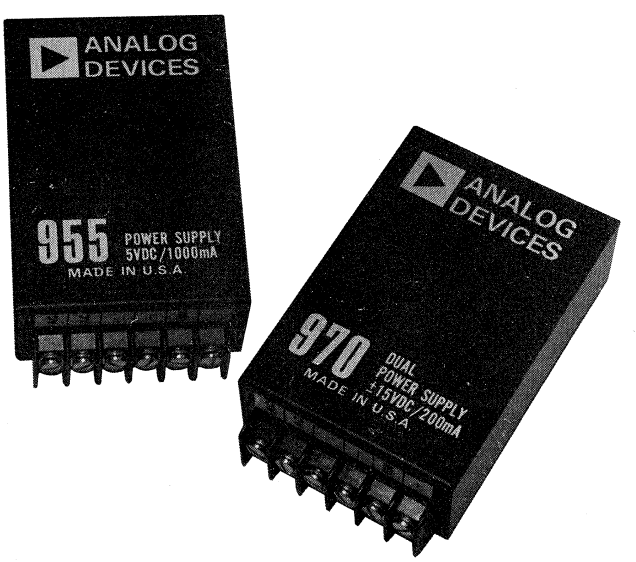
Model	Output Voltage	Output Current	Line Reg. Max	Load Reg. Max	Output Voltage Error Max	Ripple and Noise rms Max	Options Available
915	±15V	25mA	0.2%	0.2%	±1%	1mV	E, F, H
904	±15V	50mA	0.02%	0.02%	+200mV -0mV	0.5mV	E, F, H
902	±15V	100mA	0.02%	0.02%	+300mV -0mV	0.5mV	E, I, F, H
902-2*	±15V	100mA	0.02%	0.02%	+300mV -0mV	0.5mV	E, F, H
920	±15V	200mA	0.02%	0.02%	+300mV -0mV	0.5mV	E, F, H
925	±15V	350mA	0.02%	0.02%	±1%	0.5mV	E
907	±12V	25mA	0.2%	0.2%	±1%	1mV	—
908	±12V	100mA	0.02%	0.02%	±1%	1mV	—
921	±12V	240mA	0.02%	0.02%	+300mV -0mV	0.5mV	E, F, H
934	±24V	100mA	0.02%	0.02%	±1%	1mV	—

*Differs from model 902 only in case height (0.875" versus 1.25" for model 902).

LOGIC SUPPLIES

SPECIFICATIONS (typical @ +25°C and 115V ac 60Hz unless otherwise noted)

Model	Output Voltage	Output Current	Line Reg. Max	Load Reg. Max	Output Voltage Error Max	Ripple and Noise rms Max	Options Available
906	5V	250mA	0.02%	0.04%	±1%	1mV	—
903	5V	500mA	0.02%	0.04%	±1%	1mV	E, F, H
905	5V	1000mA	0.02%	0.05%	±1%	1mV	E, F, H
922	5V	2000mA	0.02%	0.05%	±1%	1mV	E, F, H



CHASSIS MOUNT SUPPLIES

SPECIFICATIONS (typical @ +25°C and 115V ac 60Hz unless otherwise noted)

Model	Output Voltage	Output Current	Line Reg. Max	Load Reg. Max	Output Voltage Error Max	Ripple and Noise rms Max	Options Available
952	±15V	100mA	0.05%	0.05%	±2%	1mV	E, F, H
970	±15V	200mA	0.05%	0.05%	±2%	1mV	E, F, H
973	±15V	350mA	0.05%	0.05%	±2%	1mV	E
975	±15V	500mA	0.05%	0.05%	±2%	1mV	E
955	5V	1000mA	0.05%	0.15%	±2%	2mV	E, F, H
956	5V	2000mA	0.05%	0.15%	±2%	2mV	E

HIGH EFFICIENCY, LOW NOISE, DC/DC CONVERTERS

940 SERIES DC/DC CONVERTERS FEATURES

- Inaudible (>20kHz) converter switching frequency.
- Continuous, Six-Sided EMI/RFI shielding except on models 944 & 946.
- Free air convection cooling - no external heat sink or specification derating is required over operating temperature range.
- Output short circuit protection (either output to common) for at least 8 hrs. at T_A = +71°C.
- Output current limiting at 150% of rated current.
- Automatic restart after short condition removed.
- Automatic starting with reverse current injected into outputs.

GENERAL SPECIFICATIONS FOR ALL MODELS

Line Regulation - full range: ±0.05% max
Load Regulation - no load to full load: ±0.05% max
Output Noise and Ripple: 1mV rms max
Input Filter Type: π
Operating Temperature Range: -25°C to +71°C
Storage Temperature Range: -40°C to +150°C
Mechanical Specification: see page 597.

DC/DC CONVERTERS

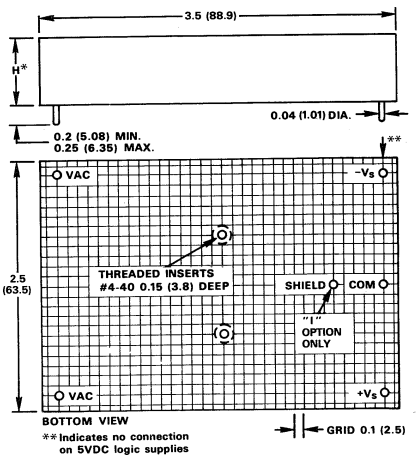
SPECIFICATIONS (typical @ +25°C over the full range of input voltages unless otherwise noted)

Model	Output Voltage	Output Current	Input Voltage	Input Voltage Range	Input Current Full Load	Output Voltage Error Max	Temperature Coefficient /°C	Efficiency Full Load Min	Breakdown Voltage Continuous
940	±15V	±150mA	5V	4.65/ 5.5V	1.35A	±0.5%	±0.01	62%	500V dc
941	±12V	±150mA	5V	4.65/ 5.5V	1.17A	±0.5%	±0.01	58%	500V dc
942	5V	600mA	5V	4.65/ 5.5V	1.02A	±1%	±0.02	55%	500V dc
943	5V	1000mA	5V	4.65/ 5.5V	1.52A	±1%	±0.02	62%	500V dc
944	±15V	±60mA	5V	4.65/ 5.5V	0.67A	±0.5%	±0.01	50%	8000V dc
945	±15V	±150mA	28V	23/31V	250mA	±0.5%	±0.01	61%	500V dc
946	±15V	±60mA	28V	23/31V	120mA	±0.5%	±0.01	48%	8000V dc

MECHANICAL OUTLINES

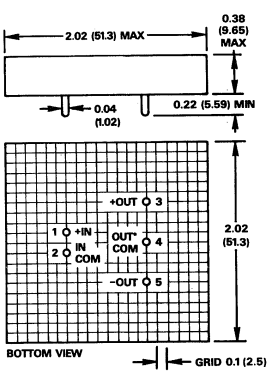
Dimensions shown in inches and (mm).

"P" CASE



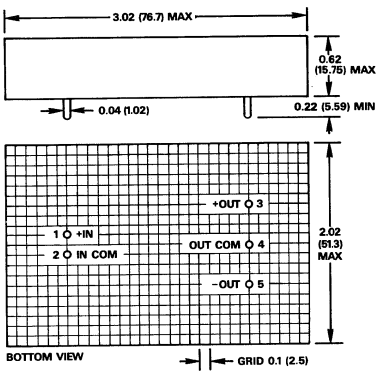
SOCKET AC1013
(SOCKET AC1028 FOR I OPTION)

"A" CASE



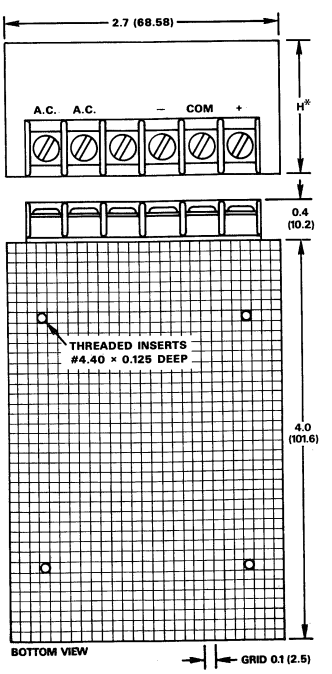
SOCKET AC1051

"B" CASE



SOCKET AC1052

CHASSIS MOUNT



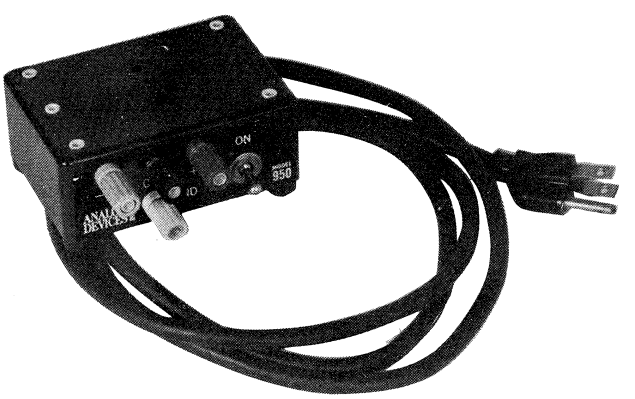
*See Reference Guide.

REFERENCE GUIDE

Model	Output (V/mA)	Height (H)	Case	Weight (grams)
902	±15/100	1.25	P	530
902-2	±15/100	0.875	P	330
903	5/500	1.25	P	530
904	±15/50	0.875	P	330
905	5/1000	1.25	P	530
906	5/250	0.875	P	330
907	±12/25	0.875	P	330
908	±12/100	0.875	P	330
915	±15/25	0.875	P	330
920	±15/200	1.25	P	530
921	±12/240	1.25	P	530
922	5/2000	1.62	P	750
925	±15/350	1.62	P	750
934	±24/100	1.25	P	530
940	±15/150	0.375	A	85
941	±12/150	0.375	A	85
942	5/600	0.375	A	85
943	5/1000	0.375	A	85
944	±15/60	0.62	B	120
945	±15/150	0.375	A	85
946	±15/60	0.62	B	120
952	±15/100	1.44	CM	590
955	5/1000	1.44	CM	590
956	5/2000	2.00	CM	880
970	±15/200	1.44	CM	590
973	±15/350	2.00	CM	880
975	±15/500	2.00	CM	880

MODEL 950 POWER SUPPLY MANIFOLD

This manifold permits use of the 900 series "P" cased modules on the design bench. In combination with these supplies the 950 provides a safe, convenient, and inexpensive bench supply for breadboarding, testing, or general laboratory use.



Appendix

Products Still Available

The data sheets published in this catalog are intended to assist the user in the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs. Naturally, data sheets on these products are available upon request.

AD351
AD502
AD512
AD514
AD520
AD523
AD550
AD553
AD555
AD801
B100
ADC-8F
ADC-8S
ADC-10F
ADC-10Z
ADC 1123
ADC-QM
ADC-QU
DAC-10H
DAC-10Q
DAC1122
MDA-8H
MDA-10H
MDA-LB
MDA-LD
MDA-UB
MDA-UD
SERDEX
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43
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45
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47
105
111
118
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141
144
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170
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230
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232
233
272
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280-1
282
283
350
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426
427
428
432
440
441
603
605
751
752
756
901
909
931
932
933
935
971

Substitution Guide for Products No Longer Available

The products listed in the left-hand column below are no longer available. In many cases, comparable functions and performance may be obtained with newer models, but — as a rule — they are not directly interchangeable. The closest recommended equivalent, physically and electrically, is listed in the right-hand column.

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
101	45	161	165
102	48	220	234
106	118	301	52
107	118	302	310
108	52	602J10	610
110	48	602J100	610
114	119	602K100	610
115	43	AD508	AD517
120	50	AD513	AD503
142	48	AD516	AD506
143	52	ADM501	ADM501/506
149	50		

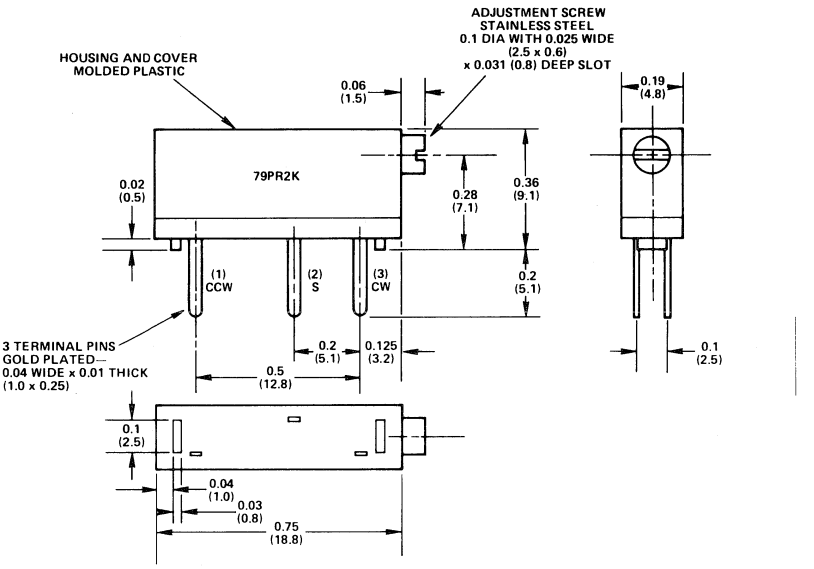
Trimming Potentiometers

MODEL 79P CERMET BALANCE POT

Analog Devices has selected the Beckman Helitrim model 79P as suitable for most applications and carries this balance pot in stock. We offer this service since you may find it more economical or convenient to order your balance pots directly from Analog Devices along with your amplifiers.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SPECIFICATIONS (typical @ +25°C)

Tempco, max	±100ppm
Input voltage, max	200V dc or rms
Power rating	0.75 watts at +25°C, derated to 0 watts at +105°C
End resistance, max	2 ohms
Resolution	essentially infinite
Ambient temperature range	−55°C to +105°C
Adjustment turns, nominal	15
Sealing (immersion test)	meets MIL-R-22097C
Temperature cycling	5 cycles −55°C to +105°C
Humidity cycling	5 cycles
Shock	50G's
Vibration	10 to 500kz, 10G's
Load life at 0.75 watts	1,000 hrs. at +25°C
Rotational life	200 cycles

ANALOG DEVICES PART NUMBER	RESISTANCE OHMS
79PR1k	1k ±10%
79PR10k	10k ±10%
79PR20k	20k ±10%
79PR50k	50k ±10%
79PR100k	100k ±10%

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